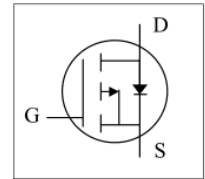


-100V P-Channel Enhancement Mode MOSFET

Description

The HM3P10MR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = -100V$ $I_D = -3.0 A$

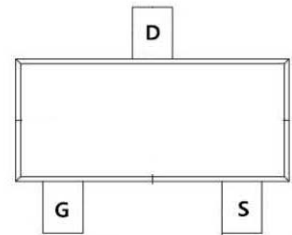
$R_{DS(ON)} < 210m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HM3P10MR	SOT23-3L	3P10	3000

Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-3.0	A
$I_D @ T_A = 70^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-2.1	A
I_{DM}	Pulsed Drain Current ²	-9.0	A
$P_D @ T_A = 25^{\circ}C$	Total Power Dissipation ³	1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	125	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	80	$^{\circ}C/W$

-100V P-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-100	---	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.0624	---	V/ $^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-10V$, $I_D=-0.8A$	---	---	210	m Ω
		$V_{GS}=-4.5V$, $I_D=-0.4A$	---	---	225	
VGS(th)	Gate Threshold Voltage		-1.2	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	---	4.5	---	mV/ $^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-80V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	10	μA
		$V_{DS}=-80V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	100	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V$, $I_D=-0.8A$	---	3	---	S
Rg	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	16	32	Ω
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-15V$, $V_{GS}=-4.5V$, $I_D=-0.5A$	---	4.5	---	nC
Qgs	Gate-Source Charge		---	1.14	---	
Qgd	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-50V$, $V_{GS}=-10V$, $R_G=3.3\Omega$, $I_D=-0.5A$	---	13.6	---	ns
Tr	Rise Time		---	6.8	---	
Td(off)	Turn-Off Delay Time		---	34	---	
Tf	Fall Time		---	3	---	
Ciss	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1MHz$	---	553	---	pF
Coss	Output Capacitance		---	29	---	
Crss	Reverse Transfer Capacitance		---	20	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-0.9	A
ISM	Pulsed Source Current ^{2,4}		---	---	-1.8	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

-100V P-Channel Enhancement Mode MOSFET

Typical Characteristics

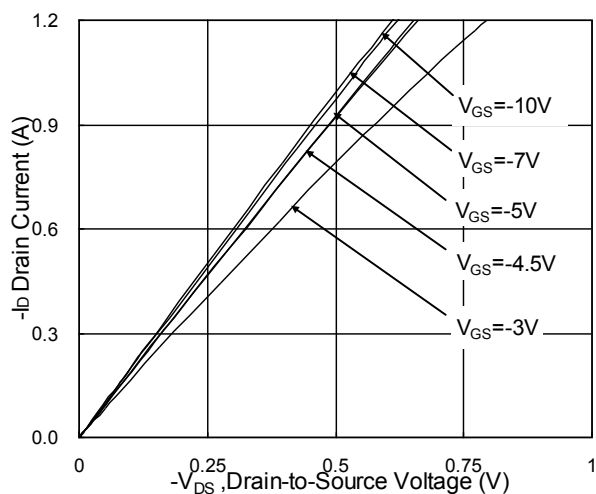


Fig.1 Typical Output Characteristics

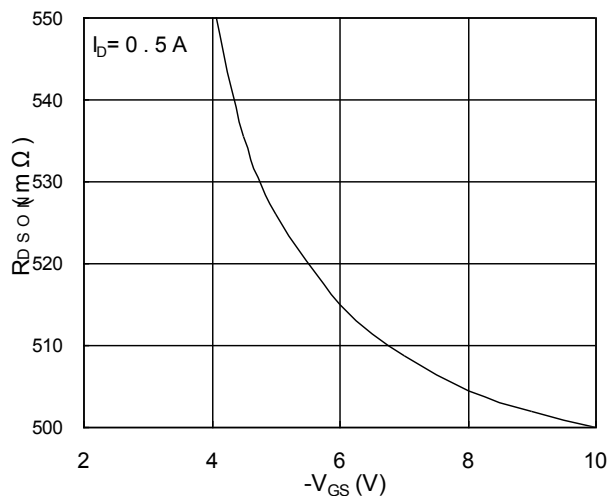


Fig.2 On-Resistance vs. Gate-Source

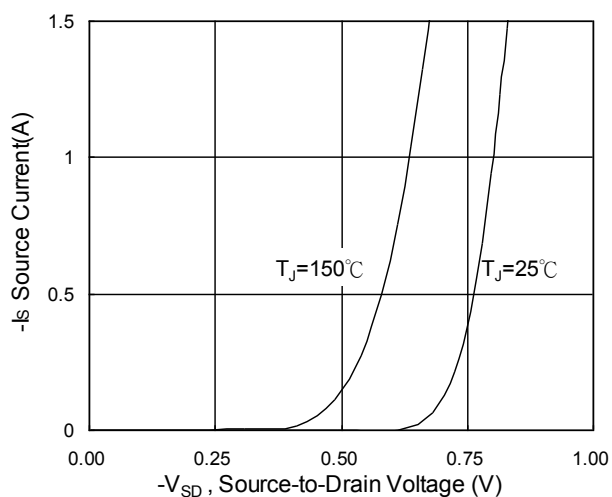


Fig.3 Forward Characteristics Of Reverse

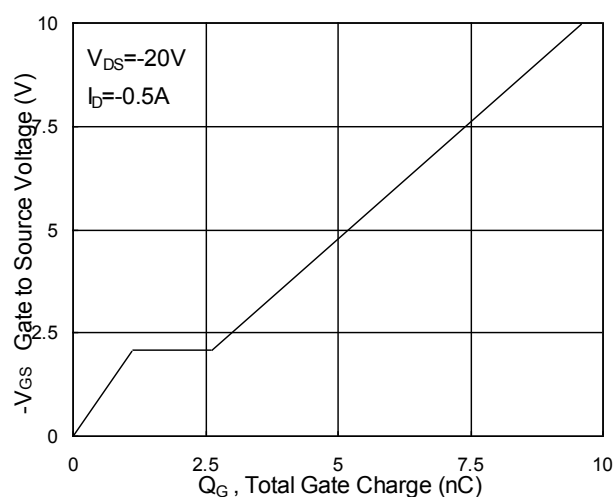


Fig.4 Gate-Charge Characteristics

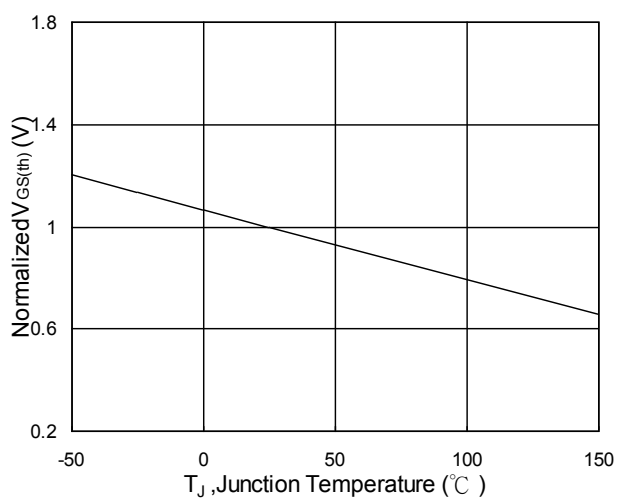


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

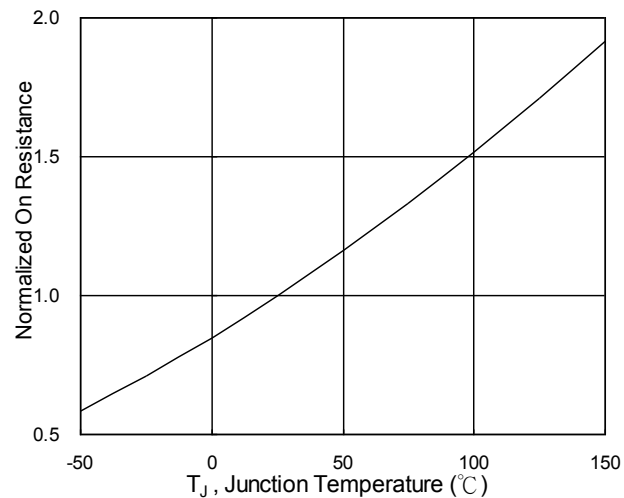


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

-100V P-Channel Enhancement Mode MOSFET

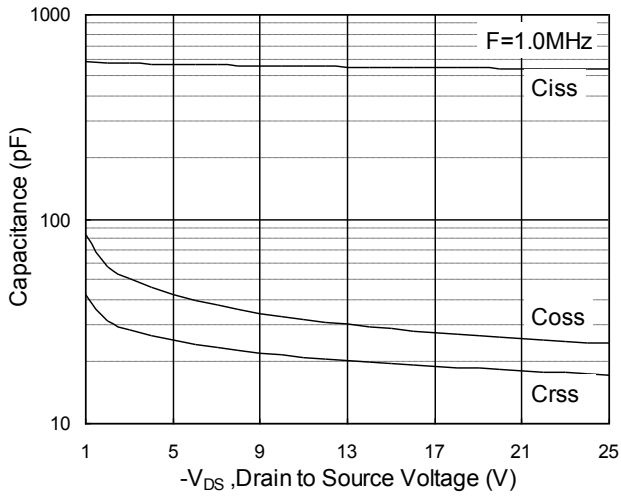


Fig.7 Capacitance

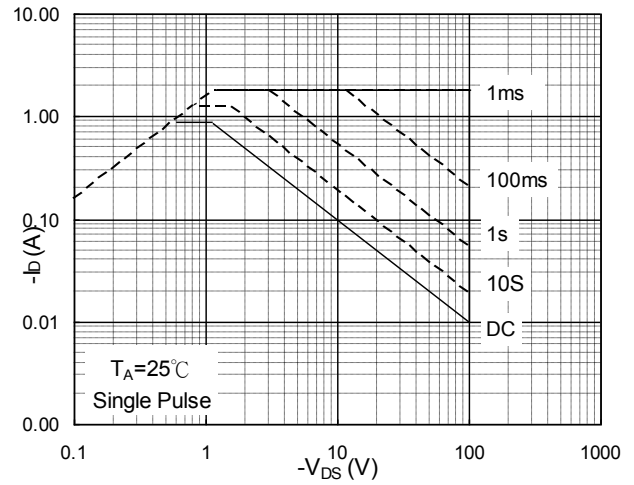


Fig.8 Safe Operating Area

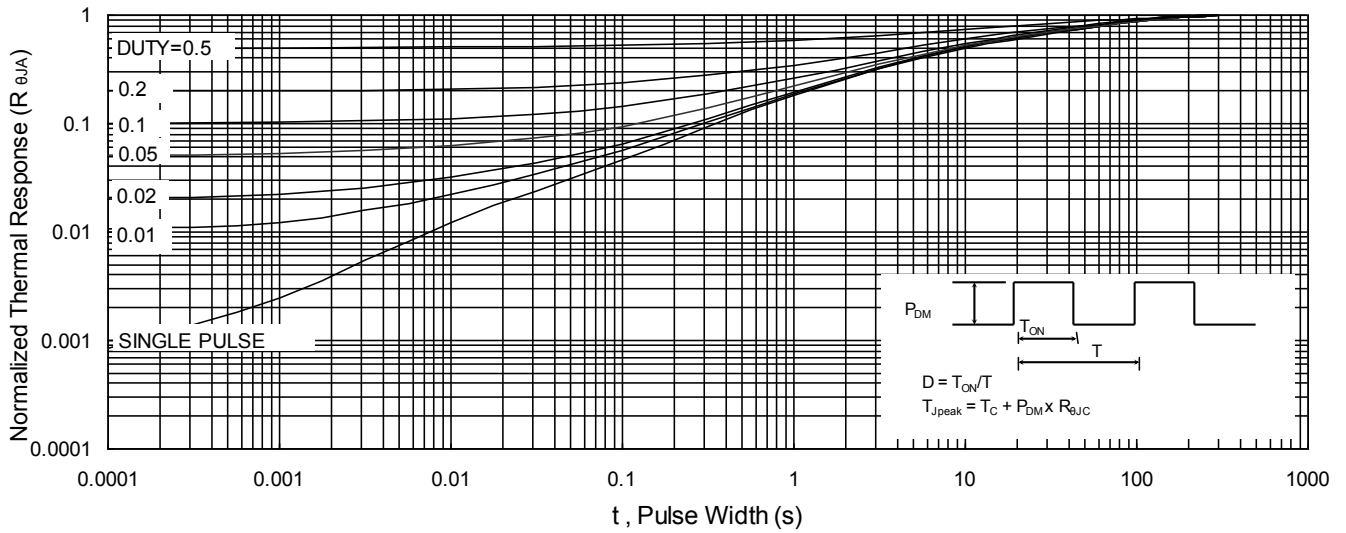


Fig.9 Normalized Maximum Transient Thermal Impedance

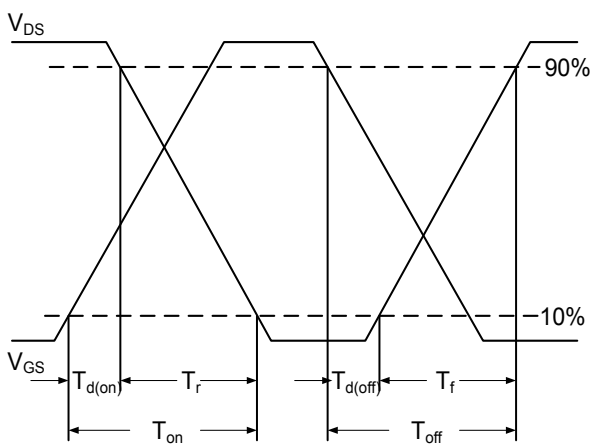


Fig.10 Switching Time Waveform

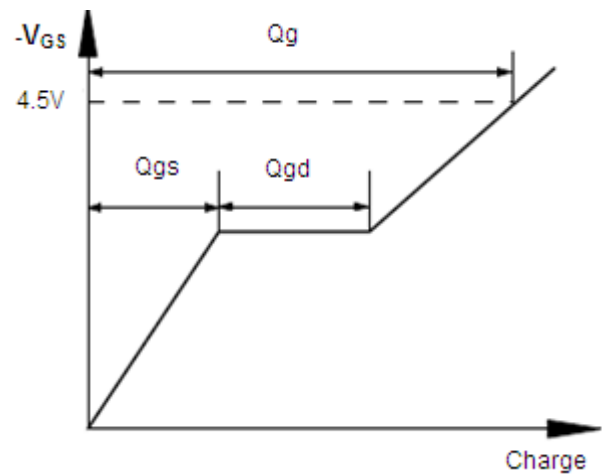
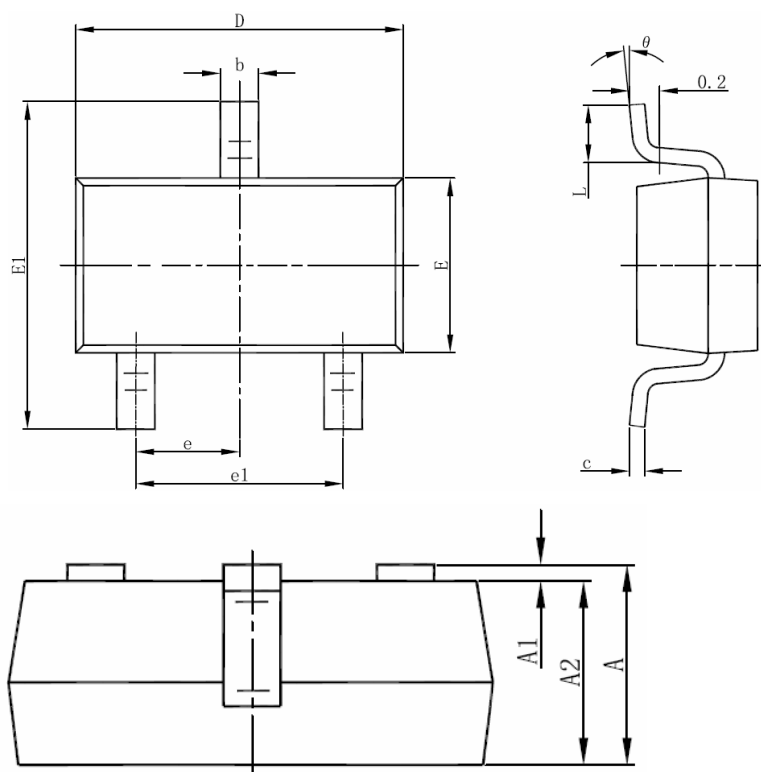


Fig.11 Gate Charge Waveform

SOT-23-3L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.