

### N-Channel Enhancement Mode Power MOSFET

### **Description**

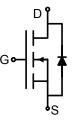
The HM2N15R uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

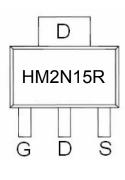
- $V_{DS}$  = 150V, $I_D$  = 2A  $R_{DS(ON)}$  < 300mΩ @  $V_{GS}$ =10V (Typ:260mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

### **Application**

- Power switching application
- Hard switched and high frequency circuits



Schematic diagram



SOT-223-3L view

## **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM2N15R	HM2N15R	SOT-223-3L	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T<sub>A</sub>=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	150	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	2	Α
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	6	Α
Maximum Power Dissipation	P <sub>D</sub>	2	W
Operating Junction and Storage Temperature Range	$T_{J}$ , $T_{STG}$	-55 To 150	$^{\circ}$ C

### **Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{ hetaJA}$	62.5	°C/W

#### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =150V,V <sub>GS</sub> =0V	-	-	1	μA





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Gate-Body Leakage Current	I <sub>GSS</sub>	$V_{GS}=\pm20V, V_{DS}=0V$	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.5	2.0	2.5	>
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =1.5A	-	260	300	mΩ
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =15V,I <sub>D</sub> =1.5A	-	3	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>lss</sub>	\/ -25\/\/ -0\/	-	235	-	PF
Output Capacitance	C <sub>oss</sub>	- V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, - F=1.0MHz	-	36	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F-1.UIVITZ	-	20	-	PF
Switching Characteristics (Note 4)	•					
Turn-on Delay Time	t <sub>d(on)</sub>		-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =75 $V$ , $I_D$ =1 $A$ , $R_L$ =75 $\Omega$	-	10	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ =10 $V$ , $R_{G}$ =6 $\Omega$	-	20	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	$Q_g$	V <sub>DS</sub> =75V.I <sub>D</sub> =1.5A.	-	8		nC
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 75V, I_D = 1.5A,$ $V_{GS} = 10V$	-	1.4	-	nC
Gate-Drain Charge	$Q_gd$	V <sub>GS</sub> -10V	-	2.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =2A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	2	Α

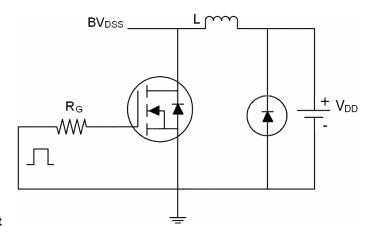
#### Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤  $300\mu$ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to product

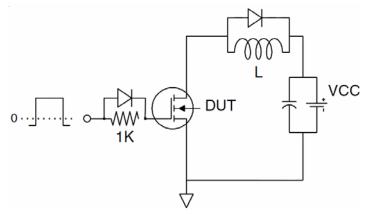


## **Test Circuit**

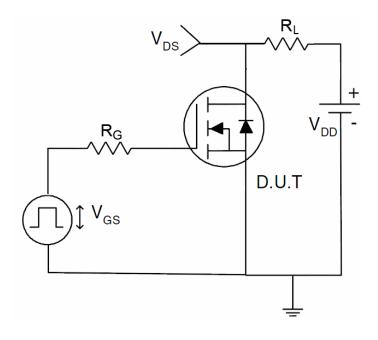
## 1) E<sub>AS</sub> Test Circuit



### 2) Gate Charge Test Circuit

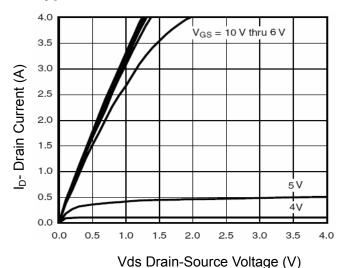


## 3) Switch Time Test Circuit

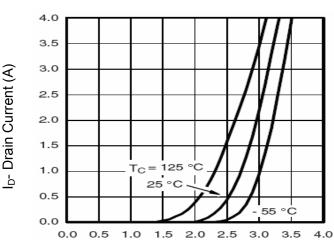




## **Typical Electrical and Thermal Characteristics (Curves)**



**Figure 1 Output Characteristics** 



Vgs Gate-Source Voltage (V)

**Figure 2 Transfer Characteristics** 

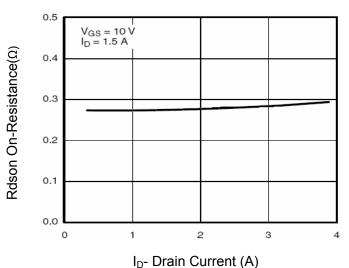
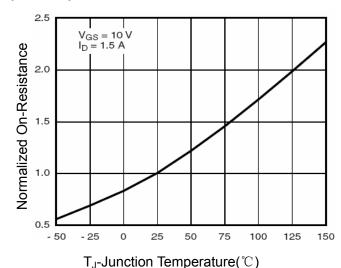


Figure 3 Rdson- Drain Current



**Figure 4 Rdson- Junction Temperature** 

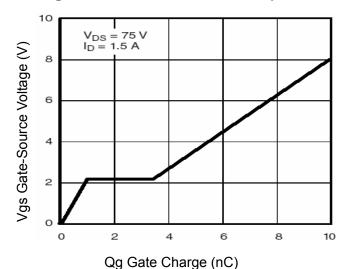


Figure 5 Gate Charge

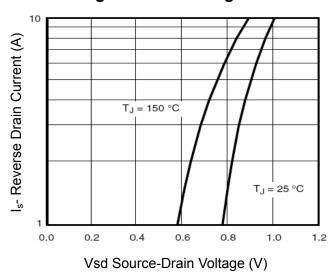


Figure 6 Source- Drain Diode Forward



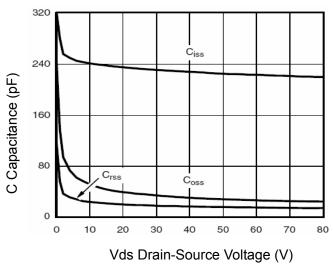


Figure 7 Capacitance vs Vds

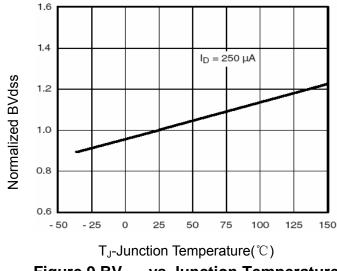
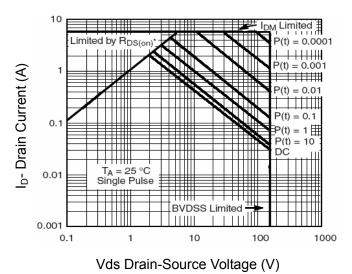
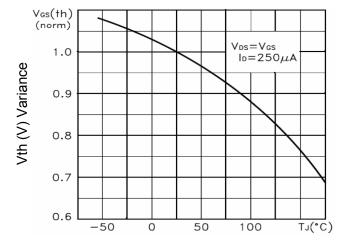


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

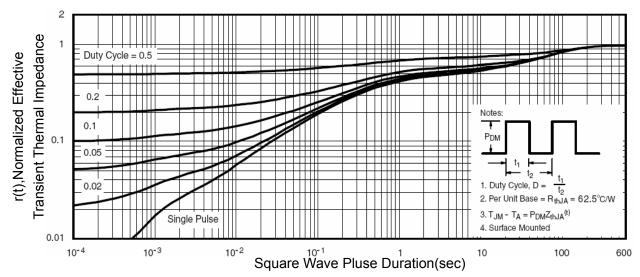




T<sub>J</sub>-Junction Temperature(°C)

Figure 8 Safe Operation Area

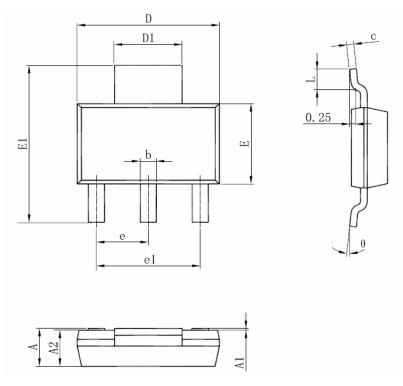
Figure 10 V<sub>GS(th)</sub> vs Junction Temperature



**Figure 11 Normalized Maximum Transient Thermal Impedance** 



# **SOT-223-3L Package Information**



Comb o I	Dimensions Ir	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	1.520	1.800	0.060	0.071	
A1	0.000	0.100	0.000	0.004	
A2	1.500	1.700	0.059	0.067	
b	0.660	0.820	0.026	0.032	
С	0.250	0.350	0.010	0.014	
D	6.200	6.400	0.244	0.252	
D1	2.900	3.100	0.114	0.122	
E	3.300	3.700	0.130	0.146	
E1	6.830	7.070	0.269	0.278	
е	2.300(BSC)		0.091(	BSC)	
e1	4.500	4.700	0.177	0.185	
L	0.900	1.150	0.035	0.045	
θ	0°	10°	0°	10°	

#### **Notes**

- 1. All dimensions are in millimeters.
- 2. Tolerance ±0.10mm (4 mil) unless otherwise specified
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
- 4. Dimension L is measured in gauge plane.
- $5. \ Controlling \ dimension \ is \ millimeter, \ converted \ inch \ dimensions \ are \ not \ necessarily \ exact.$



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