

### GENERAL DESCRIPTION

The HI-3000 is a 1 Mbps Controller Area Network (CAN) transceiver optimized for use in aerospace applications. It interfaces between a CAN protocol controller and the physical wires of the bus in a CAN network. Differential output amplitude and current drive capability are specifically enhanced to meet the needs of long cable runs typical of aerospace applications.

The HI-3000 supports two modes of operation: Normal Mode and Standby Mode. The Standby Mode is a very low-current mode which continues to monitor bus activity and allows an external controller to manage wake-up.

Superior common-mode receiver performance makes the device especially suitable for applications where ground reference voltages may vary from point to point over long distances along the CAN bus. In addition, the HI-3000 provides a SPLIT pin to give an output reference voltage of VDD/2 which can be used for stabilizing the recessive bus level when the split termination technique is used to terminate the bus.

A TXD dominant time-out feature also protects the bus from being driven into a permanent dominant state (so-called "babbling idiot") if pin TXD becomes permanently low due to application failure.

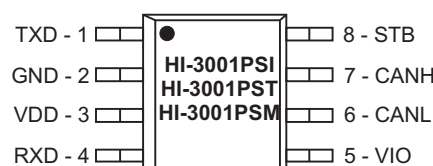
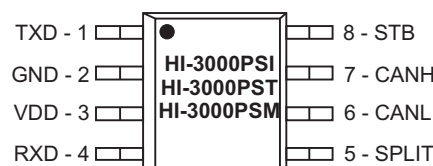
The device also has short circuit protection to +/-58V on CANH, CANL and SPLIT pins and ESD protection to +/- 6kV on all pins.

The HI-3001 is identical to the HI-3000 except the SPLIT pin is substituted with a VIO supply voltage pin. This allows the HI-3001 to interface directly with controllers with 3.3V supply voltages.

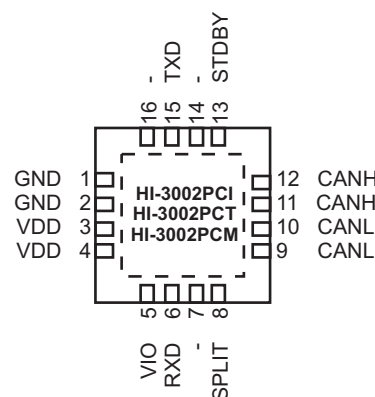
The HI-3002 provides both the SPLIT and VIO supply voltage pins in a compact 16-pin QFN.

All three devices are available in industrial -40°C to +85°C and extended -55°C to +125°C temperature ranges. "RoHS compliant" lead-free options are also available with optional burn-in for the extended temperature range.

### PIN CONFIGURATIONS (Top Views)



8 - PIN PLASTIC NARROW BODY SOIC



16 - PIN PLASTIC 4 x 4mm QFN

### FEATURES

- Compatible with ARINC 825 and ISO 11898-5 standards.
- Signaling rates up to 1Mbit/s.
- Internal VDD/2 voltage source available to stabilize the recessive bus level if split termination is used (HI-3000 SPLIT pin).
- VIO input on HI-3001 allows for direct interfacing with 3.3V controllers.
- Detection of permanent dominant on TXD pin (babbling idiot protection).
- High impedance allows connection of up to 120 nodes.
- Input levels compatible with 3.3V or 5V controllers.
- CANH, CANL and SPLIT pins short-circuit proof to +/-58V.
- Will not disturb the bus if unpowered.
- Extended temperature range and burn-in options for high reliability applications.
- Compatible with CAN 2.0A & CAN 2.0B Specification controllers

## PIN DESCRIPTIONS

| SIGNAL             | FUNCTION | DESCRIPTION                                                                                                                                                      |
|--------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TXD                | INPUT    | 100kOhm internal pull-up. Transmit Data Input.                                                                                                                   |
| GND                | POWER    | Chip 0V supply                                                                                                                                                   |
| VDD                | POWER    | Positive supply, 5V +/-5%. Bypass with 0.1uF ceramic capacitor.                                                                                                  |
| RXD                | OUTPUT   | Receive Data Output.                                                                                                                                             |
| CANL               | BUS I/O  | CAN Bus Line Low.                                                                                                                                                |
| CANH               | BUS I/O  | CAN Bus Line High.                                                                                                                                               |
| STB                | INPUT    | 100kOhm internal pull-up. Standby Mode selection input. Drive STB low or connect to GND for Normal operation. Drive STB high to select low-current Standby Mode. |
| SPLIT<br>(HI-3000) | INPUT    | Supplies a VDD/2 output to provide recessive bus level stabilization when a split termination is used to terminate the bus.                                      |
| VIO<br>(HI-3001)   | INPUT    | Connect to a 3.3V supply to allow compatibility of all digital I/O (RXD, TXD, STB) with a 3.3V controller input.                                                 |

## BLOCK DIAGRAM

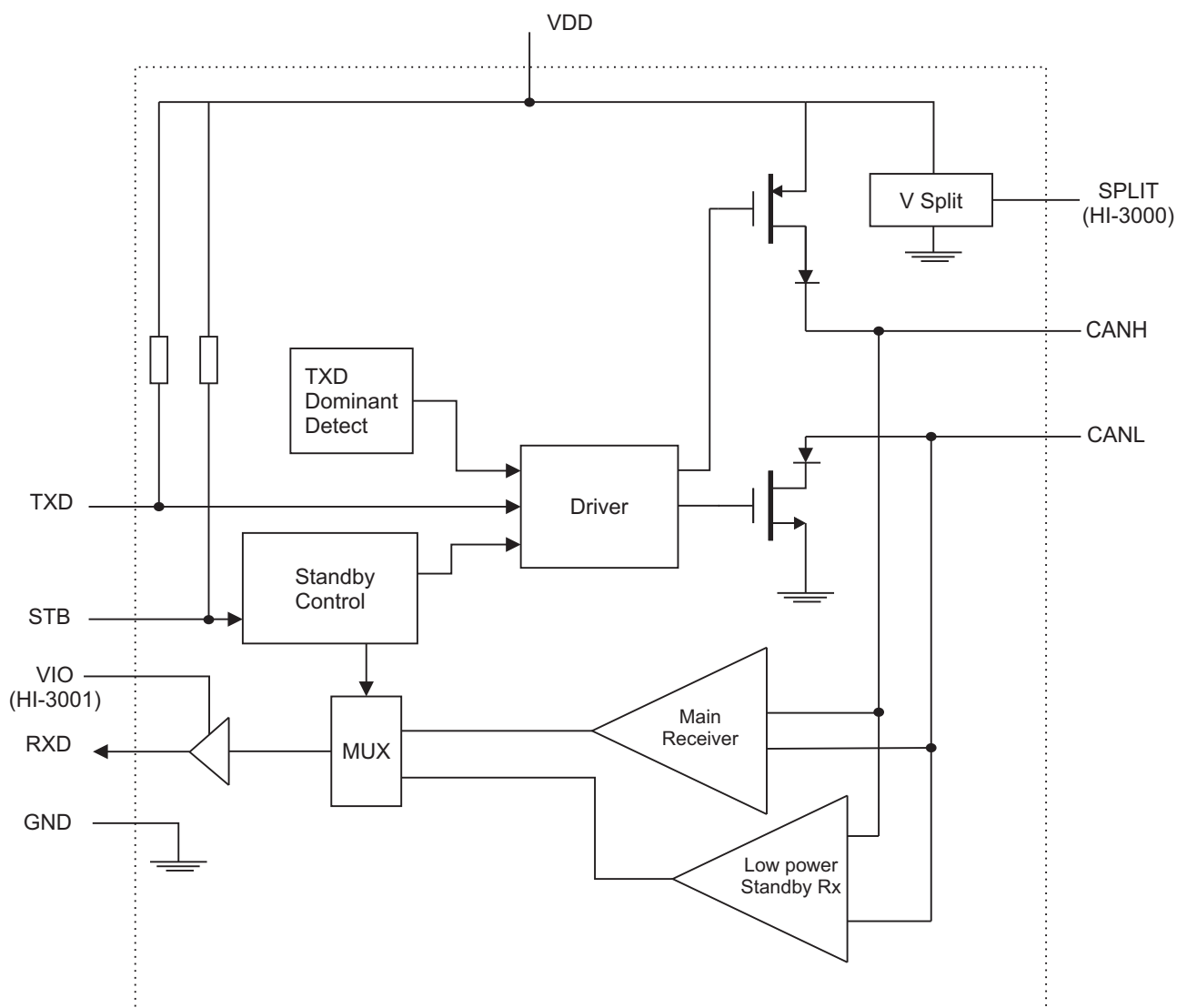


Figure 1. HI-3000 Functional Block Diagram

## FUNCTIONAL DESCRIPTION

### OPERATING MODES

The HI-3000 provides two modes of operation which are selectable via the STB pin. Table 1 summarizes the modes.

Table 1 - Operating Modes

| MODE    | STB pin |
|---------|---------|
| Normal  | LOW     |
| Standby | HIGH    |

#### Normal Mode

Normal mode is selected by setting the STB pin to a LOW logic level (GND). In this mode, the transceiver transmits and receives data in the usual way from the CANH and CANL bus lines. The differential receiver converts the analog bus data to digital data which is output on the RXD pin (Note: the RXD output on HI-3001 is compatible with 3.3V controllers if the VIO pin is connected to a 3.3V supply).

#### Standby Mode

Standby Mode is selected by setting the STB pin to a HIGH logic level. In this mode, the transmitter is switched off and a low power differential receiver monitors the bus lines for activity. A dominant signal of more than  $3\mu\text{s}$  will be reflected on the RXD pin as a logic LOW, where it may be detected by the host as a wake-up request. The device will not leave standby mode until the host forces the STB pin to a logic low.

#### SPLIT Circuit

The SPLIT pin provides a stable  $V_{DD}/2$  DC voltage. This pin can be used to stabilize the recessive common mode voltage by connecting the SPLIT pin to the center tap of the split termination (see figure 7). In the case of a recessive bus voltage dropping below the ideal value of  $V_{DD}/2$  (e.g.

due to an unpowered node with high leakage from the bus lines to ground), the split circuit will force the recessive voltage to  $V_{DD}/2$ .

### INTERNAL PROTECTION FEATURES

#### Short-circuit protection

Short-circuit protection is provided on the CANH, CANL and SPLIT pins. These pins are protected from ESD to over 6KV (HBM) and from shorts between -58V and +58V continuous, as specified in ISO 11898-5. The short circuit current is limited to less than 200mA typical.

#### TXD permanent dominant time-out

A timer circuit prevents the bus lines being driven into a permanent dominant state, which would result in a situation blocking all bus traffic. This could happen in the case of the TXD pin becoming permanently low due to a hardware or application failure. The timer is triggered by a negative edge on the TXD pin (start of dominant state). If the TXD pin is not set high (recessive state) after a typical time of 2ms, the transmitter outputs will be disabled, driving the bus lines into the recessive state. The timer is reset by a positive edge on the TXD pin. Note that the minimum TXD dominant time-out time,  $t_{dom} = 300\mu\text{s}$ , defines the minimum possible bit rate of 40kbit/s (the CAN protocol specifies a maximum of 11 successive dominant bits – 5 successive dominant bits immediately followed by an error frame).

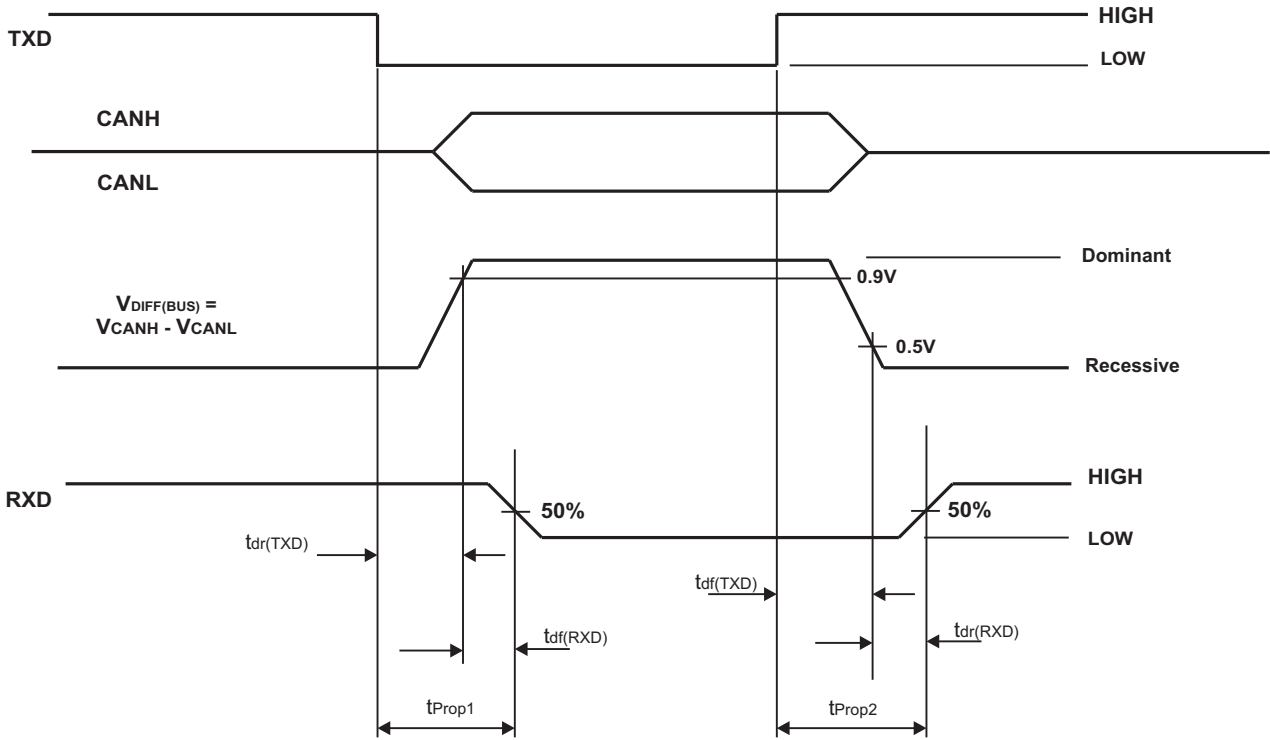
#### Fail-safe features

Pin TXD has a pull up in order to force a recessive level if pin TXD is left open.

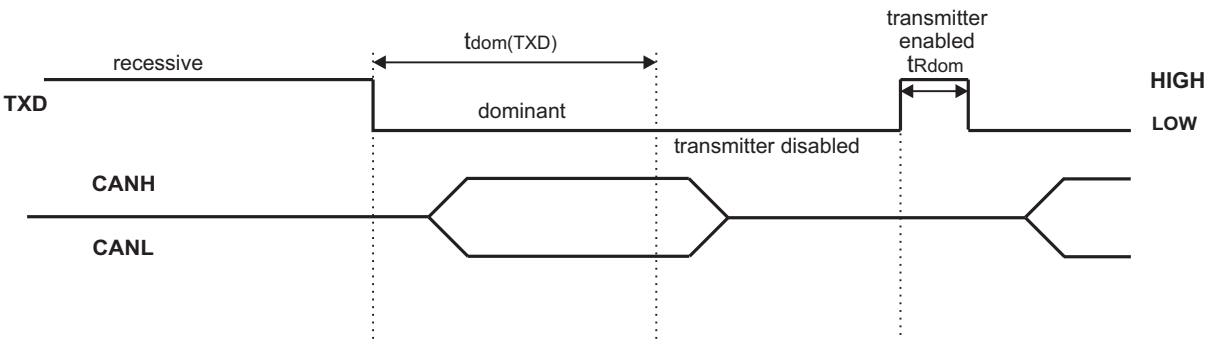
Pins TXD and STB will become floating if power is lost. This will prevent reverse currents via these pins.

TIMING DIAGRAMS

Timing Delays



TXD dominant time-out feature



## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND = 0V)

|                                                                    |                                                              |
|--------------------------------------------------------------------|--------------------------------------------------------------|
| Supply Voltage, VDD, VIO : .....7V                                 | Operating Temperature Range: (Industrial).....-40°C to +85°C |
| Current at Input pins .....-100mA to +100mA                        | (Hi-Temp).....-55°C to +125°C                                |
| DC Voltages at TXD, RXD and STB .....-0.5V to VDD +0.5V            |                                                              |
| DC Voltages at CANH, CANL and SPLIT: .....-58V to +58V             | Maximum Junction Temperature <sup>2</sup> .....175°C         |
| Internal Power Dissipation: .....900mW                             |                                                              |
| Electrostatic Discharge (ESD) <sup>1</sup> , All pins .....+/- 6kV | Storage Temperature Range: ..... -65°C to +150°C             |
|                                                                    | Reflow Soldering Temperature: ..... 260°C                    |

### NOTES:

1. Human Body Model (HBM).

2. Junction Temperature  $T_J$  is defined as  $T_J = T_{AMB} + P \times R_{th}$ , where  $T_{AMB}$  is the ambient or operating temperature,  $P$  is the power dissipation and  $R_{th}$  is a fixed thermal resistance value which depends on the package and circuit board mounting conditions.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

VDD = 5V±5%, Operating temperature range (unless otherwise noted). Positive currents flow into the IC.

| PARAMETER                                        | SYMBOL                | CONDITIONS                                                                | LIMITS  |               |                       | UNIT                 |
|--------------------------------------------------|-----------------------|---------------------------------------------------------------------------|---------|---------------|-----------------------|----------------------|
|                                                  |                       |                                                                           | MIN     | TYP           | MAX                   |                      |
| POWER SUPPLIES                                   |                       |                                                                           |         |               |                       |                      |
| VDD Supply Current                               | IDD                   | Recessive: VTXD = VDD<br>Dominant: VTXD = 0 V<br>Standby Mode: VTXD = VDD |         | 6<br>50<br>15 | 10<br>70<br>30<br>100 | mA<br>mA<br>μA<br>μA |
| VIO Supply Current                               | IIO                   |                                                                           |         |               |                       |                      |
| VIO Supply Voltage (see Note 1)                  | VIO                   |                                                                           | 2.7     |               | 5.5                   | V                    |
| DIGITAL INPUTS (Pins TXD, STB)                   |                       |                                                                           |         |               |                       |                      |
| HIGH-level input voltage (see Note 1)            | VIH                   |                                                                           | 80%VDD  |               | VDD + 0.5             | V                    |
| LOW-level input voltage                          | VIL                   |                                                                           | − 0.5   |               | 20%VDD                | V                    |
| HIGH-level input current                         | IIH                   | VTXD = VDD or VIO                                                         | − 5     | 0             | + 5                   | μA                   |
| LOW-level input current                          | IIL                   | VTXD = 0 V                                                                |         | − 50          | − 150                 | μA                   |
| DIGITAL OUTPUTS                                  |                       |                                                                           |         |               |                       |                      |
| HIGH-level output voltage (RXD Pin) (see Note 1) | VOH                   | IOH = 1mA                                                                 | 90%VDD  |               |                       | V                    |
| LOW-level output voltage (RXD Pin)               | VOL                   | IOL = 1mA                                                                 | 0       | 0.1           | 10%VDD                | V                    |
| Output voltage (SPLIT Pin)                       | VSPLIT                | − 100 μA < ISPLIT < 100 μA                                                | 0.45VDD | 0.5VDD        | 0.55VDD               | V                    |
| Standby leakage current (SPLIT Pin)              | ISTB                  |                                                                           | −5      |               | +5                    | μA                   |
| DRIVER                                           |                       |                                                                           |         |               |                       |                      |
| CANH dominant output voltage                     | VO(CANH)              | VTXD = 0 V                                                                | 3       | 3.6           | 4.25                  | V                    |
| CANL dominant output voltage                     | VO(CANL)              | VTXD = 0 V (See Fig. 2)                                                   | 0.5     | 1.4           | 1.75                  | V                    |
| Recessive output voltage                         | VCANH(r),<br>VCANL(r) | VTXD = VDD, RL = 0 (See Fig. 2)                                           | 2       | 0.5VDD        | 3                     | V                    |
| Bus output voltage in standby                    | VSTB                  | VTXD = VDD, RL = 0 (See Fig. 2)                                           | −0.1    |               | 0.1                   | V                    |
| Dominant differential output voltage             | VDIFF(d)(o)           | VTXD = 0 V, 45 Ω < RL < 65 Ω                                              | 1.5     | 1.8           | 3                     | V                    |
| Recessive differential output voltage            | VDIFF(r)(o)           | VTXD = VDD, no load (See Fig. 2)                                          | − 50    | 0             | 50                    | mV                   |

### NOTE:

1. When VIO is connected (HI-3001 or HI-3002), power supply limits are referenced wrt VIO rather than VDD. If VIO < 3.3V, VIH must be at least 2.5V.

## DC ELECTRICAL CHARACTERISTICS (cont.)

$V_{DD} = 5V \pm 5\%$ , Operating temperature range. Positive currents flow into the IC.

| PARAMETER                                                                    | SYMBOL                  | CONDITIONS                                                                                                                                                            | LIMITS                    |             |                        | UNIT                 |
|------------------------------------------------------------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-------------|------------------------|----------------------|
|                                                                              |                         |                                                                                                                                                                       | MIN                       | TYP         | MAX                    |                      |
| Matching of dominant output voltage,<br>$V_{DD} - V_{O(CANH)} - V_{O(CANL)}$ | $V_{OM}$                | (See Fig. 4)                                                                                                                                                          | - 100                     | -40         | 150                    | mV                   |
| Steady state common mode output voltage                                      | $V_{OC(ss)}$            | $V_{STB} = 0V$ , $R_L = 60 \Omega$ (See Fig. 5)                                                                                                                       | 2                         | $0.5V_{DD}$ | 3                      | V                    |
| Short-circuit steady-state output current                                    | $I_{OS(ss)}$            | $V_{CANH} = +58V$ , $V_{CANL}$ open<br>$V_{CANH} = -58V$ , $V_{CANL}$ open<br>$V_{CANL} = +58V$ , $V_{CANH}$ open<br>$V_{CANL} = -58V$ , $V_{CANH}$ open (See Fig. 6) | -20<br>-200<br>100<br>-20 |             | 20<br>100<br>200<br>20 | mA<br>mA<br>mA<br>mA |
| <b>RECEIVER</b>                                                              |                         |                                                                                                                                                                       |                           |             |                        |                      |
| Differential receiver threshold voltage                                      | $V_{Th(Rx)}(diff)$      | - 12 V < $V_{CANH}$ , $V_{CANL} < + 12 V$                                                                                                                             | 500                       | 700         | 900                    | mV                   |
| Differential hysteresis voltage                                              | $V_{Hys(Rx)}(diff)$     | - 12 V < $V_{CANH}$ , $V_{CANL} < + 12 V$                                                                                                                             | 50                        | 120         | 200                    | mV                   |
| Differential hysteresis voltage in Standby mode                              | $V_{Hys(Stb)}(diff)$    | - 12 V < $V_{CANH}$ , $V_{CANL} < + 12 V$                                                                                                                             | 500                       |             | 1150                   | mV                   |
| Input leakage current, unpowered node                                        | $I_{CANH}$ , $I_{CANL}$ | $V_{DD} = V_{IO} 0 V$<br>$V_{CANH} = V_{CANL} = 5V$                                                                                                                   | - 200                     |             | + 200                  | $\mu A$              |
| Differential input resistance                                                | $R_{IN(DIFF)}$          | $V_{TXD} = V_{DD}$<br>- 12 V < $V_{CANH}$ , $V_{CANL} < + 12 V$                                                                                                       | 25                        | 50          | 75                     | k $\Omega$           |
| Common mode input resistance                                                 | $R_{IN(CM)}$            | $V_{TXD} = V_{DD}$<br>- 12 V < $V_{CANH}$ , $V_{CANL} < + 12 V$                                                                                                       | 15                        | 30          | 45                     | k $\Omega$           |
| Deviation between common mode input resistance<br>between CANH and CANL      | $R_{IN(CM)}(m)$         | $V_{CANH} = V_{CANL}$                                                                                                                                                 | - 3                       |             | + 3                    | %                    |

## AC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 5\%$ , Operating temperature range. Positive currents flow into the IC.

| PARAMETER                                              | SYMBOL         | CONDITIONS                                                                 | LIMITS |     |      | UNIT    |
|--------------------------------------------------------|----------------|----------------------------------------------------------------------------|--------|-----|------|---------|
|                                                        |                |                                                                            | MIN    | TYP | MAX  |         |
| Bit time                                               | $t_{Bit}$      |                                                                            | 1      |     | 25   | $\mu s$ |
| Bit rate                                               | $f_{Bit}$      |                                                                            | 40     |     | 1000 | kHz     |
| Common mode input capacitance <sup>3</sup>             | $C_{IN(CM)}$   | $V_{TXD} = V_{DD}$ , 1Mbit/s data rate                                     |        | 20  |      | pF      |
| Differential input capacitance <sup>3</sup>            | $C_{DIFF(CM)}$ | $V_{TXD} = V_{DD}$ , 1Mbit/s data rate                                     |        | 10  |      | pF      |
| Delay TXD to bus active                                | $t_{dr}(TXD)$  | See Timing Diagrams                                                        |        | 40  | 90   | ns      |
| Delay TXD to bus inactive                              | $t_{df}(TXD)$  |                                                                            |        | 40  | 90   | ns      |
| Delay bus active to RXD                                | $t_{dr}(RXD)$  |                                                                            |        | 30  | 70   | ns      |
| Delay bus inactive to RXD                              | $t_{df}(RXD)$  |                                                                            |        | 70  | 150  | ns      |
| Propagation delay TXD to RXD (recessive to dominant)   | $t_{Prop1}$    | $V_{TXD} = 0 V$<br>Rising edge on TXD while in<br>permanent dominant state | 0.3    | 70  | 160  | ns      |
| Propagation delay TXD to RXD (dominant to recessive)   | $t_{Prop2}$    |                                                                            |        | 110 | 240  | ns      |
| TXD permanent dominant time-out                        | $t_{dom}$      |                                                                            |        | 2   | 6    | ms      |
| TXD permanent dominant timer reset time                | $t_{Rdom}$     |                                                                            |        |     | 1    | $\mu s$ |
| Dominant time required on bus for wake up from standby | $t_{wake}$     |                                                                            | 0.5    | 3   | 5    | $\mu s$ |

### NOTES:

1. All currents into the device pins are positive; all currents out of the device pins are negative.
2. All typicals are given for  $V_{DD} = 5V$ ,  $T_A = 25^\circ C$ .
3. Guaranteed by design but not tested.

Application and Test Information

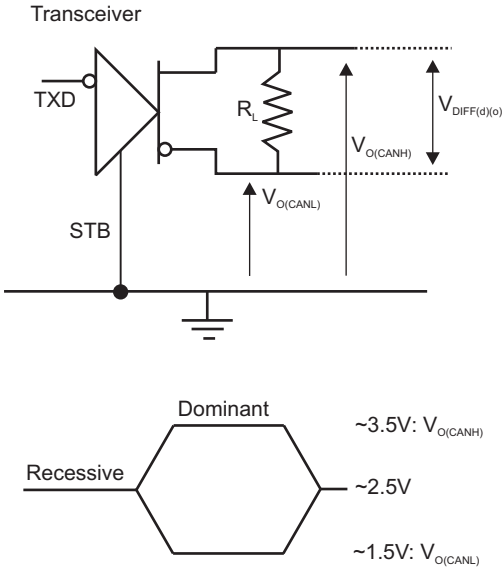


Figure 2. CAN Bus Driver Circuit

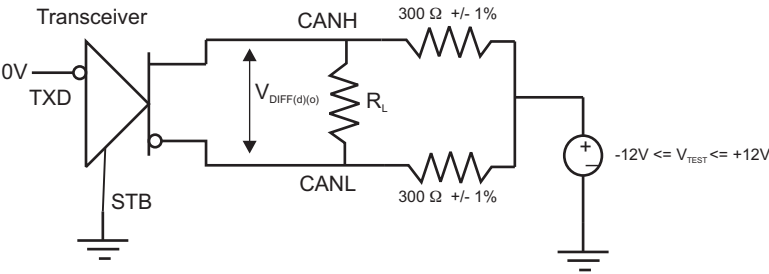


Figure 3. CAN Bus Driver (Dominant) Test Circuit

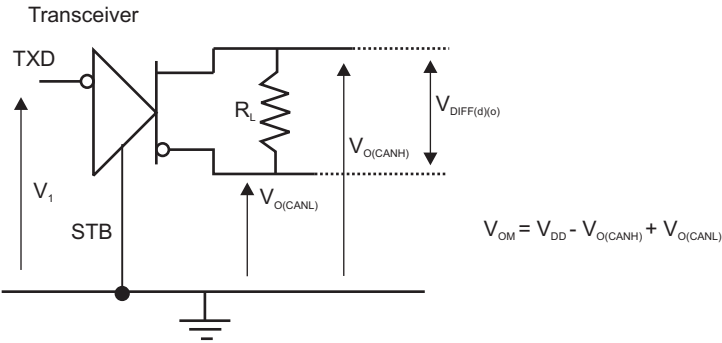


Figure 4. Driver Output Symmetry Test.

## Application and Test Information

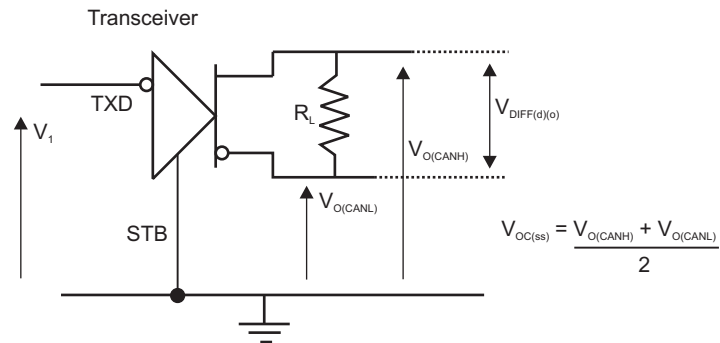


Figure 5. Common Mode Output Voltage Test.

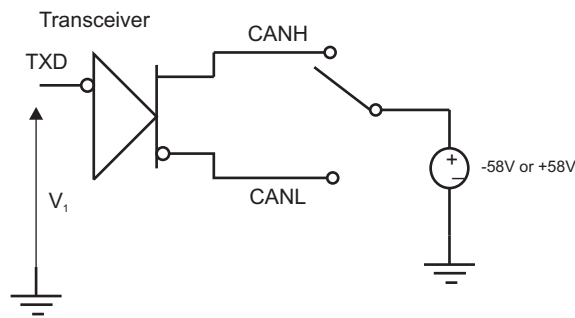


Figure 6. CAN Bus Driver Short-Circuit Test. (Note:  $V_1$  is a pulse from 0V to  $V_{DD}$  with duty cycle of 99% such that permanent dominant time-out is avoided).



Application and Test Information

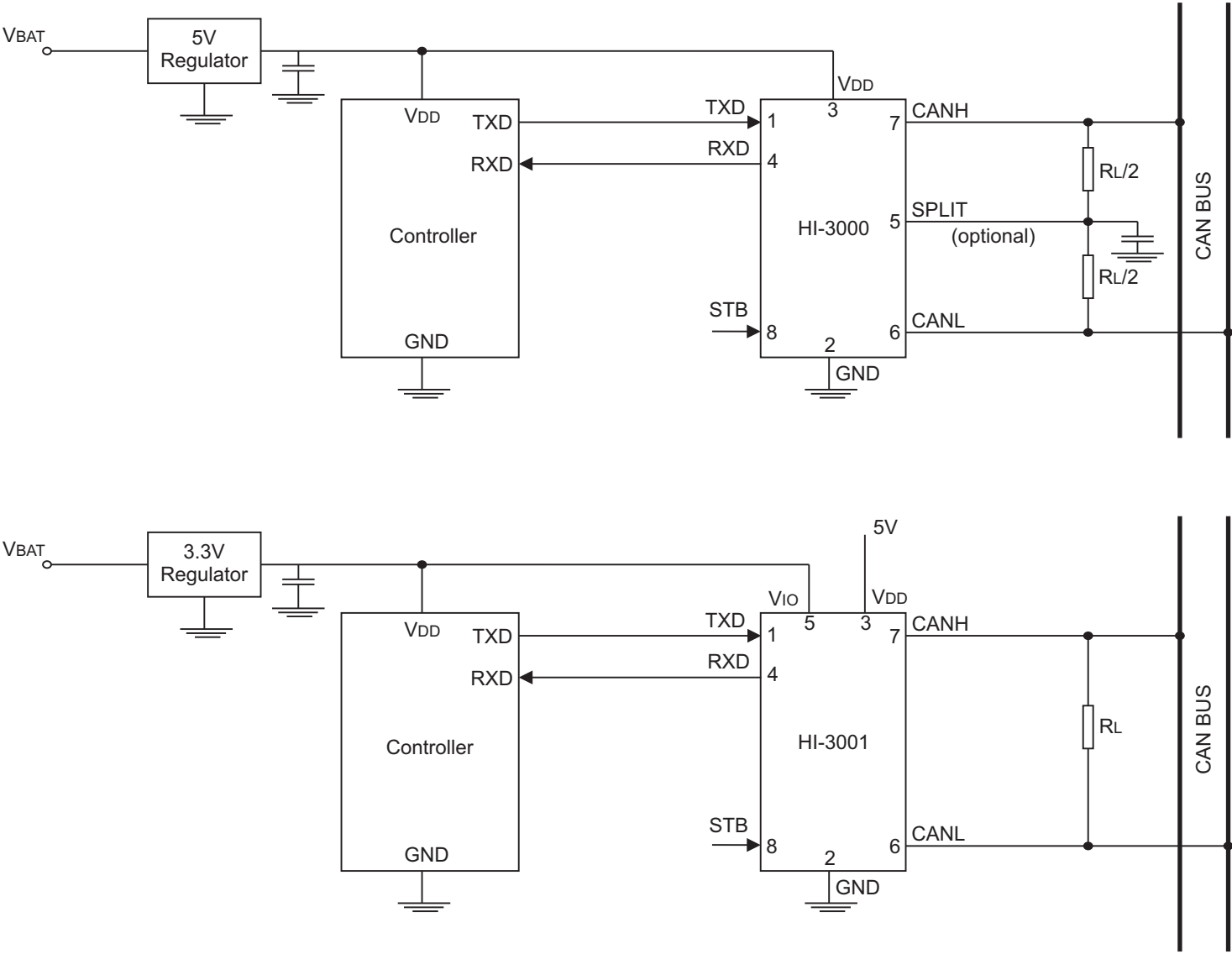


Figure 7. Typical Application Connections

## ORDERING INFORMATION

HI - 300x xx x x

| PART NUMBER | LEAD FINISH                              |
|-------------|------------------------------------------|
| Blank       | Tin / Lead (Sn / Pb) Solder              |
| F           | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I           | -40°C TO +85°C    | I    | NO      |
| T           | -55°C TO +125°C   | T    | NO      |
| M           | -55°C TO +125°C   | M    | YES     |

| PART NUMBER | PACKAGE DESCRIPTION                                               |
|-------------|-------------------------------------------------------------------|
| PS          | 8 PIN PLASTIC NARROW BODY SOIC (8HN) (HI-3000 or HI-3001 only)    |
| PC          | 16 PIN PLASTIC 4 x 4 mm QFN (16PCS) (HI-3002 only)                |
| CR          | 8 PIN Cerdip (8D) not available Pb-free (HI-3000 or HI-3001 only) |

| PART NUMBER | DESCRIPTION                       |
|-------------|-----------------------------------|
| 3000        | SPLIT pin option                  |
| 3001        | VIO pin option                    |
| 3002        | Both SPLIT and VIO pins available |

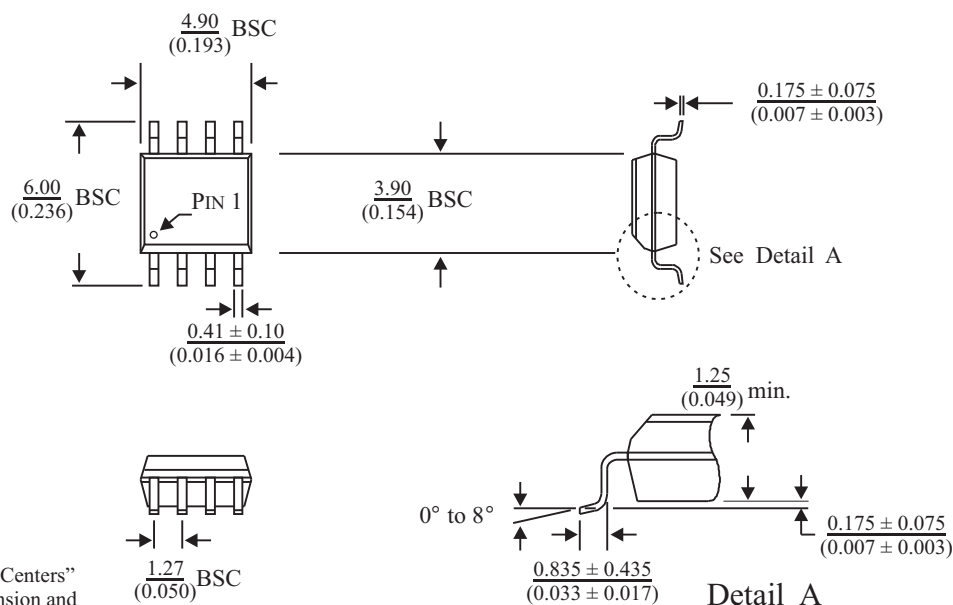
## REVISION HISTORY

| P/N    | Rev | Date     | Description of Change                                                                                                                                                                          |
|--------|-----|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DS3000 | NEW | 02/15/11 | Initial Release                                                                                                                                                                                |
|        | A   | 04/29/11 | Corrected heat-sink note on QFN package drawing.                                                                                                                                               |
|        | B   | 09/09/11 | Update pad and heat-sink dimensions for 16-lead QFN package (16PCS)                                                                                                                            |
|        | C   | 12/18/12 | Change high-level digital input voltage (VIH) to 80%VDD (or VIO) and low-level digital input voltage (VIL) to 20%VDD (or VIO). Update SOIC-8 and SOIC-16 package drawings.                     |
|        | D   | 10/30/14 | Added "Compatible with CAN 2.0A & CAN 2.0B Specification controllers" to features. Updated 8HN and 16PCS package drawings. Clarified Reflow Soldering Temperature in Absolute Maximum Ratings. |
|        | E   | 6/19/15  | Corrected package pin numbers 3 and 5 in Figure 7 HI-3001 Typical Application Connections                                                                                                      |
|        | F   | 10/14/15 | Add parameter specification for VIO to DC Characteristics Table.                                                                                                                               |

### 8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB (Narrow Body)

millimeters (inches)

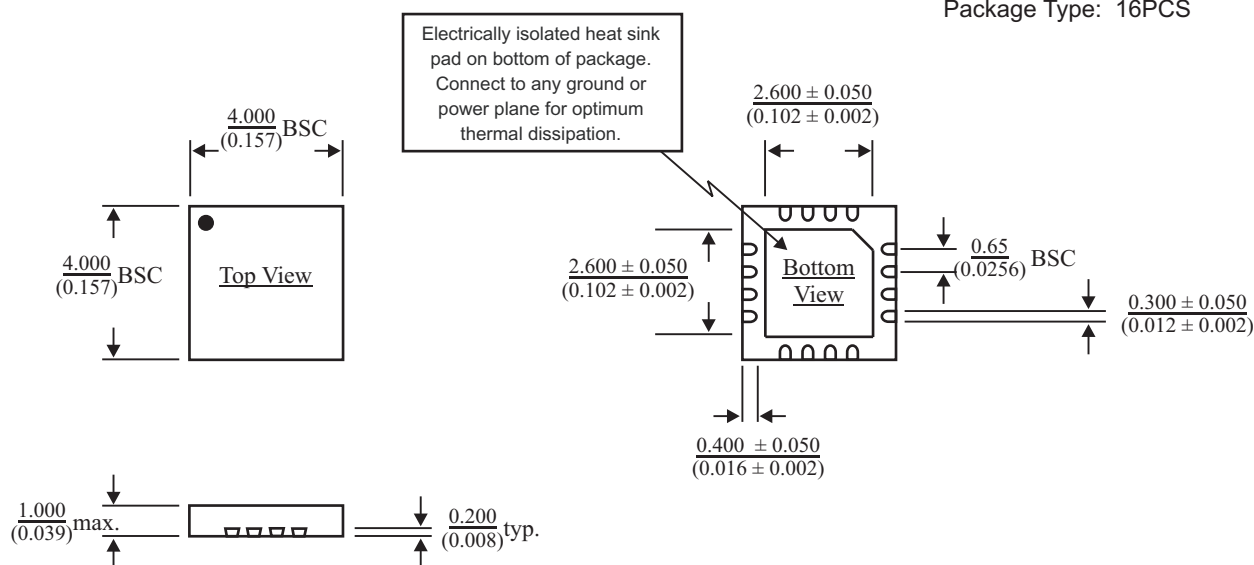
Package Type: 8HN



### 16-PIN PLASTIC CHIP-SCALE PACKAGE

millimeters(inches)

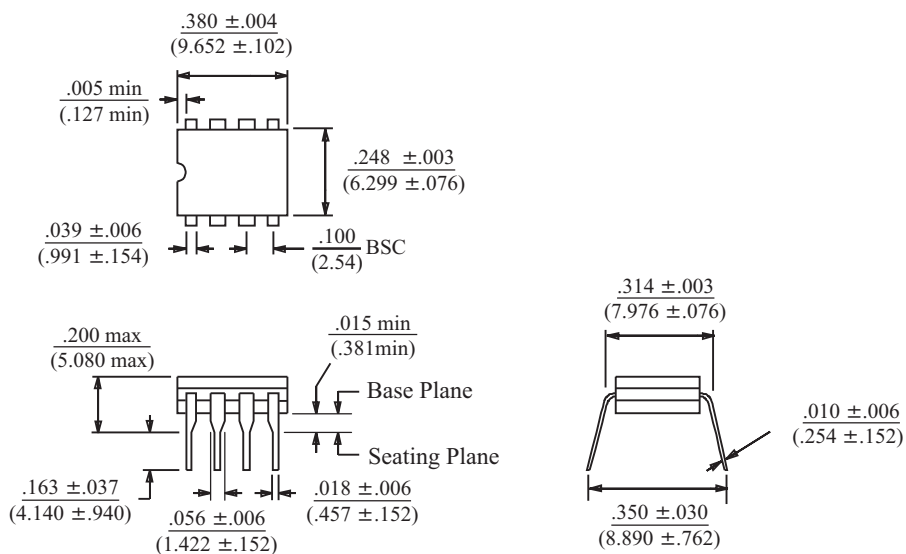
Package Type: 16PCS



**8-PIN CERDIP**

*inches (millimeters)*

Package Type: 8D



BSC = "Basic Spacing between Centers"  
is theoretical true position dimension and  
has no tolerance. (JEDEC Standard 95)