(ISO9001:2008)

OLED 模组

型　　号：HGS128646-Y-EH

版　　本：B

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杭州佳显科技有限公司

版本.	日期	内容	备注
A	2010.01.12	第一版	
	2011.01.24	在串口模式，/RD 接高电平	
B	2012.05.02	更新第 6 节示例程序	

产品编码规则

HG 320240 C – B - LW H- NV- L4- TPSD- U- T

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11)

(1):产品序列号
- HC→字符
- HG→SMT/COB 图形单色
- HGT→TAB 图形单色
- HGO→COG 图形单色
- HGR→ COLOR STN
- HGF→TFT
- HGS→OLED
- HCS→字符型 OLED

(2):规格
- 字符→字符数/每行*行数
- 图形→点/每行*点/每列

(3):产品序列号

(4):显示模式

LCD 模块：
- 省略→STN 黄绿模式
- G→STN 灰模式
- B→STN 蓝模式
- F→FSTN 半透半反
- T→FSTN 透射

OLED 模块：
- Y→黄字
- G→绿字
- B→蓝字
- W→白字

(5):背光类型
- 省略→无背光
- LY→LED 黄绿底光
- SY→LED 黄绿侧光
- LW→LED 白光
- SW→LED 超亮白光
- LB→LED 蓝光
- LR→LED 红光
- LA→LED 琥珀光
- LG→LED 绿光
- EB→EL 蓝光
- EG→EL 绿光
- EW→EL 白光
- CW→CCFL 白光

(6):温度范围
- 省略→常温
- H→宽温
- EH→特宽温

(7):电源
- 省略→5V 单电源
- NV→5V 双电源
- SV→5V 带温度补偿
- LV→3.0/3.3V 单电源
- LNV→3.0/3.3V 双电源
- LSV→3.0/3.3V 带温度补偿
- OV→单电源，V0 不接

(8):背光输入电压说明，请参照液晶详细资料

(9):特殊编号
- 省略→无触摸屏/并行/全屏
- TP→带触摸屏
- S→串行通信
- D→分屏

(10):视角
- 省略→6:00
- U→12:00
- L→9:00
- R→3:00

(11):内部编号

目录

1. 简介

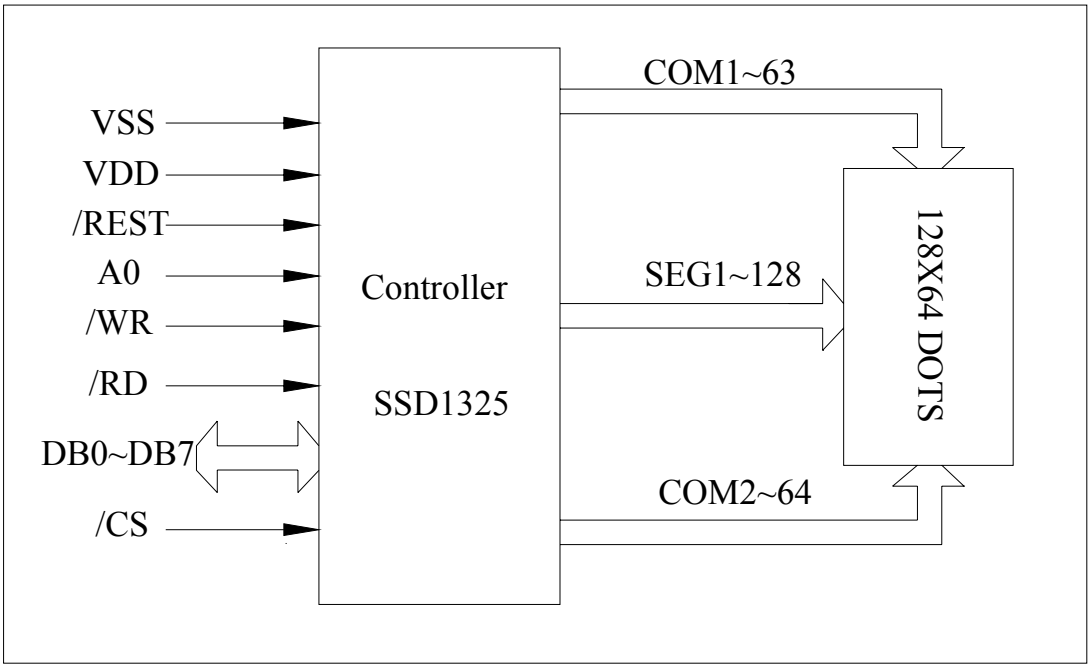
1.1 模块规格

项目	规格
显示类型	OLED/黄字
数据输入	8-bits 80、串行
占空比	1/64
驱动 IC	SSD1325
外壳	0.7 T
工作温度	-30 °C ~70 °C
储存温度	-40 °C ~ 80 °C
其他	

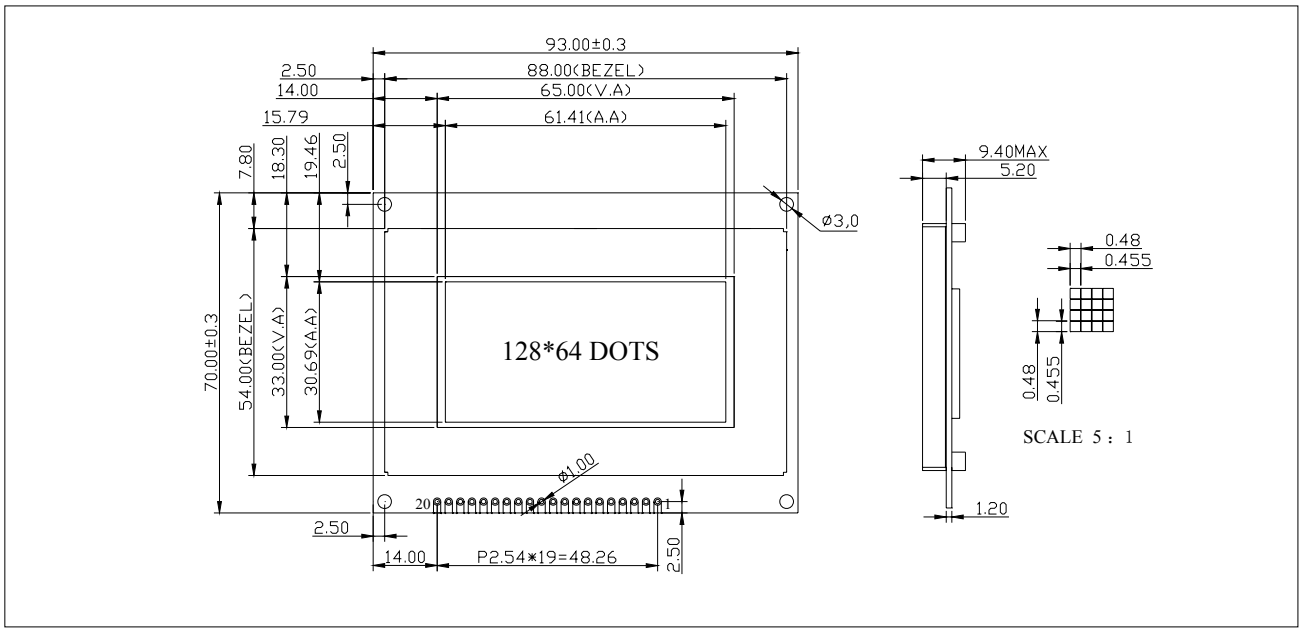
1.2 尺寸参数

项目	规格	单位	备注
外形尺寸	93.0(W)×70.0(H)×9.4MAX.(T)	mm	
可视区	65.0(W)×33.0(H)	mm	
有效区	61.41(W)×30.69(H)	mm	
点阵	128 DOTS×64 DOTS	---	
点距离	0.48(W)×0.48(H)	mm	
点大小	0.455(W)×0.455(H)	mm	

1.3 原理结构图



1.4 模块外观图



1.5 接口定义

编号	符号	电平	功能
1	VSS	0V	接地
2	VDD	+5.0V	逻辑电压
3	V0	--	空脚
4	A0	H/L	数据/指令选择
5	/WR	L	写信号
6	/RD	L	读信号
7~14	DB0~DB7	H/L	数据线 串行:D1--SI D0--SCL
15	/CS	L	使能信号
16	/REST	L	复位信号，低有效
17	M80	H/L	M80 MS:接口选择 11: 8080 00: 串行
18	MS	H/L	
19	NC	--	空脚
20	FG	--	框架接地

注意：在串口模式，/WR、DB3~DB7 接地，DB2 空脚，/RD 接高。

2. 最大范围

（Ta=25 °C, VSS=0V）

参量	符号	范围	单位
电源电压	V_{DD}-V_{SS}	-0.3 ~ 5.5	V
OLED 显示电压	V_{DD}～V_0	0 ~ 16.0	V
输入电压	V_{IN}	V_{SS} ~ V_{DD}	V
工作温度	Topr	-30 ~70	°C
储存温度	Tstg	-40 ~ 80	°C

3. 光电特性

3.1 电特性

（Ta=25 °C ,VSS=0V）

项目	符号	条件	最小值	典型值	最大值	单位	备注
逻辑工作电压	V_{DD} –V_{SS}	--	4.5	5.0	5.5	V	
输入高电平	V_{IH}	--	0.8 V_{DD}	--	--	V	
输入低电平	V_{IL}	--	--	--	0.2 V_{DD}	V	
输出高电平	V_{OH}	--	0.9 V_{DD}	--	--	V	
输出低电平	V_{OL}	--	--	--	0.1 V_{DD}	V	
逻辑工作电流	I_{DD}	NOTE	--	150	--	mA	
OLED 显示电压	V_{CC}	Ta=25 °C	14.25	15.0	15.75	V	

NOTE: V_{DD}= +5.0V, V_{CC}=15.0V, (V_{CC} 由模块内部产生，无需外加输入)50% 像素点点亮。

为了延长 OLED 模组的使用寿命，建议 OLED 亮度设置为 40H。

3.2 光特性

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BRIGHTNESS	Lbr	With Polarizer	70	100	--	Cd/m^2
C.I.E.(YELLOW)	(X) (Y)	Without Polarizer	0.44 0.46	0.48 0.50	0.52 0.54	
DARK ROOM CONTRAST	CR		--	>2000:1	--	
VIEW ANGLE			>160	--	--	degree

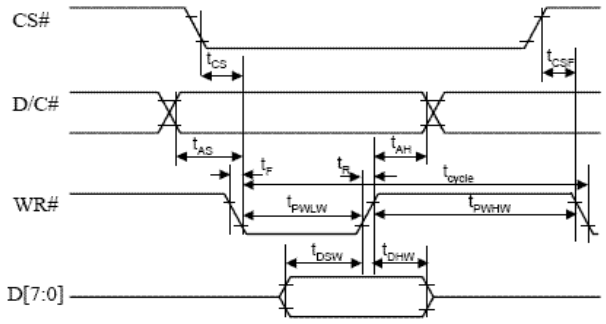
*Optical measurement taken at VDD=2.8V,VCC=15.0V.

4.时序特性

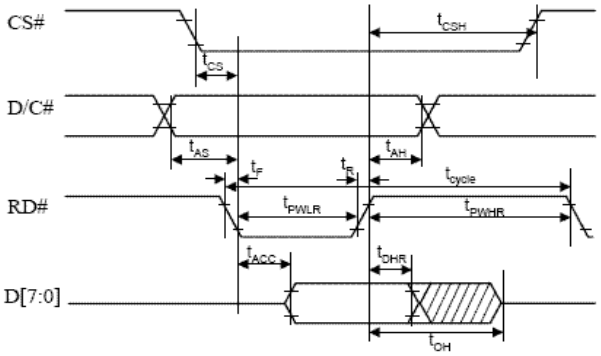
4.1 80 时序:

Symbol	Description	Min.	Max.	Unit
tcycle	Clock cycle time	300	-	ns
tAS	Address setup time	10	-	ns
tAH	Address hold time	0	-	ns
tDSW	Write data setup time	40	-	ns
tDHW	Write data hold time	15	-	ns
tDHR	Read data hold time	20	-	ns
tOH	Output disable time	-	70	ns
tACC	Access time	-	140	ns
tPWLR	Read low time	120		ns
tPWLW	Write low time	60		ns
tPWHR	Read high time	60		ns
tPWHW	Write high time	60		ns
tR	Rise time	-	15	ns
tF	Fall time	-	15	ns
tCS	Chip select setup time	0	-	ns
tCSH	Chip select hold time to read signal	0	-	ns
tCSF	Chip select hold time	20	-	ns

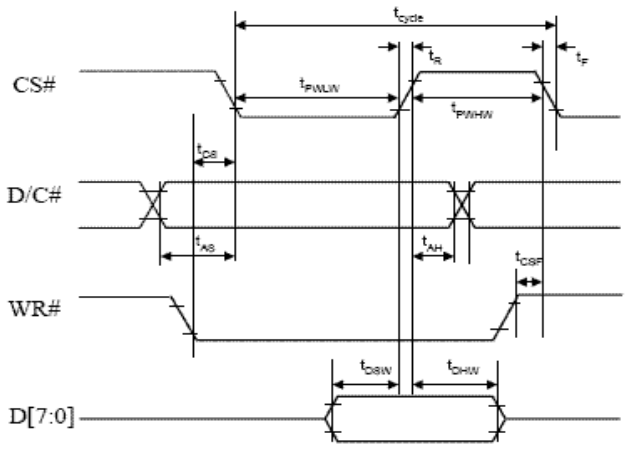
Write cycle (Form 1)



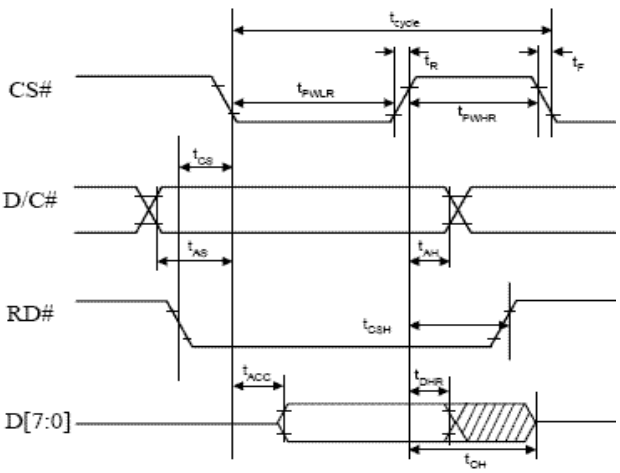
Read cycle (Form 1)



Write cycle (Form 2)

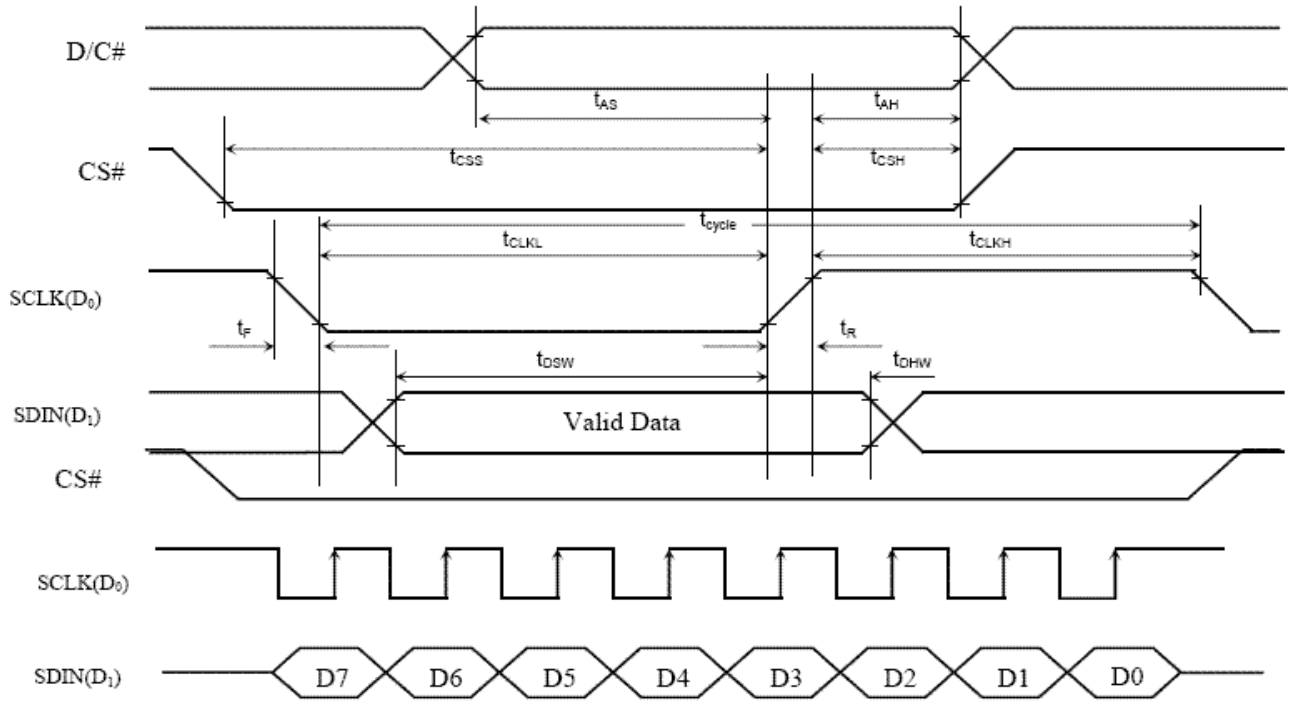


Read cycle (Form 2)



4.2 串行时序:

Symbol	Description	Min.	Max.	Unit
tcycle	Clock cycle time	250	-	ns
tAS	Address setup time	150	-	ns
tAH	Address hold time	150	-	ns
tCSS	Chip select setup time	120	-	ns
tCSH	Chip select hold time	60	-	ns
tDSW	Write data setup time	100		ns
tDHW	Write data hold time	100	-	ns
tCLKL	clock low time	100	-	ns
tCLKH	clock high time	100	-	ns
tR	Rise time	-	15	ns
tF	Fall time	-	15	ns



5. 控制器指令及功能介绍

5.1 FUNCTION DESCRIPTIONS

SSD1325 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6.

Table 6 : MCU Interface assignment under different bus interface mode：

Pin name / Bus interface	Data/Command interfcae								Control signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie High	Tie LOW	CS#	D/C#	RES#

5.1.1 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Table 8: Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 37 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics
Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

Table 9: Control pins of 8080 interface (Form 2)

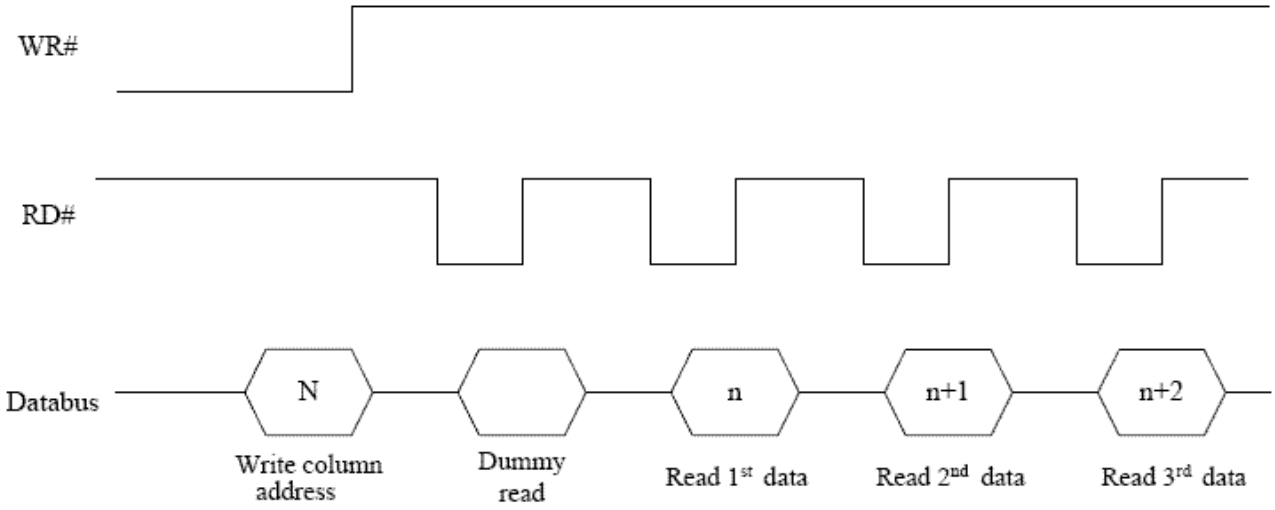
Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

(4) Refer to Figure 38 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8.

Figure 8: Display data read back procedure - insertion of dummy read



5.1.2 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7and R/W# can be connected to an external ground. E must be connected to an external high level.

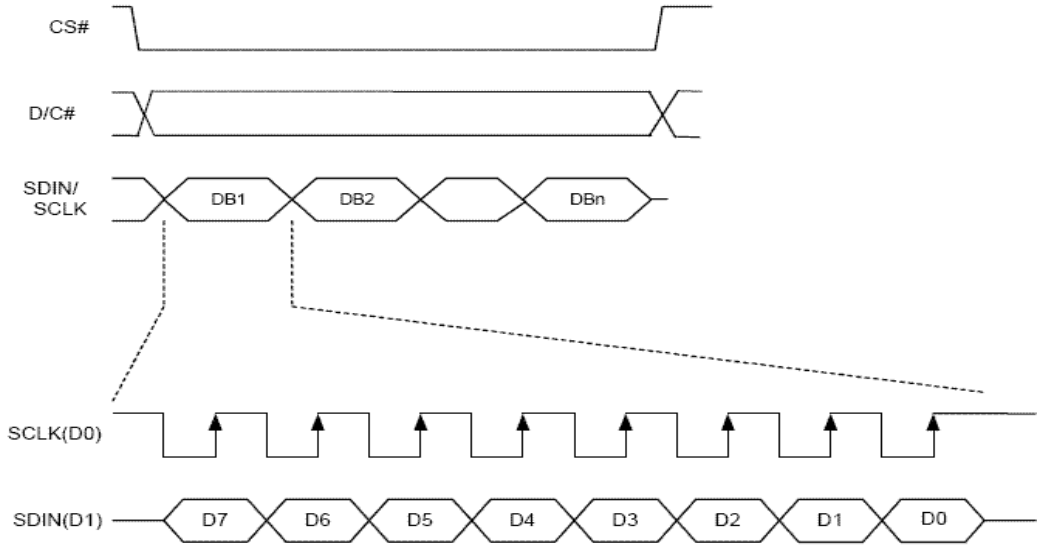
Table 10: Control pins of Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie HIGH	Tie LOW	L	L
Write data	Tie HIGH	Tie LOW	L	H

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 9: Display data write procedure in SPI mode



5.2 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, the input at D7-D0 is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D7-D0 is interpreted as a Command which will be decoded and be written to the corresponding command register.

5.3 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 80 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 40h

5.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 11 to Table 15 show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D5117, D5118, D5119 represent the 128x80 data bytes in the GDDRAM.

Table 11 shows the GDDRAM map under the following condition:

• Command “Set Re-map” A0h is set to:

Disable Column Address Re-map (A[0]=0)
Disable Nibble Re-map (A[1]=0)
Enable Horizontal Address Increment (A[2]=0)

Disable COM Re-map (A[4]=0)

• Display Start Line=00h

• Data byte sequence: D0, D1, D2 … D5119

Table 11 : GDDRAM address map 1

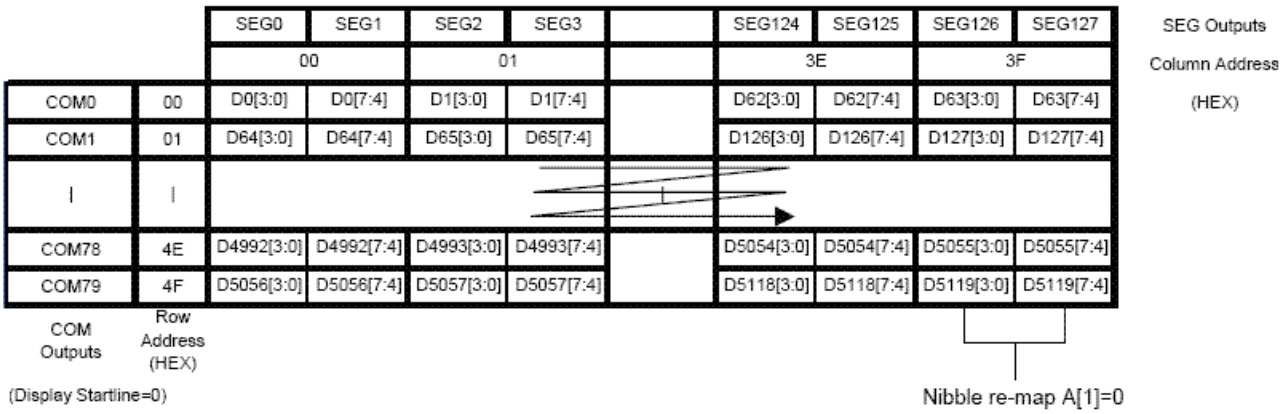


Table 12 shows the GDDRAM map under the following condition:

• Command “Set Re-map” A0h is set to:

Disable Column Address Re-map (A[0]=0)

Disable Nibble Re-map (A[1]=0)

Enable Vertical Address Increment (A[2]=1)

Disable COM Re-map (A[4]=0)

• Display Start Line=00h • Data byte sequence: D0, D1, D2 … D5119

Table 12 : GDDRAM address map 2

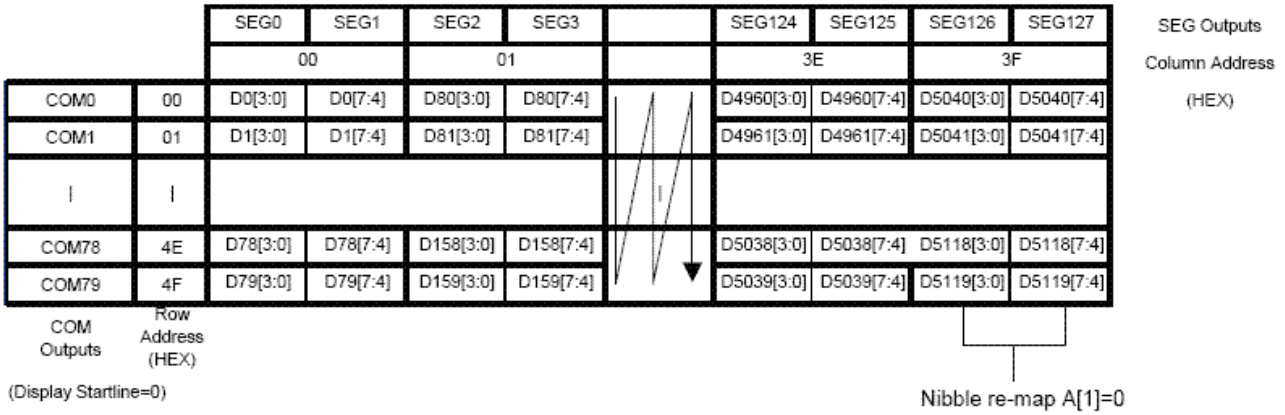


Table 13 shows the GDDRAM map under the following condition:

• Command “Set Re-map” A0h is set to:

Enable Column Address Re-map (A[0]=1)

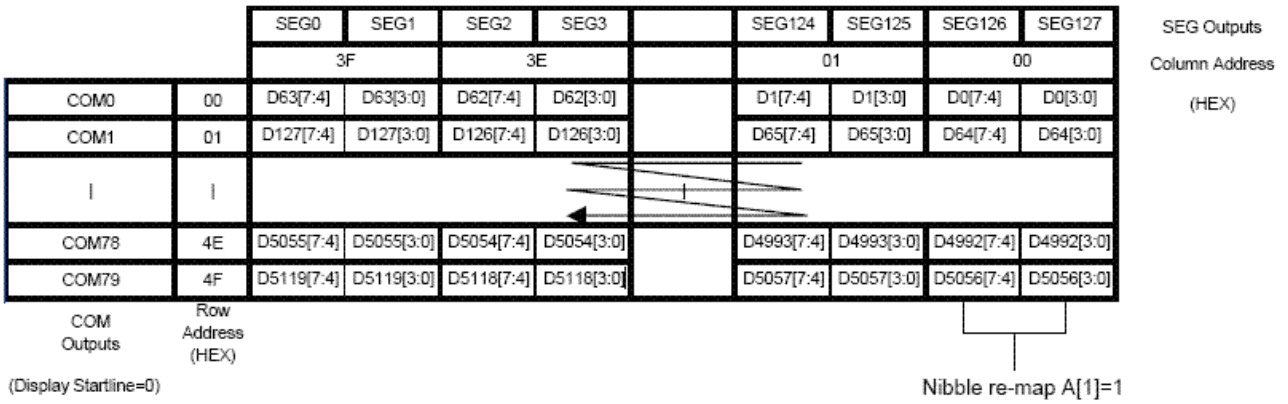
Enable Nibble Re-map (A[1]=1)

Enable Horizontal Address Increment (A[2]=0)

Disable COM Re-map (A[4]=0)

• Display Start Line=00h • Data byte sequence: D0, D1, D2 … D5119

Table 13 : GDDRAM address map 3



For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Table 14 shows the example in which the display start line register is set to 10h with the following condition:

• Command “Set Re-map” A0h is set to:

Disable Column Address Re-map (A[0]=0)
Disable Nibble Re-map (A[1]=0)
Enable Horizontal Address Increment (A[2]=0)
Enable COM Re-map (A[4]=1)

• Display Start Line=10h (corresponds to COM15)

• Data byte sequence: D0, D1, D2 … D5119

Table 14 : GDDRAM address map 4

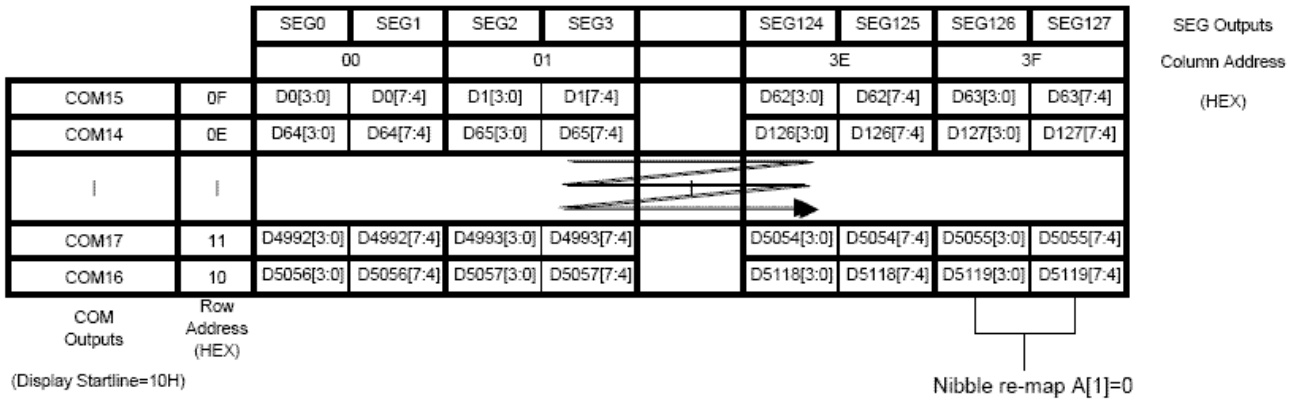


Table 15 shows the GDDRAM map under the following condition:

• Command “Set Re-map” A0h is set to:

Disable Column Address Re-map (A[0]=0)
Disable Nibble Re-map (A[1]=0)
Enable Horizontal Address Increment (A[2]=0)
Disable COM Re-map (A[4]=0)

• Display Start Line=00h

• Column Start Address=01h

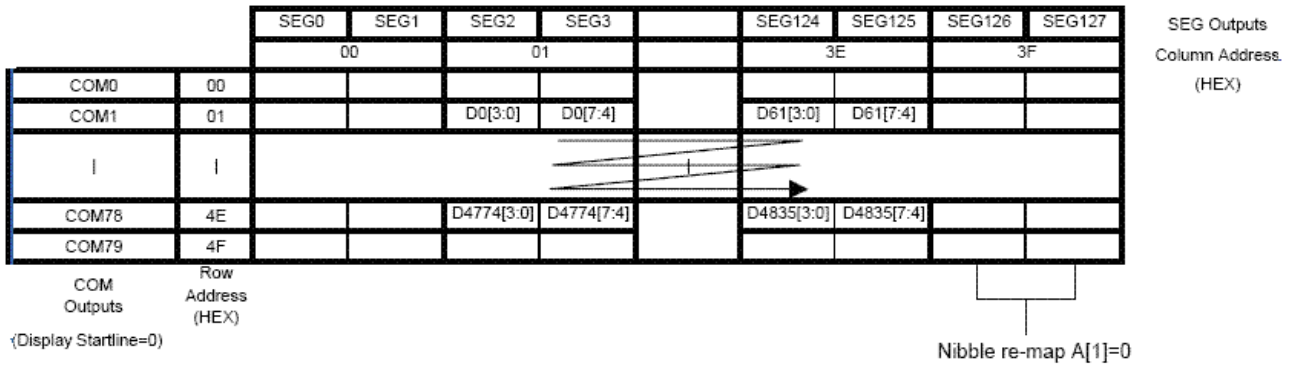
• Column End Address=3Eh

• Row Start Address=01h

• Row End Address=4Eh

• Data byte sequence: D0, D1, D2 … D4835

Table 15 : GDDRAM address map 5



Note

(1)Please refer to Table 18 for the details of setting command “Set Re-map”A0h.

(2) The “Display Start Line” is set by the command “Set Display Start Line” A1h and please refer to Table 18 for the setting details

(3) The “Column Start/End Address” is set by the command “Set Column Address” 15h and please refer to Table 18 for the setting details

(4) The “Row Start/End Address” is set by the command “Set Row Address” 75h and please refer to Table 18 for the setting detail

5.5 Gray Scale Decoder

There are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, GS0 has no pre-charge (phase 2) and no current drive (phase 3). Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

Table16 : Gray scale pulse width set table

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
. . .	. . .	. . .
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

Figure 15 : Gray scale pulse width set diagram

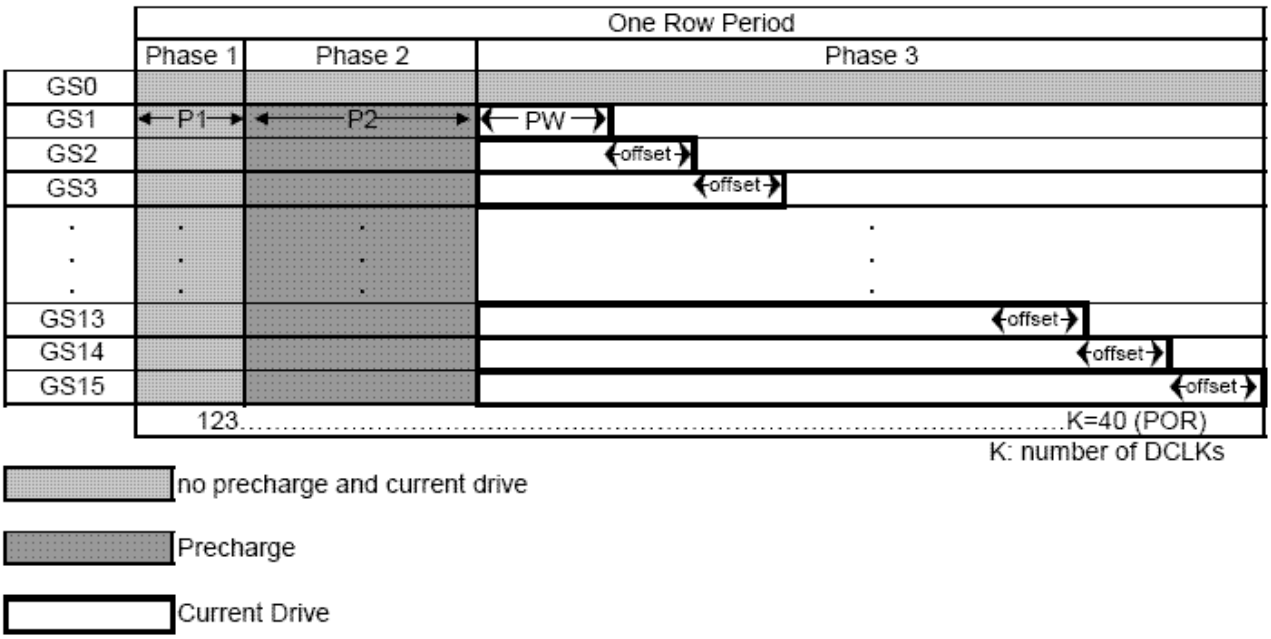


Table 17 : Gray scale pulse width default values

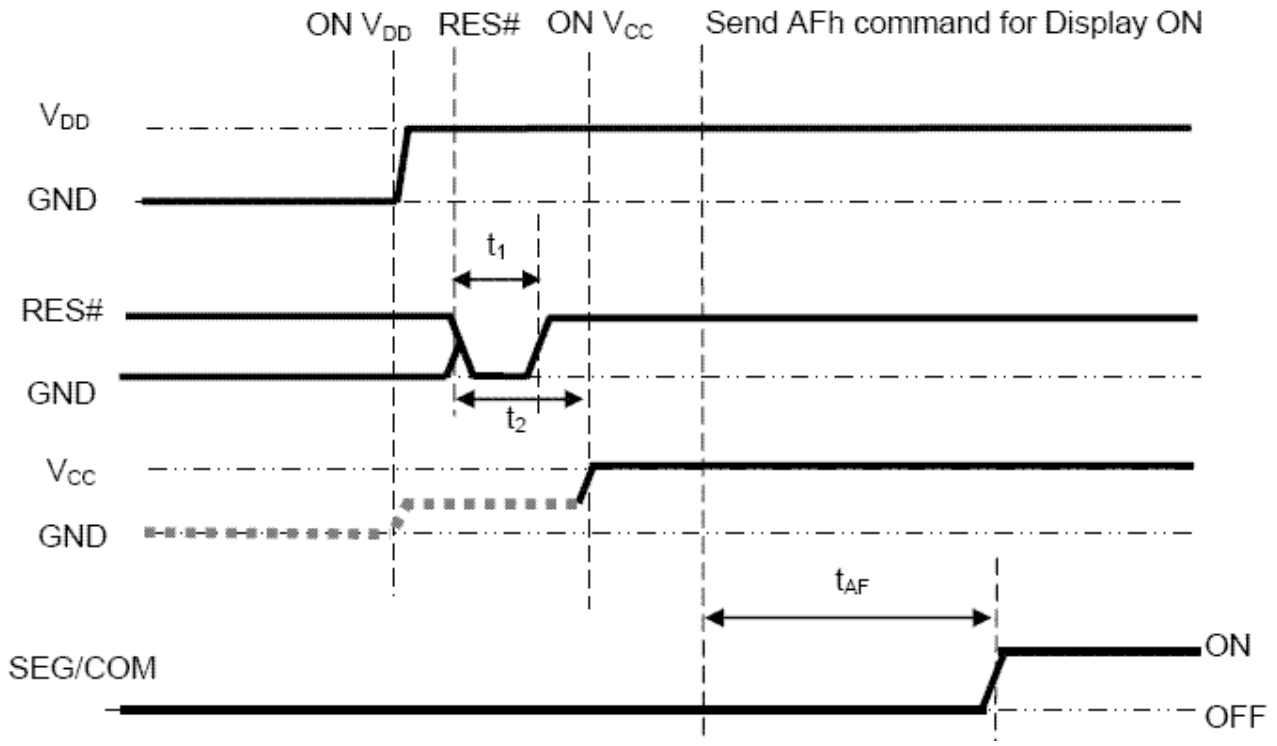
RESET	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29

5.6 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1325.

Power ON sequence:

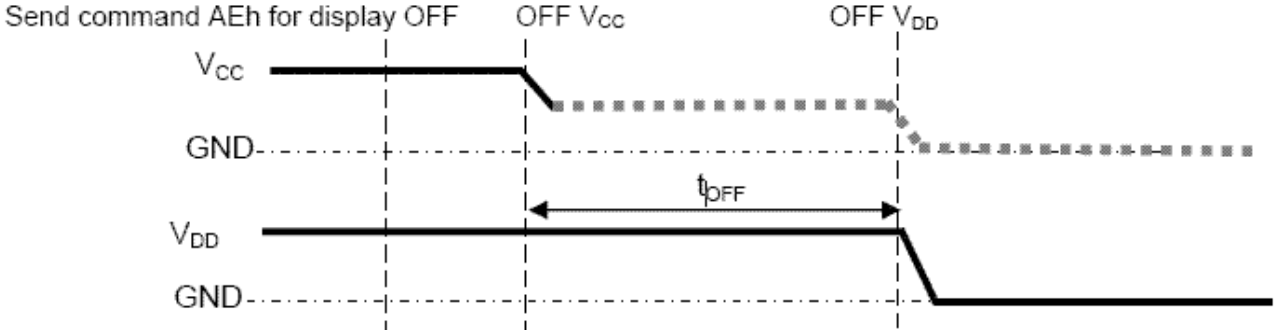
1. Power ON VDD.
2. After VDD become stable, set RES# pin LOW (logic LOW) for at least 3us (t1) and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW), wait for at least 3us (t2). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (tAF).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF VCC. (1), (2)
4. Wait for tOFF. Power OFF VDD. (where Minimum tOFF=0ms, Typical tOFF=100ms)

Figure 17 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between VDD and VCC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in Figure 16 and Figure 17.

(2) VCC should be kept float when it is OFF.

5.7 COMMAND TABLE

Table 18: Command Table

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fundamental Command Table											
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00h Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row address	Second command A[6:0]sets the row start address from 0-79, RESET = 00h Third command B[6:0] sets the row end address from 0-79, RESET = 4Fh
0 0	81 A[6:0]	1 *	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase The level is set to 40h after RESET
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84h = Quarter Current Range (RESET) 85h = Half Current Range 86h = Full Current Range
0 0	A0 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (RESET) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (RESET) A[2]=1, Vertical Address Increment
											A[4]=0, Disable COM Re-map disable (RESET) A[4]=1, Enable COM Re-map A[5]=0, Reserved (RESET) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (RESET) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-79 Display start line register is reset to 00h after RESET
0 0	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-79 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Normal Display (RESET) A5h = Entire Display ON,

Fundamental Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
											all pixels turns ON in GS level 15 A6h = Entire Display OFF, all pixels turns OFF A7h = Inverse Display
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 1	1 A_0	Set Master Configuration	A[0] = 0, Select external V_{CC} supply A[0] = 1, Reserved (RESET) **Note** (1) Bit A[0] **must be** set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display ON	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display OFF	AFh = Display ON
0 0	B0 A[5:0]	1 *	0 *	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET) A[5:0] = 28h, Enable pre-charge compensation
0 0 0	B1 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	0 A_1 *	1 A_0 *	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h Note (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Row Period (set frame frequency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)
0 0 0	B3 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	1 A_1 *	1 A_0 *	Set Display Clock Divide Ratio / Oscillator Frequency	The lower nibble (A[3:0]) of the next command defines the divide ratio (D) of display clock (DCLK) Divide ratio (D)=A[3:0]+1 (A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2)

Fundamental Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
											The higher nibble (A[7:4]) of the next command sets the Oscillator Frequency Oscillator Frequency increases with the value of A[7:4] and vice versa Range: 0000b~1111b RESET= 0100b represents 655KHz, typical step value: 5% of previous value
0	B4	1	0	1	1	0	1	0	0	Set Pre-charge	A[2:0] = 0 (RESET)
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0	Compensation Level	A[2:0] = 3h, Recommended level
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below:
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		A[2:0] = Gray scale level of GS1, RESET=1
0	B[6:4]	*	B_6	B_5	B_4	*	*	*	*		B[2:0] = Gray scale level of GS2, RESET=1
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		B[6:4] = Gray scale level of GS3, RESET=1
0	C[6:4]	*	C_6	C_5	C_4	*	*	*	*		C[2:0] = Gray scale level of GS4 RESET=1
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		C[6:4] = Gray scale level of GS5, RESET=1
0	D[6:4]	*	D_6	D_5	D_4	*	*	*	*		D[2:0] = Gray scale level of GS6, RESET=1
0	E[2:0]	*	*	*	*	*	E_2	E_1	E_0		D[6:4] = Gray scale level of GS7, RESET=1
0	E[6:4]	*	E_6	E_5	E_4	*	*	*	*		E[2:0] = Gray scale level of GS8, RESET=1
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		E[6:4] = Gray scale level of GS9, RESET=1
0	F[6:4]	*	F_6	F_5	F_4	*	*	*	*		F[2:0] = Gray scale level of GS10, RESET=1
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		F[6:4] = Gray scale level of GS11, RESET=1
0	G[6:4]	*	G_6	G_5	G_4	*	*	*	*		G[2:0] = Gray scale level of GS12, RESET=1
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		G[6:4] = Gray scale level of GS13, RESET=1
0	H[6:4]	*	H_6	H_5	H_4	*	*	*	*		H[2:0] = Gray scale level of GS14, RESET=1 H[6:4] = Gray scale level of GS15, RESET=1
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level, A[7:0] 1xxxxxxx connects to V_{COMH} (RESET) 001xxxxx 1.0 * V_{REF} 00000000 0.51* V_{REF} 00000001 0.52* V_{REF} ..... 00011111 0.84* V_{REF}
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Second command A[4:0] sets the V_{COMH} voltage level , A[4:0] 00000 0.51*V_{REF} 00001 0.52* V_{REF} ..... 11101 0.81* V_{REF} (RESET) 11110 0.82* V_{REF} 11111 0.84* V_{REF}
0	A[4 :0]	*	*	0	A4	A3	A2	A1	A0		
0	BF	1	0	1	1	1	1	1	1	Set Segment Low Voltage (VSL)	Second command A[3:0] sets the VSL voltage as follow: A[3:0] = 0010 kept VSL pin NC A[3:0] = 1110 (RESET) connect a capacitor between VSL pin and V_{SS}
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Table 19: Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	23	0	0	1	0	0	0	1	1	Graphic Acceleration Command Options	A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET) A[1] = 0b: Disable x-wrap(RESET) A[1] = 1b: Enable wrap around in x-direction during copying and scrolling A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0	A[4:0]	*	*	*	A_4	*	*	A_1	A_0		
0	24	0	0	1	0	0	1	0	0	Draw Rectangle	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[7:0]: Set Gray scale pattern E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 33 for the gray scale pattern setting examples. **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	25	0	0	1	0	0	1	0	1	Copy	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[5:0]: Column Address of New Start F[6:0]: Row Address of New Start **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$ (3) $0 \le E \le 63$ (4) $0 \le F \le 79$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[6:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Graphic acceleration command										
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0 0 0	26 A[5:0] B[6:0] C[1:0]	0 * * *	0 * B_6 *	1 A_5 B_5 *	0 A_4 B_4 *	0 A_3 B_3 *	1 A_2 B_2 *	1 A_1 B_1 C_1	0 A_0 B_0 C_0	Horizontal Scroll	A[5:0]: 1~63 horizontal offset in number of 2~127 column 0 no horizontal scroll B[6:0]: 2~80 number of rows to be H-scrolled C[1:0]: scrolling time interval 00b 12 frames 01b 64 frames 10b 128 frames 11b 256 frames **Note:** (1) Scrolling operates during display ON. (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Stop Moving	This command deactivates the scrolling action. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal Scroll command 26h. **Note** (1) The "wrap around in x-direction" function must be enabled before scrolling start. i.e. Bit A{1} of command 23h must be set to 1b before issuing 2F command.

Table 20: Read Command Table
(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1$ D_0	Status Register Read	D7 = 0:reserved D7 = 1:reserved D6 = 0:indicates the display is ON D6 = 1:indicated the display is OFF D5 = 0:reserved D5 = 1:reserved D4 = 0:reserved D4 = 1:reserved

Note
(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

5.7.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode.
In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data read. See Figure 5 and Figure 8 in Functional Description.
To write data to the GDDRAM, input LOW to R/W#(WR#) pin and HIGH to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in

write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.
It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

Table 21: Address Increment Table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

5.8 COMMAND DESCRIPTIONS

5.8.1 Fundamental command description

5.8.1.1 Set Column Address (15h)

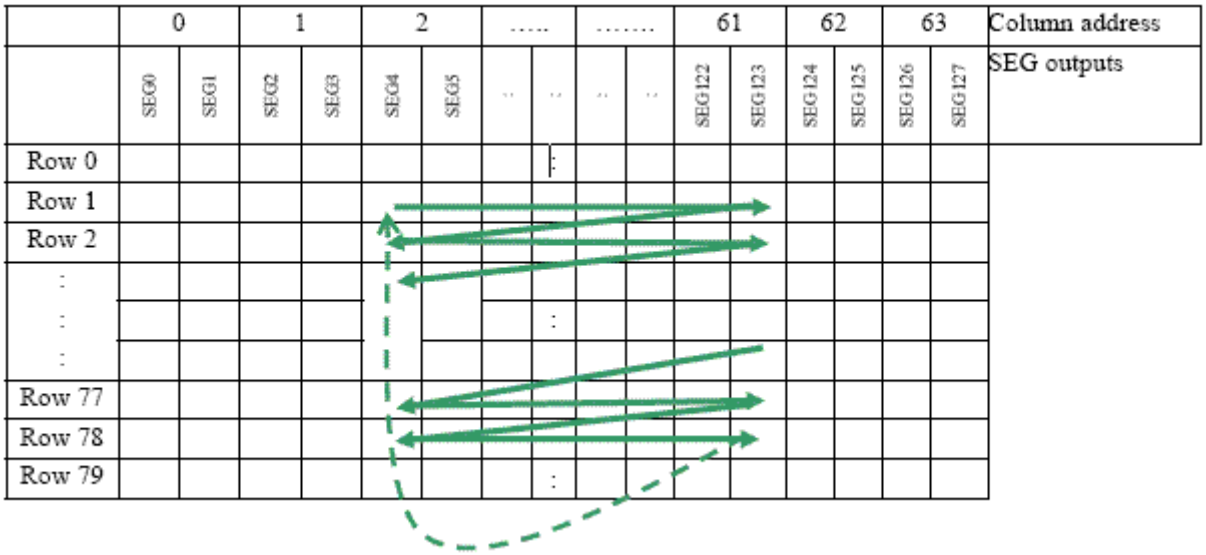
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

5.8.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.
The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 61, row start address is set to 1 and row end address is set to 78; horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 61 and from row 1 to row 78 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (solid line in Figure 18). Whenever the column address pointer finishes accessing the end column 61, it is reset back to column 2 and row address is automatically increased by 1 (solid line in Figure 18). While the end row 78 and end column 61 RAM location is accessed, the row address is reset back

to 1 and the column address is reset back to 2 (dotted line in Figure 18).

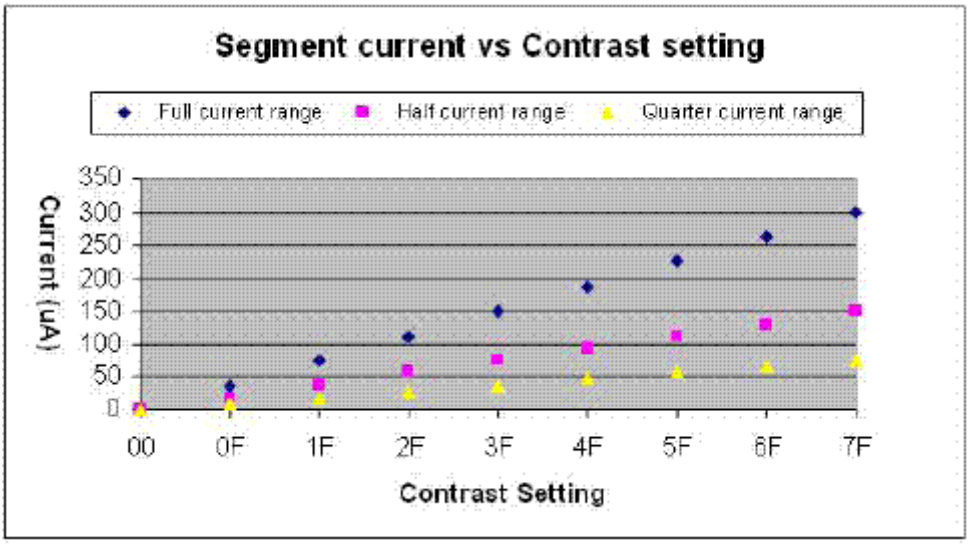
Figure 18 : Example of Column and Row Address Pointer Movement



5.8.1.3 Set Contrast Current (81h)

This command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases with the increase of contrast step. See Figure 19 below.

Figure 19 : Segment current vs Contrast setting



5.8.1.4 Set Current Range (84h, 85h, 87h)

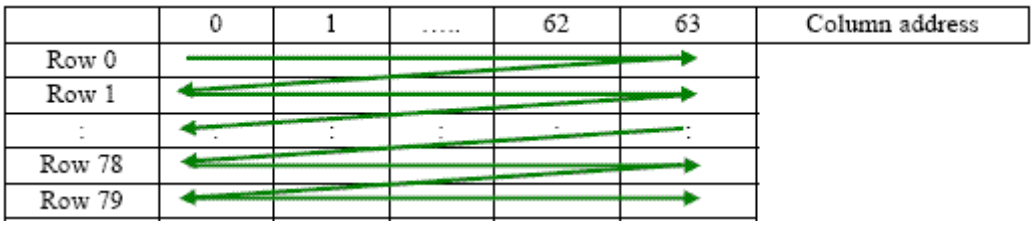
This command is used to select quarter range or half range or full range current mode. With the same contrast level, quarter range mode will give a quarter of the current output of the full range mode. Similar to half range current mode, it will give a half of the current output of the full range mode. See Figure 19. In RESET, quarter range current mode is default.

5.8.1.5 Set Re-map (A0h)

This double command has multiple configurations and each bit setting is described as follows:

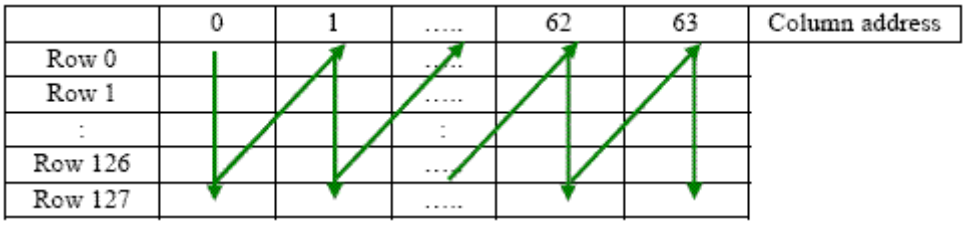
- Column Address Remapping (A[0])
  This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).
- Nibble Remapping (A[1])
  When A[1] is set to 1, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4).
  If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0~127 to SEG127~SEG0 as show in Table 13.
- Address increment mode (A[2])
  When A[2] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 20

Figure 20 : Address Pointer Movement of Horizontal Address Increment Mode



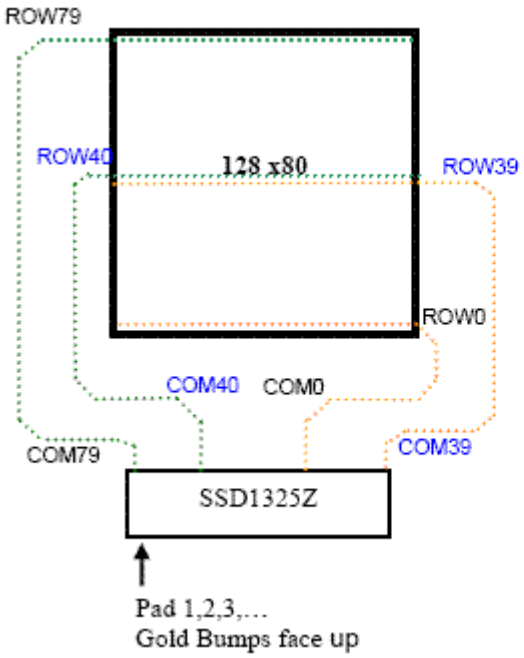
When A[2] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 21.

Figure 21: Address Pointer Movement of Vertical Address Increment Mode



- COM Remapping (A[4]) This bit defines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down (when A[4] is set to 0) or from bottom to up (when A[4] is set to 1). Table 14 shows an example of the using the COM Remapping to perform vertical scrolling.
- Splitting of Odd / Even COM Signals (A[6])
  This bit is made to match the COM layout connection on the panel.
  When A[6] is set to 0, no splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 80MUX ratio):

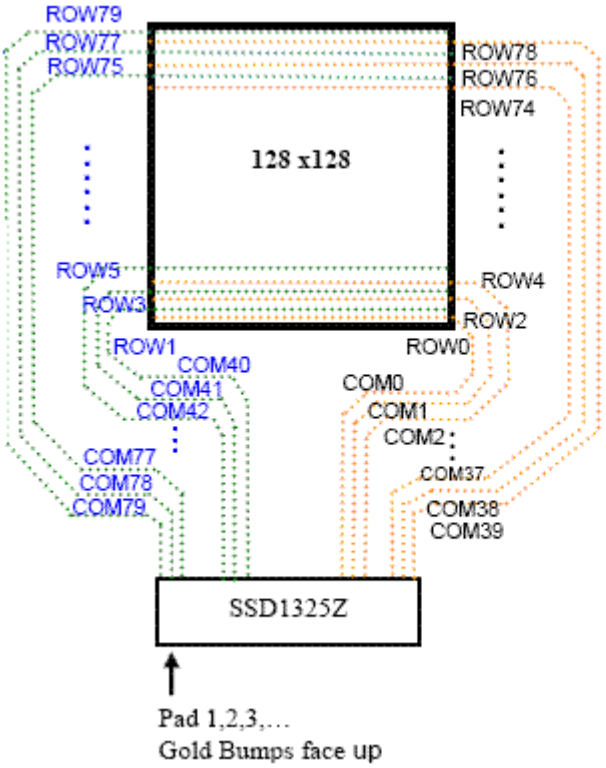
Figure 22: Output pin assignment when command A0h bit A[6]=0.



Output Pin Connection	
SSD1325Z	Panel
COM0	ROW0
COM1	ROW1
COM2	ROW2
COM3	ROW3
:	:
COM39	ROW39
COM40	ROW40
:	:
COM77	ROW77
COM78	ROW78
COM79	ROW79

When A[6] is set to 1, splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

Figure 23 : Output pin assignment when command A0h bit A[6]=1.



Output Pin Connection	
SSD1325Z	Panel
COM0	ROW0 (Even)
COM1	ROW2
COM2	ROW4
:	:
COM37	ROW74
COM38	ROW76
COM39	ROW78
COM40	ROW1 (Odd)
COM41	ROW3
COM42	ROW5
:	:
COM77	ROW75
COM78	ROW77
COM79	ROW79

5.8.1.6 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 79. Figure 24 shows an example using this command of this command when MUX ratio= 80 and MUX ratio= 54 and Display Start Line = 28. In there, “ROW” means the graphic display data RAM row.

Figure 24: Example of Set Display Start Line with no Remapping

	MUX ratio (A8h) = 80	MUX ratio (A8h) = 80	MUX ratio (A8h) = 54	MUX ratio (A8h) = 54
COM Pin	Display Start Line (A1h) = 0	Display Start Line (A1h) = 28	Display Start Line (A1h) = 0	Display Start Line (A1h) = 28
COM0	ROW0	ROW28	ROW0	ROW28
COM1	ROW1	ROW29	ROW1	ROW29
COM2	ROW2	ROW30	ROW2	ROW30
COM3	ROW3	ROW31	ROW3	ROW31
:	:	:	:	:
:	:	:	:	:
COM23	ROW23	ROW51	ROW23	ROW51
COM24	ROW24	ROW52	ROW24	ROW52
COM25	ROW25	ROW53	ROW25	ROW53
COM26	ROW26	ROW54	ROW26	ROW54
:	:	:	:	:
:	:	:	:	:
COM49	ROW50	ROW77	ROW50	ROW77
COM51	ROW51	ROW78	ROW51	ROW78
COM52	ROW52	ROW79	ROW52	ROW79
COM53	ROW53	ROW0	ROW53	ROW0
COM54	ROW54	ROW1	-	-
COM55	ROW55	ROW2	-	-
:	:	:	:	:
:	:	:	:	:
COM76	ROW76	ROW24	-	-
COM77	ROW77	ROW25	-	-
COM78	ROW78	ROW26	-	-
COM79	ROW79	ROW27	-	-
Display Example				

5.8.1.7 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0~COM79. Figure 25 shows an example using this command when MUX ratio= 80 and MUX ratio= 54 and Display Offset = 28. In there, “Row” means the graphic display data RAM row.

Figure 25: Example of Set Display Offset with no Remapping

	MUX ratio (A8h) = 80	MUX ratio (A8h) = 80	MUX ratio (A8h) = 64	MUX ratio (A8h) = 64
COM Pin	Display Offset (A2h)=0	Display Offset (A2h)=18	Display Offset (A2h)=0	Display Offset (A2h)=18
COM0	ROW0	ROW28	ROW0	ROW28
COM1	ROW1	ROW29	ROW1	ROW29
COM2	ROW2	ROW30	ROW2	ROW30
COM3	ROW3	ROW31	ROW3	ROW31
:	:	:	:	:
:	:	:	:	:
COM23	ROW23	ROW51	ROW23	ROW51
COM24	ROW24	ROW52	ROW24	ROW52
COM25	ROW25	ROW53	ROW25	ROW53
COM26	ROW26	ROW54	ROW26	-
:	:	:	:	:
:	:	:	:	:
COM49	ROW50	ROW77	ROW50	-
COM51	ROW51	ROW78	ROW51	-
COM52	ROW52	ROW79	ROW52	-
COM53	ROW53	ROW0	ROW53	ROW0
COM54	ROW54	ROW1	-	ROW1
COM55	ROW55	ROW2	-	ROW2
:	:	:	:	:
:	:	:	:	:
COM76	ROW76	ROW24	-	ROW24
COM77	ROW77	ROW25	-	ROW25
COM78	ROW78	ROW26	-	ROW26
COM79	ROW79	ROW27	-	ROW27
Display Example				

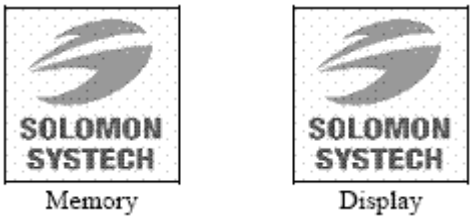
5.8.1.8 Set Display Mode (A4h ~ A7h)

These are single byte commands (A4h ~ A7h) and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display, respectively.

- Normal Display (A4h)

  Reset the "Entire Display ON, Entire Display OFF or Inverse Display" effects and turn the data to ON at the corresponding gray level. Figure 26 shows an example of Normal Display.

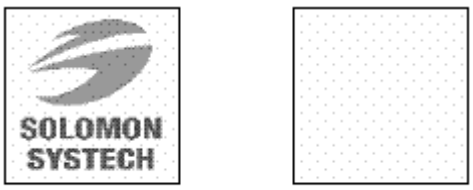
Figure 26: Example of Normal Display



- Set Entire Display ON (A5h)

  Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM, as shown on Figure 27.

Figure 27: Example of Entire Display ON



- Set Entire Display OFF (A6h)
  Force the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM, as shown on Figure 28.

Figure 28 : Example of Entire Display OFF

- Inverse Display (A7h)
  The gray scale level of display data are swapped such that “GS0” <-> “GS15”, “GS1” <-> “GS14”, etc. Figure 29 shows an example of inverse display.

Figure 29: Example of Inverse Display

5.8.1.9 Set Multiplex Ratio (A8h)

This double byte command sets multiplex ratio (MUX ratio) from 16MUX to 80MUX. In RESET, multiplex ratio is 80MUX. Please refer to Figure 24 and Figure 25 for the example of setting different MUX ratio.

5.8.1.10 Set Master Configuration (ADh)

This command selects the external VCC power supply. External VCC power should be connected to the VCC pin. A[0] bit must be set to 0b after RESET. This command will be activated after issuing Set Display ON command (AFh)

5.8.1.11 Set Display ON/OFF (AEh / AFh)

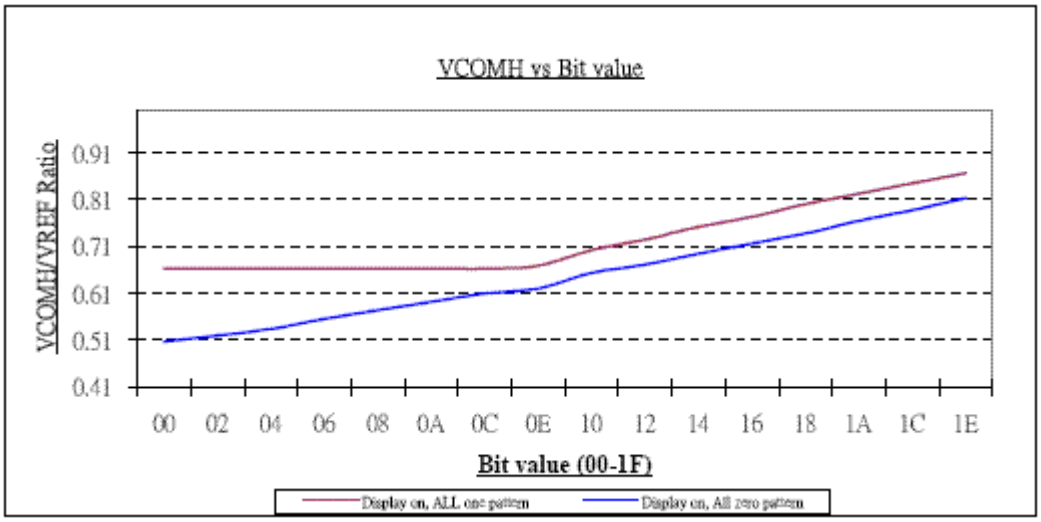
These single byte commands are used to turn the matrix display on the OLED panel display either ON or OFF. For AEh, the display is OFF, the segment and common output are in high impedance state and circuits will be turned OFF. When the sleep mode is set to OFF (AFh), the display is ON.

5.8.1.12 Set VCOMH Voltage (BEh)

This double byte command sets the high voltage level of common pins, VCOMH. The level of VCOMH is programmed with reference to VCC. Please refer to Table 18 and Figure 30for detail

information and breakdown levels of each step.

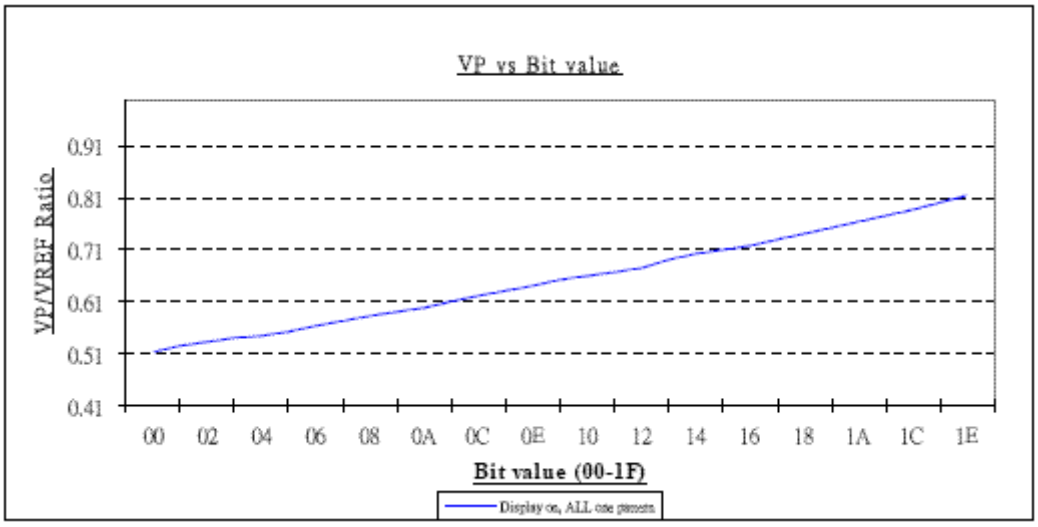
Figure 30 : VCOMH vs Bit value



5.8.1.13 Set Precharge Voltage (BCh)

This double byte command is used to set the pre-charge voltage (phase 2) level. Please refer to Table 18 and Figure 31 for detail information and breakdown levels of each step.

Figure 31 : VP vs Bit value



5.8.1.14 Set Phase Length (B1h)

This is a double byte command. In the second byte of this double command, lower nibble and higher nibble is defined separately. The lower nibble adjusts the phase length of Reset (phase 1). The higher nibble is used to select the phase length of the pre-charge phase (phase 2). The phase length is ranged from 1 to 16 DCLK's. RESET for A[3:0] is set to 3h while reset for A[7:4] is set to 5h. Please refer to Table 18 for detail breakdown levels of each step.

5.8.1.15 Set Row Period (B2h)

This command is used to set the row period. It is defined by multiplying the internal display clock period by the number of internal display clocks per row (valued from 14h to 7Fh), and RESET is 25h. The larger the value, the more precise of each gray scale level can be tuned. See “Gray Scale

Table" command (B8h) for details. Also, it is used to define the frame frequency altogether with the use of "Display Clock Divide Ratio" command (B3h). Row period equals to the sum of phase 1 and phase 2 periods and the pulse width of GS15. See equation in Table 18.

5.8.1.16 Set Display Clock Divide Ratio (B3h)

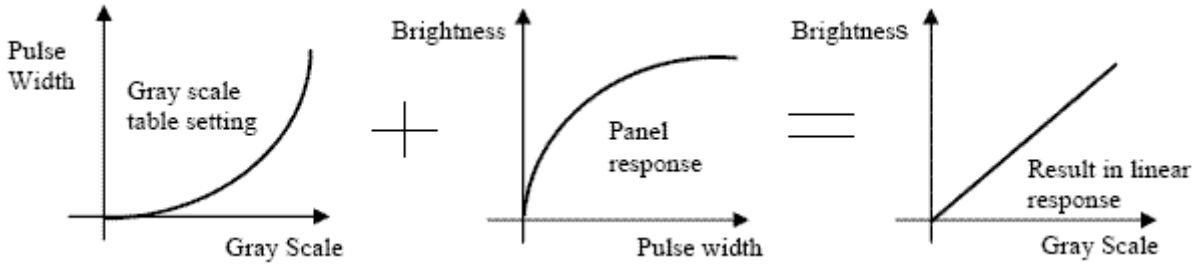
This double command is used to set the frequency of the internal display clocks, DCLK's. It is defined by dividing the oscillator frequency by the divide ratio (valued from 1 to 16). Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. The lower nibble of the second byte is used to select the oscillator frequency. Please refer to Table 18 for detail breakdown levels of each step.

5.8.1.17 Set Gray Scale Table

This command is used to set each individual gray scale level for the display. Except gray scale level GS0 that has no pre-charge and current drive, the pulse width of each gray scale level is programmed with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it is turned ON.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 32 : Example of gamma correction by gray scale table setting



As shown in Table16 and Table 17, GS1 is defined with pulse width equals to the first offset value, L1, select from 0-7 internal display clocks. GS2 is defined with pulse width equals to GS1 plus the next offset value, L2, select from1-8 internal display clocks. Similarly, the next GS level is defined with pulse width equals to its lower one GS level plus the next offset value, select from 1-8 internal display clocks. In normal operation, GS15 should take the full current drive period as its pulse width. Therefore, the row period should be set as the sum of phase 1 period, phase 2 periods, and the pulse width of GS15 with the use of "Row period" command.

5.8.1.18 NOP (E3h)

This is a no operation command.

5.8.1.19 Status register Read

This command is issued by setting D/C# LOW during a data read (refer to Figure 36 to Figure 38 parallel interface waveform). It allows the MCU to monitor the internal status of the chip.

5.8.2 Graphic Acceleration Command Set Description

5.8.2.1 Graphic Acceleration Command Options (23h)

This command has two functions.

- Enable / Disable fill (A[0])

  0 = Disable filling of rectangle in draw rectangle command.

  1 = Enable filling of rectangle in draw rectangle command. (RESET)

- Enable / Disable x-warp (A[1])

  0 = Disable wrap around in x-direction during copying and scrolling

  1 = Enable wrap around in x-direction during copying and scrolling (RESET)

- Enable / Disable reverse copy (A[4])

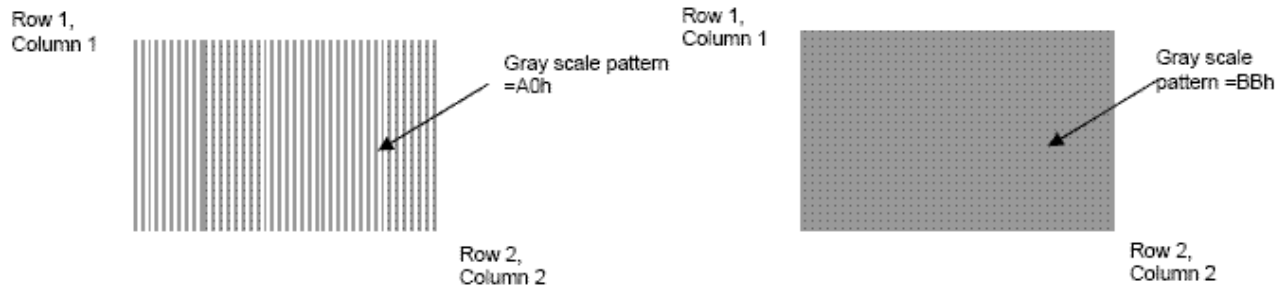
  0 = Disable reverse copy (RESET)

  1 = During copy command, the new image colors are swapped such that “GS0” <-> “GS15”, “GS1” <-> “GS14”, ….

5.8.2.2 Draw Rectangle (24h)

Specify a starting point (Row 1, Column 1) and an ending point (Row 2, Column 2) as well as giving the desire gray scale pattern, a rectangle will then be drawn.

Figure 33 : Example of draw rectangle command



The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 24h
2. Set the starting column coordinates, Column 1. e.g., 01h.
3. Set the starting row coordinates, Row 1. e.g., 01h.
4. Set the finishing column coordinates, Column 9. e.g., 09h
5. Set the finishing row coordinates, Row 5. e.g., 05h
6. Set the gray scale pattern:

   This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level

of the right pixel of each group. Please refer to Figure 33 for the gray scale pattern setting examples.

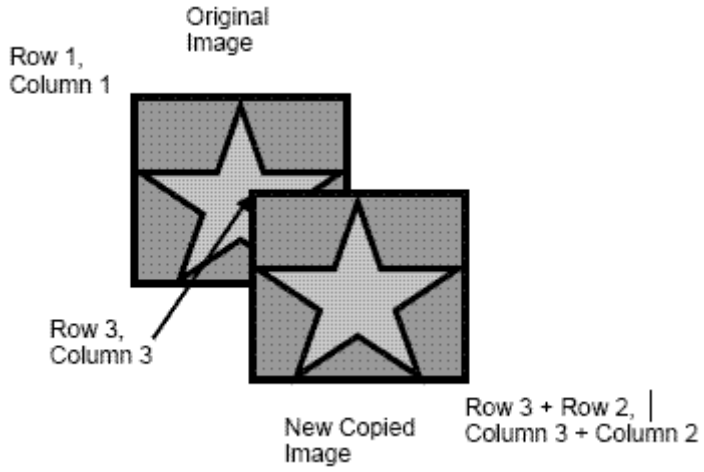
5.8.2.3 Copy (25h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the “copy mode” by execute the command 25h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

Figure 34: Example of copy command

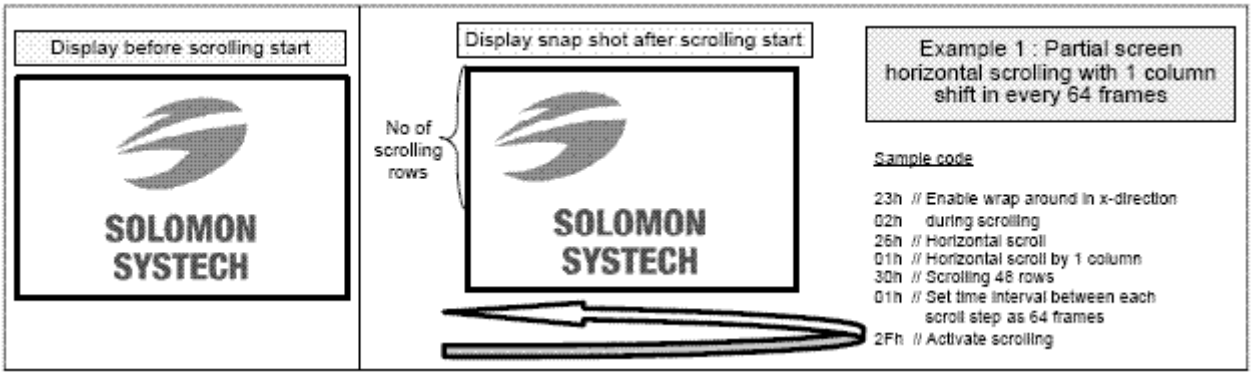


5.8.2.4 Horizontal Scroll (26h)

This command consists of 3 consecutive bytes to set up the scrolling parameters. It determined the horizontal scrolling offset, no of scrolling row and scrolling speed. Some scrolling examples are shown in Figure 35 .

Before issuing this command, the scrolling must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

Figure 35: Scrolling examples



5.8.2.5 Stop Moving (2Eh)

Stop motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

5.8.2.6 Start Moving (2Fh)

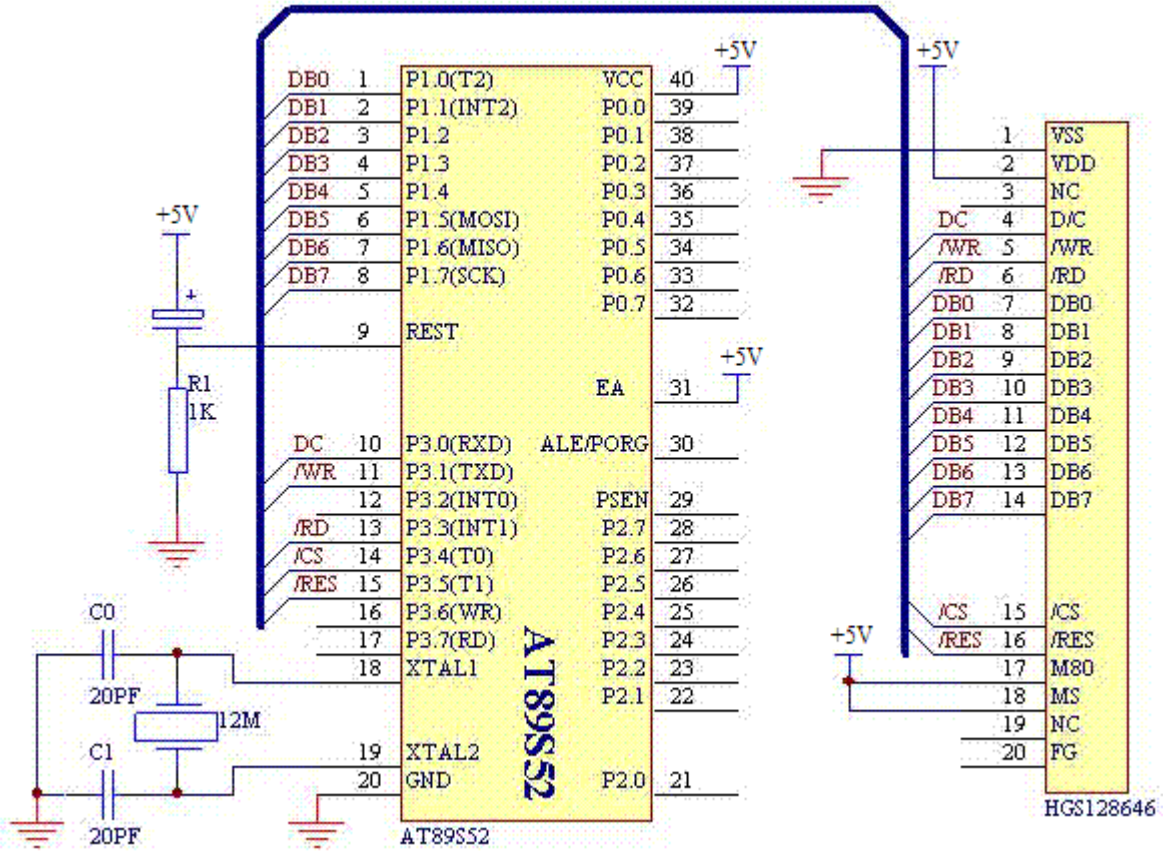
Start motion of scrolling. This command should only be issued after scrolling setup parameters are defined through command 26h and the function of wrap around in x-direction is enabled through 23h.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing scrolling setup parameters

6. 应用参考示例

（1）应用电路：（以 8080 时序为例）



（2）示例程序:

```
#include<reg51.h>
#include <string.h>
#include <intrins.h>
#include <math.h>
#define uchar unsigned char
#define uint unsigned int

#define DATA    P1
sbit CD    = P3^0;
sbit WR1 = P3^1;
sbit RD1 = P3^3;
sbit CS    = P3^4;
sbit RES = P3^5;
//17 18 脚拉高；

uchar RAM_data[4];
uchar code table_88[]={
0x00,0x00,0x00,0xE0,0x10,0x70,0x98,0x70,/*"a",0*/
0x00,0x80,0x80,0xE0,0x90,0x90,0xE0,0x00,/*"b",1*/
0x00,0x00,0x00,0x60,0x90,0x80,0x90,0x60,/*"c",2*/
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,/*" ",3*/
0x00,0x60,0x90,0x90,0x90,0x90,0x60,0x00,/*"0",4*/
0x00,0x60,0x20,0x20,0x20,0x20,0x70,0x00,/*"1",5*/
0x00,0x60,0x90,0x10,0x20,0x40,0xF0,0x00,/*"2",6*/
};// @Adobe 明体，逐行式，顺向；

uchar code table_816[]={
0x00,0x00,0x00,0x18,0x24,0x42,0x42,0x42,0x42,0x4
2,0x42,0x42,0x24,0x18,0x00,0x00,/*"0",0*/
0x00,0x00,0x00,0x10,0x70,0x10,0x10,0x10,0x10,0x1
0,0x10,0x10,0x10,0x7C,0x00,0x00,/*"1",1*/
0x00,0x00,0x00,0x3C,0x42,0x42,0x42,0x04,0x04,0x0
8,0x10,0x20,0x42,0x7E,0x00,0x00,/*"2",2*/
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x0
```

```
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,/*" ",3*/
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x3C,0x42,0x1
E,0x22,0x42,0x42,0x3F,0x00,0x00,/*"a",4*/
0x00,0x00,0x00,0x00,0xC0,0x40,0x40,0x40,0x58,0x64,0x4
2,0x42,0x42,0x42,0x64,0x58,0x00,0x00,/*"b",5*/
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x1C,0x22,0x4
0,0x40,0x40,0x22,0x1C,0x00,0x00,/*"c",6*/
}; // 宋体，逐行式，顺向；
uchar code table_1616[]={
0x40,0x40,0x23,0xFC,0x20,0x40,0x0B,0xFC,0x88,0x
40,0x57,0xFC,0x50,0x00,0x13,0xF8,0x22,0x08,0x23,
0xF8,0xE2,0x08,0x23,0xF8,0x22,0x08,0x22,0x08,0x
22,0x28,0x22,0x10,/*"清",0*/
0x00,0x00,0x40,0x80,0x30,0x80,0x10,0x80,0x0F,0xF
C,0x00,0x80,0x00,0x80,0xE0,0x80,0x21,0x40,0x21,0
x20,0x22,0x18,0x24,0x0C,0x28,0x08,0x50,0x02,0x8F
,0xFC,0x00,0x00,/*"达",1*/
0x01,0x00,0x21,0x10,0x19,0x18,0x0D,0x10,0x09,0x
20,0x01,0x04,0x7F,0xFE,0x04,0x40,0x04,0x40,0x04,
0x40,0x04,0x40,0x08,0x42,0x08,0x42,0x10,0x42,0x2
0,0x3E,0x40,0x00,/*"光",2*/
0x01,0x00,0x01,0x00,0x01,0x00,0x3F,0xF8,0x21,0x0
8,0x21,0x08,0x3F,0xF8,0x21,0x08,0x21,0x08,0x21,0
x08,0x3F,0xF8,0x21,0x08,0x01,0x02,0x01,0x02,0x00
,0xFE,0x00,0x00,/*"电",3*/
}; // 宋体，逐行式，顺向；

uchar code BMP[]={
0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0x
FF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0x80,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01
,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x40,0x00,0x00,0x00,0x00,0x00,0x00,0x01
,0x80,0x04,0x1C,0x78,0x00,0x00,0x00,0xF0,0x40,0x
00,0x01,0x00,0x00,0x1C,0x00,0x01,0x80,0x1C,0x22,
0x84,0x00,0x00,0x01,0x10,0xC0,0x00,0x00,0x00,0x0
0,0x04,0x00,0x01,0x80,0x04,0x22,0x84,0x00,0x00,0
x02,0x01,0x40,0x00,0x00,0x00,0x00,0x04,0x00,0x01
,0x80,0x04,0x02,0x48,0x01,0xB8,0x02,0xE2,0x40,0x
0F,0x87,0x1B,0x87,0x04,0x1E,0x01,0x80,0x04,0x04,
0x78,0x00,0x90,0x03,0x12,0x40,0x04,0x41,0x09,0x0
8,0x84,0x22,0x01,0x80,0x04,0x08,0x84,0x00,0x60,0
x02,0x14,0x40,0x04,0x41,0x06,0x0F,0x84,0x18,0x01
,0x80,0x04,0x10,0x84,0x00,0x60,0x02,0x13,0xE0,0x
04,0x41,0x06,0x08,0x04,0x04,0x01,0x80,0x04,0x22,
0x84,0x00,0x90,0x02,0x10,0x40,0x04,0x41,0x09,0x0
8,0x84,0x22,0x01,0x80,0x1F,0x3E,0x78,0x01,0xD8,0
x01,0xE0,0xE0,0x07,0x87,0xDD,0x87,0x1F,0x3C,0x
01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x04,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x0E,0x00,0x00,0
x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
01,0x80,0x10,0x00,0x00,0x40,0x00,0xC0,0x01,0x00,
0x00,0x04,0x01,0x00,0x00,0x00,0x01,0x80,0x10,0x0
0,0x00,0x40,0x01,0x00,0x01,0x00,0x41,0x04,0x01,0
x00,0x00,0x00,0x01,0x80,0x10,0x00,0x00,0x40,0x01
,0x00,0x01,0x00,0x00,0x04,0x01,0x00,0x00,0x00,0x
01,0x98,0x1E,0x07,0x03,0xC1,0x81,0xC1,0xE1,0xE0
,0x43,0x04,0x81,0x0E,0xC0,0xF0,0x39,0x84,0x11,0x
08,0x04,0x42,0x41,0x02,0x21,0x10,0x41,0x05,0x01,
0x09,0x20,0x88,0x45,0x9C,0x11,0x08,0x04,0x43,0x
C1,0x02,0x21,0x10,0x41,0x07,0x01,0x09,0x20,0x88,
0x45,0xA4,0x11,0x08,0x04,0x42,0x01,0x02,0x21,0x
10,0x41,0x04,0x81,0x09,0x20,0x88,0x45,0x9C,0x1E,
0x07,0x03,0xC1,0xC1,0x01,0xE1,0x10,0x41,0x04,0x
41,0x09,0x20,0x88,0x39,0x80,0x00,0x00,0x00,0x00,
0x00,0x00,0x20,0x00,0x01,0x00,0x00,0x00,0x00,0x0
0,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x01,0xC0,0
x00,0x02,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00
```

```
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x00,
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0x00
,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x01,0x80,0x00,0x06,0x00,0x20,
0x0E,0x01,0xC0,0x02,0x01,0xE0,0x0C,0x01,0xE0,0x
00,0x01,0x80,0x00,0x09,0x00,0x60,0x01,0x00,0x20,
0x06,0x01,0x00,0x10,0x00,0x20,0x00,0x01,0x80,0x0
0,0x09,0x00,0x20,0x01,0x00,0x20,0x0A,0x01,0x00,0
x10,0x00,0x40,0x00,0x01,0x80,0x00,0x09,0x00,0x20
,0x02,0x00,0xC0,0x12,0x01,0xC0,0x1C,0x00,0x40,0
x00,0x01,0x80,0x00,0x09,0x00,0x20,0x06,0x00,0x20
,0x1F,0x00,0x20,0x12,0x00,0x80,0x00,0x01,0x80,0x
00,0x09,0x00,0x20,0x08,0x00,0x20,0x02,0x00,0x20,
0x12,0x00,0x80,0x00,0x01,0x80,0x00,0x06,0x00,0x7
0,0x0F,0x01,0xC0,0x02,0x01,0xC0,0x0C,0x01,0x00,
0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x01,0x80,0x00,0x00,0x00,0x00,0x00,0x00,0x0
0,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x01,0x80,0
x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00
,0x00,0x00,0x00,0x00,0x01,0x80,0x00,0x00,0x00,0x
00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
0x00,0x01,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0x
FF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,/*"F:\
相册\新建文件夹 (2)\HGS12864-001.bmp",0*/
};// 逐行式，顺向；
/********************************************
        延时子程序；
********************************************/
void delay(uint z)
{
uint x,y;
for(x=z;x>0;x--)
    for(y=124;y>0;y--);
}
void delay_100us(uchar z)
{
z=z*16;
while(z--);
}
/********************************************
写入指令和数据；
********************************************/
void wr_data(uchar b)    //写数据   ；
{
RD1=1;
CS=0;
CD=1;
DATA=b;
WR1=0;
WR1=1;
_nop_();
CS=1;
}
void wr_com(uchar com)          //写命令；
{
RD1=1;
CS=0;
CD=0;
DATA=com;
WR1=0;
WR1=1;
_nop_();
CS=1;
}

/********************************************
转换程序 ：
16 阶灰度,一个地址 8 位,4 位一个像素,想控制 8 个
```

```
点,就须写 4 个地址的 RAM 数据;
*****************************************/
void change(uchar b)
{
uchar i;
for(i=0;i<4;i++)
      {
       switch(b&0xc0)
              {
              case 0x00:   RAM_data[i]=0x00;break;
              case0x40:    RAM_data[i]=0x0f;break;
              case 0x80:   RAM_data[i]=0xf0;break;
              case 0xc0:   RAM_data[i]=0xff;break;
              default:     break;
              }
       b=b<<2;
       wr_data(RAM_data[i]);
      }
}
/*****************************************
   工作窗口设置;
*****************************************/
void SET_AW(uchar a,uchar b,uchar c,uchar d)
{
wr_com(0x15);
wr_com(a);
wr_com(b);
wr_com(0x75);
wr_com(0x0c+c);
wr_com(0x0c+d);
}
/*****************************************
   隔行,隔列,全屏,隔点程序;
*****************************************/
void all_screen(uchar b) //128*80 整个 RAM 区清屏;
{
uchar i,j;
wr_com(0x15);
wr_com(0x00);
wr_com(0x3f);

wr_com(0x75);
wr_com(0x00);
wr_com(0x4f);
for (j=0;j<80;j++)
        for (i=0;i<64;i++) wr_data(b);
}

void  fill(uchar  b)//128*64  显示界面的操作,b=0  清屏;b=F0H 隔列;b=FFH  全屏;
{
uchar i,j;
SET_AW(0,63,0,63);
for (j=0;j<64;j++)
        for (i=0;i<64;i++) wr_data(b);
}
/*****************************************
   写入一副 128*64 的图片；(逐行式，顺向)
*****************************************/
void wr_BMP(uchar code *s)
{
uchar i,j;
SET_AW(0,63,0,63);
for (j=0;j<64;j++)
        for (i=0;i<16;i++) change(*s++);
}
/*****************************************
写入 8*8 字符；
x y-->行列地址；n 首字符序号，end_n 尾字符序号；
*****************************************/
void word_88(uchar x,uchar y,uchar n)
 //8*8 字符单个写；
{
uchar i;
SET_AW(x,x+3,y,y+7);
for(i=0;i<8;i++)    change(table_88[8*n+i]);
}

void show_88(uchar x,uchar y,uchar n,uchar end_n)
//写入 y 一串 8*8 字符，可自动换行；
{
uchar i;
for(i=n;i<=end_n;i++)
      {
      if(x>60) {y=y+8;x=0;}
      word_88(x,y,i);
      x=x+4;
       }
}
```

```
/*****************************************
写入 8*16 16*16 字符；
x y-->行列地址；n 首字符序号，end_n 尾字符序号；
*****************************************/
void word_816(uchar x,uchar y,uchar n)
//8*16 字符单个写；
{
uchar i;
SET_AW(x,x+3,y,y+15);
for(i=0;i<16;i++)    change(table_816[16*n+i]);
}

void word_1616(uchar x,uchar y,uchar n)
//16*16 字符单个写；
{
uchar i;
SET_AW(x,x+7,y,y+15);
for(i=0;i<32;i++)
change(table_1616[32*n+i]);
}

void show_816(uchar x,uchar y,uchar n,uchar end_n)
//写入 y 一串 8*16 字符，可自动换行；
{
uchar i;
for(i=n;i<=end_n;i++)
      {
      word_816(x,y,i);
      x=x+4;
       }
}
void show_1616(uchar x,uchar y,uchar n,uchar end_n)
//写入 y 一串 16*16 字符，可自动换行；
{
uchar i;
for(i=n;i<=end_n;i++)
      {
      if(x>60) {y=y+8;x=0;}
      word_1616(x,y,i);
      x=x+8;
       }
}
/*****************************************
    初始化函数；
*****************************************/
void init(void)
{
        delay(50);

        RES=1;delay(1);
        RES=0;delay(1);
        RES=1;delay(1);
  // 设置列窗口；
        wr_com(0x15);
        wr_com(0x00);     /* 左边界 0 */
        wr_com(0x3F);     /* 右边界 127*/
// 设置行窗口；
        wr_com(0x75);
        wr_com(0x0C);          /* 上边界 0*/
        wr_com(0x4b);          /* 下边界 63*/
// 设置 SEG 电流等级；
        wr_com(0x81);
        wr_com(0x40);     /* 共 128 级 */
// 设置 SEG 电流范围；
        wr_com(0x86);
/* 84H=1/4，85H=1/2，86H=1 */
// 设置逆转地图；
        wr_com(0xA0);
        wr_com(0x52);
/* BIT-0=1 列窗口反向,BIT-1=1 高半字节在前,BIT-2=1 COM 反向,BIT-6=0/1 EVEN/ODD */
// 设置显示起始行;
        wr_com(0xA1);
        wr_com(0x0C);     /* 0*/
// 设置显示分支
        wr_com(0xA2);
        wr_com(0x4C);     /* 0*/
// 设置显示模式;
        wr_com(0xA4);
/* A4H=正常显示,A5H=全显,A6H=关显示,A7H=反显 */
// 设置扫描行;
        wr_com(0xA8);
        wr_com(0x3F);     /* 64*/
// 设置 P1 P2 ;
        wr_com(0xB1);
        wr_com(0x04);       /* 4 */
        wr_com(0x06<<4);        /* 6 */
// 设置行周期;
        wr_com(0xB2);
```

```
        wr_com(0X46);       /* 70*/
// 设置 D 和 Fosc;
        wr_com(0xB3);
        wr_com(0x01);
        wr_com(0x04<<4);        /* Fosc=4 D=2 */
// 设置 Vp2
        wr_com(0xBC);
        wr_com(0x00);       /* 0.51 */
// 设置 Vcomh
        wr_com(0xBE);
        wr_com(0x00);       /* 0.51 */
// 设置 Vsl
        wr_com(0xBF);
        wr_com(0x0E);       /*  连接电容到 VSS */
// 设置灰度;
        wr_com(0xB8);
        wr_com(0x07);       /* L1[2:1] */
        wr_com(0x33);
/* L3[6:4], L2[2:0] 0001 0001*/
        wr_com(0x33);
/* L5[6:4], L4[2:0] 0010 0010*/
        wr_com(0x33);
/* L7[6:4], L6[2:0] 0011 1011*/
        wr_com(0x33);
/* L9[6:4], L8[2:0] 0100 0100*/
        wr_com(0x33);
/* LB[6:4], LA[2:0] 0101 0101*/
        wr_com(0x33);
/* LD[6:4], LC[2:0] 0110 0110*/
        wr_com(0x72);
/* LF[6:4], LE[2:0] 1000 0111*/
all_screen(0x00);
// 显示开关;
        wr_com(0xAF); /* AF=ON, AE=Sleep Mode */
// 设置 Vcc 来源;
        wr_com(0xAD);
        wr_com(0x02);    /* 03=内部   02=外部  */
}
/*****************************************
 主程序;
*****************************************/
main()
{
init();
while(1)
{
show_88(15,2,0,6);
show_816(14,10,0,6);
show_1616(13,30,0,3);delay(1000);
fill(0x00);delay(10);
wr_BMP(BMP); delay(1000);
fill(0x00);delay(10);
}
}
```

7. 质量标准

7.1 合格质量标准

检验项目	检测标准	AQL
电气特性	GB2828-81 检测水平 II 常规检测 单个样品检测	0.65
非电气特性	GB2828-81 检测水平 II 常规检测 单个样品检测	1.5
尺寸测量	GB2828-81 检测水平 II 常规检测 单个样品检测	1.5

7.2 检验环境条件

- 室温: 25±3 °C
- 湿度: 65±20%RH

7.3 检验标准

7.3.1 加电检测

检测项目	检测标准
无显示	任何像素有不显示的情况，视为不合格品
显示错误	不允许不当操作 在所选择模式，出现异常显示或显示位置不正确
显示不正常	任何一列显示不正常，视为不合格品
过流	总电流要求与模块所需电流相匹配，不允许超过模块正常工作的最大电流值.
视角	视角不要接近规格书所标最小值，如果有接近最小值的产品做不合格品处理.
对比度	对比度不要接近规格书所标最小值，如果有接近最小值的产品做不合格品处理.
OLED显示电压	见产品规格书

7.3.2 不加电检测

检测项目	检测标准
模块尺寸	见模块外形图，尺寸不允许超出公差范围
OLED屏面板划伤	如果有效区的划伤长和宽尺寸大于下面所示组合，我们做不合格处理。 数目：一个或更多 宽度：0.15 长度：5.0 三个或更多 宽度：0.10 长度：3.0 三个或更多 宽度：0.05 长度：2.0 当损坏超出这些尺寸，按不合格品处理.

8.可靠性

测试项目	测试内容	测试条件
高温存储	高温存储环境适应能力测试	60℃，200hrs
低温存储	低温存储环境适应能力测试	-10℃，200hrs
高温运行	高温环境运行测试	50℃，200hrs
低温运行	低温环境运行测试	0℃，200hrs
高温/湿存储	高温/湿存储适应能力测试	60℃,90%RH，96hrs
高温/湿运行（备注 3）	高温/湿运行测试	40℃,90%RH，96hrs
温度循环测试	温度变化循环测试： -10℃→25℃→60℃ 30min←5min←30min 1 cycle	-10℃/60℃，10 cycle
机械振动	机械振动测试	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs

备注1：在模块上不允许有任何水珠。

备注2：模块应该在正常条件下储存4小时后进行检测。

备注3：模块做三防处理后进行测试。

9. 出厂测试报告 （VDD=+5.0V ,Ta=25℃）

项目	条件	检测结果	备注
高温存储	80℃,120 hrs	无异常	---
低温存储	–40℃,120 hrs	无异常	---
高温运行	70℃,240 hrs	无异常	---
低温运行	–30℃,240 hrs	无异常	---
高温湿存储	50℃,90% RH,120 hrs	无异常	---
高温湿运行（备注 3）	40℃,90% RH,120 hrs	无异常	---
热震动	-10℃,30min→+25℃,5min→+60℃,30min	无异常	10 cycles

10. 注意事项

10.1 使用过程中注意事项

在 OLED 模块出厂前，我们已经做了精确的装配和调试,因此客户在使用操作时请注意以下几点:

（1） 模块上装有 OLED 屏，必须避免剧烈震动、冲击、挤压和从高处掉落。

（2） OLED 模块避免扭动,拆卸金属钮角.

（3） OLED 模块避免在印有线路的工作平台上操作.

（4） 防止施加直流电.

10.2 安装注意

OLED 模块是由两片薄玻璃基板组装而成的，它被固定在带有安装孔的 PCB 板上之后，很容易损坏。必须谨慎处理 OLED 模块，模块才可以被安装。

10.3 OLED 屏处理及清洗注意事项

在清理 OLED 模块屏表面时，请使用带溶剂（建议如下）的软布，轻轻擦拭。

（1）异丙醇

（2）乙醇

（3）不要用干燥或者比较硬的材料擦拭，否则很容易损坏屏表面。

以下溶剂请不要使用：

（1）水

（2）酮

（3）芳烃

10.4 严防静电

OLED 显示电路是低压、微功耗的 COMS 电路，因此我们建议将任何没有使用的输入终端连接到 VDD 或 VSS 上，在打开电源之前，请不要输入任何信号，并且保证人体、工作台及组装设备良好接地，严防静电.。我们推荐以下措施：

（1）在装配使用 OLED 模块前,请不要将其从包装袋中取出.OLED 模块所使用的包装袋是经过防静电处理的特殊包装袋. 在储存模块时也要带有包装袋储存,或者放在能充分接地的容器中储存.

（2）在操作 OLED 模块时,要始终保持操作人充分接地. 使人体和模块保持同一电位。

（3）在操作过程中所需的设备要充分接地.尤其是驱动器,必须良好接地,没有漏电,以避免干扰.

（4）OLED 模块表面都有一层保护膜, 目的在于避免造成屏被划伤,沾染污渍等。
请慢慢揭去 OLED 模块保护膜.如果快速揭去保护膜都将产生静电。

（5）注意厂房的湿度：厂房湿度范围: 50~60%RH

10.5 电流保护装置

OLED 模块上没有装电流保护装置,因此,在使用时应预备好电流保护装置.驱动电压直流成分越小越好，最好不超过 50mV，长时间施加过大的直流成分会使电极产生电化学反应而老化。

10.6 操作注意事项

（1） OLED 模块如果输入电压过高会缩短它的寿命，所以对模块的输入电压进行限制是很重要的。

（2） 如果在运行过程中有些显示区域无法驱动，导致某些字符显示异常，但是重启一次将会恢复正常。

（3） 终端如果有轻微裸露都将引起电化学反应导致终端开路。

（4） 如果工作温度在最高工作温度，那么要求湿度小于等于 50%RH.

10.7 焊接注意事项:

在焊接 OLED 模块时须注意以下几点:

▲OLED 模块上只有输入/输出连线处可以焊接.

▲焊接所需的烙铁必须绝缘.

（1）焊接时所需条件:

电铁的温度: 280℃±10℃

焊接时间: < 3-4S

焊接材料: 低熔点,可充分熔化的焊锡

避免使用融化后易流动的焊锡,因为在焊接时易渗透到 OLED 模块里面,在清理时易对模块造成污染.此外,为了避免焊接时焊锡对 OLED 模块的污染,应在焊接完成后再揭去 OLED 模块的保护膜.

（2）重复焊接时注意事项:

由于连接线是穿过模块的焊盘与模块焊接的,所以在拆除时需等到焊锡完全熔化时再移动连接线.若焊锡未能完全熔化就用力移动连接线,就极易造成焊盘损坏或脱落.在拆除连接线时最好使用”吸枪”.此外还应注意,重复焊接不得超过 3 次.

10.8 包装与存储

当 OLED 模块需要长时间储存时,应遵循以下原则:

如果储存方法不当,将影响 OLED 模块的显示效果；容易造成焊盘的氧化，不容易焊接。

（1）储存时尽可能使用出厂时的原包装.

（2）储存散装的 OLED 模块时,应先装入防静电袋,封口严密.

（3）为防止模块性能退化，不要暴露在高湿温环境对它直接操作或存储。

（4）储存应保持低湿度,最佳储存温度范围为: 0℃~35℃

（5）存储时不允许任何东西接触到 OLED 屏表面。

11.使用须知

（1） 在合作双方认为有必要提供定制样品的情况下应该提供样品。合同在样品设计好并且双方确认后生效。

（2）在遇到以下情况，必须经双方代表讨论并且同意后处理问题：

-当产品规格书出现问题时。

-当一个新的问题出现，而在此产品规格书中没有说明时。

-如果客户的检测标准或运行条件改变要告知**清达**，这些改变将使产品规格书出现问题。

-当一个新的问题在客户操作过程中出现，经分析样品也存在该问题时。