



N-Channel Enhancement Mode Field Effect Transistor

General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

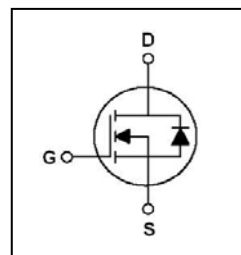
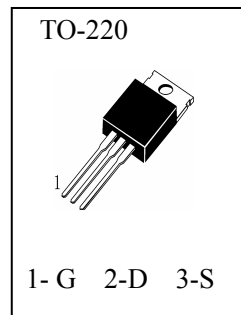
- 4A, 650V(See Note), $R_{DS(on)} < 2.9\Omega @ V_{GS} = 10V$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

Maximum Ratings (Ta=25°C unless otherwise specified)

T_{stg}	Storage Temperature	-----	-55~150°C
T_j	Operating Junction Temperature	-----	150°C
V_{DSS}	Drain-Source Voltage	-----	650V
V_{GSS}	Gate-Source Voltage	-----	±30V
I_D	Drain Current (Continuous)(T _c =25°C)	-----	4A
I_{DM}	Pulsed Drain Current (Note 1)	-----	16A
P_D	Maximum Power Dissipation (T _c =25°C)	-----	100W
	Derate Above 25°C	-----	0.8W/°C
E_{AS}	Pulsed Avalanche Energy (Note 2)	-----	180mJ
I_{AR}	Avalanche Current (Note 1)	-----	4A
E_{AR}	Repetitive Avalanche Energy (Note 1)	-----	10mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-----	4.5V/ns

Thermal Characteristics

Symbol	Items	TO-220	Unit
Rthj-case	Thermal Resistance Junction-case	Max 1.25	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 62.5	°C/W



**Electrical Characteristics** (Ta=25°C unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	650			V	I _D =250μA, V _{GS} =0V
I _{DSS}	Zero Gate Voltage Drain Current			1	μA	V _{DS} =650V, V _{GS} =0V
				10	μA	V _{DS} =520V, V _{GS} =0V, T _j =125°C
I _{GSS}	Gate - Body Leakage			±100	nA	V _{GS} =±30V, V _{DS} =0V
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	2.5		4.5	V	V _{DS} =V _{GS} , I _D =250μA
R _{DS(on)}	Static Drain-Source On-Resistance		2.3	2.9	Ω	V _{GS} =10V, I _D =2A
Dynamic Characteristics and Switching Characteristics						
C _{iss}	Input Capacitance		520	680	pF	V _{DS} =25V, V _{GS} =0V, f=1.0MHz
C _{oss}	Output Capacitance		60	80	pF	
C _{rss}	Reverse Transfer Capacitance		8.0	10.5	pF	
t _{d(on)}	Turn - On Delay Time		11	33	nS	V _{DS} =325V, I _D =4A, R _G =25Ω (Note 4,5)
t _r	Rise Time		45	90	nS	
t _{d(off)}	Turn - Off Delay Time		40	88	nS	
t _f	Fall Time		48	100	nS	V _{DS} =520V, I _D =4A, V _{GS} =10V (Note 4,5)
Q _g	Total Gate Charge		10.5	13.5	nC	
Q _{gs}	Gate - Source Charge		2.5		nC	
Q _{gd}	Gate - Drain Charge		4.0		nC	
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Continuous Source - Drain Diode Forward Current			4	A	
I _{SM}	Pulsed Drain - Source Diode Forward Current			16	A	
V _{SD}	Source - Drain Diode Forward On-Voltage			1.4	V	I _S =4A, V _{GS} =0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=18.9mH, I_{AS}=4.0A, V_{DD}=50V, R_G=25Ω, Starting T_j=25°C
3. I_{SD}≤4.0A, di/dt≤200A/μS, V_{DD}≤BV_{DSS}, Starting T_j=25°C
4. Pulse Test: Pulse width≤300μS, Duty Cycle≤2%
5. Essentially independent of operating temperature



Typical Characteristics

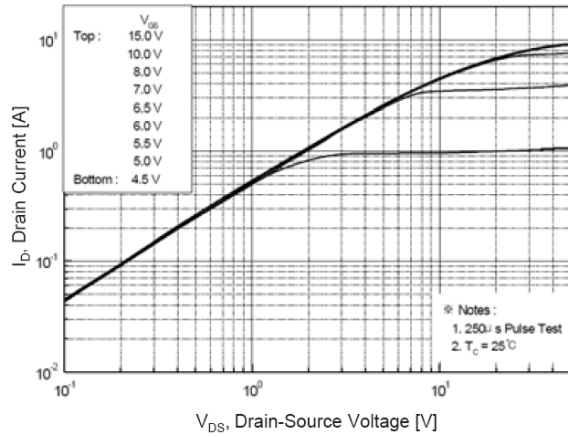


Figure 1. On Region Characteristics

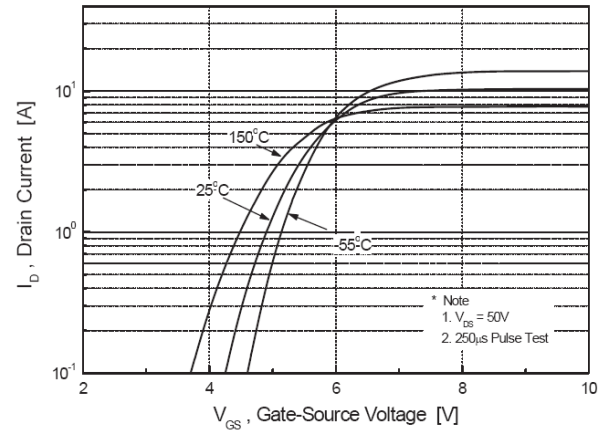


Figure 2. Transfer Characteristics

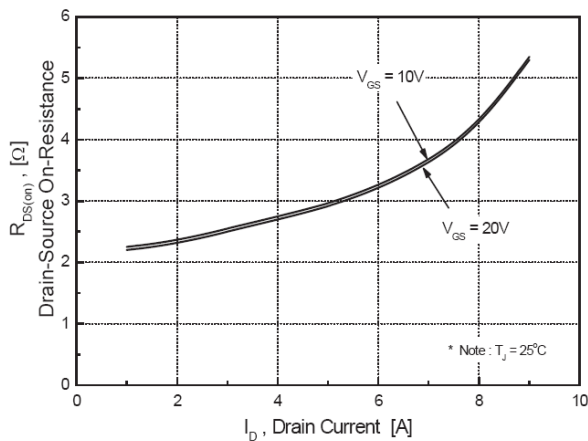


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

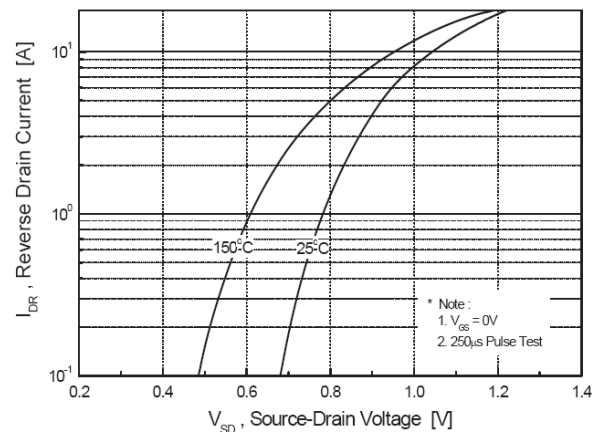


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

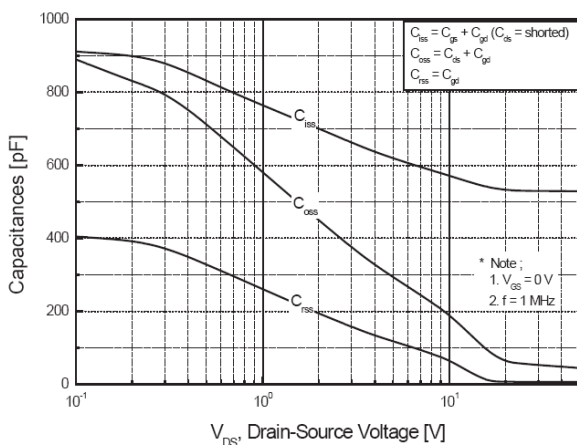


Figure 5. Capacitance Characteristics

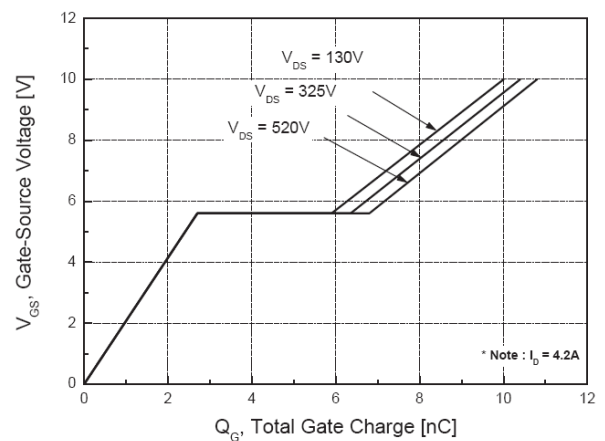


Figure 6. Gate Charge Characteristics



Typical Characteristics

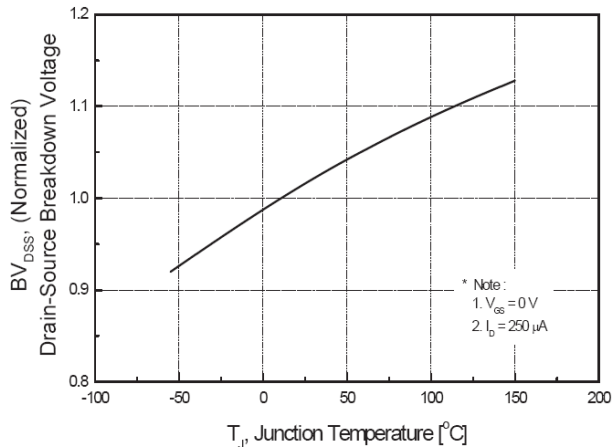


Figure 7. Breakdown Voltage Variation vs Temperature

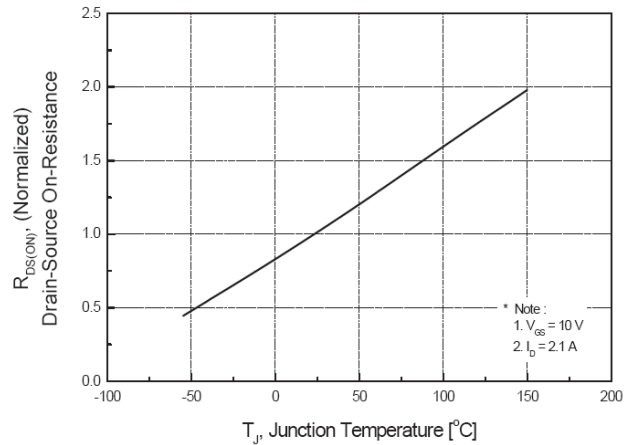


Figure 8. On-Resistance Variation vs Temperature

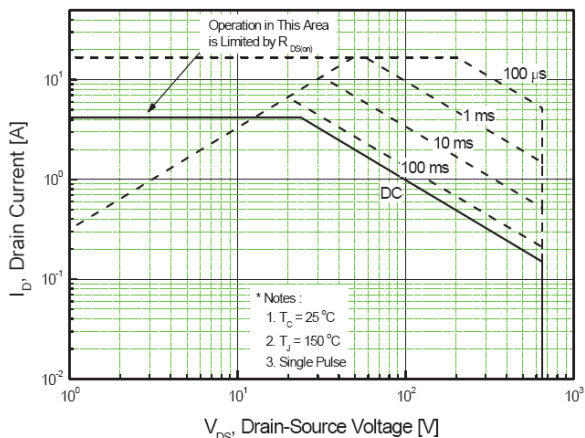


Figure 9. Maximum Safe Operating Area

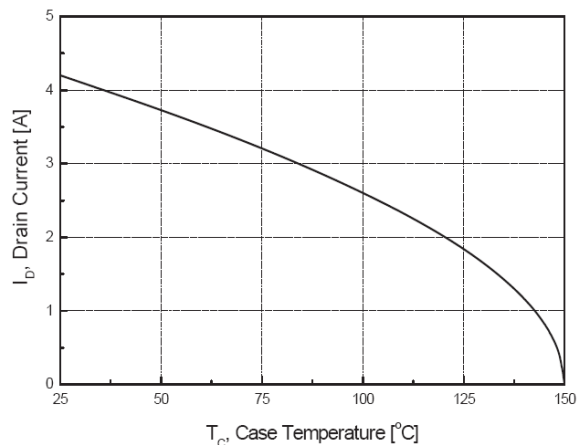


Figure 10. Maximum Drain Current vs Case Temperature

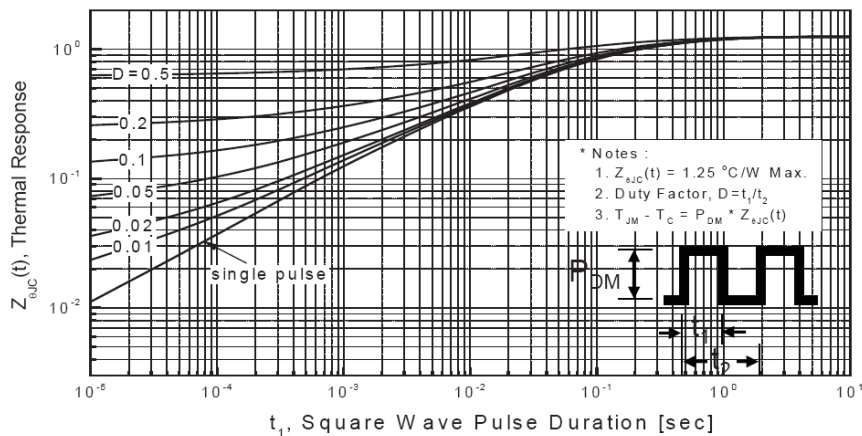


Figure 11. Transient Thermal Response Curve



Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

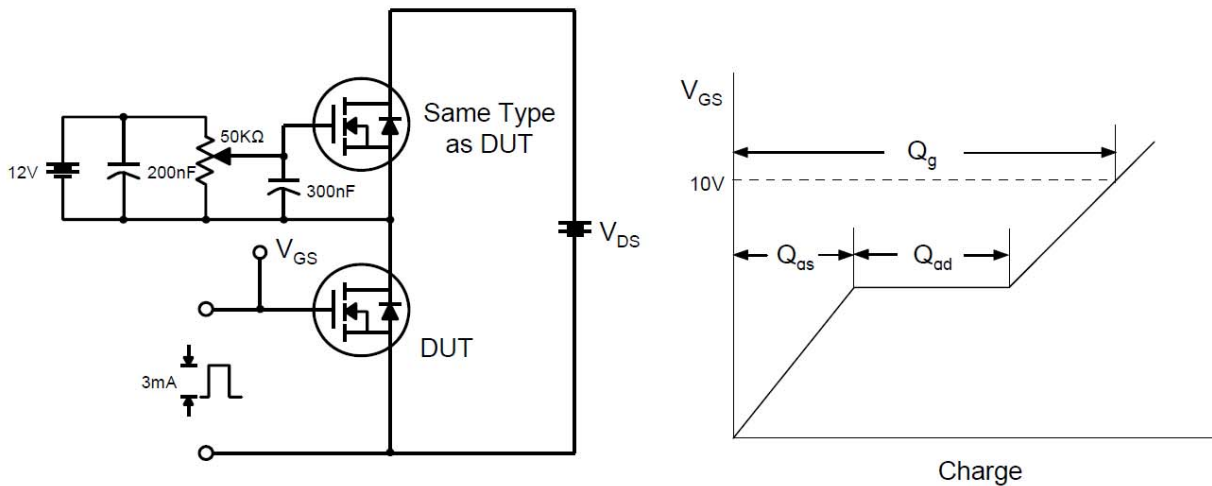


Fig 13. Resistive Switching Test Circuit & Waveforms

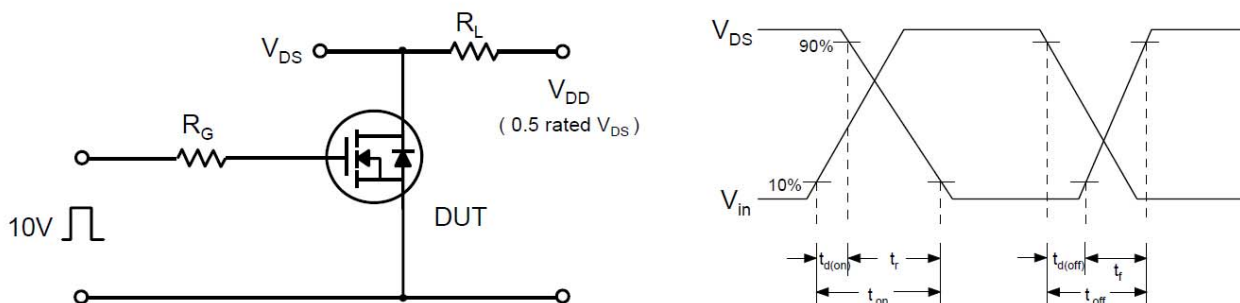
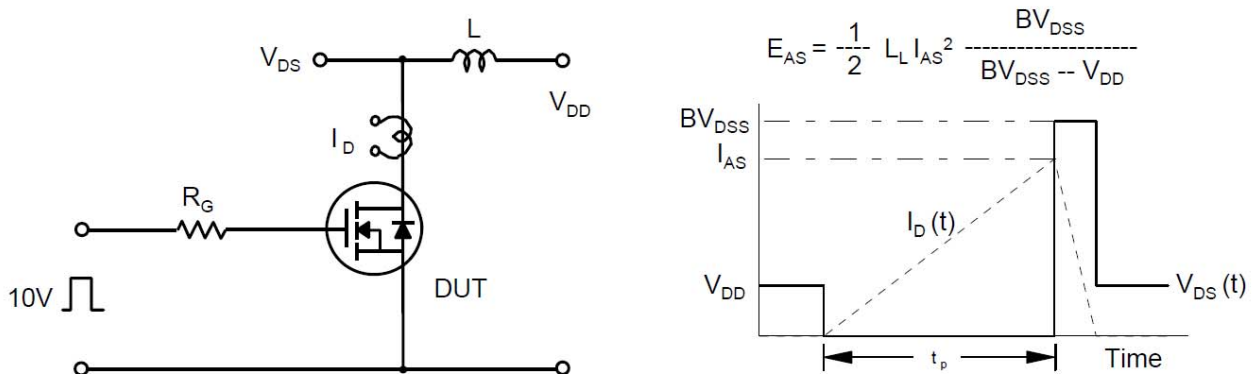


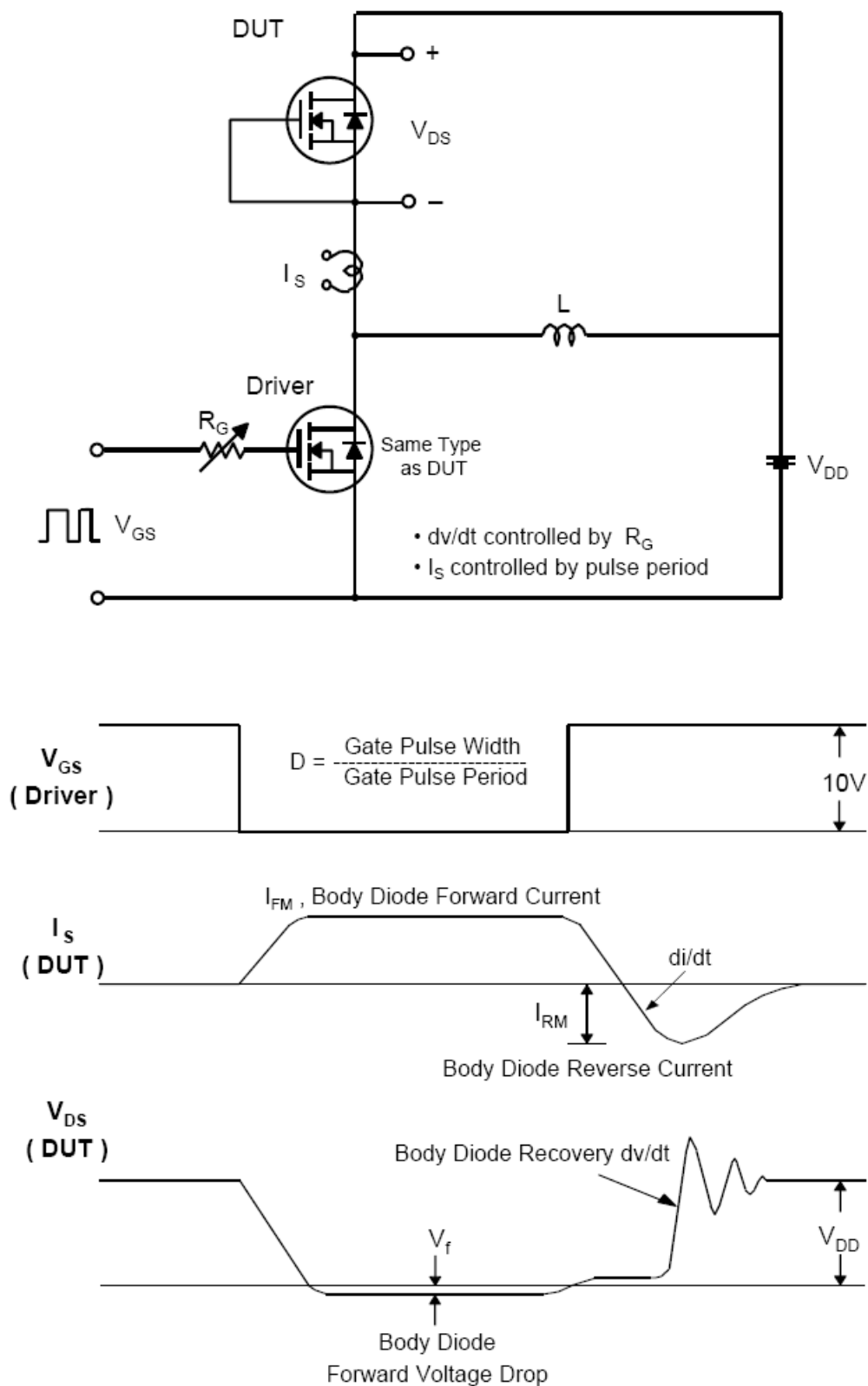
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms





■ Typical Characteristics

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





■ Package Dimensions

