HFBR-707X2DEM

10 Gb Ethernet, 1310 nm, 10GBASE-LRM, X2 Transceiver

Data Sheet

Description

The X2 LRM fiber optic transceiver is an "intelligent" optical module which incorporates the complete physical layer functionality of 10GbE on multi mode fiber with data rate of 10.3Gbps. The X2 LRM module includes a transmitter that incorporates an uncooled, directly modulated 1.3 μm Fabry-Perot laser. The receiver subassembly includes a PIN photodiode and a linear/AGC trans-impedance amplifier. To cope with the effect of modal dispersion of multi mode fibers at 10 Gbps over the distances specified in the IEEE 802.3aq LRM standard, an electronic dispersion compensation circuit is used. The MUX/DEMUX, XAUI interface and MDIO management functions are all integrated into the module, as is a precision oscillator. The module is compliant to the X2 Multi Source Agreement specifications.

Applications

- Ethernet switching systems
- Ethernet peripheral interface
- Computer system I/O

Features

- Compliant with IEEE LRM Standard
  - Draft P802.3aq™/D4.0 for Type 10GBASE-LRM
- Compliant with X2 MSA Issue 2.0b
- Standard SC Duplex fiber optic connector
- Standard 70 pin electrical connector
- Four wide XAUI Electrical interface
- MDIO Management Interface
- Front Panel hot pluggable
- Digital Optical Monitoring (DOM) provides Tx/Rx power, laser bias current, and module temperature

Specifications

- 220m reach on OM1, 0M2 and OM3 Multimode Fiber Cables
- Total Power Dissipation less than 4W

General Specifications

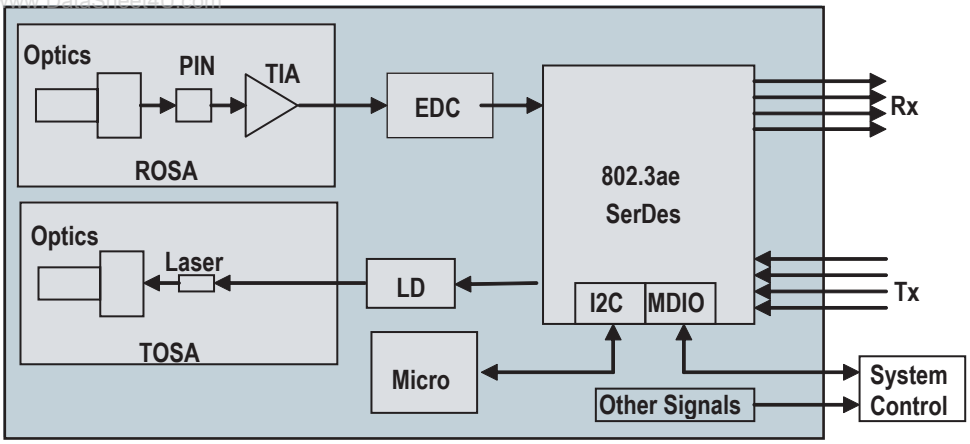


Figure 1. High level block diagram

General Optical Specifications

Optical Connector:
SC Duplex

Optical Line rate:
10.3125 Gb/s

Link Length:
220m, with 62.5um MMF/ 160/500MHz*km

220m, with 50um MMF/ 500/500MHz*km

220m, with 50um MMF/ 1500/500MHz*km

Laser:
1310nm FP Laser

Detector:
PIN diode

General Electrical Specifications

Connector:
70-pin, mates to Tyco/AMP Part No. 1367337-1 or equivalent

Supply Voltages:
+5 V, +3.3 V and APS

E->O Coding (Transmit Direction):
8B/10B coding removed, 64B/66B added

O->E Coding (Receive Direction):
64B/66B removed, 8B/10B coding added

XAUI interface:
100 Ω Differential, AC- coupled I/O on Tx and Rx, per IEEE 802.3ae Clause 47

Control interface:
MDIO, 1.2 V, per IEEE 802.3ae Clause 45.3

Non Volatile memory:
48 byte user space

Environmental Specifications

Operating temperature:
0 °C to +70 °C case

Power consumption:
4.0 W maximum

Technical Specifications

Absolute Maximum Ratings[1]

Parameter	Minimum	Typical	Maximum	Units	Notes
Storage Temperature	-40		85	°C	
Operating Temperature	0		70	°C	Case temperature
Supply Voltage (5 V)			5.5	V	
Supply Voltage (3.3 V)			3.6	V	
Supply Voltage (APS)			2.0	V	
Voltage on any XAUI pin			2.5	V	
Voltage on any LVCMOS pin	-0.7		4.0	V	
Received Average Power			1.5	dBm	

Recommended Operating Conditions[2]

Parameter	Minimum	Typical	Maximum	Units	Notes
Initialization Time		0.5	5	sec	
Supply Voltage (5 V)	4.75	5	5.25	V	
Supply Voltage (3.3 V)	3.14	3.3	3.47	V	
Supply Voltage (APS)				V	3
Supply Current (5 V)		1	3.0	mA	
Supply Current (3.3 V)		0.74	0.9	A	
Supply Current (APS)		0.66	0.8	A	
Power Consumption			4	W	
Supply Current Ramp Rate			50	mA/ms	4
Inrush current (per power supply)			150% steady state rating	A	

Notes:

1. Absolute maximum ratings are those values beyond which functional performance is not intended, device reliability is not implied, and damage to the device may occur.
2. Typical operating conditions are those values for which functional performance and device reliability is implied.
3. X2 MSA compliant.
4. Not applicable to inrush current due to small transceiver capacitive load presented to the host during hot plug which limits the total in rush charge.

Transmitter Path Summary

Figure 2 shows a block diagram of the transmit path, from the four XAUI differential inputs to the optical output. The incoming XAUI differential 8B/10B encoded electrical inputs, are reformatted and transmitted onto the outgoing fiber optic interface using 64B/66B encoding.

Receiver Path Summary

Figure 3 shows a block diagram of the receiver path, from the incoming 10.3 Gb/s, 64B/66B encoded optical interface to the four 3.125 Gb/s differential 8B/10B encoded XAUI electrical output interface. The XAUI output drivers provide low-swing differential output with 100 Ω differential output impedance and are ac coupled.

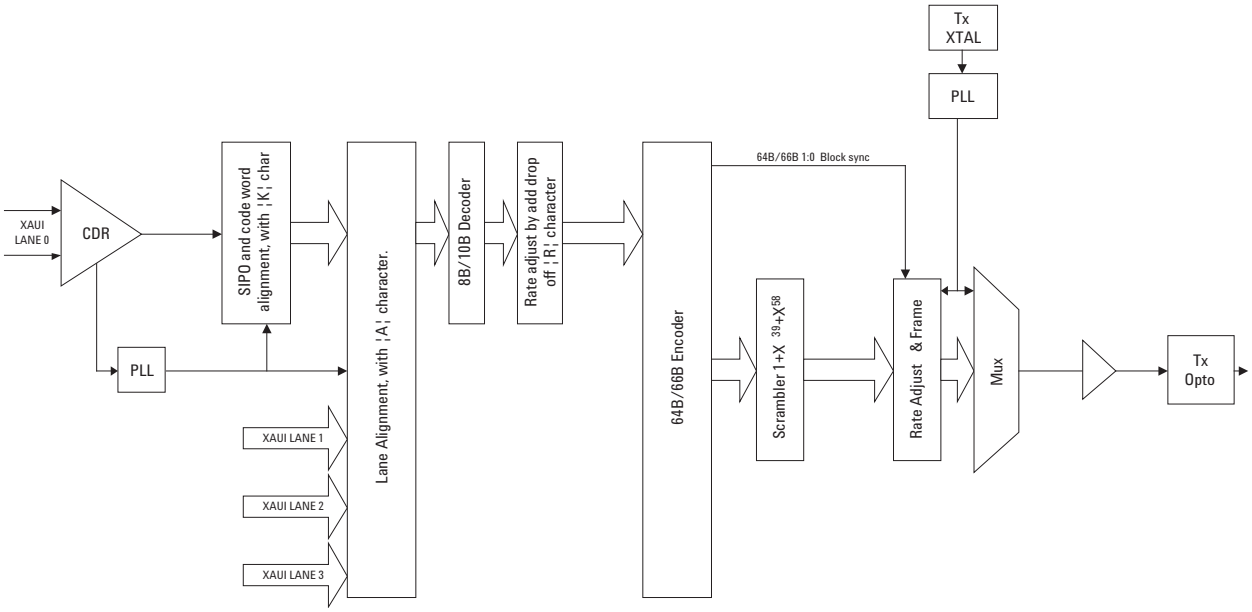


Figure 2. Transmit Path High Level Overview

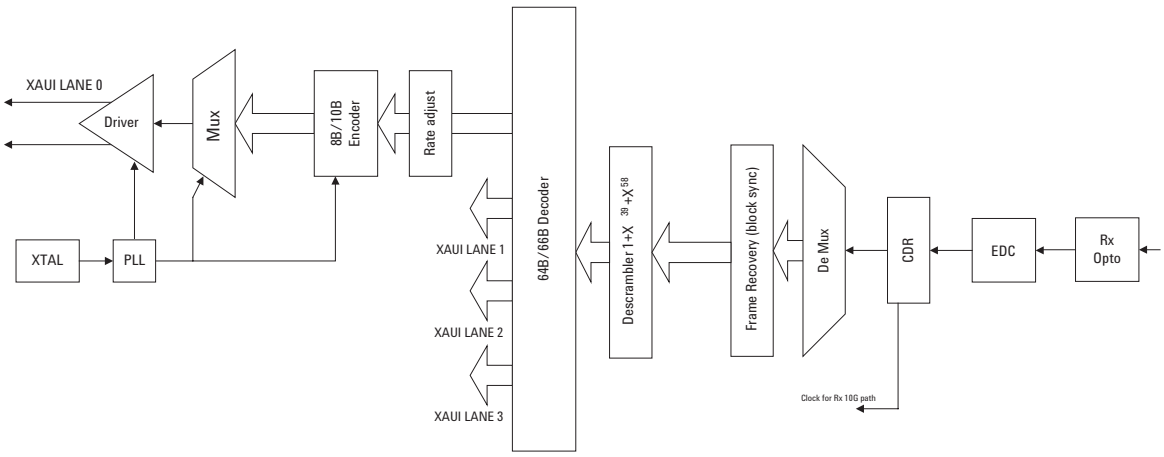


Figure 3. Receive Path High Level Overview

Optical Specifications

Parameter	Minimum	Typical	Maximum	Units	Notes
Transmitter					
Signaling Speed - nominal		10.3125		GBd	
Signaling Speed variation from nominal	-100		+100	ppm	
Center Wavelength	1260		1355	nm	
RMS Spectral Width at 1260 nm			2.4	nm	1
RMS Spectral Width between 1260 nm and 1300 nm					1, See Figure 4a
RMS Spectral Width between 1300 nm and 1355 nm			4	nm	1
Launch Power (OMA)	-4.5		1.5	dBm	2, See Figure 4b
Average Launch Power	-6.5		0.5	dBm	2, See Figure 4b
Average Launch Power of OFF transmitter			-30	dBm	
Extinction Ratio	3.5			dB	
Peak Launch Power			3	dBm	2, 3
$RIN_{20}OMA$			-128	dB/Hz	
Eye Mask parameters {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.40, 0.45, 0.25, 0.28, 0.80}			See Figure 4c
Transmitter Waveform and Dispersion Penalty (TWDP)			4.7	dB	
Uncorrelated Jitter (rms)			0.033	UI	
Encircled Flux within 5µm radius	30			%	4
Encircled Flux within 11µm radius	81			%	4
Optical Return Loss Tolerance	20			dB	
Receiver					
Signaling Speed - nominal		10.3125		GBd	
Signaling Speed variation from nominal	-100		+100	ppm	
Center Wavelength	1260		1355	nm	
Stressed Sensitivity (OMA)			-6.5	dBm	5
Stressed Sensitivity (OMA) for symmetrical test			-6	dBm	6
Overload (OMA)	1.5			dBm	
Receiver Reflectance			-12	dB	
Signal Detect On (OMA)			-7	dBm	7

Notes:

1. RMS spectral width is the standard deviations of the spectrum.
2. The OMA, average launch power and peak launch power specifications apply at TP2. This is after each type of patch cord. For information: Patch cord losses, between MDI and TP2, differ. The range of losses must be accounted for to ensure compliance to TP2.
3. Peak optical power can be determined as the maximum value from the waveform capture from the TWDP test, or equivalent method.
4. This encircled flux specification, measured per IEC 61280-1-4, defines the near field light distribution at TP2 when the MDI is coupled directly into the appropriate patch cord.
5. This value will be met for several different independent test conditions defined in Section 68 of the IEEE 802.3aq™/D4.0: 1. Comprehensive stressed receiver test (two separate conditions; Pre-Cursor and Post-Cursor tap weights); 2. Simple stressed receiver test; 3. Jitter tolerance (two separate frequency/p-p amplitude conditions)
6. This value will be met for test conditions defined in Section 68 of the IEEE 802.3aq™/D4.0 for comprehensive stressed receiver test symmetrical tap weights.
7. With ER ≤ 10dB.

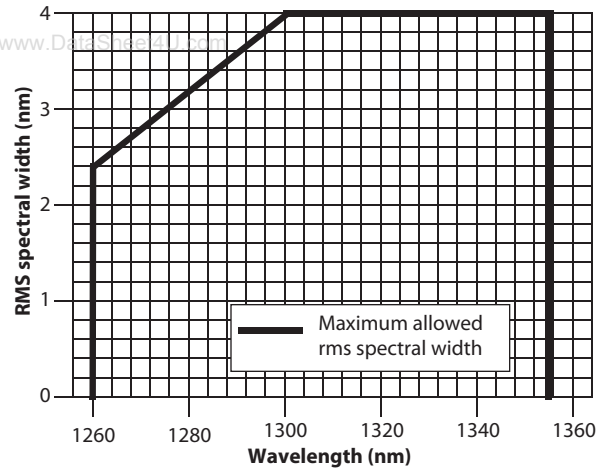
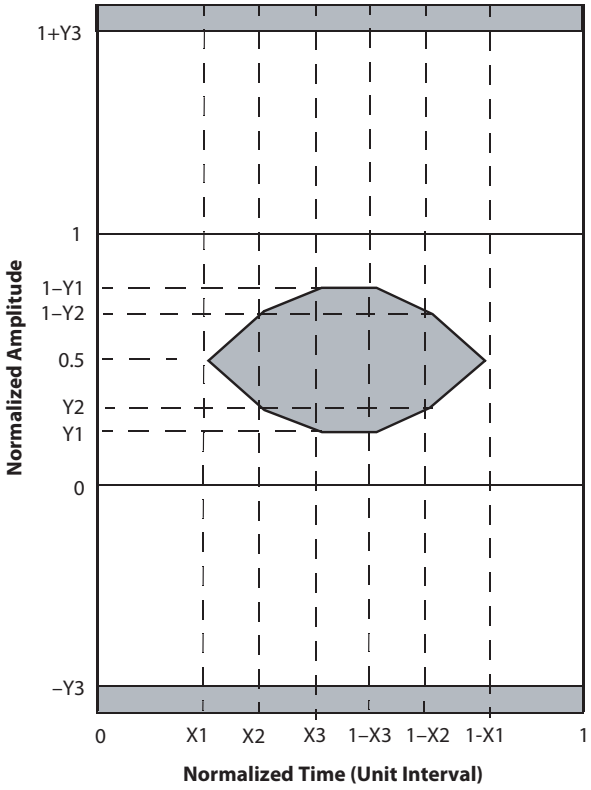


Figure 4a. 10GBASE-LRM Transmitter spectral limits



Note: where X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.40, 0.45, 0.25, 0.28, 0.80 respectively

Figure 4c. Transmitter Eye Mask Definition

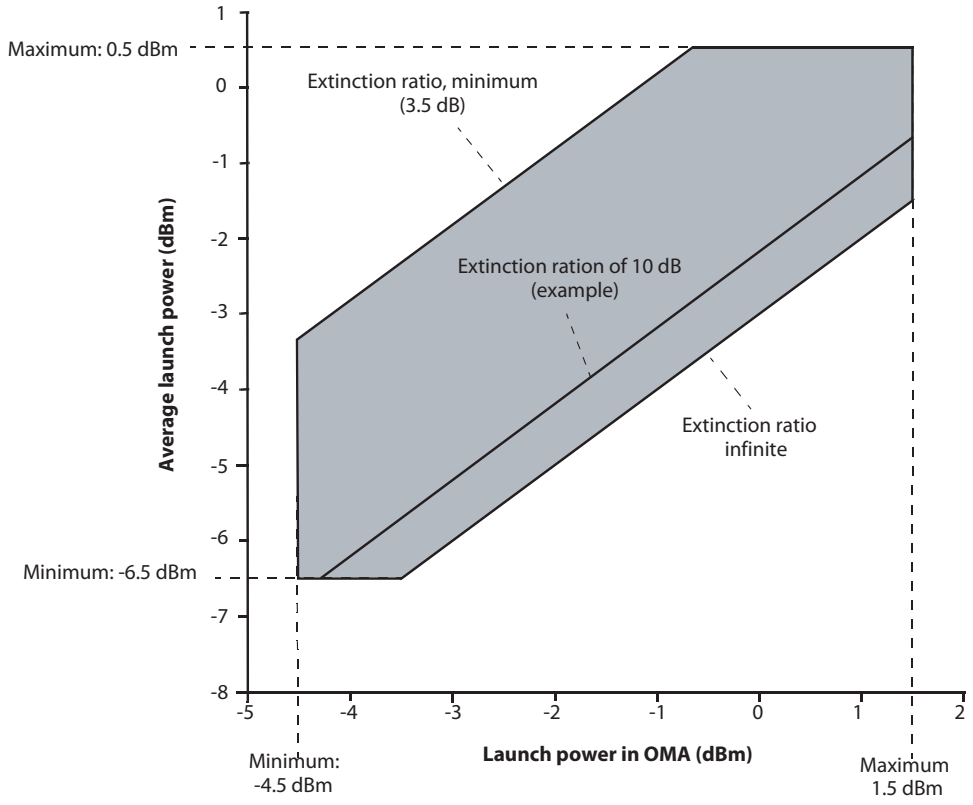


Figure 4b. Graphical representation of approximate region of transmitter compliance

Electrical Control and Sense I/O Parameters

Table 1. CMOS DC Parameters (MDC, PRTAD<4:0>, LASI)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vol	Output low voltage			0.15	V	ext. Rpullup = 10 kΩ to 1.2 V
Voh	Output high voltage	1.0		1.5	V	ext. Rpullup = 10 kΩ to 1.2V
Vih	Input high voltage	0.84		1.25	V	
Vil	Input low voltage			0.36	V	
Ipd	Input pad pulldown current	20	40	120	µA	Vin = 1.2 V
Trise	Rise time			30	ns	Cload = 300 pF
Tfall	Fall time		25	50	ns	Cload = 300 pF

Electrical MDIO Parameters

Table 2. MDIO 1.2 V dc parameters

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output high voltage	1.0		1.5	V	Ioh = -100 uA
Vol	Output low voltage	-0.3		0.2	V	Iol = +100 uA
Iol	Output low current	-4			mA	Vin = 0.3
Vih	Input high voltage	0.84		1.5	V	
Vil	Input low voltage	-0.3		0.36	V	
Cin	Input capacitance			10	pF	

Table 3. MDIO AC Parameters

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Thold	MDIO data hold time	10			ns	
Tsetup	MDIO data setup time	10			ns	
Tdelay	Delay from MDC rising edge to MDIO data change	0		300	ns	
Fmax	Maximum MDC clock rate			2.5	MHz	

Electrical High Speed I/O Parameters

Table 4. XAUI Input Interface

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
	BAUD rate for 10Gb E		3.125		Gb/s	
	BAUD rate tolerance	-100		100	ppm	
	Differential input amplitude	200		2500	mVpp	Note 1
	Differential return loss			-10	dB	100 MHz to 2.5 GHz ref to 100Ω impedance
	Common mode return loss			-6	dB	100 MHz to 2.5 GHz ref to 25Ω
	Input Differential Skew			75	ps P-P	at crossing point, Note 2
	Jitter amplitude tolerancedeter-ministic + random jitter +Sj jitter			0.55 + Sj	UIpp	See Figure 5a for SJ jitter graph

Table 5. XAUI Driver Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
	BAUD rate for 10Gb E		3.125		Gb/s	
	BAUD rate variation	-100		100	ppm	
	Differential amplitude	800		1600	mVpp	
	Transition times (20-80%)	60	90	130	ps	Note 2
	Total output jitter			± 0.175	UI	no pre-equalization
	Output deterministic jitter			± 0.085	UI	no pre-equalization
	Output differential skew			15	ps	at crossing point
	Differential output return loss				dB	312.5 MHz to 625 MHz: -10 dB625 MHz to 3.125 GHz: as per equation 47-1 IEEE 802.3ae
	Electrical eye mask					See Figure 5b

Note:

1. Maximum amplitude of 2500 mVpp is the combined effect of the driver maximum output signal of 1600 mVpp and the receiver input impedance mismatch.
2. For information only.

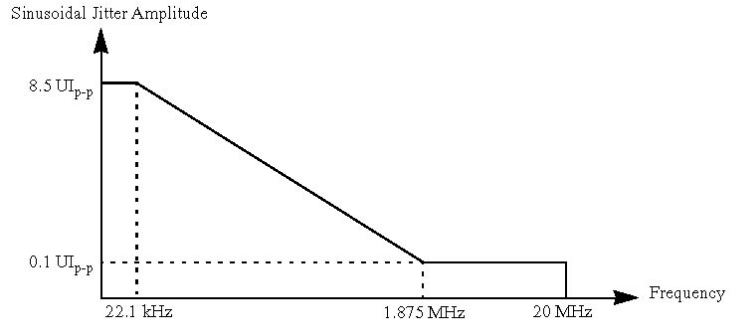


Figure 5a. Single-tone sinusoidal jitter mask

Electrical Eye Mask

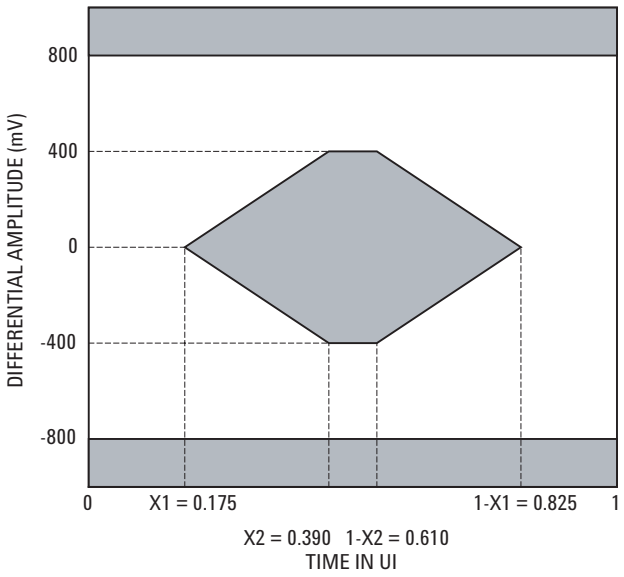


Figure 5b. XAUI Driver Near End Template

General Connector Considerations

1. Ground connections are common for Tx and Rx.
2. V_{CC} contacts are each rated at 0.5 A nominal.
3. See Figure 6 for location of Pin 1.

Table 6. DOM Accuracy

Parameter	Accuracy Specification (typ)	Accuracy Specification (max)
Rx Power Range	± 1.5 dBm	± 2 dBm
Output Power Range	± 2 dBm	± 3 dBm
Temperature Range	± 3 °C (-5 °C to +75 °C)	±5 °C
Ibias Range	±5% (2 mA to 80 mA)	±10%

EEPROM and NVR Content

X2 Module contains Non-Volatile (NVR) and Volatile memory in accordance with the Xenpak MSA rev 3.0, the IEEE 802.3ae Standard and applicable end-user specifications.

Table 7. Customer specific NVR Content – Device 1 PMA/PMD Registers: 0x8012 – 0x805C

Data Address (Hex)	Field Size (Bytes)	Name of Field	Value (Hex)	Remark
0x8012	1	Tcvr Type	02	Transceiver Type (X2=02)
0x8013	1	Connector	01	Optical Connector Type (SC=01)
0x8014	1	Encoding	01	Bit Encoding (NRZ=01)
0x8015	2	Bit Rate	28 48	Bit rate: in multiples of 1 MB/s
0x8017	1	Protocol	01	Protocol Type (10GbE=01)
0x8018	1	Compliance	00	"Unspecified" : 10GbE code 0
0x8022	2	Range	00 16	"220m for MMF"
0x8024	1	Fiber Type	01	"MM, generic"
0x8026	3	Wavelength	01 FF B8	Center Wavelength : 1310nm
0x803A	16	Vendor Name	41 56 41 47 4F 20 20 2020 20 20 20 20 20 20 20 20	AVAGO
0x804A	16	Vendor PN	48 46 42 52 2D 37 30 3758 32 44 45 4D 20 20 20	HFBR-707X2DEM
0x805C	16	Vendor SN	AGAyywwXnnn 20 20 20 20 20	yy: year; ww: work week; nnn:rolling serial number from 000 to ZZZ

Table 8. General I/O Pin Summary

Signal Type	Pins	Direction	Function
Power Supply Pins			
Ground	1:3, 33:37, 40, 43, 46, 49 52:54, 57, 60, 63, 66, 69:70		Electrical ground
3.3 V	5:6, 30:31	I	3.3 V power supply
5.0 V	4, 32	I	5.0 V power supply
Adaptive power supply	7:8, 28:29	I	Adaptive power supply (0.9 - 1.8 V)
Adaptive power supply set	25	I	APS set connection
Adaptive power supply sense	27	I	APS sense connection
Control & Sense I/O Pins			
LASI	9	O	1.2 V CMOS pull up on host
Reset	10	I	1.2 V CMOS pull up on module
Transmitter ON/OFF	12	I	1.2 V CMOS pull up on module
Port address 4:0	19:23	I	1.2 V CMOS pull up on module
MDIO Pins			
MOD DETECT	14	O	1 kΩ pull down to ground on module
Management data IO	17	I/O	1.2 V per IEEE802.3ae clause 45.3
Management data clock	18	I	1.2 V per IEEE802.3ae clause 45.3
High Speed I/O Pins			
Receiver lane 0:3 +	41, 44, 47, 50	O	XAUI per IEEE802.3ae clause 47
Receiver lane 0:3 -	42, 45, 48, 51	O	XAUI per IEEE802.3ae clause 47
Transmitter lane 0:3 +	55, 58, 61, 64	I	XAUI per IEEE802.3ae clause 47
Transmitter lane 0:3 -	56, 59, 62, 65	I	XAUI per IEEE802.3ae clause 47
Non connected pins			
Not connected	13, 26, 38:39, 67:68		NC on module
Do not connect pins			
Do not connect	11, 15:16, 24		Avago Specific

Electrical Pin Out

Top of PCB		Bottom of PCB (as viewed from top of PCB)	
70	GND	1	GND
69	GND	2	GND
68	NOT CONNECTED	3	GND
67	NOT CONNECTED	4	5.0V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	DO NOT CONNECT
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	NOT CONNECTED
57	GND	14	MOD DETECT
56	TX LANE0-	15	DO NOT CONNECT
55	TX LANE0+	16	DO NOT CONNECT
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	DO NOT CONNECT
46	GND	25	APS SET
45	RX LANE1-	26	NOT CONNECTED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0-	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	NOT CONNECTED	32	5.0V
38	NOT CONNECTED	33	GND
37	GND	34	GND
36	GND	35	GND

Figure 6. Electrical Pin Out

Electrical Pin Out Definitions

Table 9. Pin Function Definitions (Lower Row)

Pin No	Name	Direction	Function	Note
1	GND		Electrical ground	
2	GND		Electrical ground	
3	GND		Electrical ground	
4	5 V	I	5.0 V power supply	
5	3.3 V	I	3.3 V power supply	
6	3.3 V	I	3.3 V power supply	
7	APS	I	Adaptive power supply (0.9 - 1.8 V)	
8	APS	I	Adaptive power supply (0.9 - 1.8 V)	
9	LASI	O	Logic high: normal operationLogic low: LASI asserted	See Table 13
10	RESET	I	Logic high: normal operationLogic low: reset	
11	DO NOT CONNECT		Avago specific; do not connect	
12	TX ON/OFF	I	Pulled up inside module via 10 kΩ Logic high: transmitter onLogic low: transmitter off	
13	NOT CONNECTED			
14	MOD DETECT	O	Pulled low inside module through 1 kΩ to GND	
15	DO NOT CONNECT		Avago specific; do not connect	
16	DO NOT CONNECT		Avago specific; do not connect	
17	MDIO	I/O	Management data IO	
18	MDC	I	Management data clock	
19	PRTAD4	I	Port address bit 4	
20	PRTAD3	I	Port address bit 3	
21	PRTAD2	I	Port address bit 2	
22	PRTAD1	I	Port address bit 1	
23	PRTAD0	I	Port address bit 0	
24	DO NOT CONNECT		Avago specific; do not connect	
25	APS SET	I	APS set connection	
26	NOT CONNECTED			
27	APS SENSE	I	APS sense connection	
28	APS	I	Adaptive Power Supply (0.9 - 1.8 V)	
29	APS	I	Adaptive Power Supply (0.9 - 1.8 V)	
30	3.3 V	I	Power	
31	3.3 V	I	Power	
32	5 V	I	5.0 V Power Supply	
33	GND		Electrical Ground	
34	GND		Electrical Ground	
35	GND		Electrical Ground	

Table 10. Pin Function Definitions (Upper Row)

Pin No	Name	Direction	Function	Note
36	GND		Electrical Ground	
37	GND		Electrical Ground	
38	NOT CONNECTED			
39	NOT CONNECTED			
40	GND		Electrical Ground	
41	RX LANE 0+	O	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	Module XAUI Output Lane 0-	
43	GND		Electrical Ground	
44	RX LANE 1+	O	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	Module XAUI Output Lane 1-	
46	GND		Electrical Ground	
47	RX LANE 2+	O	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	Module XAUI Output Lane 2-	
49	GND		Electrical Ground	
50	RX LANE 3+	O	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	Module XAUI Output Lane 3-	
52	GND		Electrical Ground	
53	GND		Electrical Ground	
54	GND		Electrical Ground	
55	TX LANE 0+	I	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	Module XAUI Input Lane 0-	
57	GND		Electrical Ground	
58	TX LANE 1+	I	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	Module XAUI Input Lane 1-	
60	GND		Electrical Ground	
61	TX LANE 2+	I	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	Module XAUI Input Lane 2-	
63	GND		Electrical Ground	
64	TX LANE3+	I	Module XAUI Input Lane 3+	
65	TX LANE3-	I	Module XAUI Input Lane 3-	
66	GND		Electrical Ground	
67	NOT CONNECTED			
68	NOT CONNECTED			
69	GND		Electrical Ground	
70	GND		Electrical Ground	

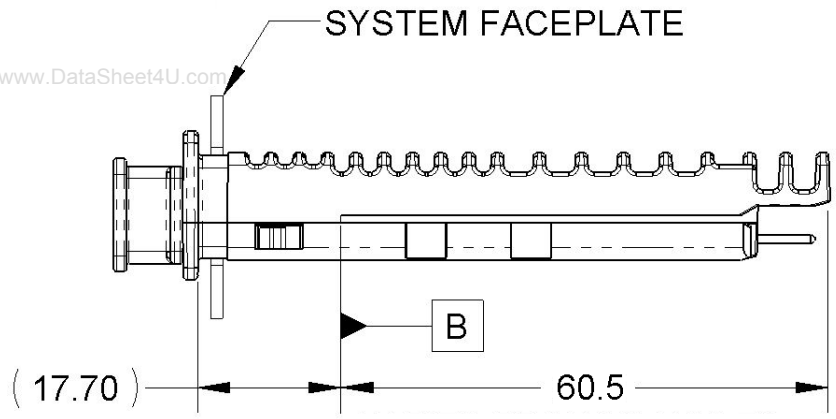


Figure 7. Mechanical Dimensions

Notes
1. All module and PCB pad dimensions are per X2 MSA Revision 2.0b unless otherwise noted in Figure 7.

Management Data Input/Output (MDIO) Interface

The MDIO interface provides a simple, two wire, serial interface to connect a station management entity (STA) and a managed PHY for the purpose of controlling the PHY and gathering status from the PHY. The management interface consists of the two wire physical interface, a frame format, a protocol specification for exchanging the frames and a register set that can be read and written using these frames. The two wires of the physical interface are the Management Data Clock (MDC) and the Management Data I/O (MDIO).

Management Data Clock (MDC)

The MDC is sourced by the Station Management entity (STA) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times.

Management Data I/O (MDIO)

MDIO is a bidirectional signal between the PHY (HFBR-707X2DEM) and the STA. It is used to transfer control and status information. Data is always driven and sampled synchronously with respect to MDC. Figure 9 shows that MDIO open drain driver configuration.

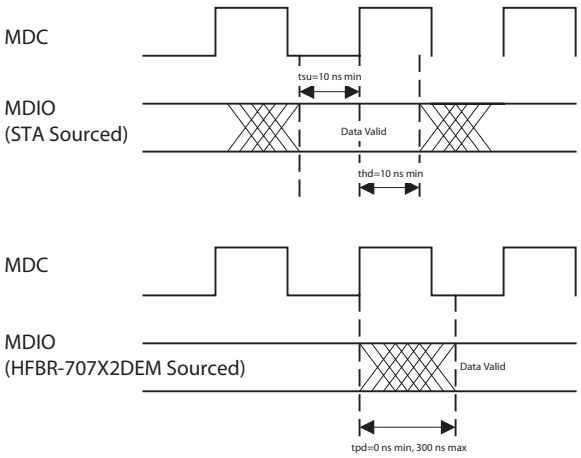


Figure 8. MDIO/MDC Timing

MDIO Timing relationship to MDC

MDIO is a bidirectional signal that can be sourced by the STA or the HFBR-707X2DEM. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC (see Figure 8). When the MDIO signal is sourced by the HFBR-707X2DEM, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock output delay from the HFBR-707X2DEM shall be a minimum of 0 ns and a maximum of 300 ns.

Management Frame Format

The HFBR-707X2DEM has an internal address register which is used to store the address for MDIO reads and writes. This MDIO address register can be set by using an address frame that specifies the register address to be accessed within a particular port device.

The following write, read or a post-read-increment-address frame to the same port device shall access the register whose address is stored in the HFBR-707X2DEM MDIO address register. An address frame should be followed immediately by its associated write, read or post-read-increment-address frame.

Upon receiving a post-read-increment-address frame and having completed the read operation, the HFBR-707X2DEM shall increment and store the address of the register accessed. If no address cycle is received before the next write, read or post-read-increment-address frame, then the HFBR-707X2DEM shall use the stored address for that register access.

The Management Frame Format for Indirect Access is specified in Table 11.

PRE - Preamble

At the beginning of each transaction the STA shall send a preamble sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC, to provide the HFBR-707X2DEM with a pattern that it can use to establish synchronization. The HFBR-707X2DEM must observe this preamble sequence before it responds to any transaction.

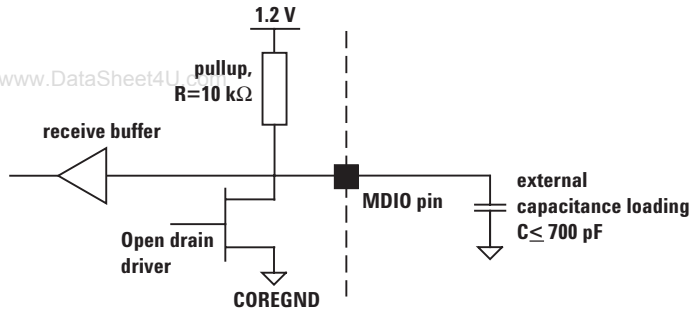


Figure 9. MDIO open Drain Driver Configuration

Table 11. Frame Format

	Management Frame Fields							
FRAME	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDR/DATA**	**IDLE**
ADDRESS	1...1	00	00	PRTAD[4:0]	DA[4:0]	10	A[15:0]	Z
WRITE	1...1	00	01	PRTAD[4:0]	DA[4:0]	10	D[15:0]	Z
READ	1...1	00	11	PRTAD[4:0]	DA[4:0]	Z0	D[15:0]	Z
READ INC	1...1	00	10	PRTAD[4:0]	DA[4:0]	Z0	D[15:0]	Z

ST - Start

The Start of Frame is indicated by a <00> pattern. This pattern ensures transitions from the default logic one line to zero and back to one.

OP - Operation Code

The operation code field indicates the type of transaction being performed by the frame.

Table 12. OP Code Definitions

OP Code	Operation
00	Register Address
01	Write Data
11	Read Data
10	Post Read Increment Address

PRTAD - Port Address

The Port Address is five bits, allowing 32 unique port addresses. HFBR-707X2DEM's port address is set through pins PRTAD<0:4>.

DEVAD - Device Address

The Device Address is five bits, allowing 32 unique devices per port. The HFBR-707X2DEM supports device addresses 1 (PMA/PMD), 3 (PCS) and 4 (PHY XS).

TA - Turnaround

The Turnaround time is a two bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction (see IEEE 802.3ae).

ADDR/DATA

The Data/Address field is 16 bits. The first bit transmitted/received is bit 15 and the last bit is bit 0.

IDLE

The idle condition is a high-impedance state. The MDIO line will be pulled to a one.

EEPROM Interface

Volatile and Non-Volatile Registers

There are two main memory/register types in the HFBR-707X2DEM which comply with the IEEE 802.3ae and XENPAK standard: volatile and nonvolatile. These areas can be further divided into user readable and writeable areas.

At power up the module register space is initialized and, where appropriate, default values are loaded from the non user accessible nonvolatile memory. The user accessible nonvolatile memory is also uploaded entirely into the user accessible volatile memory.

It is important to note that writes to the user accessible volatile memory are not stored to the corresponding user nonvolatile area and will therefore be lost upon a power down or reset. For such writes to be permanent the data must be written first to the user accessible nonvolatile area and then a reload invoked via the NVR Control/Status register, see Register 1.32768.

Access

The XENPAK MSA related Nonvolatile Control/Status register is only needed for performing writes to the nonvolatile user accessible area within the HFBR-707X2DEM because nonvolatile memory cannot be written to by normal MDIO write cycles. Other writes to volatile memory and registers may be performed directly via normal MDIO write cycles. All volatile and nonvolatile locations may be read directly via MDIO read cycles, it is not necessary to use the NVR Control/Status register, other than for status.

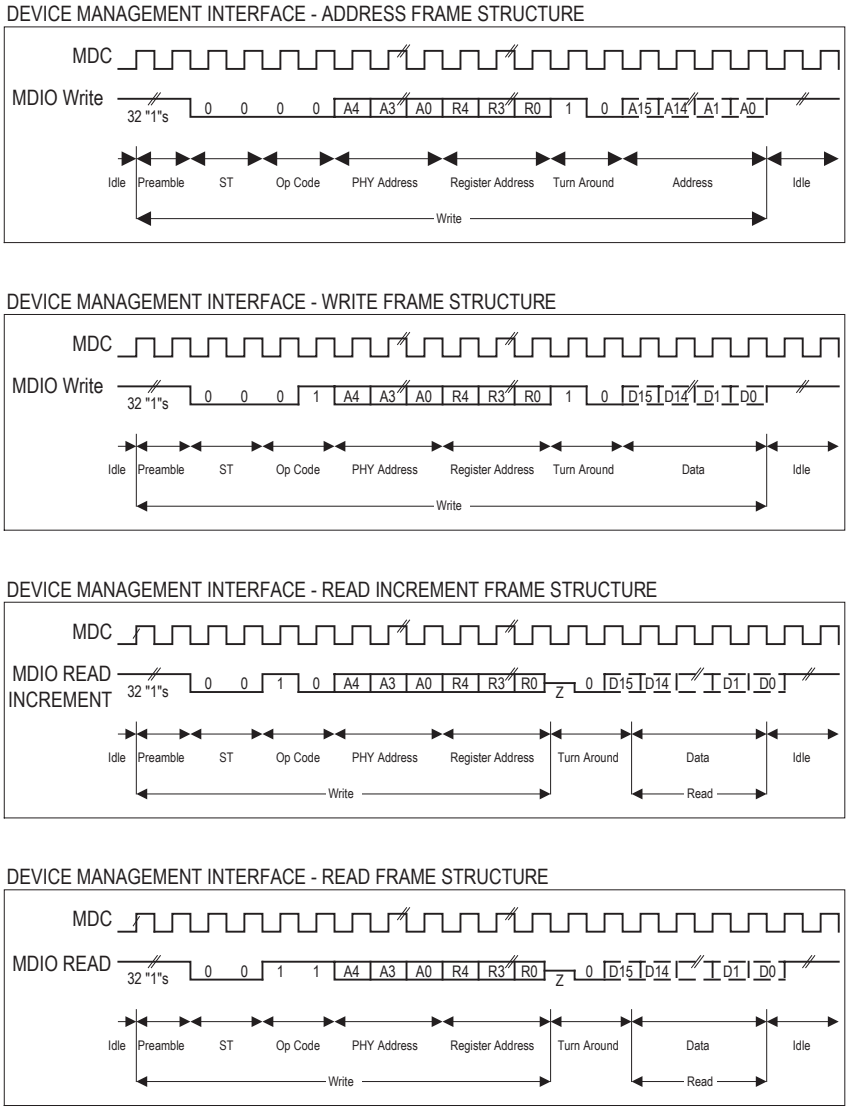


Figure 10. MDIO Frame Formats

Read/Write Command (bit5)

The XENPAK MSA related 1.32768.5 register must be set to 1 to perform writes to the NVR and zero (read) otherwise a zero written to bit 5 initiates an NVR read. A 1 written to bit 5 initiates an NVR write.

If the NVR register bit 5 is set to zero and the extended command bits set to 11 forces an upload of all values in the NVR to the volatile areas, including default register values. Such an upload is performed automatically after a hard or soft reset.

EEPROM Checksum Checking

The HFBR-707X2DEM will perform a checksum calculation and compare after every successful 256 byte read. The checksum for comparison is in EEPROM register 118 =MDIO register 1.32893.7:0. The checksum is equal to the 8 LSB 's of the sum of bytes 0 to 117 of the EEPROM. The calculated checksum is stored in MDIO register 1.49156.15:8. The result of the calculated checksum compared with the one read from EEPROM is placed in MDIO register 1.49155.7.

EEPROM 256 Byte Read Cycle

An EEPROM 256 Byte Read Cycle is initiated by setting MDIO bits 1.32768.0,1 to 0 and 1.32768.5 to 0.

The information to be read from the EEPROM stored in the 256 MDIO registers. A 256 byte read is initiated on hot plug or reset.

EEPROM Single Byte Read or Write Cycle

An EEPROM Single Byte Read/Write Cycle is initiated by setting MDIO EEPROM control register bits 1.32768.1:0 to 10. As for the 256 byte read/write commands, MDIO register 1.32768.5 determines if a read or a write cycle will be performed. The single byte EEPROM address is read from EEPROM control register 1.32768 bit15:8. The data is placed in/read from the associated MDIO register.

Monitors and Diagnostic Features

The LASI pin is used to indicate suboptimal performance in either the receive or transmit path. It can be used as an interrupt. It is the OR of the tx_alarm, rx_alarm and the ls_alarm signals each gated with their respective enables. The enables are read from MDIO register 1.36866, LASI control.

LASI ={OR of (reg 1.36869.n 'bit wise AND ' reg 1.36866.n) for n=0 to 15}.

ls_alarm

LS Alarm is latched high each time the link_status signal changes state. LS_ALARM is the output of this latch AND the LS_ALARM enable register. link_status is an indicator of the link health.

link_status = {PMD signal detect (MDIO 1.10.0) AND PCS block_lock (MDIO 3.32.0) AND PHY_XS lane_alignment (MDIO 4.24.12)}

Table 13. LASI Control Registers

Description	MDIO Status Registers (RO)	Type	MDIO Enable Registers (R/W)	Default
3.3V supply out of range	1.36869.5	RO	1.36866.5	0
APS supply out of range	1.36869.4	RO	1.36866.4	0
Reserved	1.36869.3	-	1.36866.3	X
RX_ALARM	1.36869.2	RO	1.36866.2	0
TX_ALARM	1.36869.1	RO	1.36866.1	0
LS_ALARM	1.36869.0	RO/LH	1.36866.0	0

Rx_alarm

rx_alarm is used to indicate a problem with the receive path. rx_alarm is the OR of several receive path status registers in MDIO registers 1.36867.

The ORing of each term is enabled by a companion MDIO register in 1.36864 and the overall output is enabled by the RX_ALARM enable register (1.36866.2h).

rx_alarm ={OR of (reg 1.36867 'bit wise AND ' reg 1.36864.. n) for n=0 to 15} AND {RX_ALARM enable (1.36866.2h})

tx_alarm

tx_alarm is used to indicate a problem with the transmit path. tx_alarm is the OR of several transmit path status registers in MDIO registers 1.36868 bit wise AND'd with the TX_ALARM enable register. The ORing of each term is enabled by a companion MDIO register in 1.36865.

tx_alarm = {OR of (reg 1.36868 'bit wise AND' reg 1.36865) for n=0 to 15} AND {TX_ALARM enable (reg 1.36866.1)}

Table 14. Receive Alarm Registers

Description	MDIO Status Registers (RO)	Mirrors	Type	MDIO Enable Registers (R/W)	Default
WIS local fault	1.36867.9		RO	1.36864.9	0
Reserved	1.36867.6-8		-	1.36864.6-8	X
Receive Optical Power fault	1.36867.5		RO/LH[1]	1.36864.5	1
PMA/PMD fault	1.36867.4	1.8.10	RO/LH	1.36864.4	1
PCS fault	1.36867.3	3.8.10	RO/LH	1.36864.3	1
Reserved	1.36867.2		-	1.36864.2	X
RX_FLAG	1.36867.1		RO	1.36864.1	0
PHY XS fault	1.36867.0	4.8.10	RO/LH	1.36864.0	1

1. This bit will be read only if bit 9 of the Optional Settings Register at 1.49175 is set to 1, and RO/LH if it is set to 0.

Table 15. Transmit Alarm Registers

Description	MDIO Status Registers (RO)	Mirrors	Type	MDIO Enable Registers (R/W)	Default
Laser Bias Current fault	1.36868.9		RO	1.36865.9	1
Laser Temp fault	1.36868.8		RO	1.36865.8	1
Laser Output Power fault	1.36868.7		RO	1.36865.7	1
Transmit fault	1.36868.6		RO/LH	1.36865.6	0
Reserved	1.36868.5		-	1.36865.5	X
PMA/PMD fault	1.36868.4	1.8.11	RO/LH	1.36865.4	1
PCS fault	1.36868.3	3.8.11	RO/LH	1.36865.3	1
Reserved	1.36868.2		-	1.36865.2	X
TX_FLAG	1.36868.1		RO	1.36865.1	0
PHY XS fault	1.36868.0	4.8.11	RO/LH	1.36865.0	1

Loopbacks

When in any system (PMA, PCS or PHY XS system) loopback mode the HFBR-707X2DEM shall accept data from the transmit path and return it on the receive path.

During PMA or PHY XS system loopback, a continuous stream of zeros is propagated through the remaining transmit data path. In PCS loopback mode, a continuous pattern of 0x00FF is propagated through the remaining transmit data path. Transmit data will be propagated through the remaining transmit data path instead if the associated 'loopback data output enable bit' is set high for the enabled loopback mode.

When in PMA network loopback mode, the recovered and retimed 10.3125 GBd signal is looped to the transmitter. The receive path XAUI output data will be received data.

In PHY XS network loopback the recovered received data is looped back to the transmit path in the XAUI block.

Enabling of more than one loopback path is invalid.

Reset Operation

Writing a '1' to any of MDIO registers 1.0.15, 3.0.15 or 4.0.15 causes all the HFBR-707X2DEM registers to be reset to their default values. These bits are all self-clearing after the reset function is complete.

Pulling the RESET pin low causes a full chip reset.

Writes to any bits of the Control register while the RESET is asserted are ignored. All status and control registers are reset to their default states. The NVR read sequence is started when RESET goes high. MDIO register bits 1.0.15, 3.0.15, and 4.0.15 will be held to 1 until the reset sequence is complete.

Table 16. Loopback Summary

loopback name	loopback direction	loopback control register	bypassed path default output	data output enable register	bypassed path output control' =1
PMA system loopback	Tx -> Rx	1.0.0	stream of 0's	3.49152.5	transmit data
PCS loopback	Tx -> Rx	3.0.14	0x00FF	3.49152.5	transmit data
PHY XS system loopback	Tx -> Rx	4.49152.14	stream of 0's	4.49152.15	transmit data
PMA network loopback	Rx -> Tx	1.49153.4	received data	NA	NA
PHY XS network loop-back	Rx -> Tx	4.0.14	received data	NA	NA

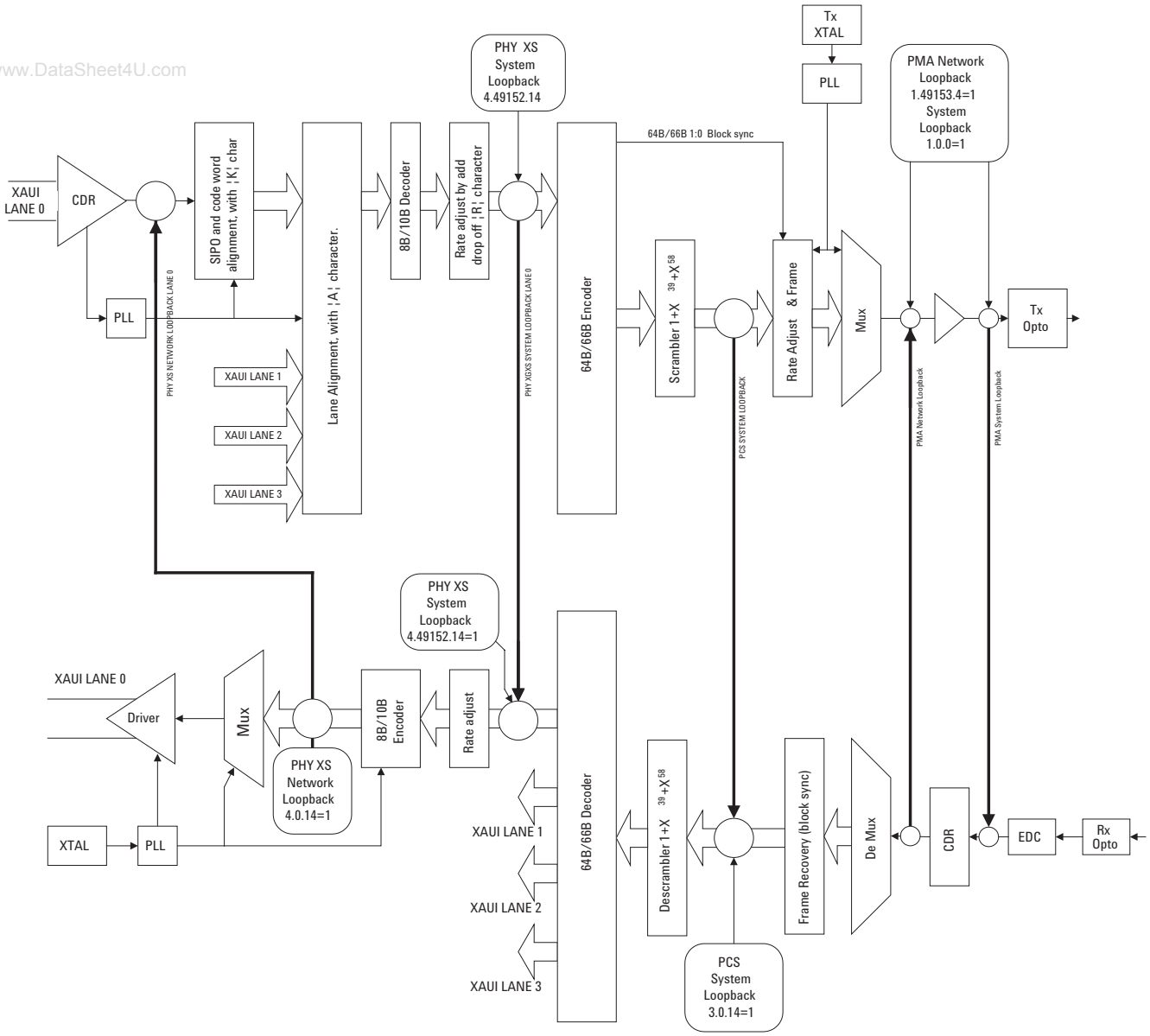


Figure 11. HFBR-707X2DEM Loopback Modes

XENPAK Digital Optical Monitoring (DOM) Overview

The XENPAK Digital Optical Monitoring (DOM) interface is a derivative of *SFF-8472: Digital Diagnostic Monitoring Interface for Optical Transceivers* appropriate to XENPAK transceivers. This specification defines a 256 byte block of register space that is accessible over the 2 wire serial MDIO/MDC interface.

A memory map is used to access measurements of *transceiver temperature*, *receive optical power*, *laser output power*, and *laser bias current* through the 2 wire serial MDIO/MDC interface. Support for these measurements is indicated through the capability registers (1.32890 : DOM Capability and 1.41071: DOM Capability - Extended). The transceiver generates this monitoring data by digitization of internal analog signals, which are calibrated to absolute measurements. Measured parameters are reported in 16 bit data fields (two concatenated bytes).

Alarm flags are required so DOM indicators can be made inputs to the Link Alarm Status Interrupt (LASI) function. Calibrated alarm and warning threshold data is written during device manufacture.

Table 17. XENPAK Digital Optical Monitoring MDIO Register Space

Device	From Decimal	Hex	To Decimal	Hex	Register Name
1	32890	807A	32890	807A	DOM Capability
1	40960	A000	40999	A027	Alarm and Warning Thresholds
1	41056	A060	41065	A069	Monitored A/D Values
1	41070	A06E	41071	A06F	Optional Status and DOM Extended Capabilities
1	41216	A100	41216	A100	Optional DOM Control/Status

Table 18. Register 1.32890 - DOM Capability

Bit(s)	Name	Description	R/W[1]	Default Value
1.32890.7	DOM Register Implemented	DOM Control/Status Register: 0 = not implemented 1 = implemented	RO	Specified by Customer
1.32890.6	DOM Implemented	Set when DOM implemented	RO	mirrors 1.32890.7
1.32890.5	WDM capability	WDM lane by lane DOM capability: setting this bit indicates that registers A0CO-A0FF are valid. Setting this bit will NOT override indications placed in register A06F (DOM capability)	RO	0
1.32890.4	Laser bias scale	Laser bias scale factor: 0 = 2 µA 1 = 10 µA	RO	1
1.32890.3		Reserved	RO	X
1.32890.2:0	External DOM	Address of external DOM device	RO	XXX

Alarm and Warning Flags

MDIO registers 1.41072 to 1.41079 contain alarm and warning flags that monitor A/D values in registers 1.41056-1.41065.

Two flag types are defined:

- Alarm flags (registers 1.41072 - 1.41073) associated with transceiver temperature, receive optical power, laser output power, and laser bias current. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.
- Warning flags (registers 1.41076 - 1.41077) associated with transceiver temperature, receive optical power, laser output power, and laser bias current. Warning flags indicate conditions outside the normally guaranteed bounds, but not necessarily causes of immediate link failures.

Table 19. Registers Alarm and Warning Flag Memory Map

Bit(s)	Name	Description	Type	Default Value (dec)
1.41072.7	Transceiver Temp High Alarm	Set when transceiver temp exceeds high alarm level	RO	0
1.41072.6	Transceiver Temp Low Alarm	Set when transceiver temp is below low alarm level	RO	0
1.41072.4-5	Reserved			
1.41072.3	Laser Bias Current High Alarm	Set when laser bias current exceeds high alarm level	RO	0
1.41072.2	Laser Bias Current Low Alarm	Set when laser bias current is below low alarm level	RO	0
1.41072.1	Laser Output Power High Alarm	Set when laser output power exceeds high alarm level	RO	0
1.41072.0	Laser Output Power Low Alarm	Set when laser output power is below low alarm level	RO	0
1.41073.7	Receive Optical Power High Alarm	Set when receive optical power exceeds high alarm level	RO	0
1.41073.6	Receive Optical Power Low Warning	Set when receive optical power is below low warning level	RO	0
1.41073.0-5	Reserved			
1.41074-75.7:1	Reserved			
1.41076.7	Transceiver Temp High Warning	Set when transceiver temp exceeds high warning level	RO	0
1.41076.6	Transceiver Temp Low Warning	Set when transceiver temp is below low warning level	RO	0
1.41076.4-5	Reserved			
1.41076.3	Laser Bias Current High Warning	Set when laser bias current exceeds high warning level	RO	0
1.41076.2	Laser Bias Current Low Warning	Set when laser bias current is below low warning level	RO	0
1.41076.1	Laser Output Power High Warning	Set when laser output power exceeds high warning level	RO	0
1.41076.0	Laser Output Power Low Warning	Set when laser output power is below low warning level	RO	0
1.41077.7	Receive Optical Power High Warning	Set when receive optical power exceeds high warning level	RO	0
1.41077.6	Receive Optical Power Low Warning	Set when receive optical power is below low warning level	RO	0

Operation

A top-level block diagram of Digital Optical Monitoring (DOM) incorporated into the Link Alarm Status Interrupt (LASI) function is shown in Figure 12.

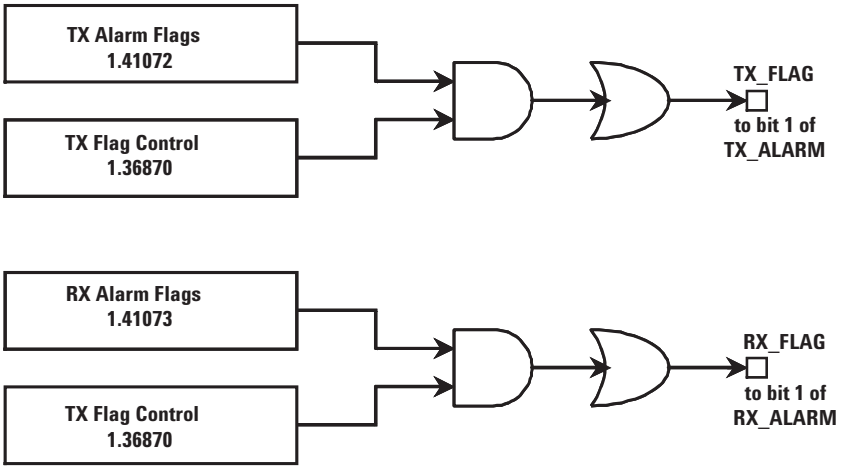


Figure 12. DOM/LASI Block Diagram

TX_FLAG Status

Assertion of TX_FLAG indicates that one or more of the transmitter operating parameters (transceiver temperature, laser bias current, or laser output power) exceeds the alarm levels. Tx alarm flags only monitor A/D values in registers 1.41056-1.41069. TX_FLAG shall be the logic OR of the bits in register 1.41072. The contents of the TX_FLAG status register are shown below. Bit 1 of TX_ALARM (TX_FLAG) will have the properties of latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

TX_FLAG Control

TX_FLAG may be programmed to assert only when specific transmit operation parameters exceed their alarm levels. The programming is performed by writing the contents of a mask register located at offset 1.36870. The contents of register 1.41072 shall be AND'ed with the contents of register 1.36870 prior to application of the OR function that generates the TX_FLAG signal.

Table 20. Register 1.36870: TX_FLAG Control Bits

Bit(s)	Name	Description	Type	Default Value (dec)
1.36870.7	Temp high Enable	Transceiver Temp High Alarm Enable	RW	0
1.36870.6	Temp low enable	Transceiver Temp Low Alarm Enable	RW	0
1.36870.5:4		Reserved	RW	0
1.36870.3	Current High enable	Laser Bias Current High Alarm Enable	RW	0
1.36870.2	Current low enable	Laser Bias Current Low Alarm Enable	RW	0
1.36870.1	LoP high enable	Laser Output Power High Alarm Enable	RW	0
1.36870.0	LoP low enable	Laser Output Power Low Alarm Enable	RW	0

RX_FLAG Status

Assertion of RX_FLAG indicates that one or more of the receiver operating parameters (receive optical power) exceeds the alarm levels. Rx alarm flags only monitor A/D values in registers 1.41056-1.41070. RX_FLAG shall be the logic OR of the bits in register 1.41073. The contents of the RX_FLAG status register are shown below. Bit 1 of RX_ALARM (RX_FLAG) will have the properties of latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

RX_FLAG Control

RX_FLAG may be programmed to assert only when specific receive operation parameters exceed their alarm levels. The programming is performed by writing the contents of a mask register located at offset 1.36871. The contents of register 1.41072 shall be AND'ed with the contents of register 1.36871 prior to application of the OR function that generates the RX_FLAG signal.

Table 21. Register 1.36871: RX_FLAG Control Bits

Bit(s)	Name	Description	Type	Default Value (dec)
1.36871.7	Rx power High enable	Receive Optical Power High Alarm Enable	RW	0
1.36871.6	Rx power low enable	Receive Optical Power Low Alarm Enable	RW	0
1.36871.5:0		Reserved	RW	0

Regulatory Compliance

The HFBR-707X2DEM is intended to enable commercial system designers to develop equipment that complies with the various regulations governing Certification of Information Technology equipment (see Table 22).

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important. The first case is during handling of the transceiver prior to plugging into the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas. The second case to consider is static charges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the SC duplex connector of the transceiver part is exposed outside of the equipment chassis, the HFBR-707X2DEM transceiver is designed to withstand types and levels of ESD indicated in Table 22 to enable equipment compliance to the system level criteria it is intended to meet.

Electromagnetic Interference (EMI)

Most equipment design utilizing these high speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. Performance of the HFBR-707X2DEM transceiver is dependent upon customer board and chassis design.

Immunity

Equipment utilizing these transceivers will be subject to radio frequency electromagnetic fields in some environments. These transceivers have been characterized without the benefit of the normal equipment chassis enclosure and results are reported below. Performance of a system containing these transceivers within a well-designed chassis enclosure is expected to be better than the results of these tests without a chassis enclosure.

Laser Eye Safety

The HFBR-707X2DEM transceiver is a Class 1 laser product, compliant with IEC 60825-1:2001-8. The output radiation wavelength is in the 1260-1355 nm range. The maximum output power radiation of a module affected by a single fault is 5 mW. Also see table 22.

Table 22. Regulatory Compliance

Feature	Test Method	Performance
General	Telcordia GR-468-CORE	Qualified in accordance with Remote terminal requirements
Electrostatic Discharge - Human Body Model	MIL STD 883 Method 3015	500 V
Electrostatic Discharge - Charged Device Model	JEDEC JES D22-C101	500 V
Electrostatic Discharge - Contact Discharge Air Discharge	IEC 61000-4-2	8000 V15000 V
Electromagnetic Interference	FCC Class BCENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Margins are dependant on customer board and chassis design
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 80 MHz to 10 GHz applied to the transceiver without a chassis enclosure.
Laser Eye Safety	US FDA CDRH AEL Class 1 US 21 CFR, Subchapter J, 1040.10 and Laser Notice # 50 (IEC) EN60825-1:2001-8	CDRH: in progress TUV: in progress
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL certificate number PENDING

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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