



HEF4894B-Q100

12-stage shift-and-store register LED driver

Rev. 3 — 13 August 2024

Product data sheet

1. General description

The HEF4894B-Q100 is a 12-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel LED driver outputs (QP0 to QP11). Data is shifted on positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the output whenever the output enable (OE) input signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4894B-Q100 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4894B-Q100 devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4894BT-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
HEF4894BTT-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

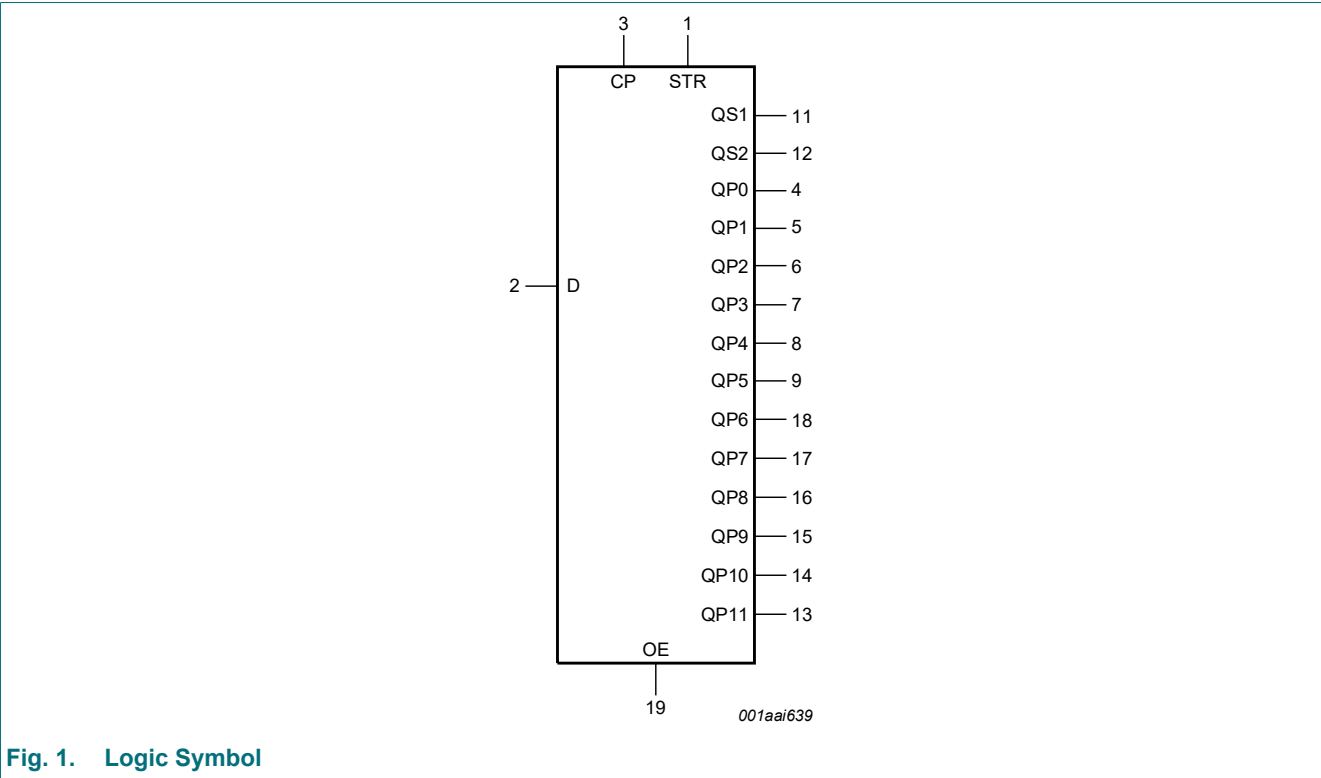


Fig. 1. Logic Symbol

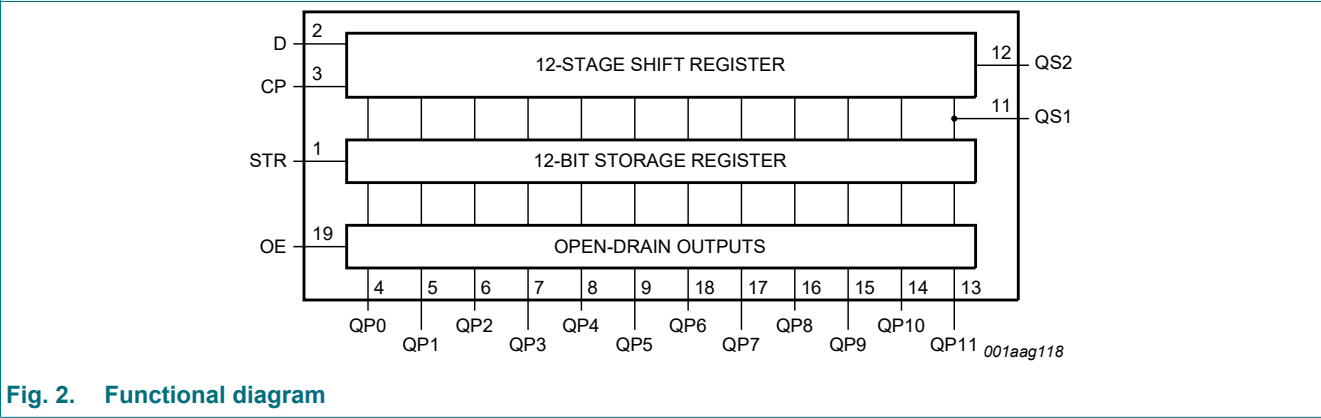


Fig. 2. Functional diagram

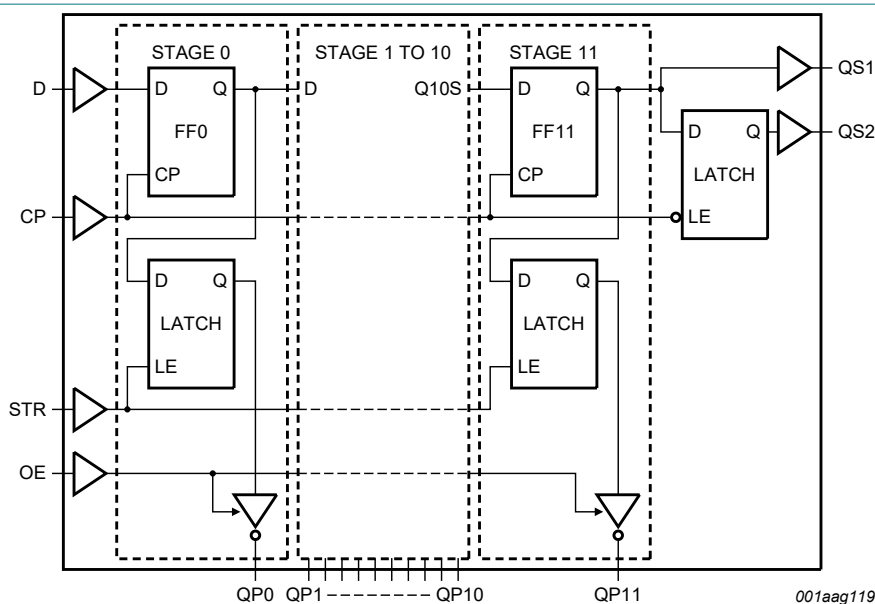
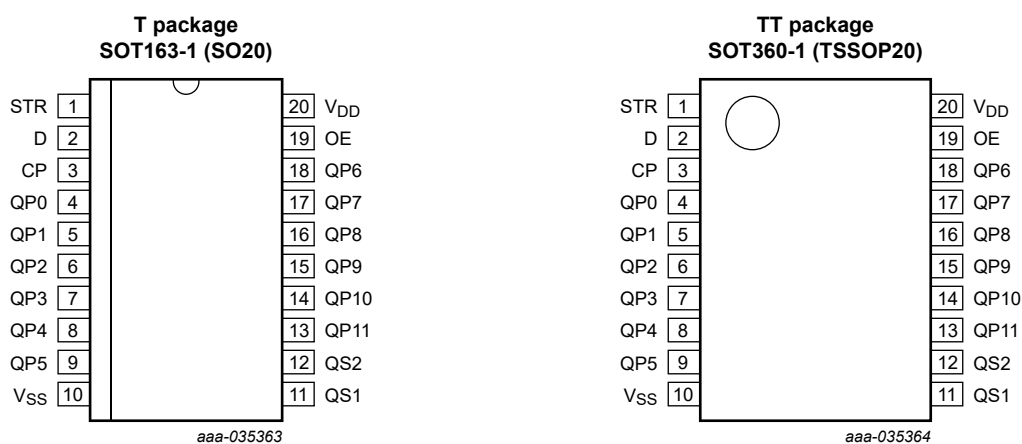


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D	2	serial input
QP0 to QP11	4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	parallel output
QS1	11	serial output
QS2	12	serial output
CP	3	clock input
STR	1	strobe input
OE	19	output enable input
V _{DD}	20	supply voltage
V _{SS}	10	ground (0 V)

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW clock transition; Z = high-impedance OFF-state.
At the LOW-to-HIGH clock transition, the information in the 10th register stage is transferred to the 11th register stage and the QS output.

Control			Input	Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1[1]	QS2[2]
↑	L	X	X	Z	Z	Q10S	no change
↓	L	X	X	Z	Z	no change	Q11S
↑	H	L	X	no change	no change	Q10S	no change
↑	H	H	L	Z	QPn - 1	Q10S	no change
↑	H	H	H	L	QPn - 1	Q10S	no change
↓	H	H	H	no change	no change	no change	Q11S

[1] Q10S = the data in register stage 10 before the LOW-to-HIGH clock transition.
[2] Q11S = the data in register stage 11 before the HIGH-to-LOW clock transition.

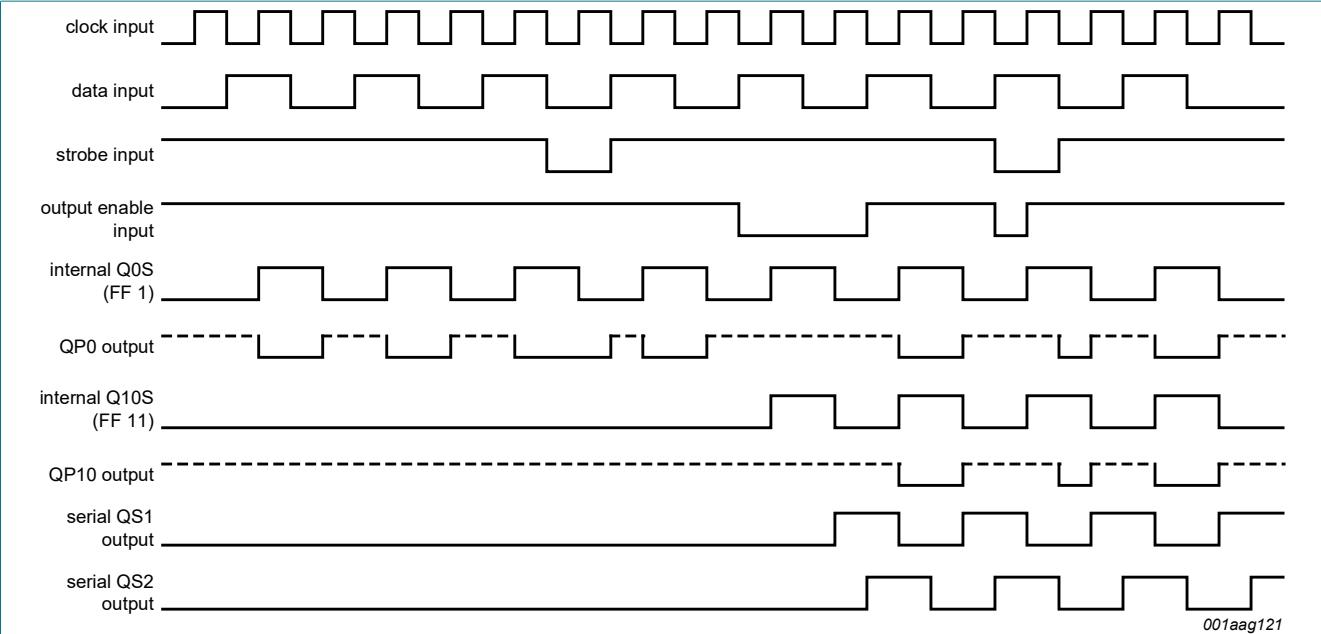


Fig. 4. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	QSn outputs; $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
		QPn outputs; $V_O < 0.5\text{ V}$	-	40	mA
I_I	input leakage current		-	± 10	mA
I_O	output current	QSn outputs	-	± 10	mA
		QPn outputs	-	40	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = +25\text{ }^{\circ}\text{C}$		$T_{amb} = +85\text{ }^{\circ}\text{C}$		$T_{amb} = +125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	QSn outputs; $ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	QSn outputs; $ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
		QPn outputs; $ I_O < 20\text{ mA}$	5 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			10 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			15 V	-	0.75	-	0.75	-	1.5	-	1.5	V
I_{OH}	HIGH-level output current	QSn outputs										
		$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	QSn outputs										
		$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{OZ}	OFF-state output current	QPn output is HIGH; $V_O = 15\text{ V}$	5 V	-	2	-	2	-	15	-	15	μA
			10 V	-	2	-	2	-	15	-	15	μA
			15 V	-	2	-	2	-	15	-	15	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$ unless otherwise specified. For test circuit see [Fig. 9](#).

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	CP to QS1; see Fig. 5	5 V	[1] 132 ns + (0.55 ns/pF)C _L	-	160	320	ns
			10 V	53 ns + (0.23 ns/pF)C _L	-	65	130	ns
			15 V	37 ns + (0.16 ns/pF)C _L	-	45	90	ns
		CP to QS2; see Fig. 5	5 V	92 ns + (0.55 ns/pF)C _L	-	120	240	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _{PLH}	LOW to HIGH propagation delay	CP to QS1; see Fig. 5	5 V	[1] 102 ns + (0.55 ns/pF)C _L	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
		CP to QS2; see Fig. 5	5 V	102 ns + (0.55 ns/pF)C _L	-	130	260	ns
			10 V	49 ns + (0.23 ns/pF)C _L	-	60	120	ns
			15 V	37 ns + (0.16 ns/pF)C _L	-	45	90	ns
t _{PZL}	OFF-state to LOW propagation delay	CP to QPn; see Fig. 5	5 V		-	240	480	ns
			10 V		-	80	160	ns
			15 V		-	55	110	ns
		STR to QPn; see Fig. 6	5 V		-	140	280	ns
			10 V		-	70	140	ns
			15 V		-	55	110	ns
t _{PLZ}	LOW to OFF-state propagation delay	CP to QPn; see Fig. 5 and Fig. 6	5 V		-	170	340	ns
			10 V		-	75	150	ns
			15 V		-	60	120	ns
		STR to QPn; see Fig. 6	5 V		-	100	200	ns
			10 V		-	40	100	ns
			15 V		-	35	70	ns
t _{en}	enable time	OE to QPn; see Fig. 7	5 V	[2]	-	100	200	ns
			10 V		-	55	110	ns
			15 V		-	50	100	ns
t _{dis}	disable time	OE to QPn; see Fig. 7	5 V	[2]	-	80	160	ns
			10 V		-	40	80	ns
			15 V		-	30	60	ns
t _t	transition time	QS1, QS2; see Fig. 5	5 V	[1][3] 35 ns + (1.00 ns/pF)C _L	-	85	170	ns
			10 V	19 ns + (0.42 ns/pF)C _L	-	40	80	ns
			15 V	16 ns + (0.28 ns/pF)C _L	-	30	60	ns
t _W	pulse width	CP; LOW and HIGH; see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		STR; HIGH; see Fig. 6	5 V		80	40	-	ns
			10 V		60	30	-	ns
			15 V		24	12	-	ns

12-stage shift-and-store register LED driver

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{su}	set-up time	D to CP; see Fig. 8	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
t _h	hold time	D to CP; see Fig. 8	5 V		+5	-15	-	ns
			10 V		20	5	-	ns
			15 V		20	5	-	ns
f _{clk(max)}	maximum clock frequency	CP; see Fig. 5	5 V		5	10	-	MHz
			10 V		11	22	-	MHz
			15 V		14	28	-	MHz

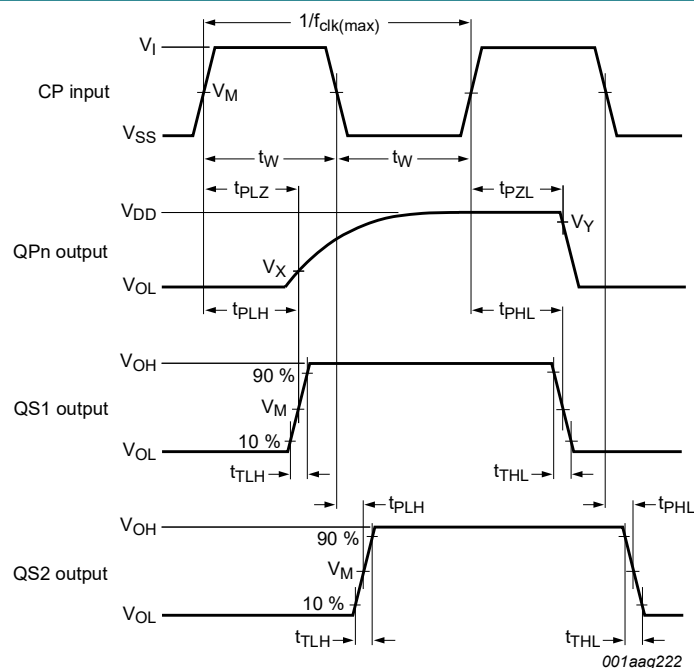
- [1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
- [2] t_{en} is the same as t_{pZL} and t_{dis} is the same as t_{pLZ} .
- [3] t_t is the same as t_{TLH} and t_{THL} .

Table 8. Dynamic power dissipation

P_D can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V _{DD}	Typical formula	Where
P _D	dynamic power dissipation	5 V	$P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2 \mu W$	f _i = input frequency in MHz;
		10 V	$P_D = 5550 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2 \mu W$	f _o = output frequency in MHz;
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2 \mu W$	C _L = output load capacitance in pF; Σ(f _o × C _L) = sum of the outputs; V _{DD} = supply voltage in V.

10.1. Waveforms and test circuit



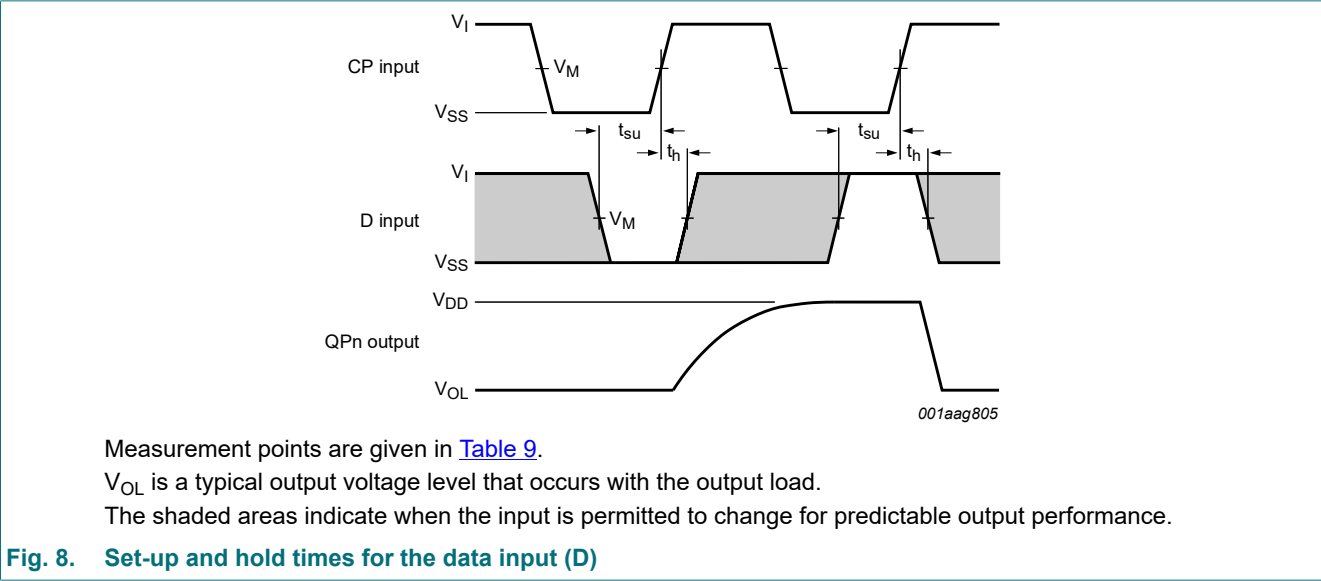
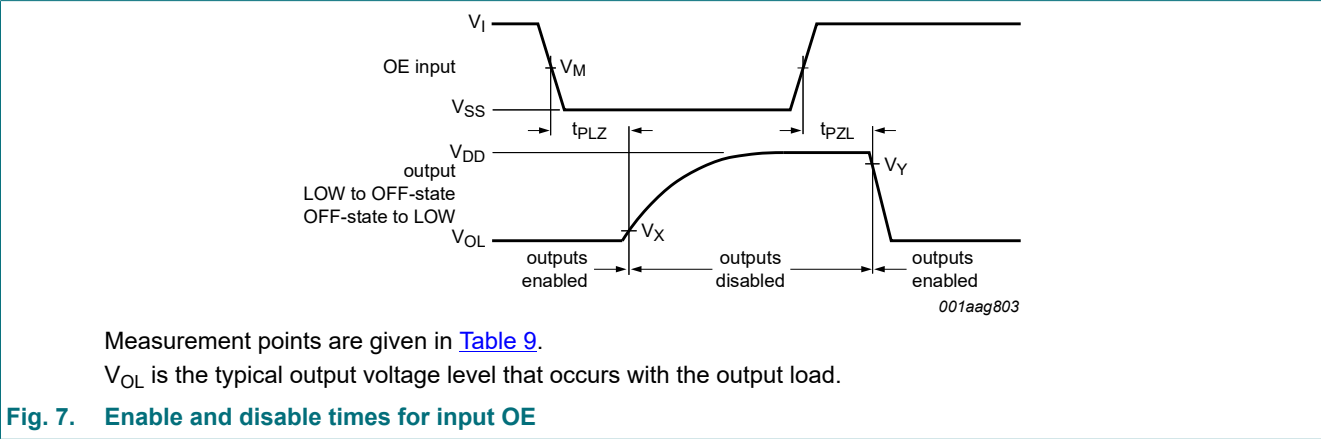
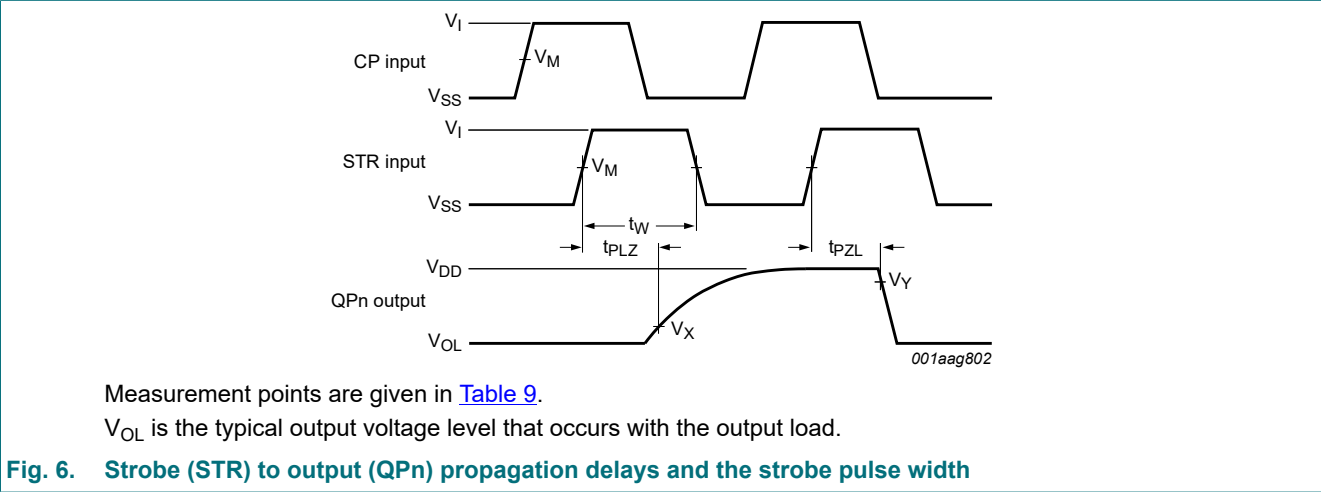
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency

Table 9. Measurement points

Supply	Input	Output		
V _{DD}	V _M	V _M	V _X	V _Y
5 V to 15 V	0.5V _{DD}	0.5V _{DD}	0.1V _O	0.9V _O



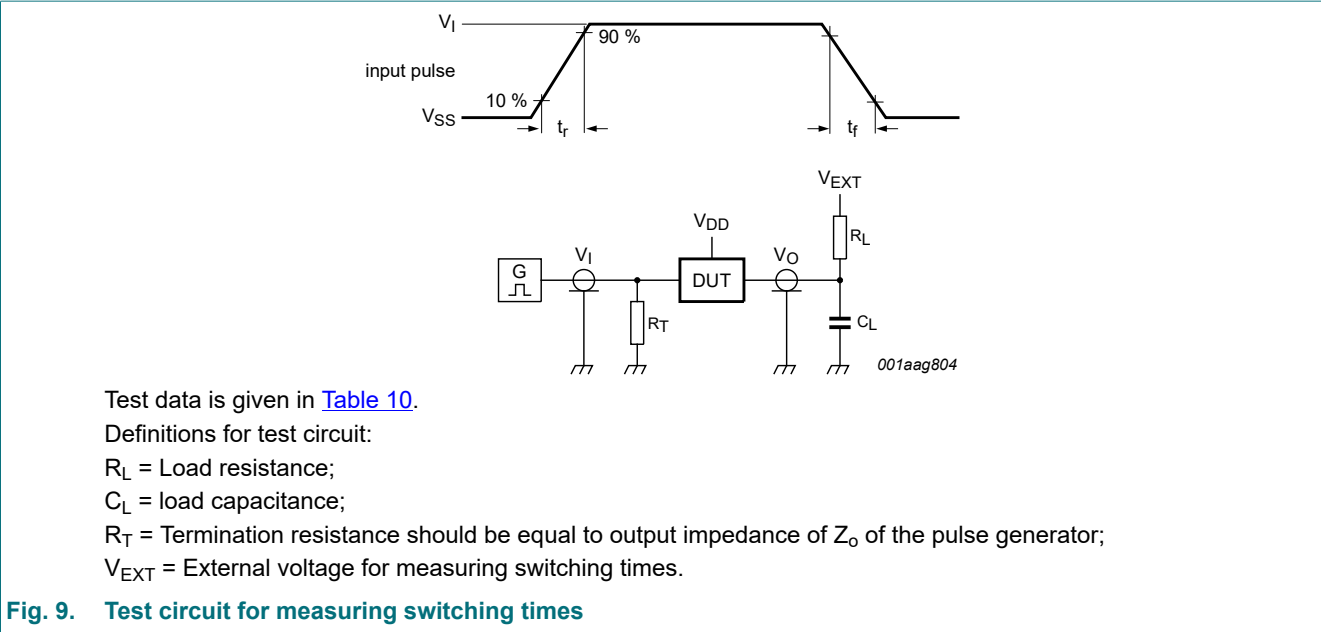
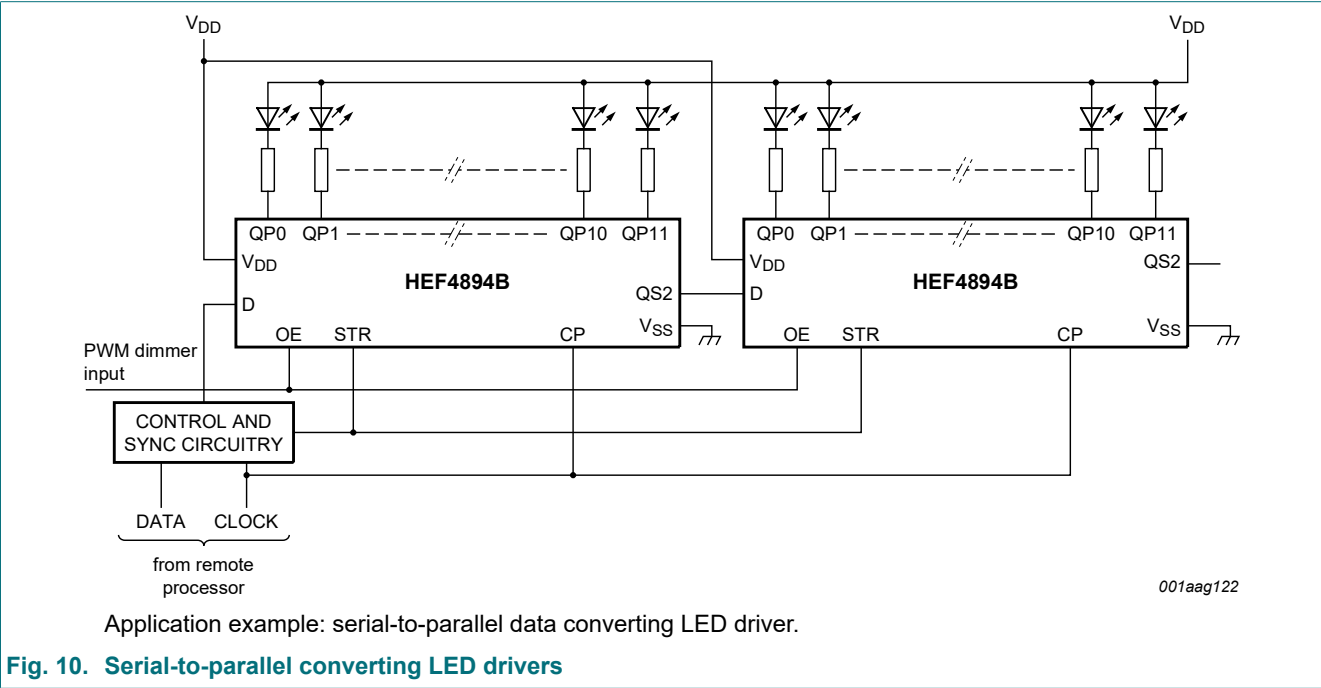


Table 10. Test data

Supply	Input		V_{EXT}		Load	
V_{DD}	V_I	t_r, t_f	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}	C_L	R_L
5 V to 15 V	V_{DD}	≤ 20 ns	V_{DD}	open	50 pF	1 k Ω

11. Application information



12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

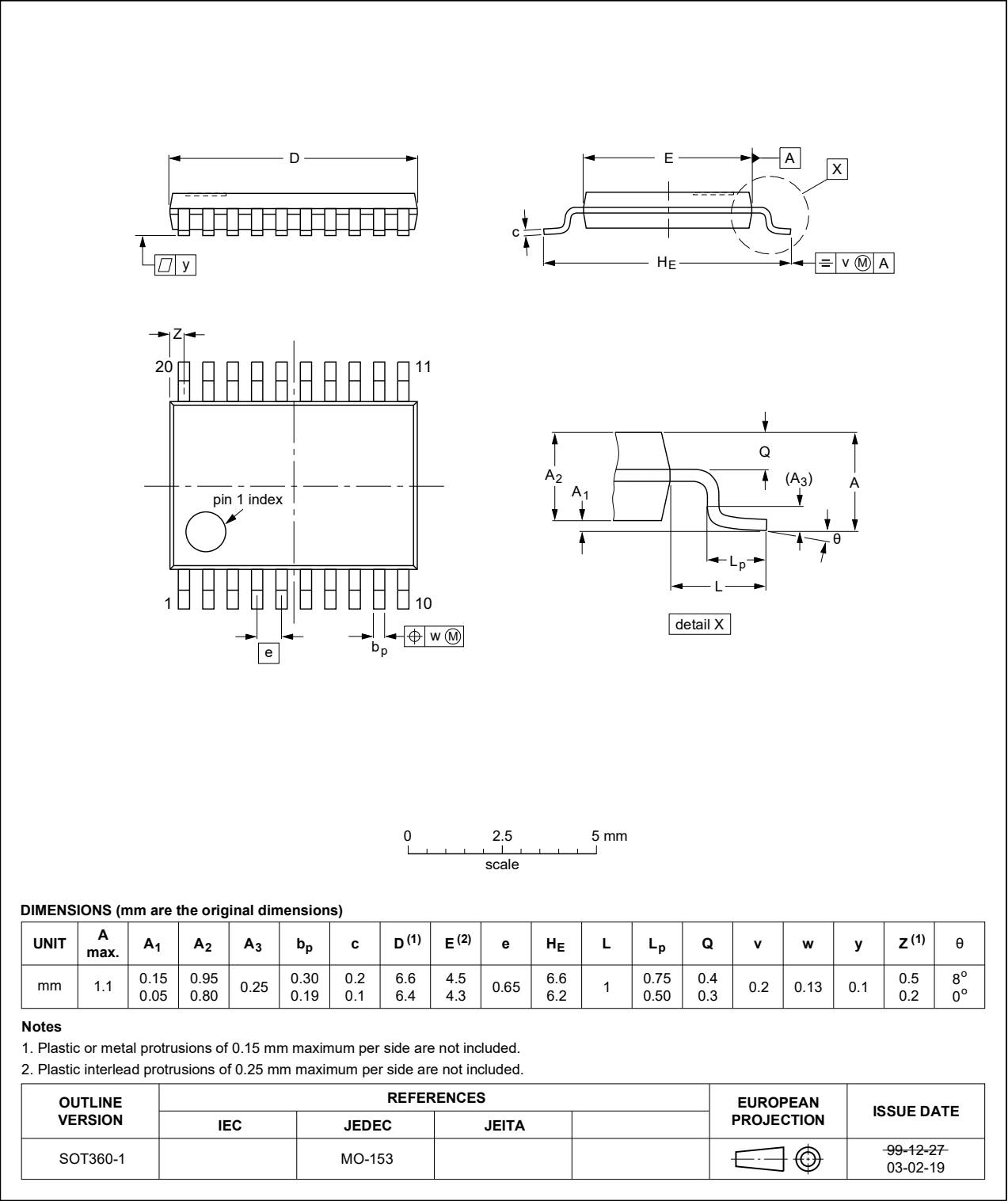


Fig. 12. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LED	Light Emitting Diode

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4894B_Q100 v.3	20240813	Product data sheet	-	HEF4894B_Q100 v.2
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.			
HEF4894B_Q100 v.2	20211123	Product data sheet	-	HEF4894B_Q100 v.1
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Section 7: Derating values for P_{tot} total power dissipation updated.Section 2 updated.			
HEF4894B_Q100 v.1	20120712	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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