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## 1. General Description

HE83R123 is a member of 8-bit MCU series developed by King Billion. 32 LCD segment driver pins are multiplexed with I/O pins to provide flexibility of wide variety of combinations to suit the needs of applications. Users can choose any one of combinations from 320 dots LCD Driver with 8 Bit I/O Port to 64 dots LCD Driver with 40-bit I/O Port, etc. by mask option. The built-in LCD power regulator can provide stable LCD display effect over wide range of battery voltage. The Pulse Width Modulation with complementary outputs provides the complete speech output mechanism. The 64K ROM can store around 20 second of speech. This chip is applicable to the small/medium systems such as LCD Games, Perpetual Calendar etc. The instruction set of HE80000 is easy to learn and use. Most of instructions take only 3 cycles.

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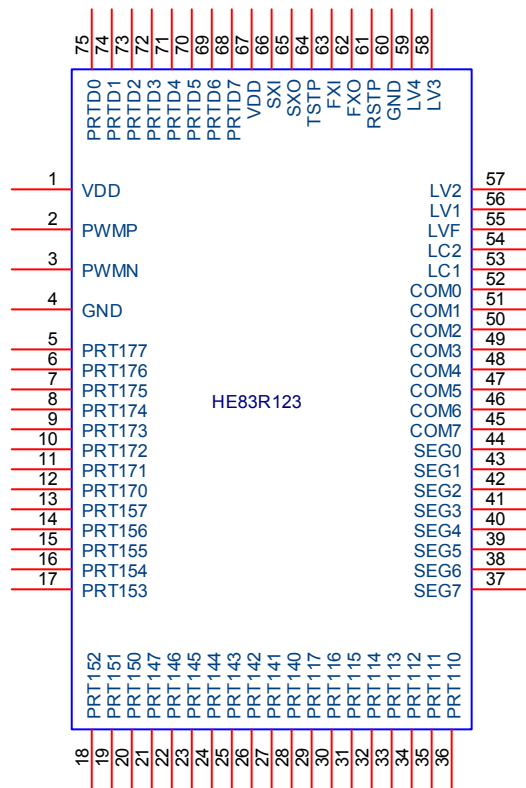
oscillator clocks. This chip is suitable for the applications that require higher performance.

## 2. Features

- ✓ Operation Voltage: 2.4V ~ 5.5V
- ✓ System Clock: DC ~ 8 MHz @ 5.0V  
DC ~ 4 MHz @ 2.4V
- ✓ Internal ROM: 64 KB
- ✓ Internal RAM: 256 Bytes
- ✓ Dual Clock System: Fast clock: 32768 ~ 8M Hz  
Slow clock: 32768 Hz
- ✓ 4 Operation Modes: Fast, Slow, Idle, Sleep modes.
- ✓ Watch Dog Timer to prevent deadlock condition.
- ✓ 40-bit Bi-directional I/O port with push-pull or Open-Drain output type selectable for each I/O pin by mask option. 32 of them are multiplexed with LCD segment pins.
- ✓ 64 (8 COM x 8 SEG) ~ 320 (8 COM x 40 SEG) dot LCD driver.
- ✓ Built-in LCD power regulator to provide stable working voltage (~3Volt)
  - ◆ When  $VDD \geq 2.4\text{V}$ , LV4 output voltage around 3volts.
  - ◆ When  $VDD < 2.4\text{V}$ ; LV4, 3, 2, 1 output voltage will going down with VDD
- ✓ Complementary Pulse-Width Modulation outputs.
- ✓ Two external interrupts and two internal timer interrupts.
- ✓ Two 16-bit timers.
- ✓ Instruction set: 32 instructions with 4 addressing modes.
- ✓ Application field: LCD Games, Perpetual Calendar, etc.



## 3. Pin Description



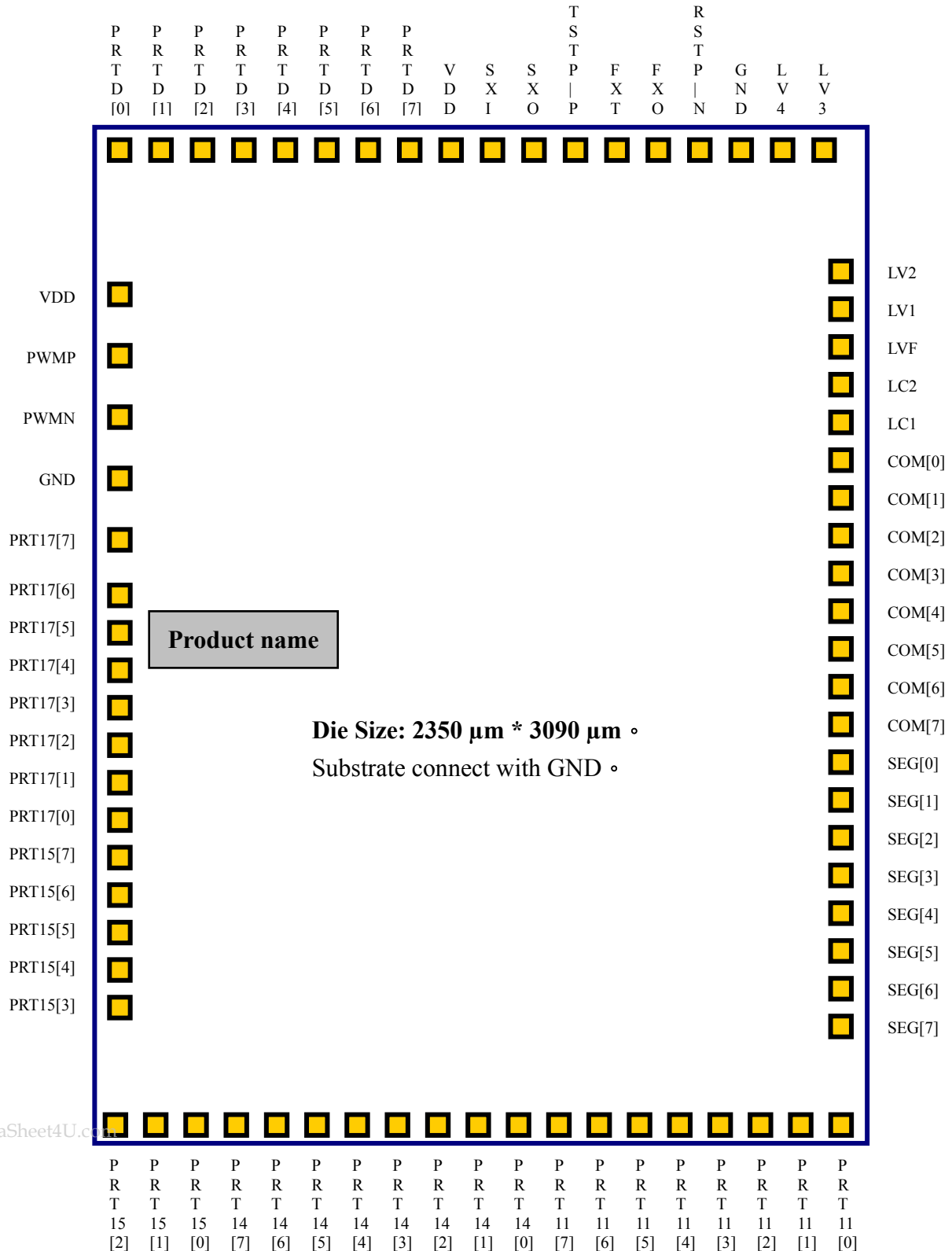
Pin Name	Pin #	I/O	Description
VDD	1	P	Dedicated Power for Pulse Width Modulation output.
PWMP	2	O	Pulse Width Modulation output.
PWMN	3	O	Complementary output to PWMP.
GND	4	P	Dedicated Power for Pulse Width Modulation output.
PRT17[7..0]	5 ~ 12	B/ O	8-bit bi-directional I/O port 17 is shared with LCD segment pads SEG[39..32]. The function of the pad can be selected individually by mask options MO_LIO17[7..0]. ('1' for LCD and '0' for I/O). The output type of I/O pad can also be selected by mask option MO_17PP[7..0] (1 for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, "1" must be outputted before reading.
PRT15[7..0]	13 ~ 20	B/ O	8-bit bi-directional I/O port 15 is shared with LCD segment pads SEG[31..24]. The function of the pad can be selected individually by mask options MO_LIO15[7..0]. ('1' for LCD and '0' for I/O). The output type of I/O pad can also be selected by mask option MO_15PP[7..0] (1 for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, "1" must be outputted before reading.
PRT14[7..0]	21 ~ 28	B/ O	8-bit bi-directional I/O port 14 is shared with LCD segment pads SEG[23..16]. The function of the pad can be selected individually by mask options MO_LIO14[7..0]. ('1' for LCD and '0' for I/O). The output type of I/O pad can also be selected by mask option MO_14PP[7..0] (1 for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using



Pin Name	Pin #	I/O	Description
			the I/O as input, “1” must be outputted before reading.
PRT11[7..0]	29 ~ 36	B/ O	8-bit bi-directional I/O port 11 is shared with LCD segment pads SEG[15..8]. The function of the pad can be selected individually by mask options MO_LIO11[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_11PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
SEG[7..0]	37 ~ 44	O	LCD SEGMENT SEG[7..0] outputs.
COM[7..0]	45 ~ 52	O	LCD COMMON Driver pads.
LC1	53	B	Charge Pump Capacitor Pin
LC2	54	B	Charge Pump Capacitor Pin
LVF	55	I	Regulator Feedback input. The regulator output voltage can be adjusted by the resistor between LV1 and LVF pads
LV1	56	B	LCD Charge Pump Voltage V1
LV2	57	B	LCD Charge Pump Voltage V2
LV3	58	B	LCD Charge Pump Voltage V3
LV4	59	B	LCD Charge Pump Voltage V4
GND	60	P	Power ground Input.
RSTP_N	61	I	System Reset input pin. Level trigger, active low on this pin will put the chip in reset state.
FXO, FXI	62, 63	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL (‘0’ for RC type and ‘1’ for crystal type). For RC type oscillator, one resistor need to be connected between FXI and GND. For crystal oscillator, one crystal need to be placed between FXI and FXO. Please refer to application for details.
TSTP_P	64	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	65, 66	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose ‘0’ for RC type and ‘1’ for crystal oscillator.
VDD	67	P	Positive power Input. 0.1 $\mu$ F decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
PRTD[7..0]	68 ~ 75	B	8-bit bi-directional general purpose I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, ‘1’ must be outputted before reading the pin. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be used as external interrupt sources.



## 4. Pad Location





PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	VDD	-1110.00	1173.40	39	SEG[5]	1110.00	-890.90
2	PWMP	-1110.00	974.10	40	SEG[4]	1110.00	-775.50
3	PWMN	-1110.00	699.30	41	SEG[3]	1110.00	-660.10
4	GND	-1110.00	500.10	42	SEG[2]	1110.00	-544.70
5	PRT17[7]	-1110.00	263.10	43	SEG[1]	1110.00	-429.30
6	PRT17[6]	-1110.00	147.70	44	SEG[0]	1110.00	-313.90
7	PRT17[5]	-1110.00	32.30	45	COM[7]	1110.00	-198.50
8	PRT17[4]	-1110.00	-83.10	46	COM[6]	1110.00	-83.10
9	PRT17[3]	-1110.00	-198.50	47	COM[5]	1110.00	32.30
10	PRT17[2]	-1110.00	-313.90	48	COM[4]	1110.00	147.70
11	PRT17[1]	-1110.00	-429.30	49	COM[3]	1110.00	263.10
12	PRT17[0]	-1110.00	-544.70	50	COM[2]	1110.00	378.50
13	PRT15[7]	-1110.00	-660.10	51	COM[1]	1110.00	493.90
14	PRT15[6]	-1110.00	-775.50	52	COM[0]	1110.00	609.30
15	PRT15[5]	-1110.00	-890.90	53	LC1	1110.00	724.70
16	PRT15[4]	-1110.00	-1006.30	54	LC2	1110.00	840.10
17	PRT15[3]	-1110.00	-1121.70	55	LVF	1110.00	955.50
18	PRT15[2]	-1076.35	-1480.00	56	LV1	1110.00	1070.90
19	PRT15[1]	-960.95	-1480.00	57	LV2	1110.00	1186.30
20	PRT15[0]	-807.55	-1480.00	58	LV3	1018.00	1480.00
21	PRT14[7]	-692.15	-1480.00	59	LV4	902.60	1480.00
22	PRT14[6]	-576.75	-1480.00	60	GND	787.20	1480.00
23	PRT14[5]	-461.35	-1480.00	61	RSTP_N	671.80	1480.00
24	PRT14[4]	-345.95	-1480.00	62	FXO	556.40	1480.00
25	PRT14[3]	-230.55	-1480.00	63	FXI	441.00	1480.00
26	PRT14[2]	-115.15	-1480.00	64	TSTP_P	325.60	1480.00
27	PRT14[1]	0.25	-1480.00	65	SXO	166.20	1480.00
28	PRT14[0]	115.65	-1480.00	66	SXI	5.05	1480.00
29	PRT11[7]	231.05	-1480.00	67	VDD	-110.35	1480.00
30	PRT11[6]	346.45	-1480.00	68	PRTD[7]	-288.90	1480.00
31	PRT11[5]	461.85	-1480.00	69	PRTD[6]	-404.30	1480.00
32	PRT11[4]	577.25	-1480.00	70	PRTD[5]	-519.70	1480.00
33	PRT11[3]	692.65	-1480.00	71	PRTD[4]	-635.10	1480.00
34	PRT11[2]	808.05	-1480.00	72	PRTD[3]	-750.50	1480.00
35	PRT11[1]	923.45	-1480.00	73	PRTD[2]	-865.90	1480.00
36	PRT11[0]	1076.85	-1480.00	74	PRTD[1]	-981.30	1480.00
37	SEG[7]	1110.00	-1121.70	75	PRTD[0]	-1096.70	1480.00
38	SEG[6]	1110.00	-1006.30				

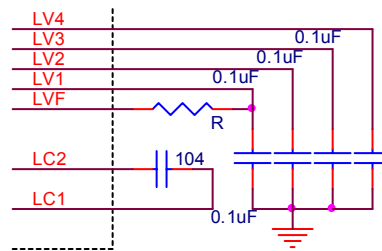
## 5. LCD Power Supply

The LCD power supply is equipped with input power regulator, voltage charge pump, and bias voltage generating resistor network. The input power of MCU is regulated and multiplied by 4 times to generate LCD bias for LCD driver. The regulator output voltage can be adjusted by the resistor between LV1 and

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LVF pads.



With the regulated LCD power, the LCD display can give steady visual effect over a wide range of operating voltage. The built-in regulator must be enabled by mask option MO\_LVRG to function.

MO_LVRG	Function
0	Disable LCD regulator
1	Enable LCD regulator

Please note that to emulate the visual effect of 1/4 bias on the ICE 3.X version the LR2 and LR3 on the top board need be shorted.

## 6. LCDC Control register

LCD Control Register LCDC controls the functions of LCD driver; such as contrast level, LCD waveform type, On/Off, Blank, etc.

LCDC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	-	-	TYPE	BLANK	LCDE

Field	Value	Function
TYPE	0	Select Type A LCD waveform
	1	Select Type B LCD waveform
BLANK	0	Normal display
	1	LCD display blanked. LCD driver changes only COM output signal, SEG signal remains unchanged.
LCDE	0	LCD driver disabled, LCD driver has no output signal.
	1	LCD driver Enabled

Please note that LCD driver must be turned off before the entering sleep mode. That means user must clear the bit 0 of LCDC to turn off LCD driving circuit before setting bit 6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please also note that LCD driver uses slow clock as clock source. The LCD display will not display normally if it works in Fast clock only mode because the LCD refresh action is too fast.

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V1.0E

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## 7. LCD RAM map

	SEG[39..32]	SEG[31..24]	SEG[23..16]	SEG[15..8]	SEG[7..0]
COM0	F8H	F0H	E8H	E0H	D8H
COM1	F9H	F1H	E9H	E1H	D9H
COM2	FAH	F2H	EAH	E2H	DAH
COM3	FBH	F3H	EBH	E3H	DBH
COM4	FCH	F4H	ECH	E4H	DCH
COM5	FDH	F5H	EDH	E5H	DDH
COM6	FEH	F6H	EEH	E6H	DEH
COM7	FFH	F7H	EFH	E7H	DFH

## 8. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. So that system designer can select oscillator types based on the cost target, timing accuracy requirements etc. With two clock sources available, the system can switch among operation modes of normal, slow, idle, and sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	1	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	-	-	-	-	-
Mode	R/W	R/W	R/W	-	-	-	-	-
Reset	0	-	-	0	-	-	-	-

Crystal, Resonator or the RC oscillator or internal RC can be used as fast clock source. If the internal RC oscillator is used, then no external component is necessary. Please note that oscillation frequency of internal RC oscillator may vary with parameters of IC fabrication process. Therefore if timing accuracy is essential in targeted applications, then internal RC is not recommended.

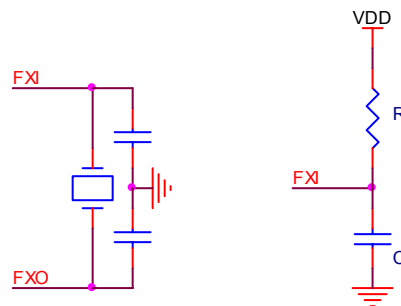
Name	Value	Function
MO_FOSCE	0	Internal fast OSC
	1	External fast OSC
MO_FRFCI_S[2:0]	000	RFRC_I $\sim$ 500k
	001	RFRC_I $\sim$ 1M
	010	RFRC_I $\sim$ 1.5M
	011	RFRC_I $\sim$ 2M
	100	RFRC_I $\sim$ 2.5M



	101	RFRC I $\sim$ 3M
	110	RFRC I $\sim$ 3.5M
	111	RFRC I $\sim$ 4M

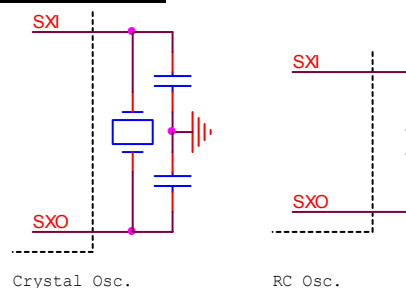
When Crystal oscillator or external RC are used, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO\_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.



Two types of oscillator, crystal and RC, can be used as slow clock by mask option MO\_SXTAL. If used in for time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	RC oscillator
1	Crystal oscillator



If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

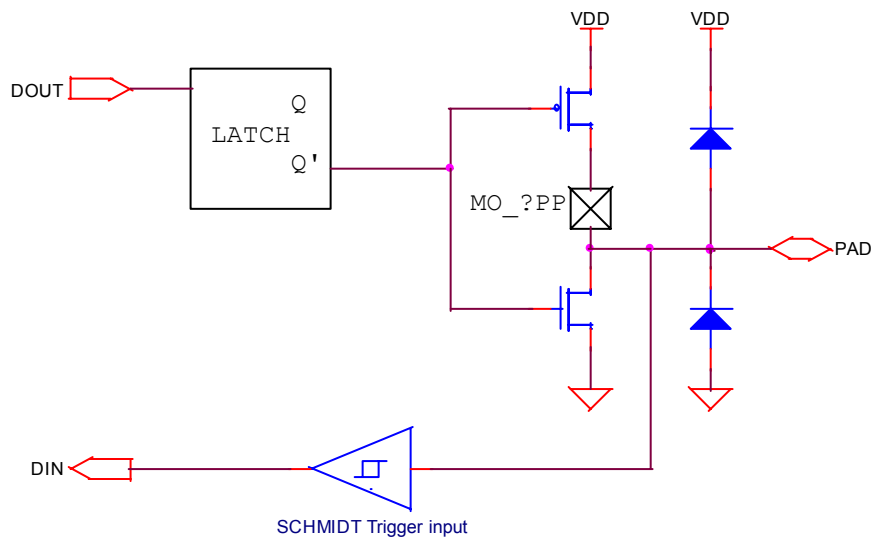
## 9. General Purpose I/O

There is one dedicated general purpose I/O port PRTD. All the I/O Ports are bi-directional and of non-tri-state output structure. The output has weak sourcing (50  $\mu$ A) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask

option. The input port has built-in Schmidt trigger to prevent it from chattering. The hysteresis level of Schmidt trigger is 1/3 VDD.

MO_DPP[7..0]	Output Structure
0	Open-drain output
1	Push-pull output

When the I/O port is used as input, the weakly high sourcing PMOS can be used as pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin, otherwise, the pin will always be stuck at '0'. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.



PRT11[7..0], PRT14[7..0], PRT15[7..0] and PRT17[7..0] share pads with SEG[8..39]. The function of the pins is selected by mask option MO\_LIO11, MO\_LIO14, MO\_LIO15, MO\_LIO17 respectively as shown in the following figure.



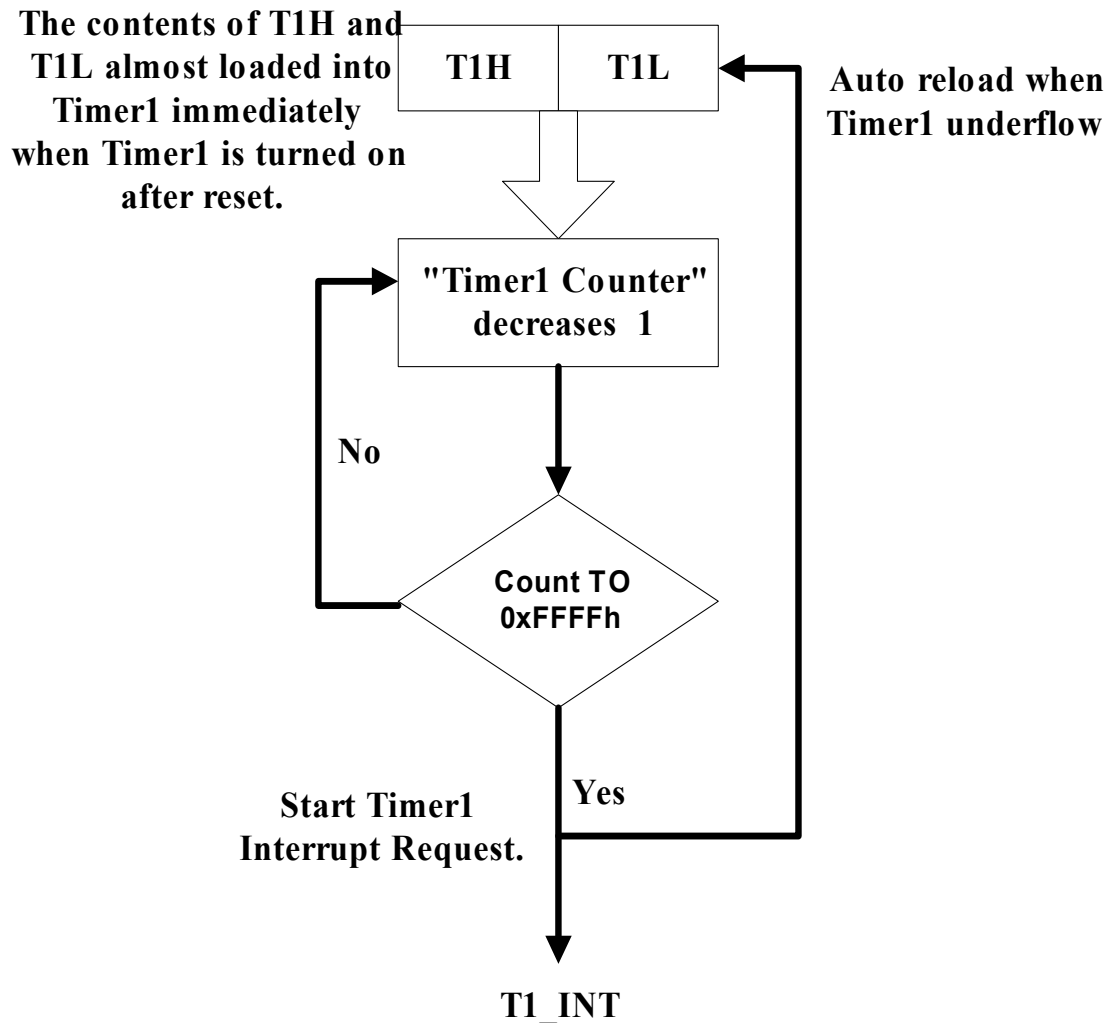
MO_LIO11=0			MO_LIO11=1		
PRT110	PRT110	SEG8	PRT110	PRT110	SEG8
PRT111	PRT111	SEG9	PRT111	PRT111	SEG9
PRT112	PRT112	SEG10	PRT112	PRT112	SEG10
PRT113	PRT113	SEG11	PRT113	PRT113	SEG11
PRT114	PRT114	SEG12	PRT114	PRT114	SEG12
PRT115	PRT115	SEG13	PRT115	PRT115	SEG13
PRT116	PRT116	SEG14	PRT116	PRT116	SEG14
PRT117	PRT117	SEG15	PRT117	PRT117	SEG15
-----			-----		
MO_LIO14=0			MO_LIO14=1		
PRT140	PRT140	SEG16	PRT140	PRT140	SEG16
PRT141	PRT141	SEG17	PRT141	PRT141	SEG17
PRT142	PRT142	SEG18	PRT142	PRT142	SEG18
PRT143	PRT143	SEG19	PRT143	PRT143	SEG19
PRT144	PRT144	SEG20	PRT144	PRT144	SEG20
PRT145	PRT145	SEG21	PRT145	PRT145	SEG21
PRT146	PRT146	SEG22	PRT146	PRT146	SEG22
PRT147	PRT147	SEG23	PRT147	PRT147	SEG23
-----			-----		
MO_LIO15=0			MO_LIO15=1		
PRT150	PRT150	SEG24	PRT150	PRT150	SEG24
PRT151	PRT151	SEG25	PRT151	PRT151	SEG25
PRT152	PRT152	SEG26	PRT152	PRT152	SEG26
PRT153	PRT153	SEG27	PRT153	PRT153	SEG27
PRT154	PRT154	SEG28	PRT154	PRT154	SEG28
PRT155	PRT155	SEG29	PRT155	PRT155	SEG29
PRT156	PRT156	SEG30	PRT156	PRT156	SEG30
PRT157	PRT157	SEG31	PRT157	PRT157	SEG31
-----			-----		
MO_LIO17=0			MO_LIO17=1		
PRT170	PRT170	SEG32	PRT170	PRT170	SEG32
PRT171	PRT171	SEG33	PRT171	PRT171	SEG33
PRT172	PRT172	SEG34	PRT172	PRT172	SEG34
PRT173	PRT173	SEG35	PRT173	PRT173	SEG35
PRT174	PRT174	SEG36	PRT174	PRT174	SEG36
PRT175	PRT175	SEG37	PRT175	PRT175	SEG37
PRT176	PRT176	SEG38	PRT176	PRT176	SEG38
PRT177	PRT177	SEG39	PRT177	PRT177	SEG39
-----			-----		

## 10. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
<b>IER</b>	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
<b>T1L</b>	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
<b>T1H</b>	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
<b>OP1</b>	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

## 11. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "F<sub>SYS</sub>". The system clock "F<sub>SYS</sub>" varies depending on the operation modes of the MCU.

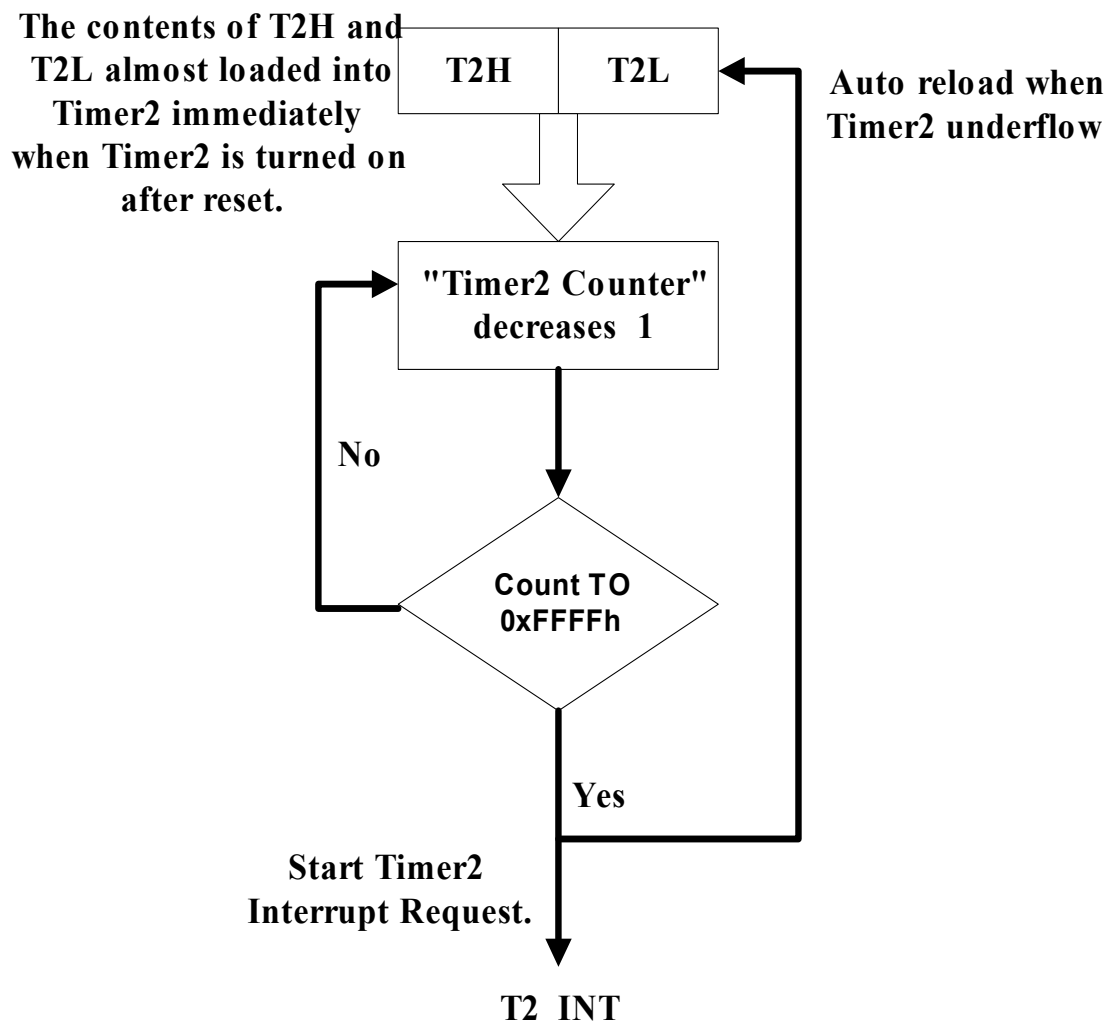
The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will

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be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.



The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
<b>IER</b>	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
<b>T2L</b>	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
<b>T2H</b>	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
<b>OP1</b>	0x09	TC2E	3	R/W	0: TC2 is disabled. (default)



Register	Address	Field	Bit position	Mode	Description
					1: TC2 is enabled.

## 12. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution. WDT needs to be enabled in Mask Option.

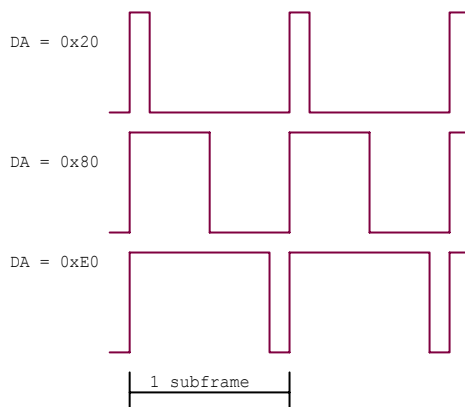
MO_WDTE	Function
0	WDT disable
1	WDT enable

To use WDT function, “CLRWDT” instruction needs to be executed in every possible program path when the program runs normally in order to clear the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

WDT is the enabling signal generated by calculating 32768-clock overflow. Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source. WDT function can be generated in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

## 13. Pulse-Width Modulation

The pulse-width modulator (PWM) converts 7-bit unsigned speech data written to PWMC data register to proportional duty cycle of PWM output. PWM module shares the PWMC data register with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the DA value.



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The PWM bit of VOC register controls register to enable the circuit and output driver. When PWM bit of



VOC is '0', PWME bit and output drivers settings are both cleared. To use PWM for voice output, PWM bit has to be set to '1' first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of PWMC command register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into Sleep mode or Idle mode, it will automatically turn off all voice outputs by clearing VOC[2..1] to "00". To activate voice output again when returning to Normal Mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register PWMC[6..4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

PWMC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

## 14. Summary of Registers and Mask Options

All the registers and mask options used in this chip are listed in the following tables.

Address	NAME	Field								Mode	RESET
00h	TPL	table pointer high byte								W	xxxx xxxx
01h	TPH	table pointer low byte								W	xxxx xxxx
02h	IER	-	-	-	-	INT1	T1	T2	INT2	R/W	--00 0000
03h	T1L	Timer 1 low byte								W	xxxx xxxx
04h	T1H	Timer 1 high byte								W	xxxx xxxx
05h	T2L	Timer 2 low byte								W	xxxx xxxx
06h	T2H	Timer 2 high byte								W	xxxx xxxx
07h	SP	stack pointer								R/W	1111 1111
08h	DP	data RAM pointer								R/W	xxxx xxxx
09h	OP9	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C	R/W	1000 00xx
0ah	OPA	IDLE	PNWK	TCWK	-	-	-	-	-	R/W	0xx- ----
0bh	PP	RAM page pointer								R/W	0000 0000
0dh	PRTD	I/O port D								R/W	1111 1111
0eh	PWMC	1	PWM O/P driver			-	-	-	PWME	W	x000 xxxx
0eh	PWMC	0	7-bit DA and PWM output data							W	xxxx xxxx
0fh	LCDC	-	-	-	-	-	TYPE	BLANK	LCDE	W	xx1x xx10



Address	NAME	Field								Mode	RESET
11h	PRT11	I/O port 11								R/W	1111 1111
13h	VOC	-	-	-	-	-	PWM	DAC	OP	W	---- -000
14h	PRT14	I/O port 14								R/W	0000 0011
15h	PRT15	I/O port 15								R/W	0000 0011
16h	TPP	ROM table page pointer								W	0000 0000
17h	PRT17	I/O port 17								R/W	1111 1111

Mask Options:

NAME	VALUE	NOTE
MO_PORE	0	power-on reset disable
	1	power-on reset enable
MO_FOSCE	0	internal fast OSC
	1	external fast OSC, use it now
MO_FXTAL	0	R/C oscillator For fast clock
	1	Crystal oscillator For fast clock
MO_FRFCI_S[2:0]	000	RFRC I ~ = 500k
	001	RFRC I ~ = 1M
	010	RFRC I ~ = 1.5M
	011	RFRC I ~ = 2M
	100	RFRC I ~ = 2.5M
	101	RFRC I ~ = 3M
	110	RFRC I ~ = 3.5M
	111	RFRC I ~ = 4M
MO_SXTAL	0	R/C oscillator For 32k clock
	1	Crystal oscillator For 32k clock
MO_FCK/SCKN	00	slow clock only
	01	illegal
	10	dual clock
	11	fast clock only
MO_WDTE	0	WDT disable
	1	WDT enable
MO_CPP[7:0]	0	open-drain output
	1	push-pull output
MO_DPP[7:0]	0	open-drain output
	1	push-pull output
MO_11PP[7:0]	0	open-drain output
	1	push-pull output
MO_14PP[1:0]	0	open-drain output
	1	push-pull output
MO_15PP[1:0]	0	open-drain output
	1	push-pull output
MO_17PP[7:0]	0	open-drain output
	1	push-pull output
MO_LIO11[1:0]	0	IO pin
	1	LCD pin
MO_LIO14[7:0]	0	IO pin
	1	LCD pin
MO_LIO15[1:0]	0	IO pin
	1	LCD pin
MO_LIO17[7:0]	0	IO pin
	1	LCD pin
MO_LVRG	0	LCD regulator disable
	1	LCD regulator enable





## 15. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V <sub>DD</sub>	-0.5V ~ 8V	
Input Voltage	V <sub>IN</sub>	-0.5V ~ V <sub>DD</sub> +0.5V	
Output Voltage	V <sub>O</sub>	-0.5V ~ V <sub>DD</sub> +0.5V	
Operating Temperature	T <sub>OP</sub>	0°C ~ 70°C	
Storage Temperature	T <sub>ST</sub>	-50°C ~ 100°C	

## 16. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V <sub>DD</sub>	2.4V ~ 5.5V	
Input Voltage	V <sub>IH</sub>	0.9 V <sub>DD</sub> ~ V <sub>DD</sub>	
	V <sub>IL</sub>	0.0V ~ 0.1 V <sub>DD</sub>	
Operating Frequency	F <sub>MAX</sub>	8MHz	V <sub>DD</sub> =5.0V
		4MHz	V <sub>DD</sub> =2.4V
Operating Temperature	T <sub>OP</sub>	0°C ~ 70°C	
Storage Temperature	T <sub>ST</sub>	-50°C ~ 100°C	

## 17. AC/DC Characteristics

Test Condition: Temp. = 25°C, V<sub>DD</sub> = 3V±10%, GND=0V

PARAMETER	Symbol	MIN	TYP	MAX	UNIT	CONDITION
Normal mode current	I <sub>FAST</sub>		0.75	1	mA	2M ext. R/C
Slow mode current	I <sub>SLOW</sub>		10	20	μA	32768 Hz, LCD Disabled
Idle mode current	I <sub>IDLE</sub>		6	10	μA	32768 Hz, LCD Disabled
Additional current if LCD ON	I <sub>LCD</sub>		12	20	μA	LCD Enabled, regulator on
Sleep mode current	I <sub>SLEEP</sub>			1	μA	
Input high voltage	V <sub>IH</sub>	0.8			V <sub>DD</sub>	Input pins
Input Low Voltage	V <sub>IL</sub>			0.2	V <sub>DD</sub>	Input pins
Input Hysteresis Width	V <sub>HYS</sub>		1/3		V <sub>DD</sub>	I/O, RSTP_N, Threshold=2/3V <sub>DD</sub> (input from low to high) Threshold=1/3V <sub>DD</sub> (input from high to low)
Output source current	I <sub>OH</sub>	50			μA	Output drive high*1, V <sub>OH</sub> =2.0V
Output sink current	I <sub>OL1</sub>	1.0			mA	Output drive low, V <sub>OL</sub> = 0.4V
Input Low Current	I <sub>IL2</sub>		100		μA	I/O, V <sub>IL</sub> = GND, pull high Internally
Input Low Current	I <sub>IL1</sub>		20		μA	RSTP_N, V <sub>IL</sub> = GND, pull high Internally
PWM Output Current	I <sub>PWM</sub>	10	14		mA	PWM *2 With 32Ω Loading
		6	8		mA	With 64Ω Loading
		4	5		mA	With 100Ω Loading

Note:

March 13, 2003

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V1.0E

This specification is subject to change without notice. Please contact sales person for the latest version before use.



1. Source current spec. applies to Push-Pull I/O port only
2. This spec. is based on one driver only. There are totally five drivers, so user must multiply the number of driver actually used to get the total amount of current. ( $I_{PWM} \times N$ ;  $N=0,1,2,3,4,5$ )

## 18. Application Circuit

