



A. HE83138 Introduction

HE83138 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. This IC provides 512 pixels LCD display and built-in OP comparator can be used with light, voice, temperature and humidity sensor or used to detect the battery low. The 7-bit current-type D/A converter and PWM drive output provide the complete speech output mechanism.

The 48K bytes ROM size can be used to store 15 seconds speech data. It can be applicable to the LCD game, medium level educational toy, lower second voice recording system or used with external command mode SRAM or Flash RAM for higher second voice recording etc.

The instruction sets of HE80000 series are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The performance of HE83750S is enough for most of battery operation system.

B. HE83138 Features

- Operation Voltage: 2.4V ~ 5.5V
- System Clock 4MHz ~ 8MHz
- Clock Source: Internal/External Fast clock, Internal/External slow clock
- Dual Clock System : Normal (Fast) clock 32.768KHz ~ 8MHz
Slow clock 32.768 KHz
- Operation Mode : DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- Internal ROM: 48K Bytes.
- Internal RAM: 1K Bytes.
- Watch dog timer.
- 16 Bi-directional I/O ports.
- 512 pixels LCD driver with A, B type choice
- LCD Bias : 1/5
- LCD Charge Pump: 1 or 1.5 times of VDD
- One 7-bits current-type DAC output.
- One built-in OP comparator.
- PWM device.
- Built-in DTMF Generator.
- Speech recognition function
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timers.
- Instruction set : 32 instructions, 4 addressing mode. 10-bit DATA POINTER for RAM and 16-bit TABLE POINTER for ROM.

C. Pin Description

Pin #	Pin name	I/O	Function	Description
78 77	FXI, FXO	B, O	External fast clock input/output pins are used to connect crystal or RC to generate the 32.768KHz ~ 8MHz system clock.	Mask Option setting: MO_FCK/SCKN= 00 : Slow Clock only 01 : Illegal 10 : Dual Clock 11 : Fast Clock only MO_FOSCE= 0 : Internal fast clock 1 : External fast clock MO_FXTAL= 0 : R,C OSC. for Fast Clock 1 : Crystal OSC. for Fast Clock MO_SXTAL= 0 : R,C OSC. for 32.768K Clock 1 : Crystal OSC. for 32.768K Clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
81 80	SXI, SXO	I, O	External slow clock input/output pins used to connect the 32.768KHz crystal to generate slow clock for system operation (slow mode), LCD display or timer 1 clock source.	
76	RSTP_N	I	System reset signal	Active low and level trigger reset signal. User can also set the mask option MO_PORE=1 to enable the build-in Power-on reset circuit besides using the reset pin. Watch Dog Timer can also be enabled/disabled by the mask option, MO_WDTE = 0 : Disable Watch Dog Timer = 1 : Enable Watch Dog Timer
79	TSTP_P	I	IC Test Pin	Please bond this pin to ground by a 0 ohm resistor to let it accessible when it's necessary for some testing.
91,92, 93,1	NC		No Connection Pin	
83:90	PRTD[7:0]	B	Bi-directional I/O port D. PRTD [7:2] also used as wake-up pin, and PRTD [7:6] also used as external interrupt pin.	Mask options setting: MO_DPP [7:0] = 1 : Push-pull output. = 0 : Open-drain output. Output must be "1" before reading whenever uses them as input (Non tri-state structure).
12..19	PRT17[7:0]	B	Bi-directional I/O port 17	Mask options setting: MO_17PP [7:0] = 1 : Push-pull output. = 0 : Open-drain output. Output must be "1" before reading whenever uses them as input (Non tri-state structure).
11..4 52..59	COM[15:0]	O	LCD COM Output	LCD common/segment driving pins.
20..51	SEG[31:0]	O	LCD SEG Output	LCD Data filled from 80H; please refer the LCD RAM map.
61	LC2	B	Charge Pump Switch 1	When LV3=VDD, the charge pump for LCD is turn off. The capacitor between LC1 and LC2 shall be removed to reduce power consumption.
60	LC1	B	Charge Pump Switch 2	
63	LV3	B	Charge Pump V3	Refer to application circuit.
62	LV1	B	Charge Pump V1	

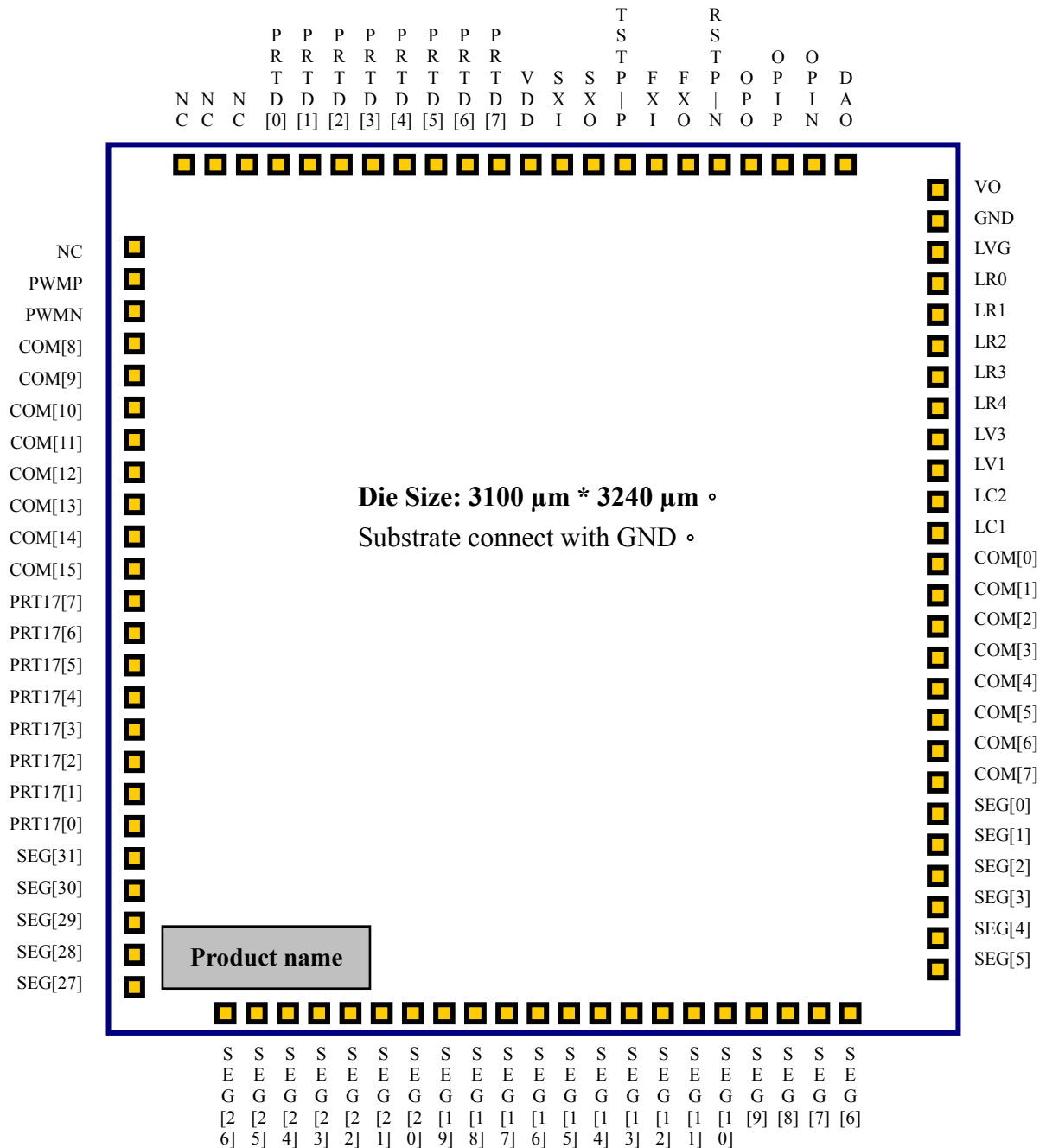


Pin #	Pin name	I/O	Function	Description
64..68	LR[4:0]	B	LCD Resister level 4 ~ 0	Refer to application circuit.
69	LVG	I	LCD Virtual Ground	Refer to application circuit.
2	PWMP	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2(PWM=1) of VOC register and bit0 of PWMC register to turn on PWM
3	PWMN	O	The PWM positive output can drive speaker or buzzer directly.	
71	VO	O	Voice output.	Set the bit0(OP=0) and bit1(DA=1) of VOC register to turn on VO
72	DAO	O	DAC Output	Set the bit0(OP=1) and bit1(DA=1) of VOC register to turn on DAO
73	OPIN	I	OPAMP negative input pin.	Built-in OP comparator.
74	OPIP	I	OPAMP positive input pin.	Enable DAO to work with OP. Refer to application note for detailed operation.
75	OPO	O	OPAMP output pin.	
82	VDD	P	Positive Power Input	Adding a 0.1 μ F capacitor as by-pass capacitor between VDD and GND.
70	GND	P	Power Ground Input	

D. LCD RAM MAP

Page 0	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]
COM0	80H	90H	A0H	B0H
COM1	81H	91H	A1H	B1H
COM2	82H	92H	A2H	B2H
:	:	:	:	:
:	:	:	:	:
COM13	8DH	9DH	ADH	BDH
COM14	8EH	9EH	AEH	BEH
COM15	8FH	9FH	AFH	BFH

E. Pin Diagram





F. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	NC	X= -1475.80	Y= 1246.95	48	SEG[3]	X= 1474.30	Y= -1236.15
2	PWMP	X= -1475.80	Y= 1107.20	49	SEG[2]	X= 1474.30	Y= -1120.65
3	PWMN	X= -1475.80	Y= 943.85	50	SEG[1]	X= 1474.30	Y= -1005.15
4	COM[8]	X= -1475.80	Y= 804.75	51	SEG[0]	X= 1474.30	Y= -889.65
5	COM[9]	X= -1475.80	Y= 689.25	52	COM[7]	X= 1474.30	Y= -774.15
6	COM[10]	X= -1475.80	Y= 573.75	53	COM[6]	X= 1474.30	Y= -658.65
7	COM[11]	X= -1475.80	Y= 458.25	54	COM[5]	X= 1474.30	Y= -543.15
8	COM[12]	X= -1475.80	Y= 342.75	55	COM[4]	X= 1474.30	Y= -427.65
9	COM[13]	X= -1475.80	Y= 227.25	56	COM[3]	X= 1474.30	Y= -312.15
10	COM[14]	X= -1475.80	Y= 111.75	57	COM[2]	X= 1474.30	Y= -196.65
11	COM[15]	X= -1475.80	Y= -3.75	58	COM[1]	X= 1474.30	Y= -81.15
12	PRT17[7]	X= -1475.80	Y= -119.25	59	COM[0]	X= 1474.30	Y= 34.35
13	PRT17[6]	X= -1475.80	Y= -234.75	60	LC1	X= 1474.30	Y= 149.85
14	PRT17[5]	X= -1475.80	Y= -350.25	61	LC2	X= 1474.30	Y= 265.35
15	PRT17[4]	X= -1475.80	Y= -465.75	62	LV1	X= 1474.30	Y= 380.85
16	PRT17[3]	X= -1475.80	Y= -581.25	63	LV3	X= 1474.30	Y= 496.35
17	PRT17[2]	X= -1475.80	Y= -696.75	64	LR4	X= 1474.30	Y= 611.85
18	PRT17[1]	X= -1475.80	Y= -812.25	65	LR3	X= 1474.30	Y= 727.35
19	PRT17[0]	X= -1475.80	Y= -927.75	66	LR2	X= 1474.30	Y= 842.85
20	SEG[31]	X= -1475.80	Y= -1043.25	67	LR1	X= 1474.30	Y= 958.35
21	SEG[30]	X= -1475.80	Y= -1158.75	68	LR0	X= 1474.30	Y= 1073.85
22	SEG[29]	X= -1475.80	Y= -1274.25	69	LVG	X= 1474.30	Y= 1189.35
23	SEG[28]	X= -1475.80	Y= -1389.75	70	GND	X= 1474.30	Y= 1304.85
24	SEG[27]	X= -1475.80	Y= -1505.25	71	VO	X= 1474.30	Y= 1438.50
25	SEG[26]	X= -1155.05	Y= -1541.50	72	DAO	X= 1124.45	Y= 1539.10
26	SEG[25]	X= -1039.55	Y= -1541.50	73	OPIN	X= 990.80	Y= 1539.10
27	SEG[24]	X= -924.05	Y= -1541.50	74	OPIP	X= 875.30	Y= 1539.10
28	SEG[23]	X= -808.55	Y= -1541.50	75	OPO	X= 759.80	Y= 1539.10
29	SEG[22]	X= -693.05	Y= -1541.50	76	RSTP_N	X= 644.30	Y= 1539.10
30	SEG[21]	X= -577.55	Y= -1541.50	77	FXO	X= 528.80	Y= 1539.10
31	SEG[20]	X= -462.05	Y= -1541.50	78	FXI	X= 413.30	Y= 1539.10
32	SEG[19]	X= -346.55	Y= -1541.50	79	TSTP_P	X= 297.80	Y= 1539.10
33	SEG[18]	X= -231.05	Y= -1541.50	80	SXO	X= 182.30	Y= 1539.10
34	SEG[17]	X= -115.55	Y= -1541.50	81	SXI	X= 66.80	Y= 1539.10
35	SEG[16]	X= -0.05	Y= -1541.50	82	VDD	X= -48.70	Y= 1539.10
36	SEG[15]	X= 115.45	Y= -1541.50	83	PRTD[7]	X= -164.20	Y= 1539.10
37	SEG[14]	X= 230.95	Y= -1541.50	84	PRTD[6]	X= -279.70	Y= 1539.10
38	SEG[13]	X= 346.45	Y= -1541.50	85	PRTD[5]	X= -395.20	Y= 1539.10
39	SEG[12]	X= 461.95	Y= -1541.50	86	PRTD[4]	X= -510.70	Y= 1539.10
40	SEG[11]	X= 577.45	Y= -1541.50	87	PRTD[3]	X= -626.20	Y= 1539.10
41	SEG[10]	X= 692.95	Y= -1541.50	88	PRTD[2]	X= -741.70	Y= 1539.10
42	SEG[9]	X= 808.45	Y= -1541.50	89	PRTD[1]	X= -857.20	Y= 1539.10
43	SEG[8]	X= 923.95	Y= -1541.50	90	PRTD[0]	X= -972.70	Y= 1539.10

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
44	SEG[7]	X= 1039.45	Y= -1541.50	91	NC	X= -1088.20	Y= 1539.10
45	SEG[6]	X= 1154.95	Y= -1541.50	92	NC	X= -1203.70	Y= 1539.10
46	SEG[5]	X= 1474.30	Y= -1467.15	93	NC	X= -1319.20	Y= 1539.10
47	SEG[4]	X= 1474.30	Y= -1351.65				

G. DC/AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ $V_{dd}+0.5V$	
Output Voltage	V_o	-0.5V ~ $V_{dd}+0.5V$	
Operating Temperature	T_{op}	0°C ~ 70°C	
Storage Temperature	T_{st}	-50°C ~ 100°C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1 V_{dd}	
Operating Frequency	Fmax	8MHz	$V_{dd}=5.0V$
		4MHz	$V_{dd}=2.4V$
Operating Temperature	T_{op}	0°C ~ 70°C	
Storage Temperature	T_{st}	-50°C ~ 100°C	

Testing condition : TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		10	20	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		6	10	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=300Kohm Voltage-doubler OFF		12	20	μA
			LCD Enable, LCD option=30Kohm, Voltage-doubler ON		100	120	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPWM}	PWM Output Drive Current	PWMP, PWMN ^{*2}	V _{DD} =3V; V _{oh} =2V	12	15		mA
I_{oLPWM}	PWM Output Sink Current	PWMP, PWMN ^{*2}	V _{DD} =3V; V _{oL} =1V	33	40		mA
I_{oVO}	DAC Output Current	VO, DAO	V _{DD} =3V; VO=0~2V, Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V _{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V _{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V _{DD} (input from low to high) Threshold=1/3V _{DD} (input from high to low)		1/3 V _{DD}		V
I_{oH}	Output Drive Current	I/O pull-high ^{*1}	V _{oL} =2.0V	50			μA
I_{oL 1}	Output Sink Current	I/O pull-low ^{*1}	V _{oL} =0.4V	1.0			mA
I_{iL 1}	Input Low Current	RSTP_N	V _{iL} =GND, pull high Internally		20		μA
I_{iL 2}	Input Low Current	I/O	V _{iL} =GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only

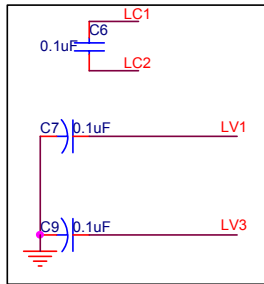
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current.

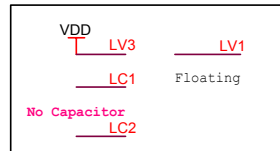
(I_{oHPWM} 、 I_{oLPWM} * N; N=0,1,2,3,4,5)

H. Application Circuit

Twice Charge Pump is selected
 LCD Max. Voltage=LV3=3/2*VDD

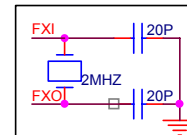


Twice Charge Pump is selected
 LCD Max. Voltage=LV3=VDD

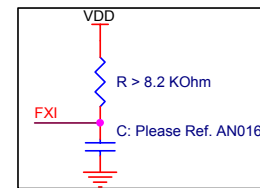


No External Parts is necessary if user adopt Internal Fast RC Clock

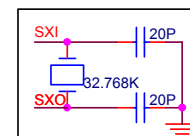
External Fast Clock:
 Crystal osc.



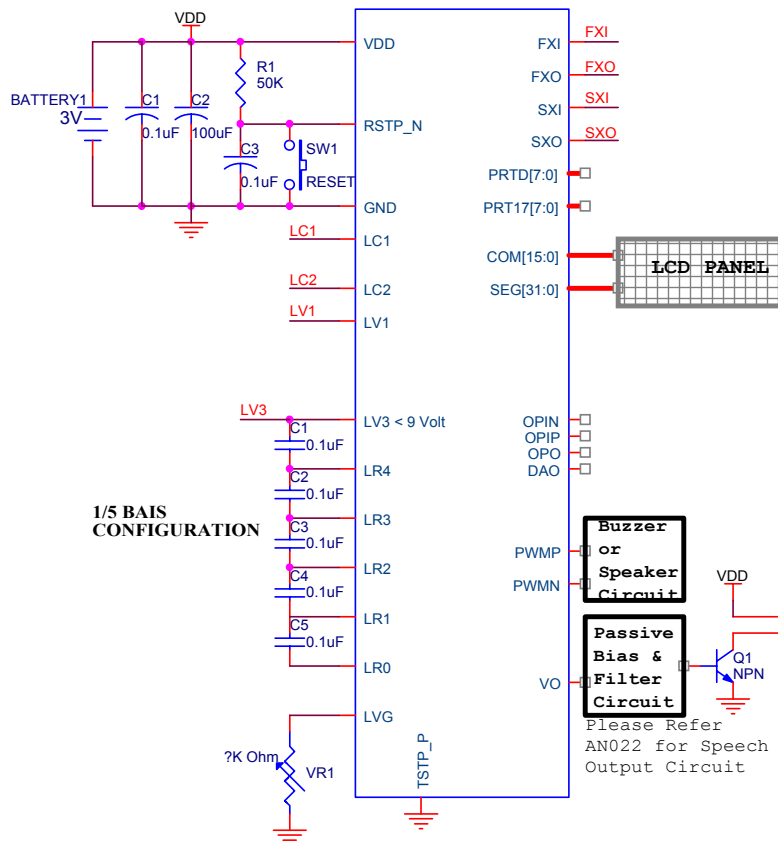
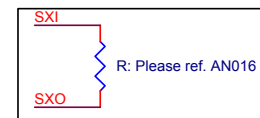
External Fast Clock:
 RC osc.



External Slow Clock:
 Crystal osc.



External Slow Clock:
 RC osc.

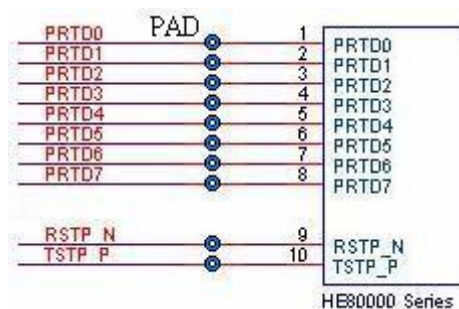


I. Important Note

- Please always take in mind that ICE is different from IC which is your target body. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that your target IC didn't have these resources, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resources that don't exist in your target IC. Please check the following table and refer to the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R.	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
☉	☉	☉	48KB	—	16-bit	☉	1KB	2-bit	8-bit	16	—	☉	T1,T2
VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
☉	☉	☉	☉	512	16*32	1/5	—	1,3/2	—	4:0	☉	Ext.	I

- LCD driving circuit must be turn off before IC goes into sleep mode.
- Please bonds the TSTP_P, RSTP_N and PRTD [7:0] with test points on PCB (can be soldered and probed) as you can, then some testing can be performed on PCB if necessary. The TSTP_P is suggested to connect to ground by a 0 ohm resistor. The following figure is an example (Testing point with through hole).



4.

J. Updated Record

Version	Date	Section	Original Content	New Content