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# 1. General Description

HE83003 is a member of 8-bit micro-controller series developed by King Billion. It's a power speech controller. The built-in OP comparator can be used with (light, voice, temperature, humility) sensor and used as battery low detection. And the 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 36K ROM size can be used in the storage of speech (20 seconds at 3Kbytes per second)

The instruction set of HE83003 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

# 2. Features

- Operation Voltage: 2.4V – 5.5V
- System Clock: DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM: 36K Bytes (36K Program ROM)
- Internal RAM: 128 Bytes.
- Dual Clock System: Normal (Fast) clock: 32.768 KHz ~ 8MHz
  Slow clock: 32.768 KHz
- Operation modes: Dual, Fast, Slow, Idle, Sleep modes.
- With WDT (Watch Dog Timer) to prevent deadlock condition.
- 16 bit Bi-directional I/O port. Mask Option can select Push-Pull or Open Drain output mode for each I/O pin.
- One built-in OP comparator.
- One 7-bit current-type DAC output (VO).
- PWM device.
- Two external interrupts and two internal timer interrupts.
- Two 16-bit timers. (Clock Source reference by Fast Clock)
- Instruction set: 32 instructions, 4 addressing modes.

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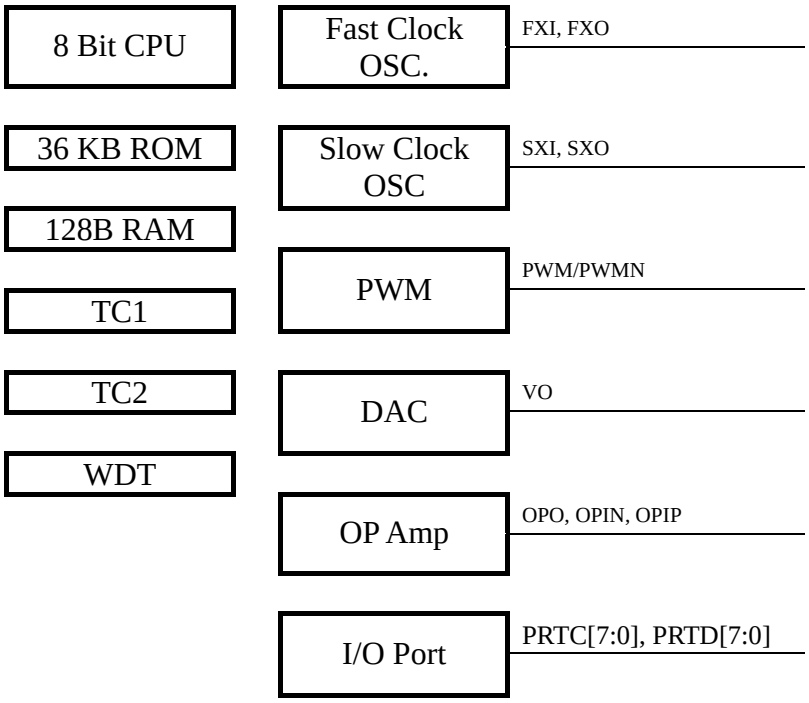
# 3. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resources that real IC don't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resources that don't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.




# 4. Pin Description

| Pin Name | I/O | Description |
|---|---|---|
| **FXI, FXO** | B, O | External fast clock pin. Two types of oscillator can be selected by MO_FXTAL ('0' for RC type and '1' for crystal type). For RC type oscillator, one resistor needs to be connected between FXI and GND. For crystal oscillator, one crystal needs to be placed between FXI and FXO. Please refer to application circuit for details. |
| **SXI, SXO** | I, O | External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose '0' for RC type and '1' for crystal oscillator. |
| **RSTP_N** | I | System reset input pin. Level trigger, active low on this pin will put the chip in reset state. |
| **TSTP_P** | I | Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND. |
| **PRTC[7:0]** | B | 8-bit bi-directional I/O port C. The output type of I/O pad can also be selected by mask option MO_CPP[7: 0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin. |
| **PRTD[7:0]** | B | 8-bit bi-directional I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7: 0] ('1' for push-pull and '0' for open-drain).<br>As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin.<br>PRTD[7..2] can be used as wake-up pins.<br>PRTD[7..6] can be as external interrupt sources. |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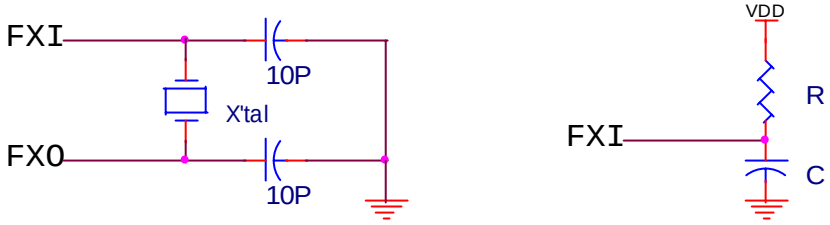
| Pin Name | I/O | Description |
|---|---|---|
| | | PRTD[1..0] general I/O bi-direction pins. |
| **PWMP/PWMN** | O | The PWM output can drive speaker or buzzer directly. Using PWMP & PWMN to drive output device. |
| **VO** | O | Current DAC Output. |
| **OPIN** | I | Inverting input of OP Amp. |
| **OPIP** | I | Non-inverting input of OP Amp. |
| **OPO** | O | Output of OP Amp. |
| **VDD** | P | Positive power Input. A 0.1 µF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect. |
| **GND** | P | Power ground Input. |

I: Input, O: Output, B: Bidirectional, P: Power.

# 5. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. System designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

**FXI (Bi-direction), FXO (Output)**




| Mask Option | Description |
|---|---|
| MO_FXTAL | 0: RC Oscillator.<br>1: Crystal Oscillator. |
| MO_FCK | 0: Fast clock disable<br>1: Fast clock enable |

**SXI (Bi-direction), SXO (Output)**

Two types of oscillator, crystal and RC, can be used as slow clock selectable by mask option MO_SXTAL. If used time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to save cost.

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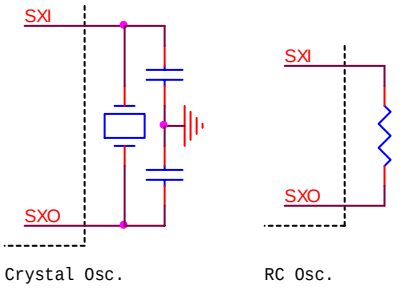


| Mask Option | Description |
|---|---|
| MO_SXTAL | 0: RC Oscillator.<br>1: Crystal Oscillator. |
| MO_SCKN | 0: Slow clock enable<br>1: Slow clock disable |

With two clock sources available, the system can switch among operation modes of Normal, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

| OP1 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | DRDY | STOP | SLOW | INTE | T2E | T1E | Z | C |
| **Mode** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Reset** | 1 | 0 | 0 | 0 | 0 | 0 | - | - |

| OP2 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | IDLE | PNWK | TCWK | - | - | | | |
| **Mode** | R/W | R | R | - | - | - | - | - |
| **Reset** | 0 | - | - | - | - | - | - | - |

# 6. General Purpose I/O

The PRTC[7..0] and PRTD[7..0] are dedicated general purpose I/O port. All the I/O ports are bi-directional and non-tristate output structure. The output has weak sourcing (50μA) and stronger sinking (1mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. The hysteresis level of Schmidt trigger is 1/3*VDD.

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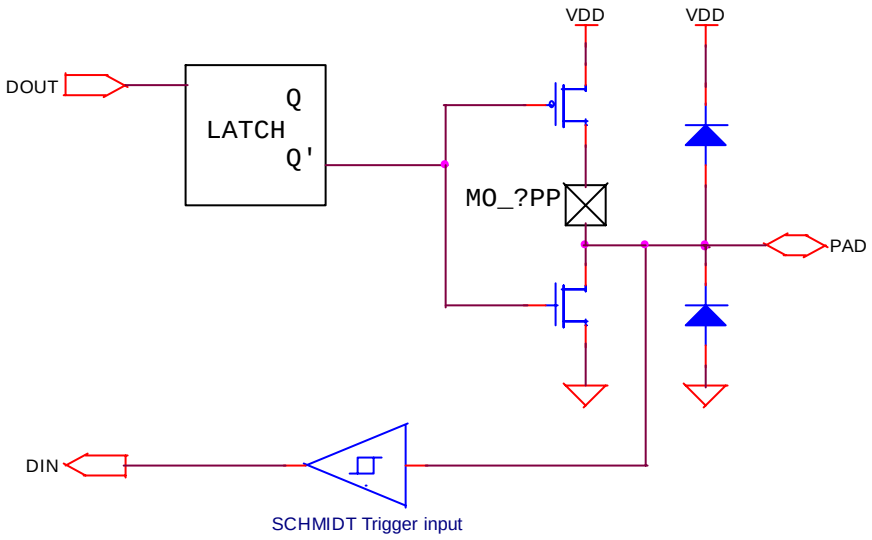


# 7. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.

The Timer1 related control registers are list as below:

| Register | Address | Field | Bit position | Mode | Description |
|---|---|---|---|---|---|
| **IER** | 0x02 | TC1_IER | 2 | R/W | 0: TC1 interrupt is disabled. (default)<br>1: TC1 interrupt is enabled. |
| **T1L** | 0x03 | T1L[7:0] | 7~0 | W | Low byte of TC1 pre-load value |
| **T1H** | 0x04 | T1H[7:0] | 7~0 | W | High byte of TC1 pre-load value |
| **OP1** | 0x09 | TC1E | 2 | R/W | 0: TC1 is disabled. (default)<br>1: TC1 is enabled. |

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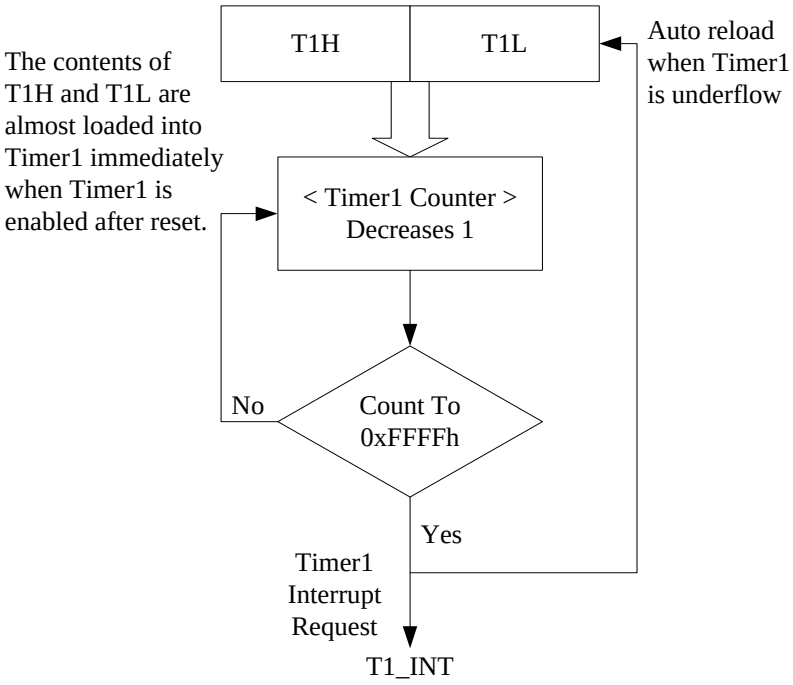


# 8. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.

The Timer2 related control registers are list as below:

| Register | Address | Field | Bit Position | Mode | Description |
|---|---|---|---|---|---|
| **IER** | 0x02 | TC2_IER | 1 | R/W | 0: TC2 interrupt is disabled. (default)<br>1: TC2 interrupt is enabled. |
| **T2L** | 0x05 | T2L[7:0] | 7~0 | W | Low byte of TC2 pre-load value |
| **T2H** | 0x06 | T2H[7:0] | 7~0 | W | High byte of TC2 pre-load value |
| **OP1** | 0x09 | TC2E | 3 | R/W | 0: TC2 is disabled. (default)<br>1: TC2 is enabled. |

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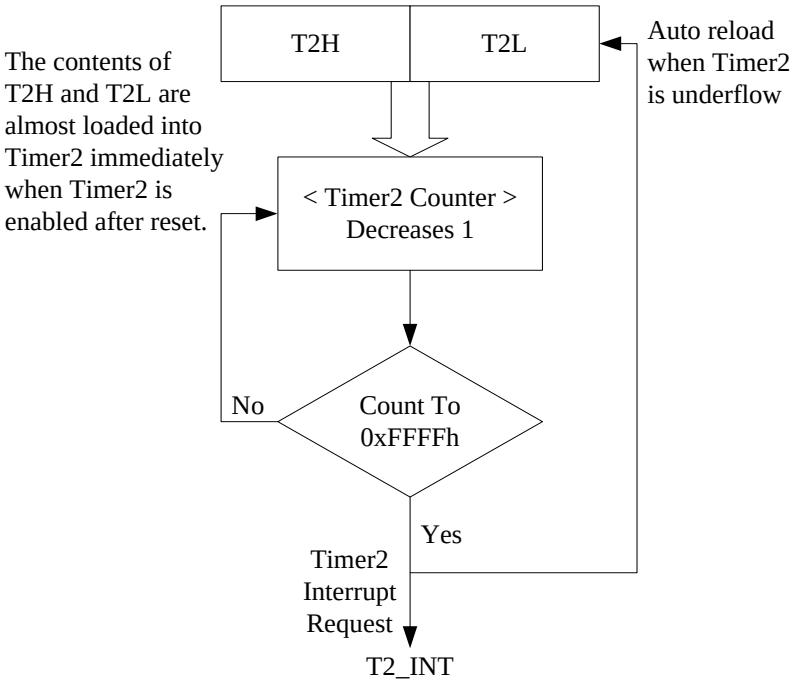


# 9. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution. WDT needs to be enabled in Mask Option.

| MO_WDTE | Function |
|---|---|
| 0 | WDT disable |
| 1 | WDT enable |

To use WDT function, "CLRWDT" instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

WDT is the enabling signal generated by calculating 32768-clock overflow. Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source. WDT function can be generated in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

# 10. PWM & DAC

The current DAC output pin is VO and its primary function is intended for speech generation, but the DAC output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter for applications such as speech recording, speech recognition or sensor interfaces.

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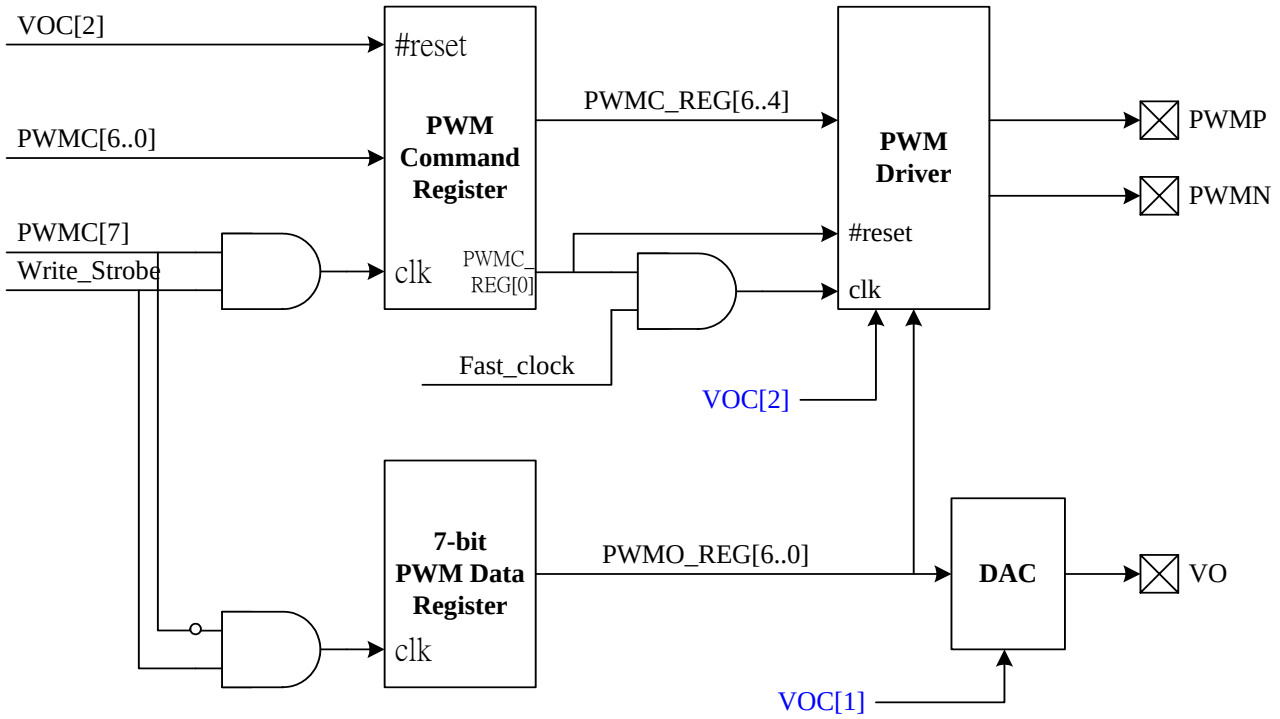
## 7-bit Voice Output Architecture




The 7-bit voice output is controlled by PWMC and VOC register, and the PWMC is a command/data register which is determined by PWMC[7] bit. The voice output control (VOC) register is used to control the PWM and DAC enable/disable. These two functions can be enabled simultaneously.

| VOC | address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Field | 0x13 | - | - | - | - | - | PWM | DAC | Reserved |
| Reset | | - | - | - | - | - | 0 | 0 | 0 |

| Bit | Name | Value | Function description |
|---|---|---|---|
| VOC[2] | PWM | 1 | PWM Module Enable |
| | | 0 | PWM Module Disable |
| VOC[1] | DAC | 1 | Digital-to-Analog Converter Enable |
| | | 0 | Digital-to-Analog Converter Disable |

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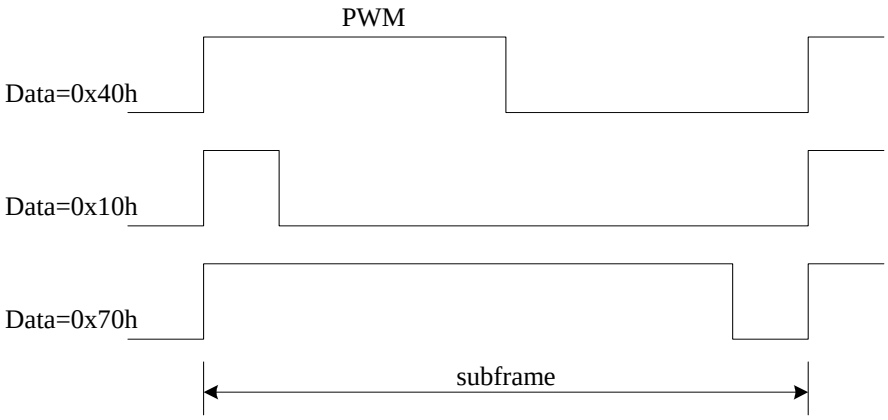
## VOC

| VOC[2] | VOC[1] | Output Function |
|---|---|---|
| 0 | 0 | All Disabled |
| 0 | 1 | VO |
| 1 | 0 | PWM |
| 1 | 1 | PWM+VO |

| PWMC register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| DAC & PWM Data | **0** | DAC and PWM output value | | | | | | |
| Control | **1** | PWM O/P driver | | | **Reserved** | | | PWME |

In the PWMC register, the PWMC[7] bit determines the written PWMC[6..0] value is PWM/DAC data or commands. If the PWMC[1] is '0', the PWMC[6..0] is stored into the data register, otherwise PWMC[6..0] is stored into command register shown on the above diagram. The command register controls the PWM output driver current and its enable/disable. If user want to enable the PWM function, both VOC[2] and PWME bits shall be set to '1'.

The fast clock is used to provide as PWM driver time base, and user shall set the PWMC[7]='1' and VOC[2]='1' to enable the PWM output. When the system enters into sleep or idle mode, it will automatically turn off the voice device by clearing VOC[2:0] to "000". In order to activate voice output again when the system returns and enters into normal mode, the related bits of VOC register need to be set again.




When the DAC is used as sound generator, the bias & filter circuit is used for bias voltage setting and waveform filter regulation and the DAC is output to the VO (Voice Output) pin and please see application notes for detailed calculation example and application. The driving capability of DAC is shown below.

| | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VO/DAO | $V_{DD}$=3V;VO=0~2V;Data=7Fh | 2.5 | 3 | | mA |

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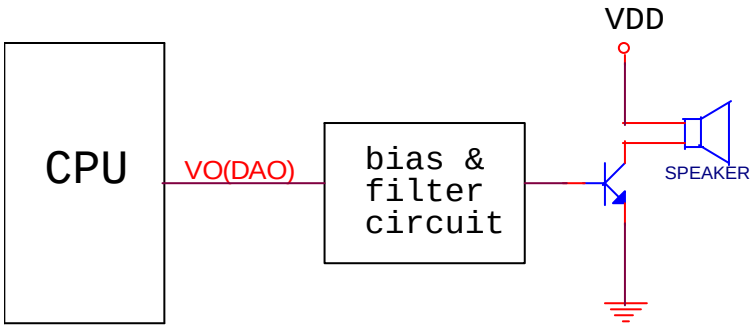


The PWM output volume can be adjusted by command register PWMC[6..4]. The PWMC[6] and PWMC[5] control 2 time driver, while PWMC [4] controls 1 time driver, thus it has maximum 5 levels of driver output. The sound volume of PWM output can be controlled by these PWMC[6..4] bits. Please note that this adjustment only apply to PWM. When the system enters into sleep mode or idle mode, it will automatically disable all voice outputs by clearing VOC[6..0] to ”0000000”. To activate voice output again when returning to normal mode, the VOC register needs to be set again.

| PWMC[6..4] | Number of PWM Output Driver |
|---|---|
| 000 | off |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 2 |
| 101 | 3 |
| 110 | 4 |
| 111 | 5 |

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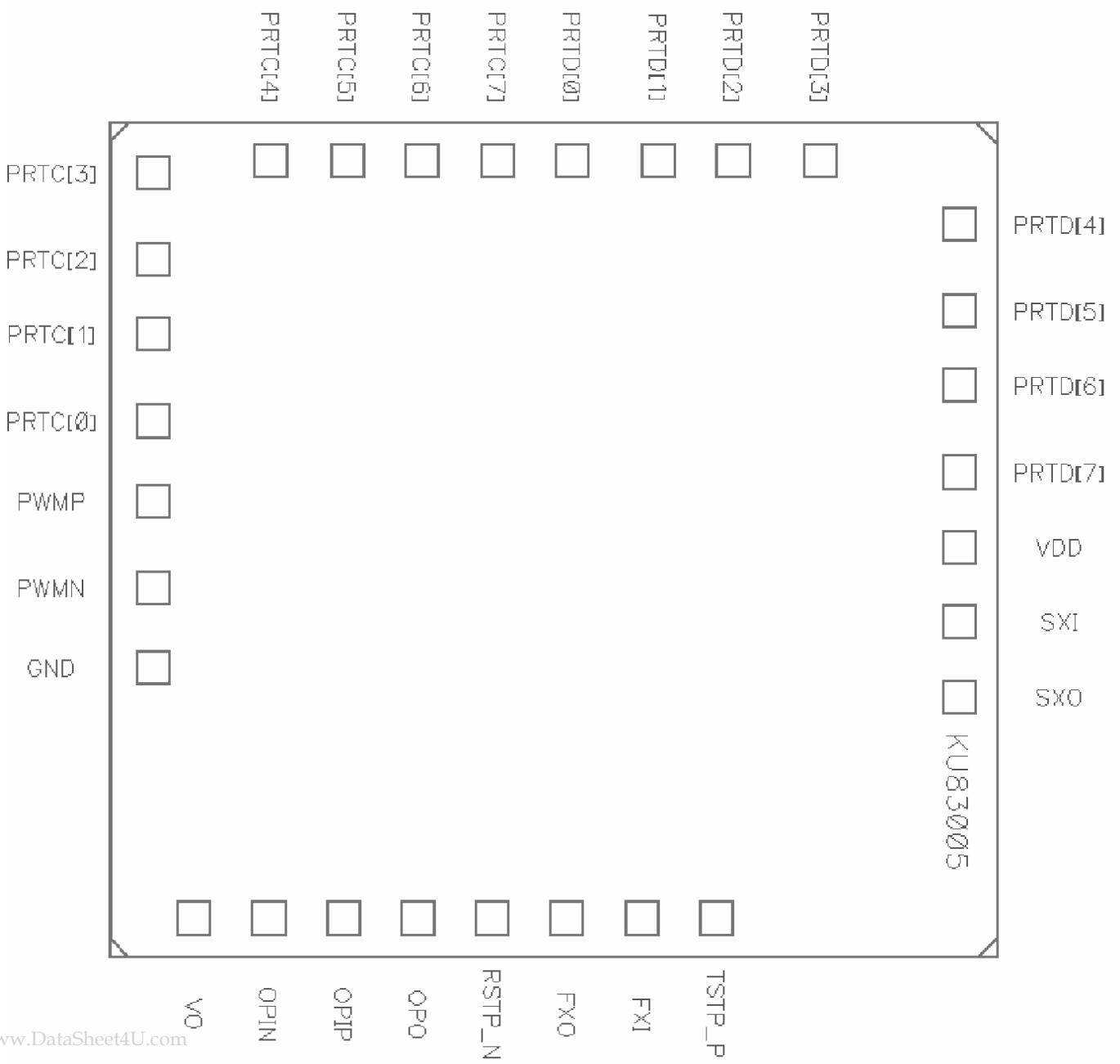
# 11. Pad Diagram & Location

***Which version of HE83003 delivered to customer is decided by KingBillion, user shall make sure the delivered version before PCB is manufactured. The locations of chips logo are different from each other.***

**A1 Version:Die Size= 2050 µm * 2180 µm**

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| A1 Version HE83003 | | | |
|---|---|---|---|
| **PIN Number** | **PIN Name** | **X Coordinate** | **Y Coordinate** |
| 1 | PRTD[3] | X= -923.95 | Y= 646.60 |
| 2 | PRTD[2] | X= -923.95 | Y= 433.80 |
| 3 | PRTD[1] | X= -923.95 | Y= 250.60 |
| 4 | PRTD[0] | X= -923.95 | Y= 37.80 |
| 5 | PRTC[7] | X= -923.95 | Y= -145.40 |
| 6 | PRTC[6] | X= -923.95 | Y= -331.80 |
| 7 | PRTC[5] | X= -923.95 | Y= -515.00 |
| 8 | PRTC[4] | X= -923.95 | Y= -701.40 |
| 9 | PRTC[3] | X= -895.15 | Y= -992.85 |
| 10 | PRTC[2] | X= -682.35 | Y= -992.85 |
| 11 | PRTC[1] | X= -499.15 | Y= -992.85 |
| 12 | PRTC[0] | X= -286.35 | Y= -992.85 |
| 13 | PWMP | X= -89.35 | Y= -992.85 |
| 14 | PWMN | X= 122.25 | Y= -992.85 |
| 15 | GND | X= 319.05 | Y= -992.85 |
| 16 | VO | X= 934.70 | Y= -890.70 |
| 17 | OPIN | X= 934.70 | Y= -707.90 |
| 18 | OPIP | X= 934.70 | Y= -524.40 |
| 19 | OPO | X= 934.70 | Y= -341.60 |
| 20 | RSTP_N | X= 934.70 | Y= -158.10 |
| 21 | FXO | X= 934.70 | Y= 24.70 |
| 22 | FXI | X= 934.70 | Y= 208.85 |
| 23 | TSTP_P | X= 934.70 | Y= 392.65 |
| 24 | SXO | X= 391.15 | Y= 990.00 |
| 25 | SXI | X= 206.35 | Y= 990.00 |
| 26 | VDD | X= 22.85 | Y= 990.00 |
| 27 | PRTD[7] | X= -160.15 | Y= 990.00 |
| 28 | PRTD[6] | X= -373.00 | Y= 990.00 |
| 29 | PRTD[5] | X= -556.20 | Y= 990.00 |
| 30 | PRTD[4] | X= -769.00 | Y= 990.00 |

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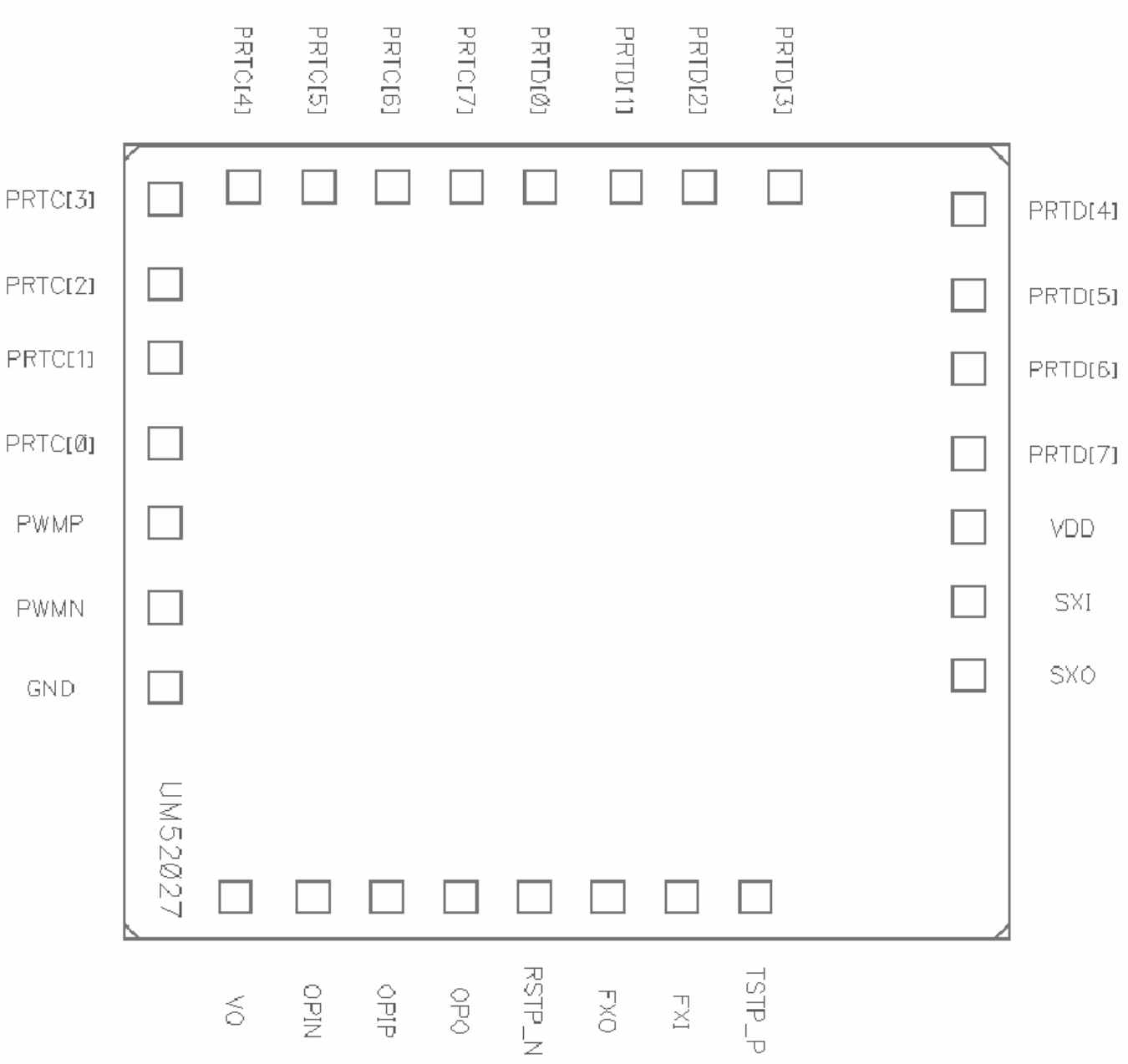
***A2 Version:Die Size= 1980 µm * 2210 µm***

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| A2 Version HE83003 | | | |
|---|---|---|---|
| **PIN Number** | **PIN Name** | **X Coordinate** | **Y Coordinate** |
| 1 | PRTD[3] | X= -885.80 | Y= 543.30 |
| 2 | PRTD[2] | X= -885.80 | Y= 330.50 |
| 3 | PRTD[1] | X= -885.80 | Y= 147.30 |
| 4 | PRTD[0] | X= -885.80 | Y= -65.50 |
| 5 | PRTC[7] | X= -885.80 | Y= -248.70 |
| 6 | PRTC[6] | X= -885.80 | Y= -435.10 |
| 7 | PRTC[5] | X= -885.80 | Y= -618.30 |
| 8 | PRTC[4] | X= -885.80 | Y= -804.70 |
| 9 | PRTC[3] | X= -855.75 | Y= -1002.00 |
| 10 | PRTC[2] | X= -642.95 | Y= -1002.00 |
| 11 | PRTC[1] | X= -459.75 | Y= -1002.00 |
| 12 | PRTC[0] | X= -246.95 | Y= -1002.00 |
| 13 | PWMP | X= -48.75 | Y= -1002.00 |
| 14 | PWMN | X= 162.85 | Y= -1002.00 |
| 15 | GND | X= 361.45 | Y= -1002.00 |
| 16 | VO | X= 884.20 | Y= -826.30 |
| 17 | OPIN | X= 884.20 | Y= -632.30 |
| 18 | OPIP | X= 884.20 | Y= -448.20 |
| 19 | OPO | X= 884.20 | Y= -264.20 |
| 20 | RSTP_N | X= 884.20 | Y= -80.40 |
| 21 | FXO | X= 884.20 | Y= 103.00 |
| 22 | FXI | X= 884.20 | Y= 287.45 |
| 23 | TSTP_P | X= 884.20 | Y= 471.25 |
| 24 | SXO | X= 329.75 | Y= 1002.00 |
| 25 | SXI | X= 147.50 | Y= 1002.00 |
| 26 | VDD | X= -36.60 | Y= 1002.00 |
| 27 | PRTD[7] | X= -220.20 | Y= 1002.00 |
| 28 | PRTD[6] | X= -433.00 | Y= 1002.00 |
| 29 | PRTD[5] | X= -616.20 | Y= 1002.00 |
| 30 | PRTD[4] | X= -829.00 | Y= 1002.00 |

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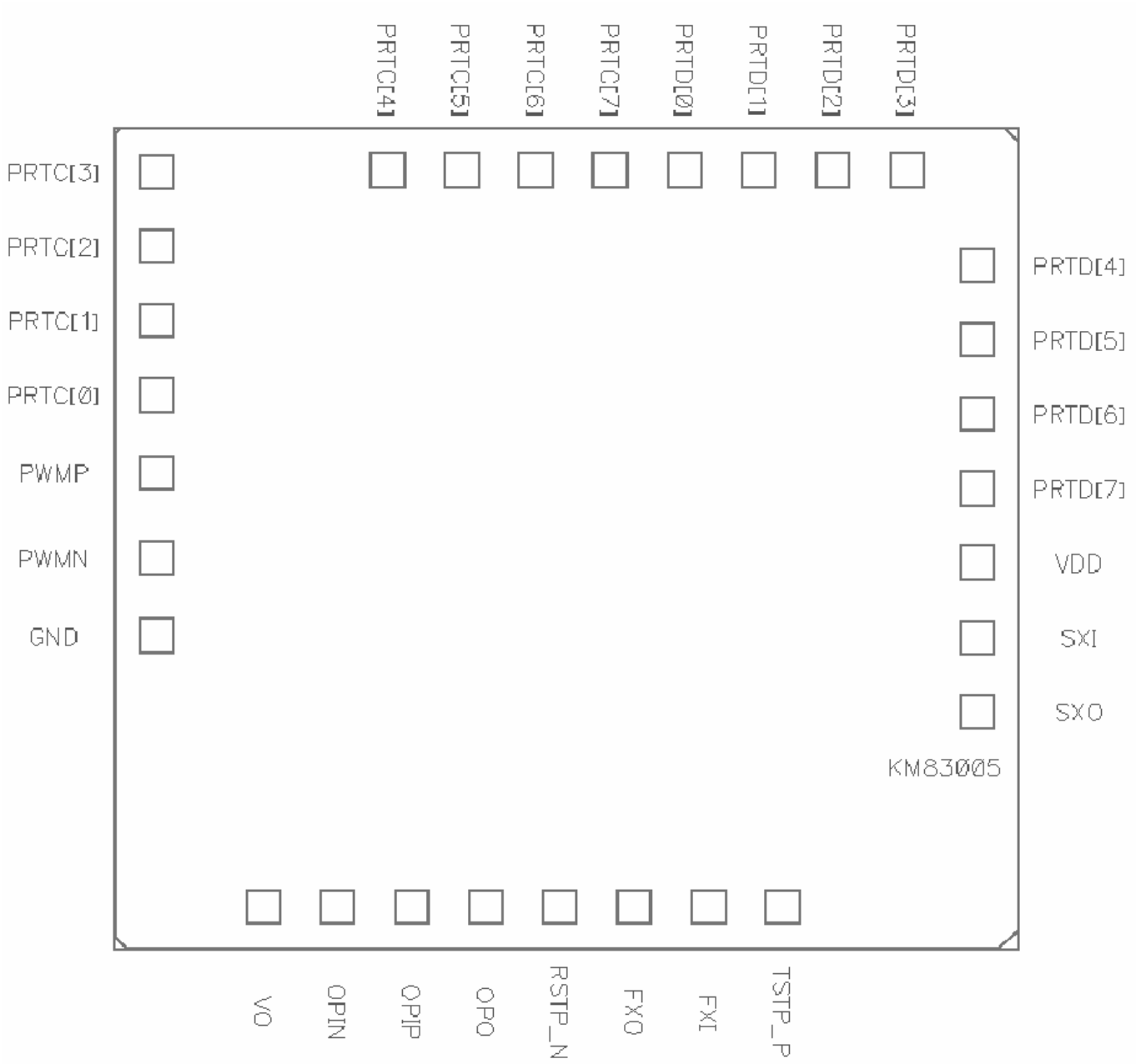
**C Version:Die Size= 1970 μm * 2170 μm**

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| C Version HE83003 | | | |
|---|---|---|---|
| **PIN Number** | **PIN Name** | **X Coordinate** | **Y Coordinate** |
| 1 | PRTD[3] | X= -1057.45 | Y= 742.30 |
| 2 | PRTD[2] | X= -1057.45 | Y= 564.50 |
| 3 | PRTD[1] | X= -1057.45 | Y= 385.90 |
| 4 | PRTD[0] | X= -1057.45 | Y= 208.10 |
| 5 | PRTC[7] | X= -1057.45 | Y= 29.50 |
| 6 | PRTC[6] | X= -1057.45 | Y= -148.30 |
| 7 | PRTC[5] | X= -1057.45 | Y= -326.90 |
| 8 | PRTC[4] | X= -1057.45 | Y= -504.70 |
| 9 | PRTC[3] | X= -1052.90 | Y= -1058.50 |
| 10 | PRTC[2] | X= -874.30 | Y= -1058.50 |
| 11 | PRTC[1] | X= -696.50 | Y= -1058.50 |
| 12 | PRTC[0] | X= -517.90 | Y= -1058.50 |
| 13 | PWMP | X= -332.30 | Y= -1058.50 |
| 14 | PWMN | X= -126.40 | Y= -1058.50 |
| 15 | GND | X= 59.20 | Y= -1058.50 |
| 16 | VO | X= 709.15 | Y= -803.20 |
| 17 | OPIN | X= 709.15 | Y= -625.40 |
| 18 | OPIP | X= 709.15 | Y= -446.80 |
| 19 | OPO | X= 709.15 | Y= -269.00 |
| 20 | RSTP_N | X= 709.15 | Y= -90.40 |
| 21 | FXO | X= 709.15 | Y= 87.40 |
| 22 | FXI | X= 709.15 | Y= 266.00 |
| 23 | TSTP_P | X= 709.15 | Y= 443.80 |
| 24 | SXO | X= 240.70 | Y= 909.10 |
| 25 | SXI | X= 62.90 | Y= 909.10 |
| 26 | VDD | X= -115.70 | Y= 909.10 |
| 27 | PRTD[7] | X= -293.50 | Y= 909.10 |
| 28 | PRTD[6] | X= -472.10 | Y= 909.10 |
| 29 | PRTD[5] | X= -649.90 | Y= 909.10 |
| 30 | PRTD[4] | X= -828.50 | Y= 909.10 |

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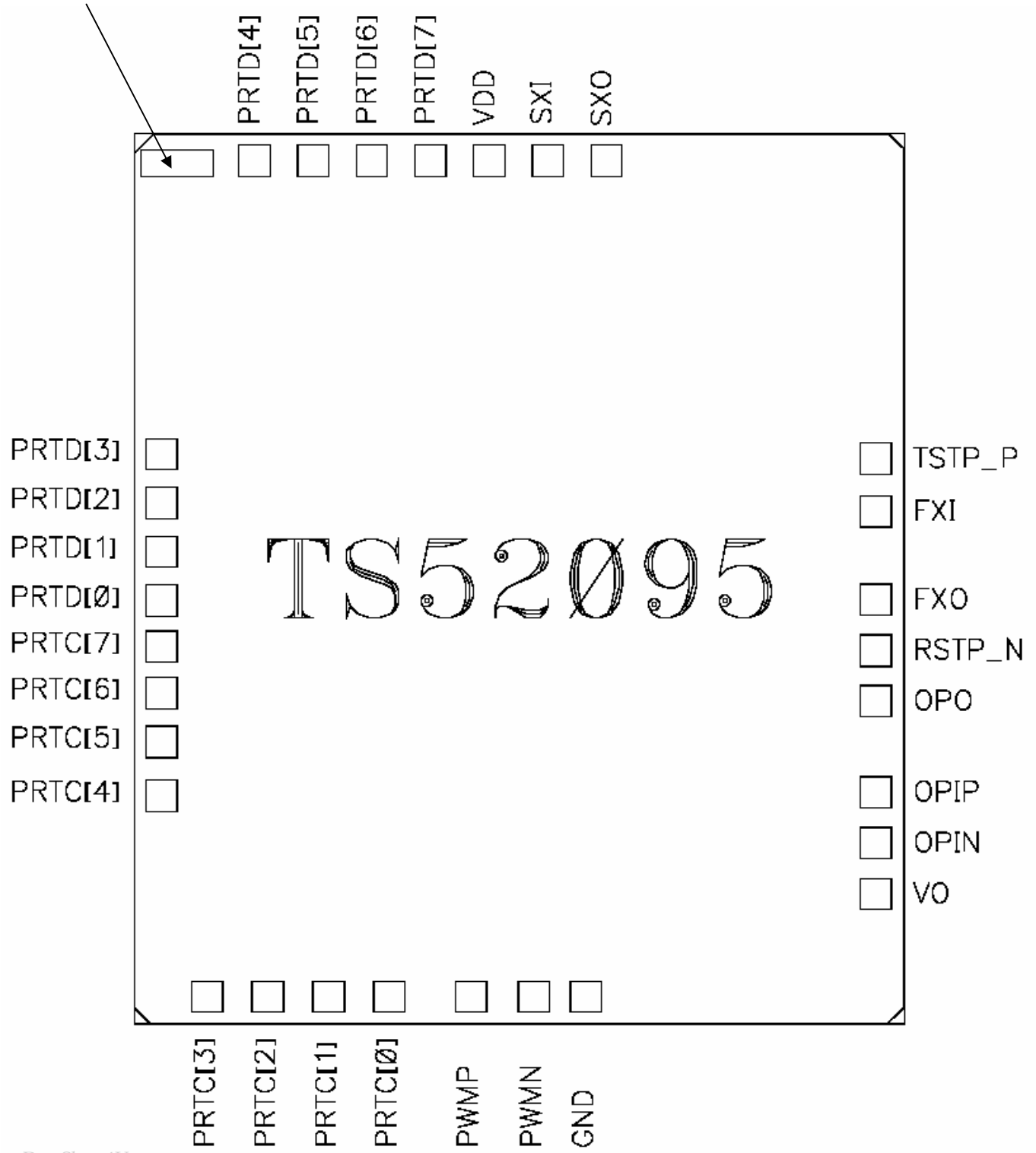
**D1 Version: Die Size= 1970 µm * 2280 µm**

**Logo location**

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| D1 Version HE83003 | | | |
|---|---|---|---|
| **PIN Number** | **PIN Name** | **X Coordinate** | **Y Coordinate** |
| 1 | PRTD[3] | X= -921.50 | Y= 318.40 |
| 2 | PRTD[2] | X= -921.50 | Y= 193.40 |
| 3 | PRTD[1] | X= -921.50 | Y= 68.40 |
| 4 | PRTD[0] | X= -921.50 | Y= -57.10 |
| 5 | PRTC[7] | X= -921.50 | Y= -175.10 |
| 6 | PRTC[6] | X= -921.50 | Y= -293.15 |
| 7 | PRTC[5] | X= -921.50 | Y= -418.15 |
| 8 | PRTC[4] | X= -921.50 | Y= -556.05 |
| 9 | PRTC[3] | X= -804.25 | Y= -1070.65 |
| 10 | PRTC[2] | X= -649.25 | Y= -1070.65 |
| 11 | PRTC[1] | X= -494.25 | Y= -1070.65 |
| 12 | PRTC[0] | X= -339.25 | Y= -1070.65 |
| 13 | PWMP | X= -130.20 | Y= -1070.65 |
| 14 | PWMN | X= 31.20 | Y= -1070.65 |
| 15 | GND | X= 164.20 | Y= -1070.65 |
| 16 | VO | X= 905.40 | Y= -807.85 |
| 17 | OPIN | X= 905.40 | Y= -677.85 |
| 18 | OPIP | X= 905.40 | Y= -547.85 |
| 19 | OPO | X= 905.40 | Y= -314.60 |
| 20 | RSTP_N | X= 905.40 | Y= -184.60 |
| 21 | FXO | X= 905.40 | Y= -55.10 |
| 22 | FXI | X= 905.40 | Y= 170.70 |
| 23 | TSTP_P | X= 905.40 | Y= 305.70 |
| 24 | SXO | X= 217.25 | Y= 1064.65 |
| 25 | SXI | X= 64.15 | Y= 1069.45 |
| 26 | VDD | X= -82.95 | Y= 1069.35 |
| 27 | PRTD[7] | X= -233.45 | Y= 1069.35 |
| 28 | PRTD[6] | X= -383.45 | Y= 1069.35 |
| 29 | PRTD[5] | X= -533.45 | Y= 1069.30 |
| 30 | PRTD[4] | X= -683.45 | Y= 1069.35 |

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# 12. Absolute Maximum Rating

| Item | Symbol | Rating | Condition |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5V ~ 7.0V | |
| Input Voltage | $V_{IN}$ | -0.5V ~ $V_{DD}$ +0.5V | |
| Output Voltage | $V_o$ | -0.5V ~ $V_{DD}$ +0.5V | |
| Operating Temperature | $T_{op}$ | 0℃ ~ 70℃ | |
| Storage Temperature | $T_{st}$ | -50℃ ~ 100℃ | |

# 13. Recommended Operating Conditions

| Item | Symbol | Rating | Condition |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.4V ~ 5.56V | |
| Input Voltage | $V_{IH}$ | 0.9 $V_{DD}$ ~ $V_{DD}$ | |
| | $V_{IL}$ | 0.0V ~ 0.1 $V_{DD}$ | |
| Operating Frequency | Fmax. | 8M Hz | $V_{DD}$ =5.0V |
| | | 4M Hz | $V_{DD}$ =2.4V |
| Operating Temperature | $T_{op}$ | $0^0$C ~ $70^0$C | |
| Storage Temperature | $T_{st}$ | -$50^0$C ~ $100^0$C | |

# 14. AC/DC Characteristics

Testing Condition: TEMP=25℃, VDD=3V±10%

| | PARAMETER | | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{Fast}$ | NORMAL Mode Current | System | 2M ext. R/C | | 0.75 | 1 | mA |
| $I_{Slow}$ | SLOW Mode Current | System | 32.768K X'tal | | 6 | 9 | µA |
| $I_{Idle}$ | IDLE Mode Current | System | 32.769K X'tal | | 4 | 7 | µA |
| $I_{Sleep}$ | Sleep Mode Current | System | | | | 1 | µA |
| $I_{oHPWM}$ | PWM Output Drive Current | PWMP, PWMN*2 | $V_{DD}$=3V; $V_{OH}$=2V | 12 | 15 | | mA |
| $I_{oLPWM}$ | PWM Output Sink Current | PWMP, PWMN*2 | $V_{DD}$=3V; $V_{OL}$=1V | 33 | 40 | | mA |
| $I_{oVO}$ | DAC Output Current | VO | $V_{DD}$=3V;VO=0~2V,Data=7F | 2.5 | 3 | | mA |
| $V_{iH}$ | Input High Voltage | I/O pins | | 0.8 $V_{DD}$ | | | V |
| $V_{iL}$ | Input Low Voltage | I/O pins | | | | 0.2 $V_{DD}$ | V |
| $V_{hys}$ | Input Hysteresis Width | I/O, RSTP_N | Threshold=2/3$V_{DD}$(input from low to high) Threshold=1/3$V_{DD}$(input from high to low) | | 1/3 $V_{DD}$ | | V |
| $I_{OH}$ | Output Drive Current | I/O pull-high*1 | $V_{OL}$=2.0V | 50 | | | µA |
| $I_{OL\_1}$ | Output Sink Current | I/O pull-low*1 | $V_{OL}$=0.4V | 1.0 | | | mA |
| $I_{IL\_1}$ | Input Low Current | RSTP_N | $V_{IL}$=GND, pull high Internally | | 20 | | µA |

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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $\mathbf{I_{IL\_2}}$ | Input Low Current | I/O | $V_{IL}$=GND, if pull high Internally by user | | 100 | | μA |

Note:

*1: Drive Current Spec. for Push-Pull I/O port only Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

*2: This Spec. base on one driver only. There are five build-in drivers, so users just multiply the number of driver he used to one driver current to get the total amount of current. ( $\mathbf{I_{oHPWM}}$、$\mathbf{I_{oLPWM}}$ * N; N=0,1,2,3,4,5)

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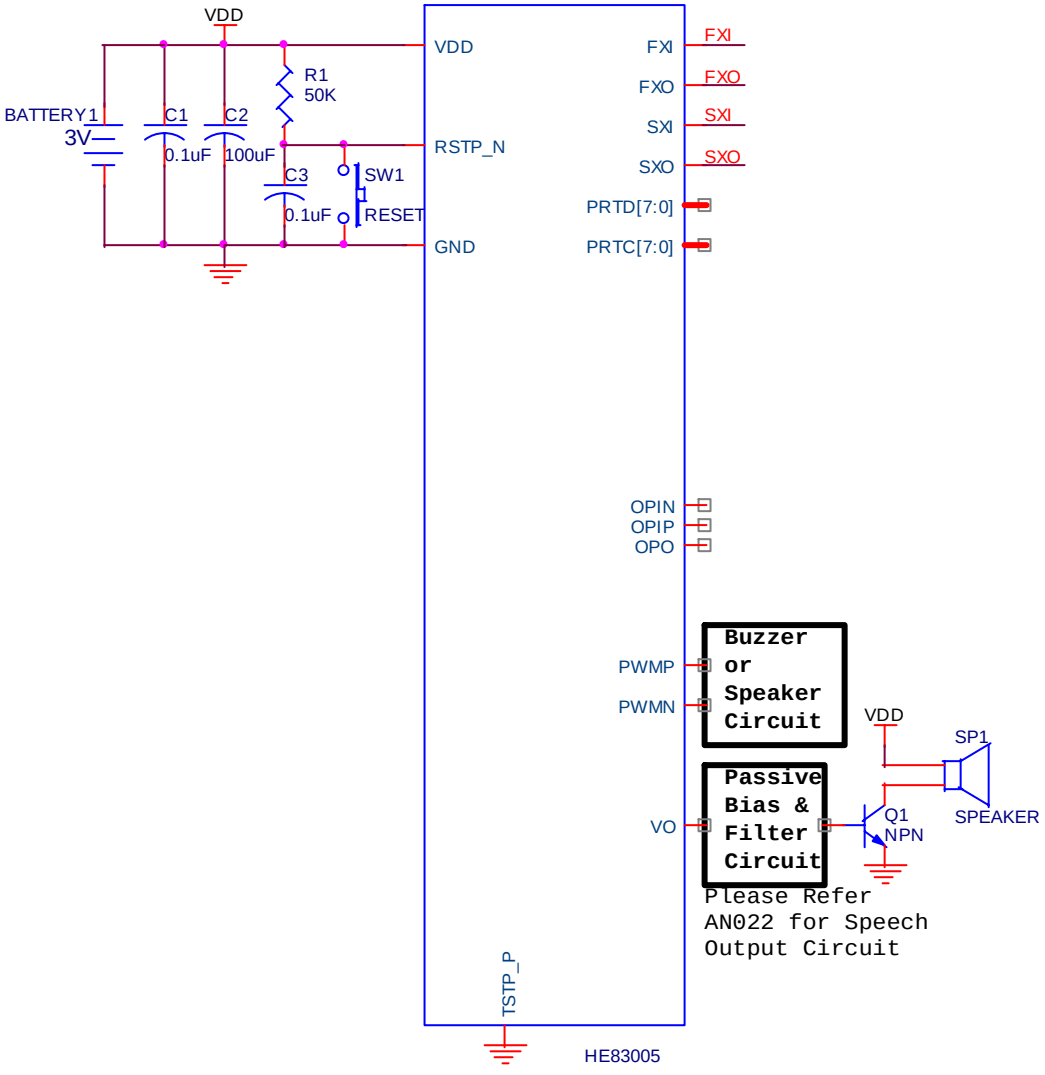
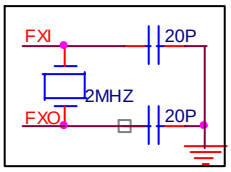
# 15. Application Circuit

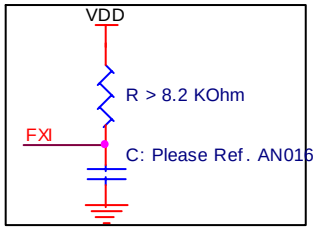



**No External Parts is necessary if user adopt Internal Fast RC Clock**

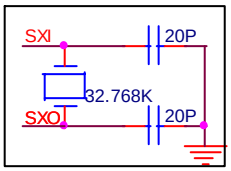
**External Fast Clock: Crystal osc.**



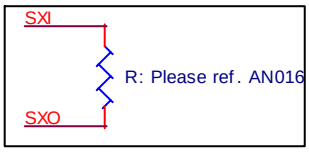

**External Fast Clock: RC osc.**




**External Slow Clock: Crystal osc.**




**External Slow Clock: RC osc.**

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# 16. Important Note

1. Please note the ICE is a superset of HE80000 series IC. Each member of the family only has parts of all resources. Do not use any hardware resource that your target chip doesn't have, for example, RAM and register. KBIDS and compiler can't prevent user from using some hardware resources that don't exist in your target chip.

2. Please bond the TSTP_P, RSTP_N and PRTD [7:0] with test points on PCB (can be soldered and probed) as you can, then some testing can be performed on PCB when it's necessary. The TSTP_P is suggested to connect to ground by a 0 ohm resistor.

3. Users should turn off the PWM and DAC function by firmware before the system enters into the sleep and idle modes. Otherwise, there are some current leakages in the PWM/DAC circuit, and the current will be large in the sleep and idle mode.

# 17. Updated History

| Version | Date | New Content |
|---|---|---|
| V1.0 | 9/30/03 | New create |
| V1.1 | 9/30/03 | ROM size 32KB -> 36 KB |
| | | |
| | | |
| | | |
| | | |
| | | |

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