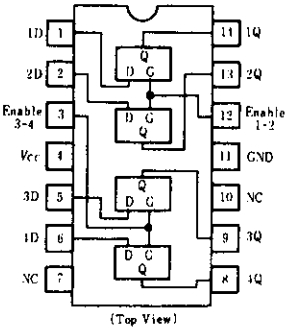
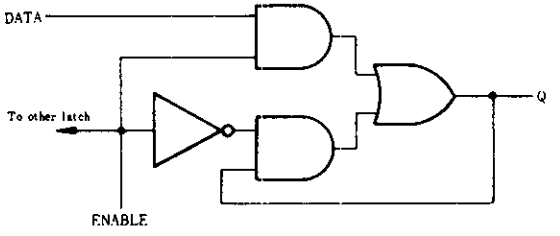
HD74LS77 ●4-bit Bistable Latches

The HD74LS77 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

Inputs		Output
D	G	Q
L	H	L
H	H	H
X	L	Q_0

Notes) H; high level, L; low level, X; irrelevant
Q_0; level of Q before the indicated steady-state input conditions were established.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Pulse width	t_w	20	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	5	—	—	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—	—	V
		V_{IL}			—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	—	—	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	—	—	0.4	V
				$I_{OL}=8mA$	—	—	0.5	
Input current	D	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	G				—	—	80	
	D	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	G				—	—	−1.6	
	D	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
	G				—	—	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	—	−100	mA
Supply current **		I_{CC}	$V_{CC}=5.25V$		—	6.9	13	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

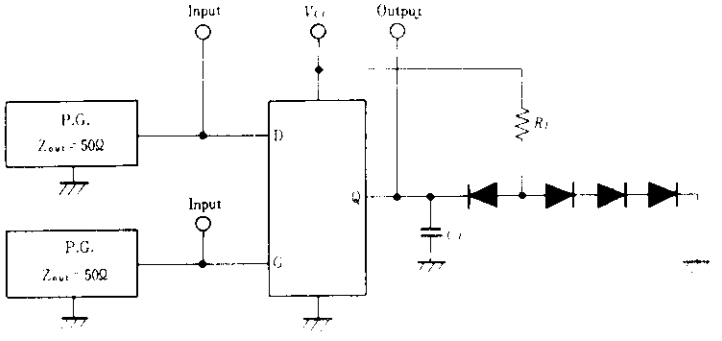
* $V_{CC}=5V$, $Ta=25°C$
** I_{CC} is measured with all outputs open and all inputs grounded.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	D	Q	C_L 15pF R_L 2kΩ	-	11	19	ns
	t_{PHL}				-	9	17	
	t_{PLH}	G	Q		-	10	18	
	t_{PHL}				-	10	18	

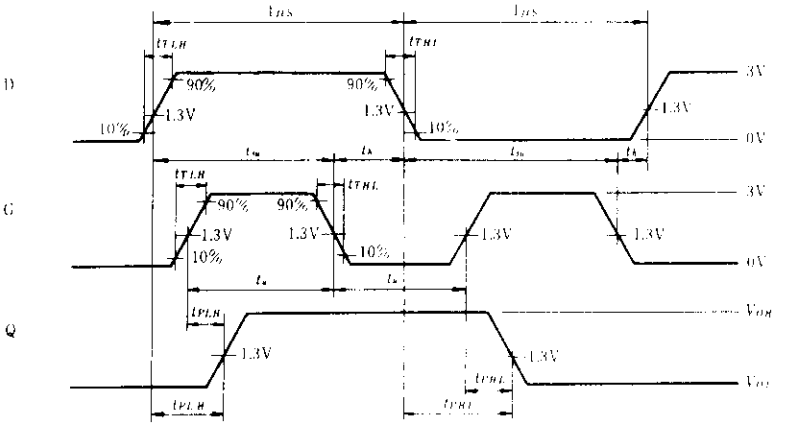
■TESTING METHOD

1) Test Circuit



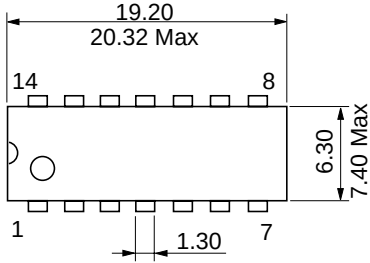
Notes) 1. Test is put into the each latch
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

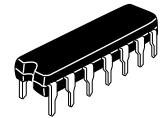
Waveform

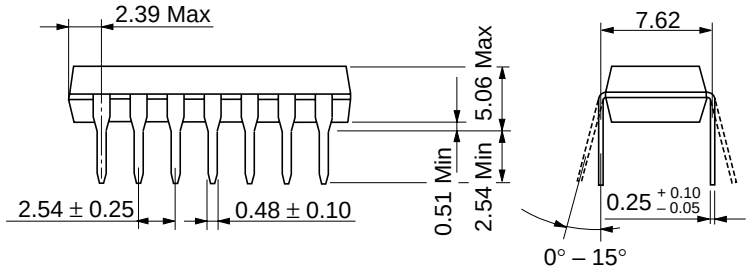


Notes) 1. Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$.
2. When measuring propagation delay times from the D input, the corresponding G input must be held high.

Unit: mm

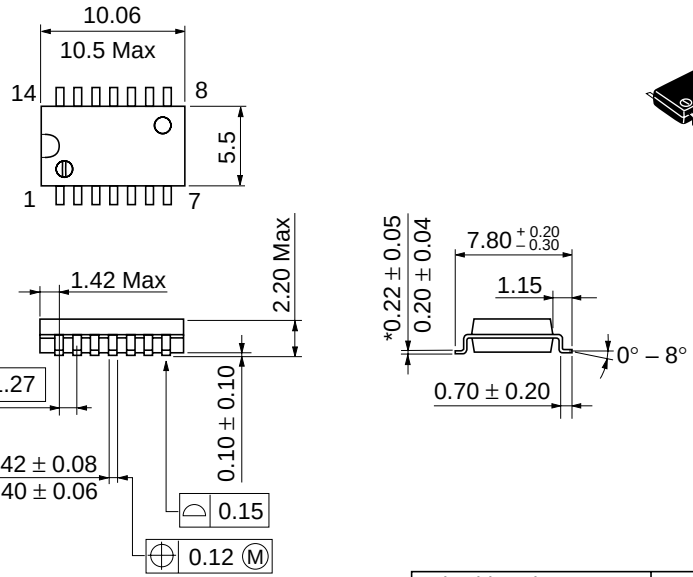


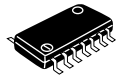




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

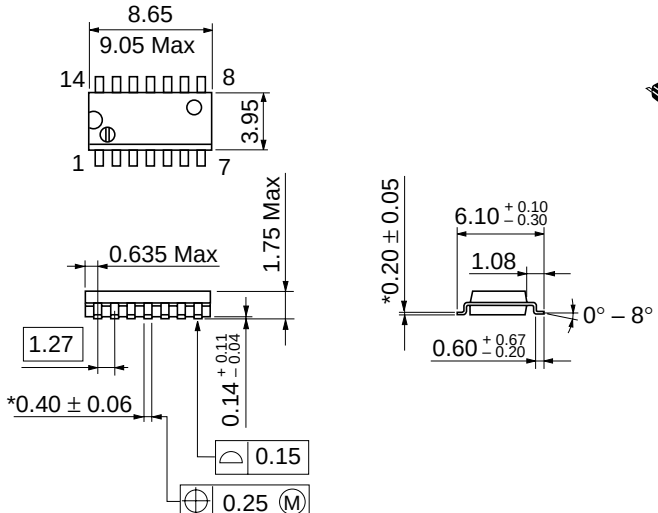




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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