# HD74LS190

## Synchronous Up / Down Decade Counter (signal clock line)

REJ03D0452–0200
Rev.2.00
Jul.15.2005

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down / up input. When low, the counter counts up and when high, it counts down. Level changes at the down / up input should be made only when the clock input is high. This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down / up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum / minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycles to the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow conditions exists.

The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum / minimum count output can be used to accomplish look-ahead for high-speed operation.



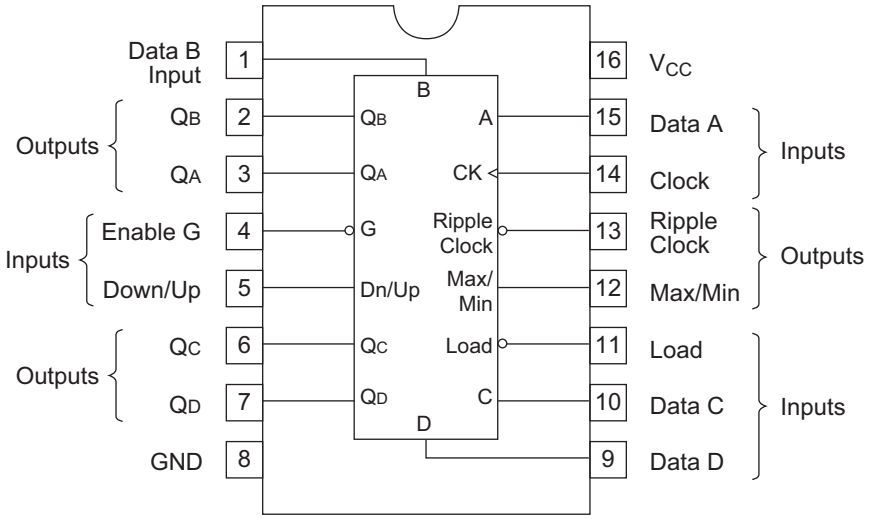
### Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LS190P | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74LS190FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |

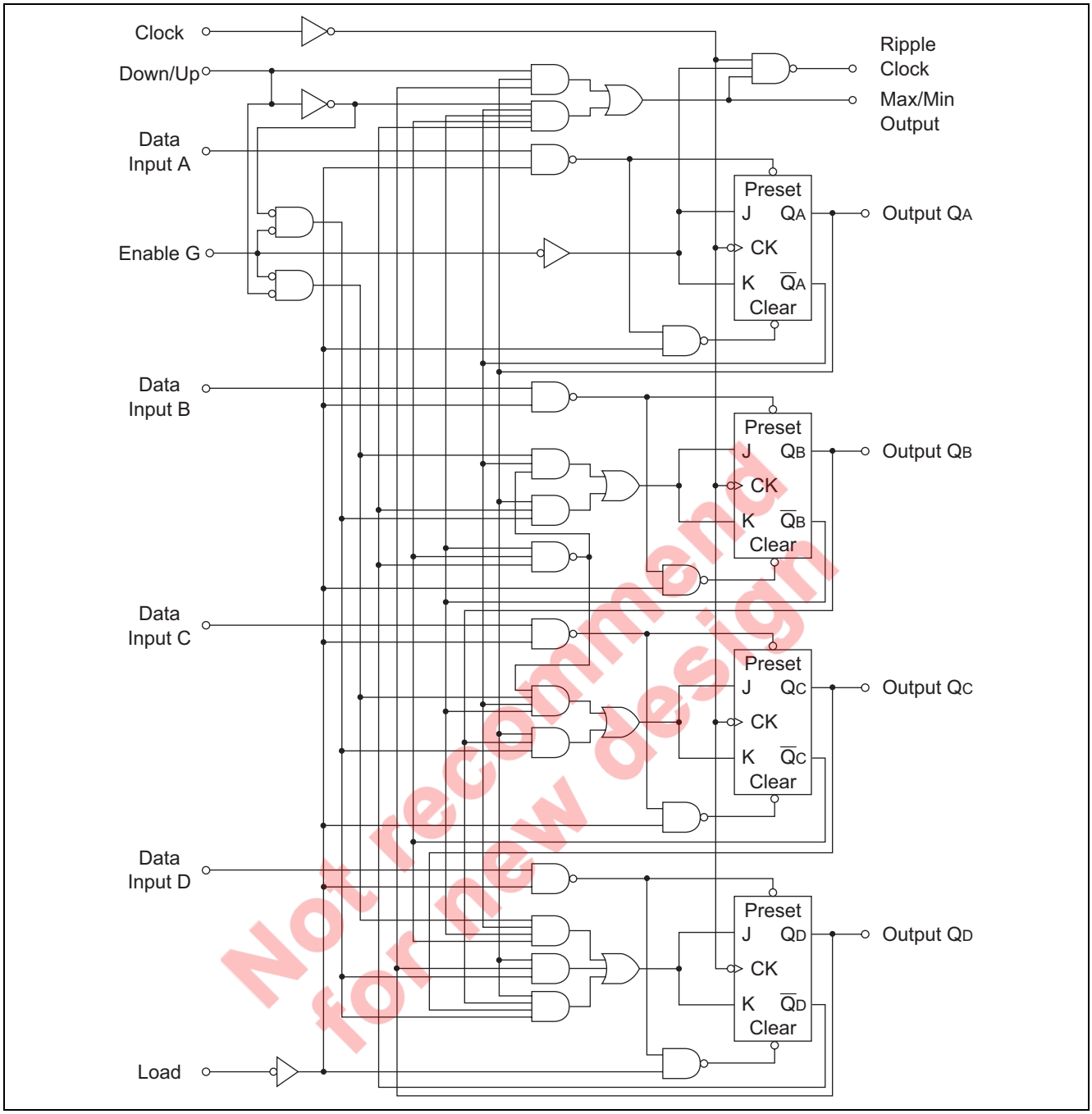
Notes: Please consult the sales office for the above package availability.

## Pin Arrangement




(Top view)

## Block Diagram




## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_{IN}$ | 7 | V |
| Power dissipation | $P_T$ | 400 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | –400 | µA |
| | $I_{OL}$ | — | — | 8 | mA |
| Operating temperature | $T_{opr}$ | –20 | 25 | 75 | °C |
| Clock frequency | $f_{clock}$ | 0 | — | 20 | MHz |
| Clock pulse width | $t_{w\ (CK)}$ | 25 | — | — | ns |
| Load pulse width | $t_{w\ (Load)}$ | 35 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_{h\ (data)}$ | 3 | — | — | ns |
| Enable time | $t_{enable}$ | 40 | — | — | ns |

## Electrical Characteristics

(Ta = –20 to +75 °C)

| Item | | Symbol | min. | typ.* | max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | 2.0 | — | — | V | |
| | | $V_{IL}$ | — | — | 0.8 | V | |
| Output voltage | | $V_{OH}$ | 2.7 | — | — | V | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = –400 µA |
| | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 4 mA, $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V |
| | | | — | — | 0.5 | | $I_{OL}$ = 8 mA |
| Input current | Enable | $I_{IH}$ | — | — | 60 | µA | $V_{CC}$ = 5.25 V, $V_I$ = 2.7 V |
| | Others | | — | — | 20 | | |
| | Enable | $I_{IL}$ | — | — | –1.2 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V |
| | Others | | — | — | –0.4 | | |
| | Enable | $I_I$ | — | — | 0.3 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 7 V |
| | Others | | — | — | 0.1 | | |
| Short-circuit output current | | $I_{OS}$ | –20 | — | –100 | mA | $V_{CC}$ = 5.25 V |
| Supply current** | | $I_{CC}$ | — | 20 | 35 | mA | $V_{CC}$ = 5.25 V |
| Input clamp voltage | | $V_{IK}$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V, $I_{IN}$ = –18 mA |

Notes: * $V_{CC}$ = 5 V, Ta = 25°C

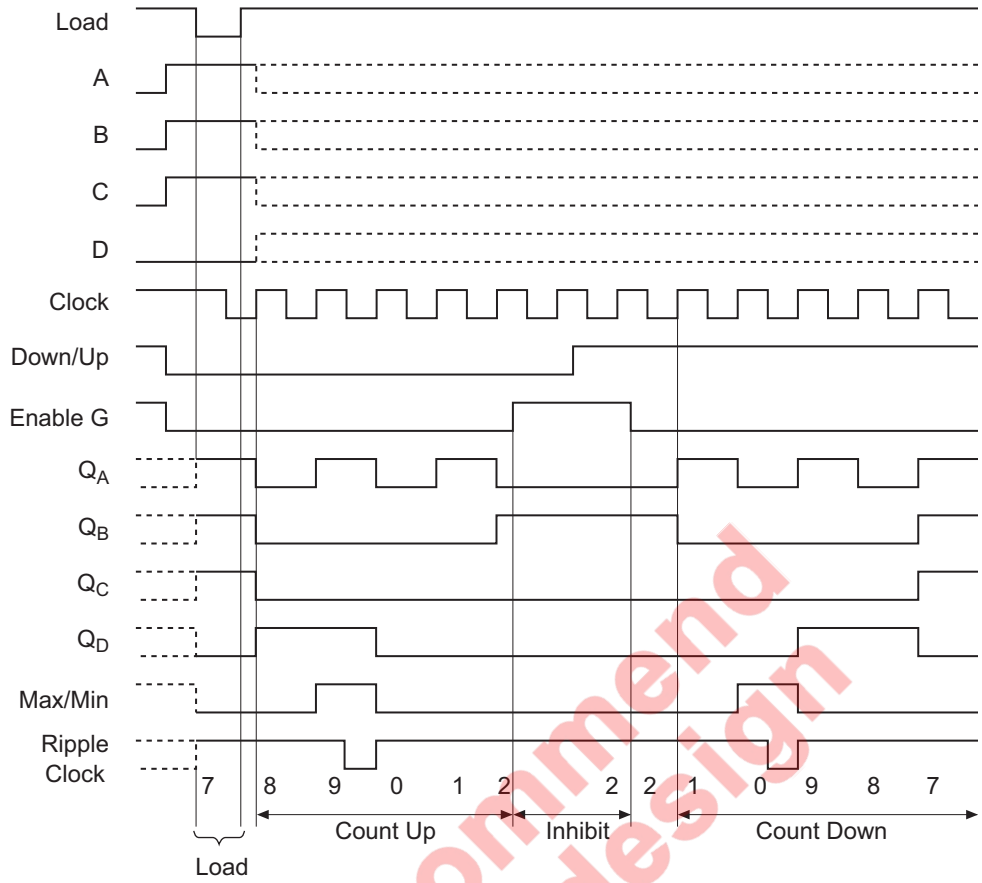
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## Switching Characteristics

($V_{CC}$ = 5 V, Ta = 25°C)

| Item | Symbol | Inputs | Outputs | min. | typ. | max. | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | 20 | 25 | — | MHz | $C_L$ = 15 pF, $R_L$ = 2 kΩ |
| Propagation delay time | $t_{PLH}$ | Load | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | — | 22 | 33 | ns | |
| | $t_{PHL}$ | | | — | 33 | 50 | | |
| | $t_{PLH}$ | A, B, C, D | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | — | 20 | 32 | ns | |
| | $t_{PHL}$ | | | — | 27 | 40 | | |
| | $t_{PLH}$ | Clock | Ripple Clock | — | 13 | 20 | ns | |
| | $t_{PHL}$ | | | — | 16 | 24 | | |
| | $t_{PLH}$ | Clock | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | — | 16 | 24 | ns | |
| | $t_{PHL}$ | | | — | 24 | 36 | | |
| | $t_{PLH}$ | Clock | Max / Min | — | 28 | 42 | ns | |
| | $t_{PHL}$ | | | — | 37 | 52 | | |
| | $t_{PLH}$ | Down / Up | Ripple Clock | — | 30 | 45 | ns | |
| | $t_{PHL}$ | | | — | 30 | 45 | | |
| | $t_{PLH}$ | Down / Up | Max / Min | — | 21 | 33 | ns | |
| | $t_{PHL}$ | | | — | 22 | 33 | | |
| | $t_{PLH}$ | Enable | Ripple Clock | — | 21 | 33 | ns | |
| | $t_{PHL}$ | | | — | 22 | 33 | | |

## Count Sequences

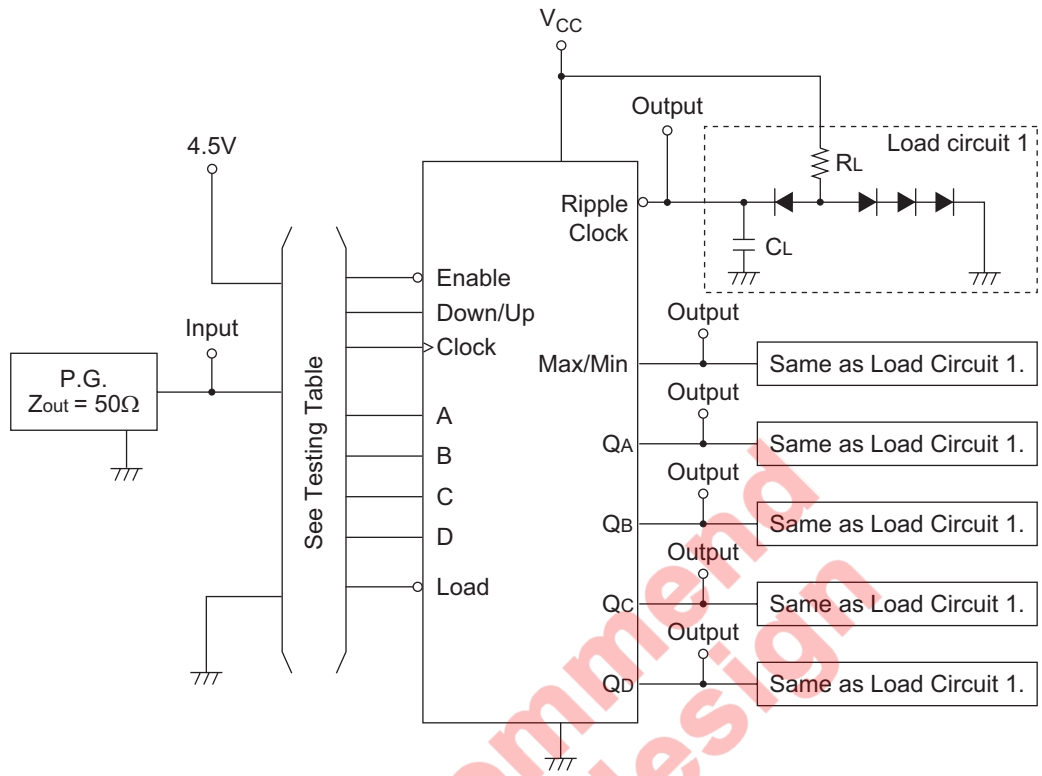



Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven.

## Testing Method

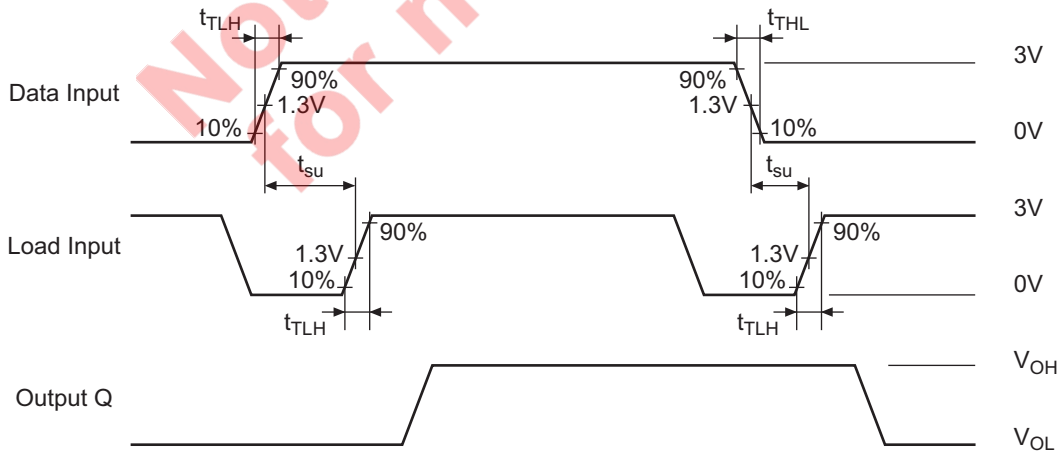
### Test Circuit




Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074(H).



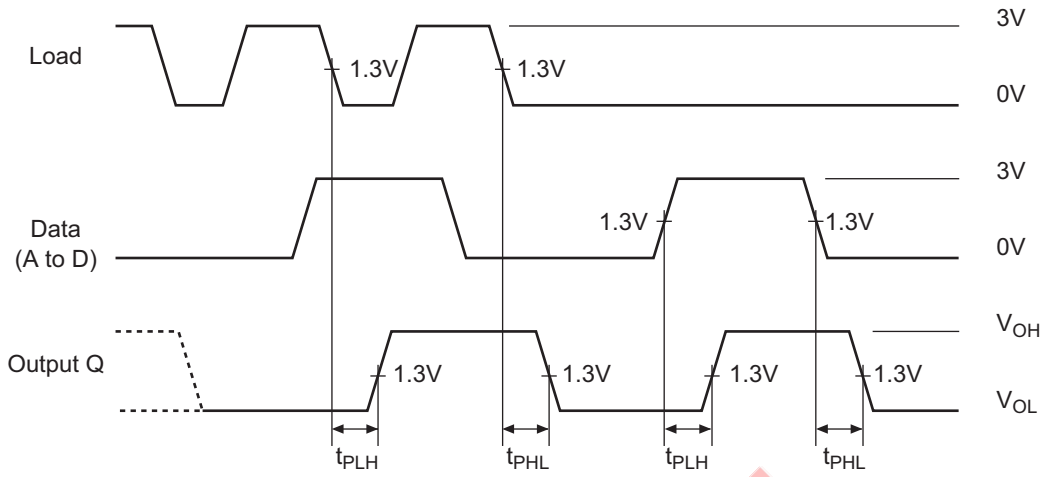
### Waveforms 1




Note: Input pulse: $t_{TLH}$, $t_{THL} \leq 10$ ns, PRR = 1 MHz, duty cycle ≤ 50%

### Waveforms 2

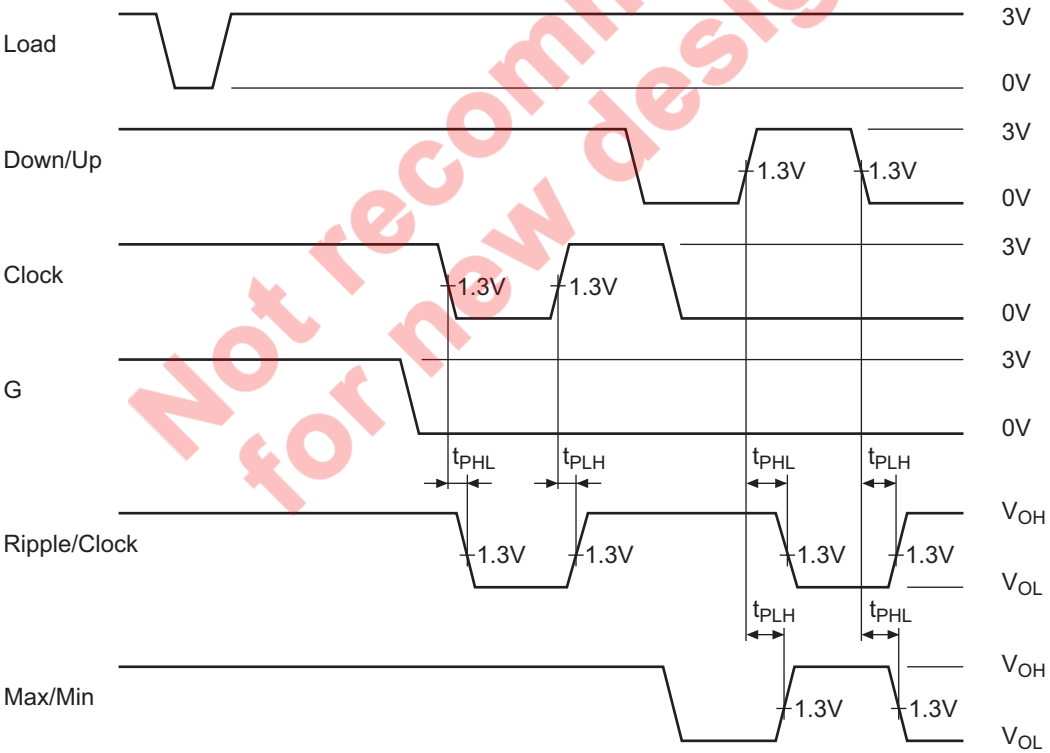
Load→Q, Data→Q




Note: Conditions on other inputs are irrelevant.

### Waveforms 3

G→Ripple CK, CK→Ripple CK, Down / Up→Ripple CK, Down / Up→Max / Min

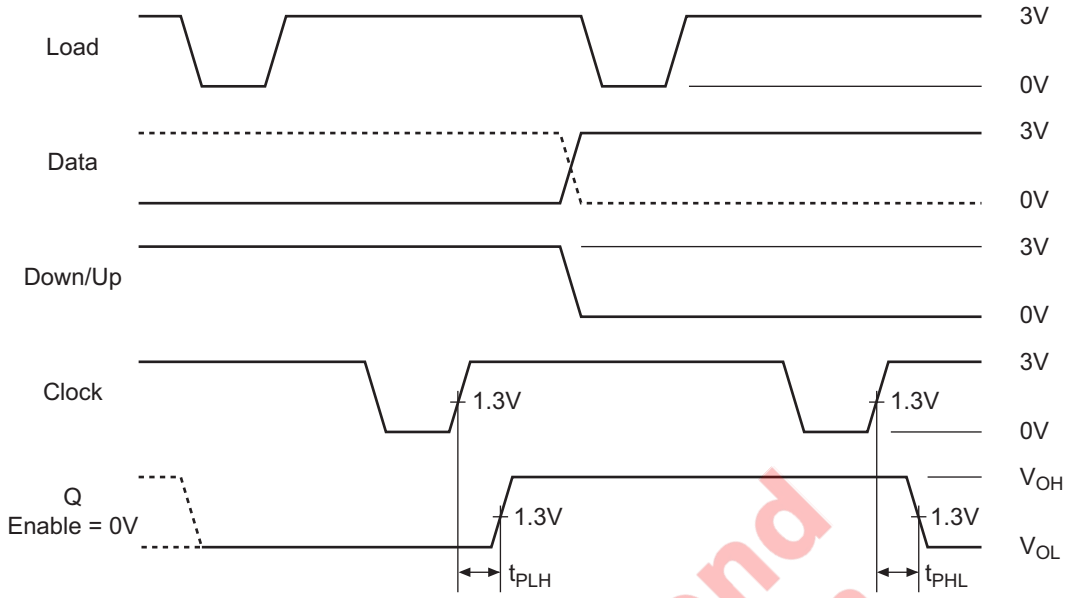





Note: All data inputs are low.

### Waveforms 4

Clock→Q

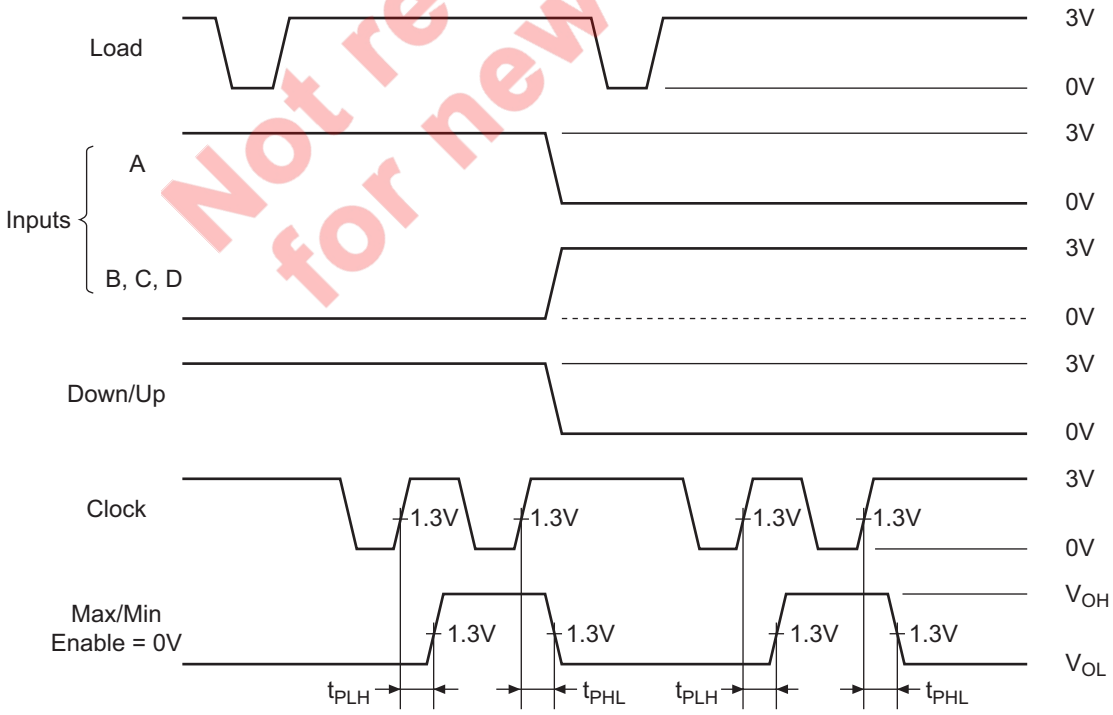



Notes:
1. When test the $Q_A$, $Q_B$, and $Q_C$ outputs, data inputs A, B and C are shown by the solid line, and data input D is shown by the dashed line.
2. When test the $Q_D$ output, data inputs A and D are shown by the solid line, and data inputs B and C are held at the low logic level.



### Waveforms 5

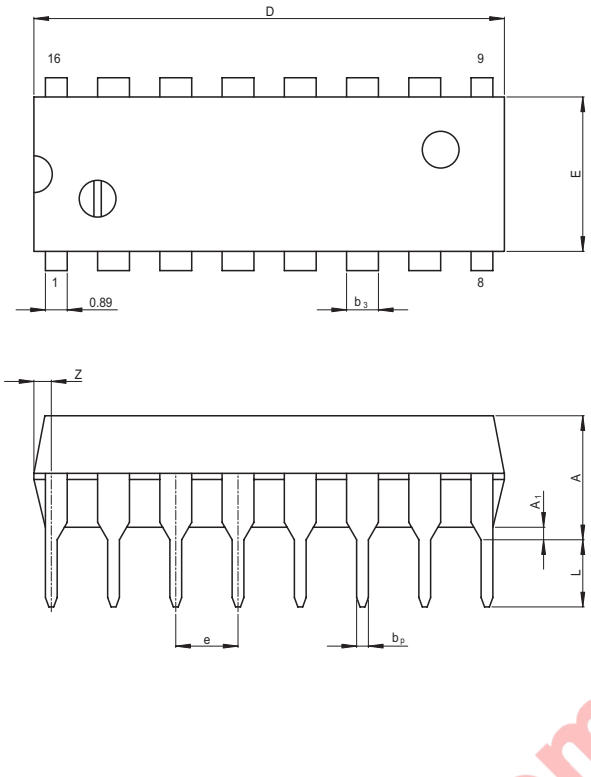
Clock→Max / Min




Note: Data inputs B and C are shown by the dashed line. Data input D is shown by the solid line.

## Package Dimensions

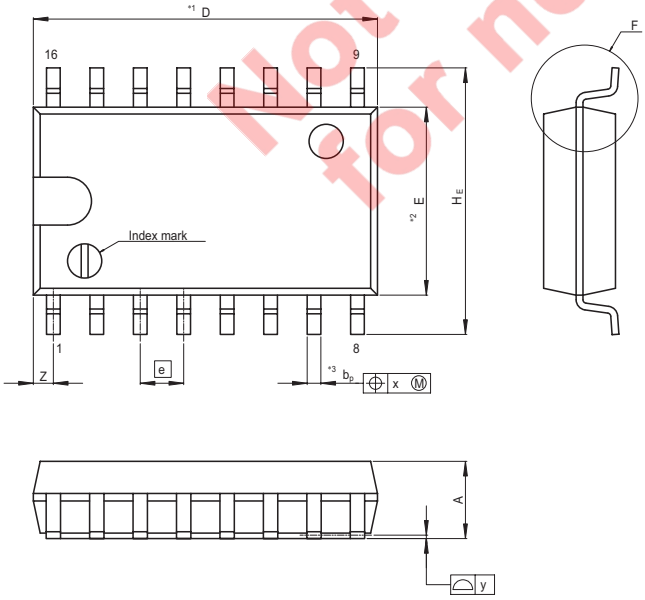
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-DIP16-6.3x19.2-2.54 | PRDP0016AE-B | DP-16FV | 1.05g |



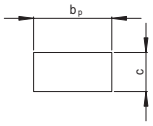

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e 1 | — | 7.62 | — |
| D | — | 19.2 | 20.32 |
| E | — | 6.3 | 7.4 |
| A | — | — | 5.06 |
| A 1 | 0.51 | — | — |
| b p | 0.40 | 0.48 | 0.56 |
| b 3 | — | 1.30 | — |
| c | 0.19 | 0.25 | 0.31 |
| θ | 0° | — | 15° |
| e | 2.29 | 2.54 | 2.79 |
| Z | — | — | 1.12 |
| L | 2.54 | — | — |



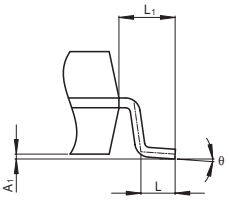
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-B | FP-16DAV | 0.24g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.




Terminal cross section
( Ni/Pd/Au plating )




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.50 | — |
| A 2 | — | — | — |
| A 1 | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| b p | 0.34 | 0.40 | 0.46 |
| b 1 | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| c 1 | — | — | — |
| θ | 0° | — | 8° |
| H E | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| L 1 | — | 1.15 | — |

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan





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**Renesas Technology Singapore Pte. Ltd.**
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Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

**Renesas Technology Malaysia Sdn. Bhd.**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510



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