

# HD74LS174 / HD74LS175

## Hex / Quadruple D-type Flip-Flops (with clear)

REJ03D0451-0300

Rev.3.00

Jul.15.2005

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

### Features

- Ordering Information

#### • HD74LS174

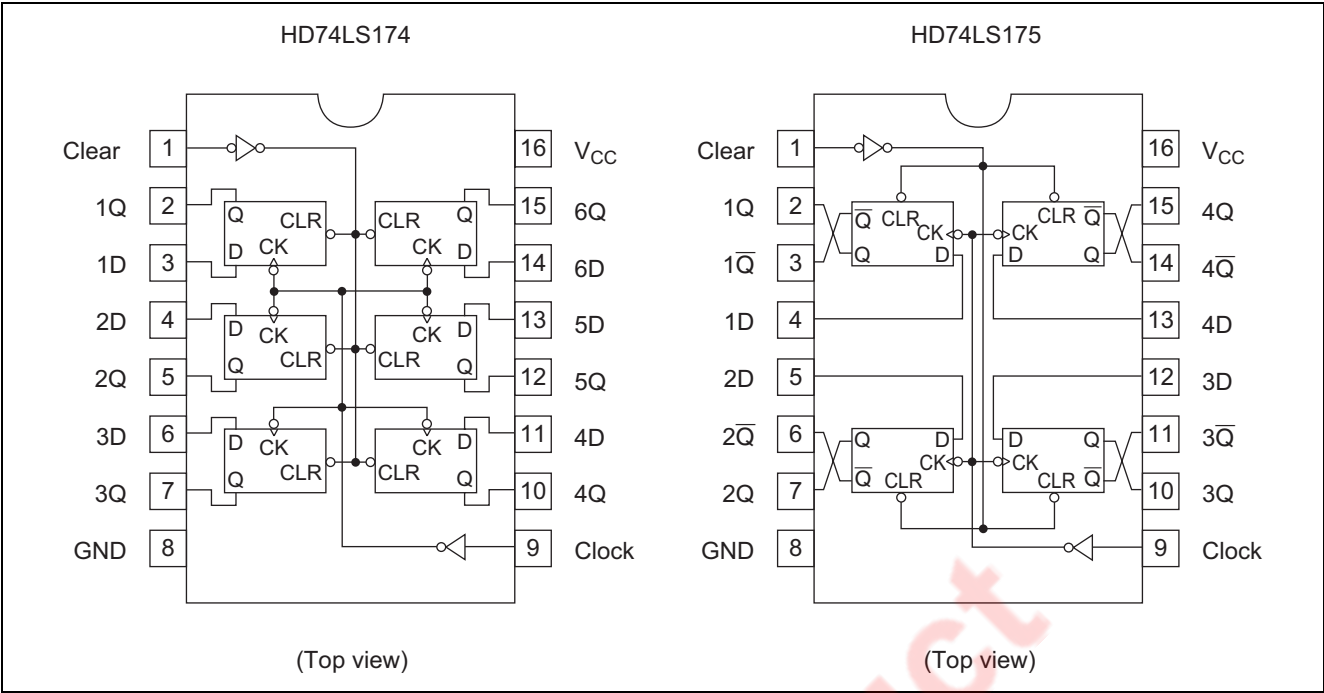
| Part Name     | Package Type       | Package Code<br>(Previous Code) | Package<br>Abbreviation | Taping Abbreviation<br>(Quantity) |
|---------------|--------------------|---------------------------------|-------------------------|-----------------------------------|
| HD74LS174P    | DILP-16 pin        | PRDP0016AE-B<br>(DP-16FV)       | P                       | —                                 |
| HD74LS174FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B<br>(FP-16DAV)      | FP                      | EL (2,000 pcs/reel)               |
| HD74LS174RPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A<br>(FP-16DNV)      | RP                      | EL (2,500 pcs/reel)               |

#### • HD74LS175

| Part Name     | Package Type       | Package Code<br>(Previous Code) | Package<br>Abbreviation | Taping Abbreviation<br>(Quantity) |
|---------------|--------------------|---------------------------------|-------------------------|-----------------------------------|
| HD74LS175P    | DILP-16 pin        | PRDP0016AE-B<br>(DP-16FV)       | P                       | —                                 |
| HD74LS175FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B<br>(FP-16DAV)      | FP                      | EL (2,000 pcs/reel)               |
| HD74LS175RPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A<br>(FP-16DNV)      | RP                      | EL (2,500 pcs/reel)               |

Note: Please consult the sales office for the above package availability.

Pin Arrangement

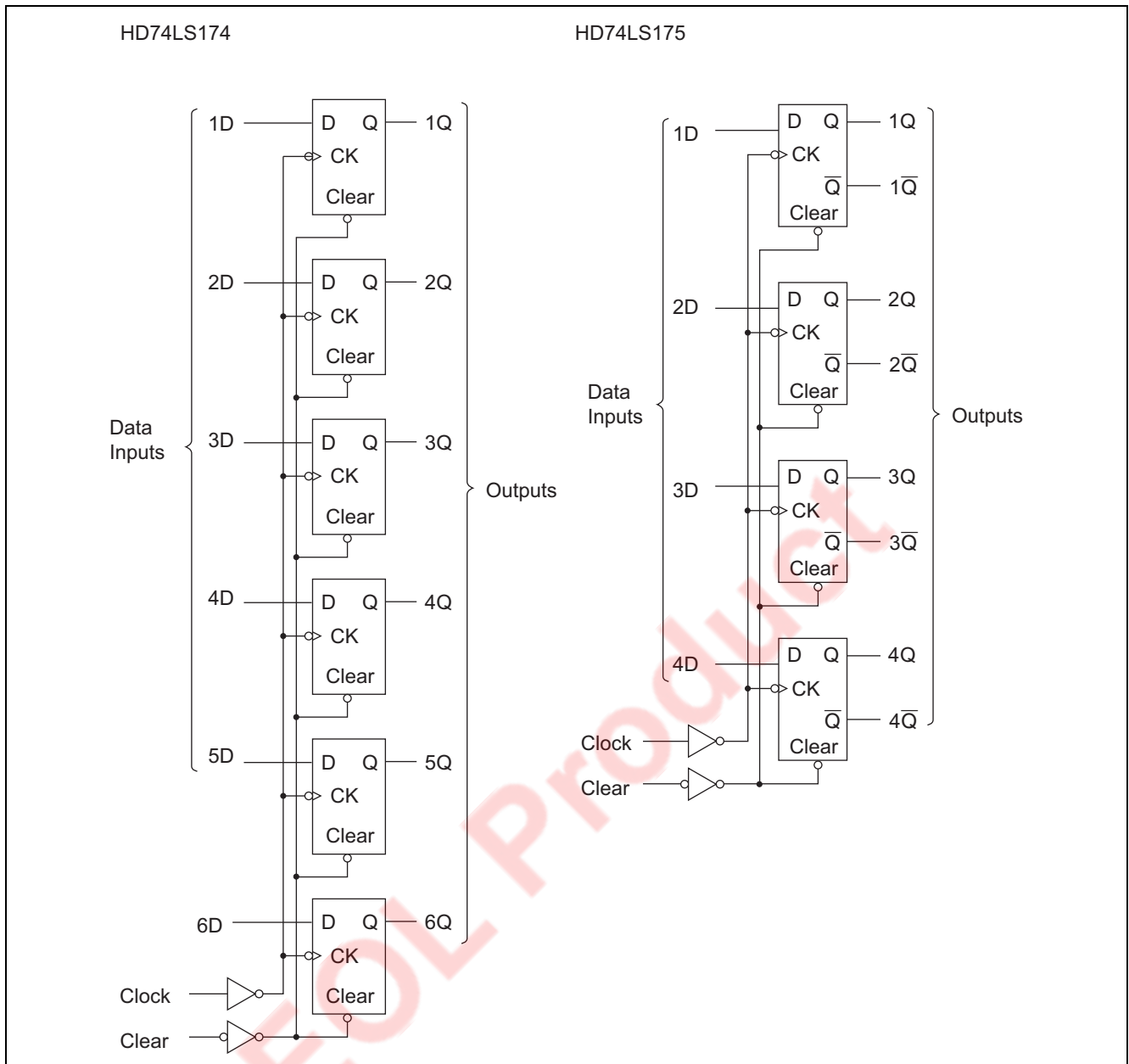


Function Table

| Inputs |       |   | Outputs |             |
|--------|-------|---|---------|-------------|
| Clear  | Clock | D | Q       | $\bar{Q}$   |
| L      | X     | X | L       | H           |
| H      | ↑     | H | H       | L           |
| H      | ↑     | L | L       | H           |
| H      | L     | X | $Q_0$   | $\bar{Q}_0$ |

- Notes:
1. H; high level, L; low level, X; irrelevant
  2. ↑; transition from low to high level
  3.  $Q_0$ ; the level of Q before the indicated steady-state input conditions were established.
  4.  $\bar{Q}$  is applied to HD74LS175 only.

## Block Diagram



## Absolute Maximum Ratings

| Item                | Symbol    | Ratings     | Unit |
|---------------------|-----------|-------------|------|
| Supply voltage      | $V_{CC}$  | 7           | V    |
| Input voltage       | $V_{IN}$  | 7           | V    |
| Power dissipation   | $P_T$     | 400         | mW   |
| Storage temperature | $T_{stg}$ | -65 to +150 | °C   |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

## • HD74LS174

| Item                  | Symbol               | Min             | Typ  | Max  | Unit    |
|-----------------------|----------------------|-----------------|------|------|---------|
| Supply voltage        | $V_{CC}$             | 4.75            | 5.00 | 5.25 | V       |
| Output current        | $I_{OH}$             | —               | —    | −400 | $\mu A$ |
|                       | $I_{OL}$             | —               | —    | 8    | mA      |
| Operating temperature | $T_{opr}$            | −20             | 25   | 75   | °C      |
| Clock frequency       | $f_{clock}$          | 0               | —    | 30   | MHz     |
| Clock pulse width     | $t_w (CK)$           | 20              | —    | —    | ns      |
| Clear pulse width     | $t_w (CLR)$          | 20              | —    | —    | ns      |
| Setup time            | Data input           | $t_{su} (data)$ | 20   | —    | ns      |
|                       | Clear inactive-state | $t_{su} (CLR)$  | 25   | —    | ns      |
| Data hold time        | $t_h (data)$         | 5               | —    | —    | ns      |

## • HD74LS175

| Item                  | Symbol               | Min             | Typ  | Max  | Unit    |
|-----------------------|----------------------|-----------------|------|------|---------|
| Supply voltage        | $V_{CC}$             | 4.75            | 5.00 | 5.25 | V       |
| Output current        | $I_{OH}$             | —               | —    | −400 | $\mu A$ |
|                       | $I_{OL}$             | —               | —    | 8    | mA      |
| Operating temperature | $T_{opr}$            | −20             | 25   | 75   | °C      |
| Clock frequency       | $f_{clock}$          | 0               | —    | 30   | MHz     |
| Clock pulse width     | $t_w (CK)$           | 20              | —    | —    | ns      |
| Clear pulse width     | $t_w (CLR)$          | 20              | —    | —    | ns      |
| Setup time            | Data input           | $t_{su} (data)$ | 20   | —    | ns      |
|                       | Clear inactive-state | $t_{su} (CLR)$  | 25   | —    | ns      |
| Data hold time        | $t_h (data)$         | 5               | —    | —    | ns      |

## Electrical Characteristics

(Ta = −20 to +75 °C)

| Item                         | Symbol   | min. | typ.* | max.       | Unit    | Condition                                                                          |
|------------------------------|----------|------|-------|------------|---------|------------------------------------------------------------------------------------|
| Input voltage                | $V_{IH}$ | 2.0  | —     | —          | V       |                                                                                    |
|                              | $V_{IL}$ | —    | —     | 0.8        | V       |                                                                                    |
| Output voltage               | $V_{OH}$ | 2.7  | —     | —          | V       | $V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -400 \mu A$               |
|                              | $V_{OL}$ | —    | —     | 0.5<br>0.4 | V       | $I_{OL} = 8 mA$<br>$I_{OL} = 4 mA$ $V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V$ |
| Input current                | $I_{IH}$ | —    | —     | 20         | $\mu A$ | $V_{CC} = 5.25 V, V_I = 2.7 V$                                                     |
|                              | $I_{IL}$ | —    | —     | −0.4       | mA      | $V_{CC} = 5.25 V, V_I = 0.4 V$                                                     |
|                              | $I_I$    | —    | —     | 0.1        | mA      | $V_{CC} = 5.25 V, V_I = 7 V$                                                       |
| Short-circuit output current | $I_{OS}$ | −20  | —     | −100       | mA      | $V_{CC} = 5.25 V$                                                                  |
| Supply current**             | $I_{CC}$ | —    | 16    | 26         | mA      | HD74LS174                                                                          |
|                              |          | —    | 11    | 18         | mA      | HD74LS175                                                                          |
| Input clamp voltage          | $V_{IK}$ | —    | —     | −1.5       | V       | $V_{CC} = 4.75 V, I_{IN} = -18 mA$                                                 |

Notes: \*  $V_{CC} = 5 V, T_a = 25^\circ C$ \*\* With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary grounded, then 4.5 V, is applied to clock.

## Switching Characteristics

## • HD74LS174

(V<sub>CC</sub> = 5 V, Ta = 25°C)

| Item                    | Symbol           | Inputs | Outputs | min. | typ. | max. | Unit | Condition                                          |
|-------------------------|------------------|--------|---------|------|------|------|------|----------------------------------------------------|
| Maximum clock frequency | $f_{\max}$       | Clock  | Q       | 30   | 40   | —    | MHz  | $C_L = 15\text{ pF}$ ,<br>$R_L = 2\text{ k}\Omega$ |
| Propagation delay time  | $t_{\text{PHL}}$ | Clear  | Q       | —    | 23   | 35   | ns   |                                                    |
|                         | $t_{\text{PLH}}$ | Clock  | Q       | —    | 20   | 30   |      |                                                    |
|                         | $t_{\text{PHL}}$ | Clock  | Q       | —    | 21   | 30   |      |                                                    |

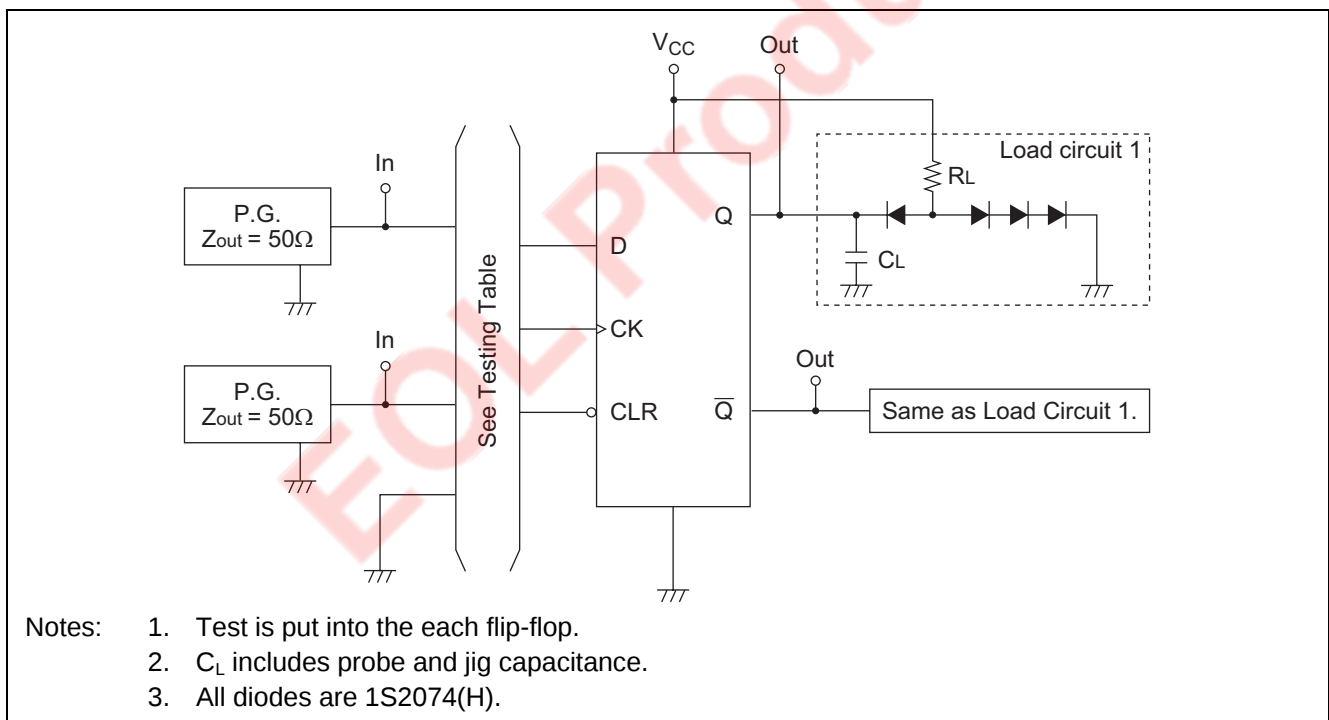
## • HD74LS175

(V<sub>CC</sub> = 5 V, Ta = 25°C)

| Item                    | Symbol           | Inputs | Outputs           | min. | typ. | max. | Unit | Condition                                        |
|-------------------------|------------------|--------|-------------------|------|------|------|------|--------------------------------------------------|
| Maximum clock frequency | $f_{\max}$       | Clock  | Q, $\overline{Q}$ | 30   | 40   | —    | MHz  | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 2 kΩ |
| Propagation delay time  | t <sub>PLH</sub> | Clear  | $\overline{Q}$    | —    | 16   | 25   | ns   |                                                  |
|                         | t <sub>PHL</sub> |        | Q                 | —    | 20   | 30   |      |                                                  |
|                         | t <sub>PLH</sub> | Clock  | Q, $\overline{Q}$ | —    | 13   | 25   |      |                                                  |
|                         | t <sub>PHL</sub> | Clock  | Q, $\overline{Q}$ | —    | 16   | 25   |      |                                                  |

## Testing Method

## Test Circuit

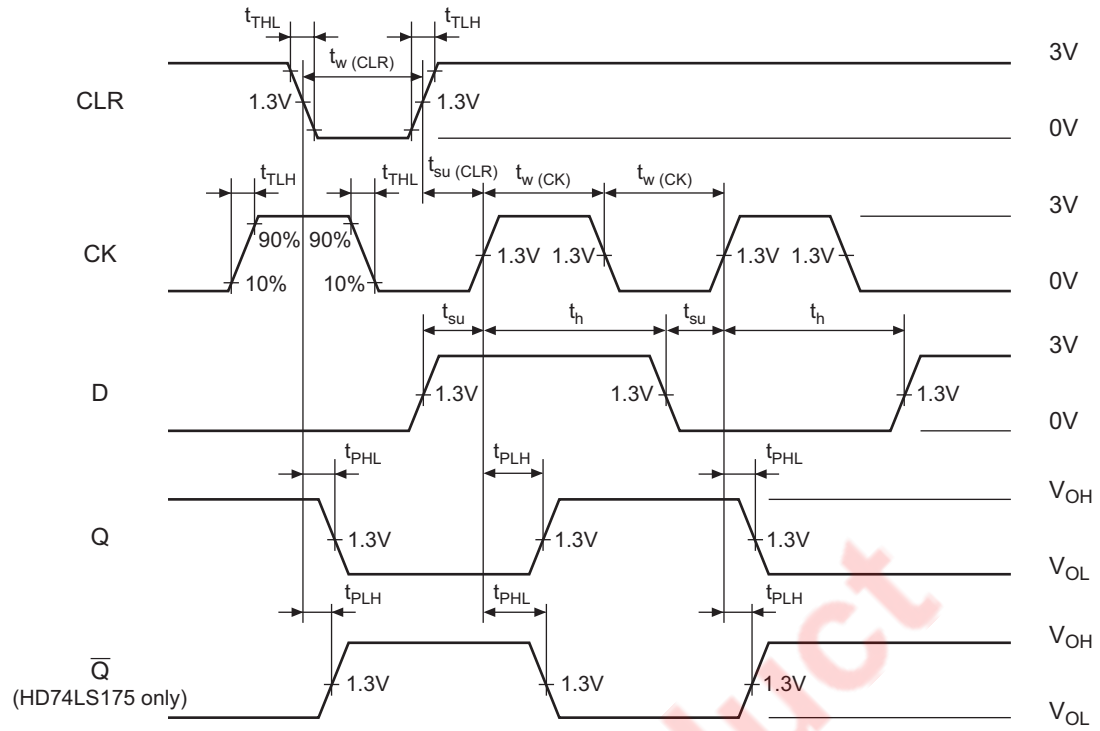


## Testing Table

| Item             | From input to output | Inputs |    |       | Outputs |           |
|------------------|----------------------|--------|----|-------|---------|-----------|
|                  |                      | CLR    | CK | D     | Q       | $\bar{Q}$ |
| $f_{\max}$       | CK→Q, $\bar{Q}^*$    | 4.5 V  | IN | IN    | OUT     | OUT       |
| t <sub>PLH</sub> | CK→Q, $\bar{Q}^*$    | 4.5 V  | IN | IN    |         |           |
| t <sub>PHL</sub> | CLR→Q, $\bar{Q}^*$   | IN     | IN | 4.5 V |         |           |

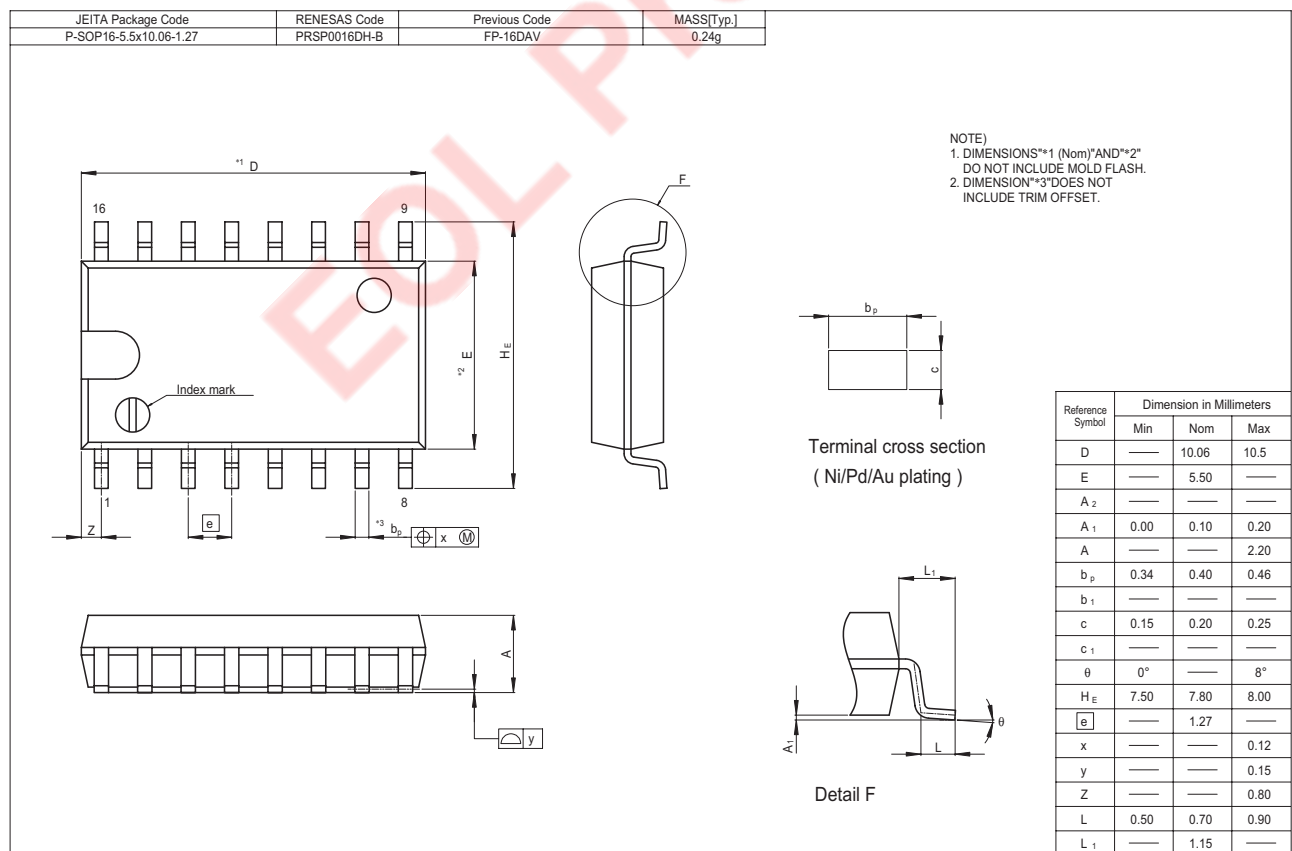
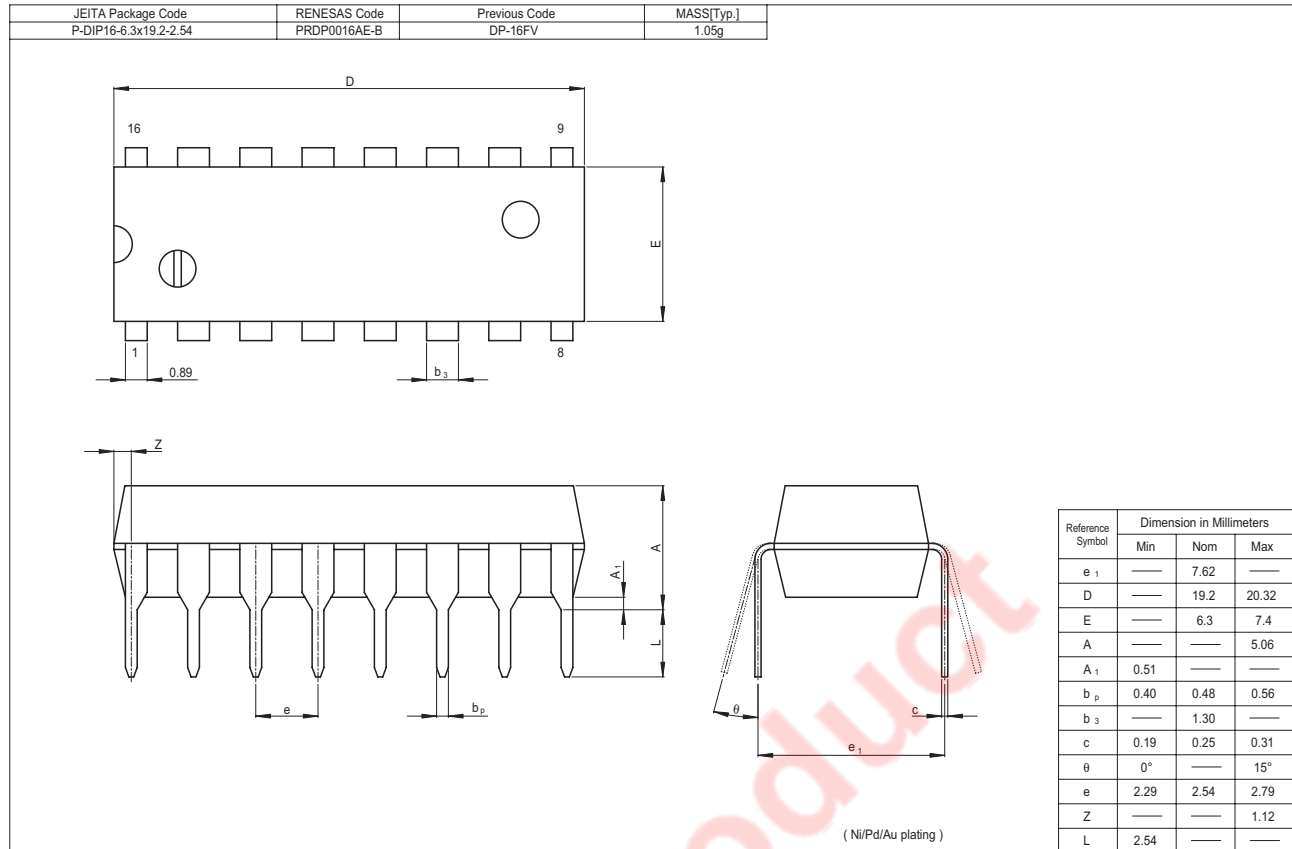
Note: \*. HD74LS175 only

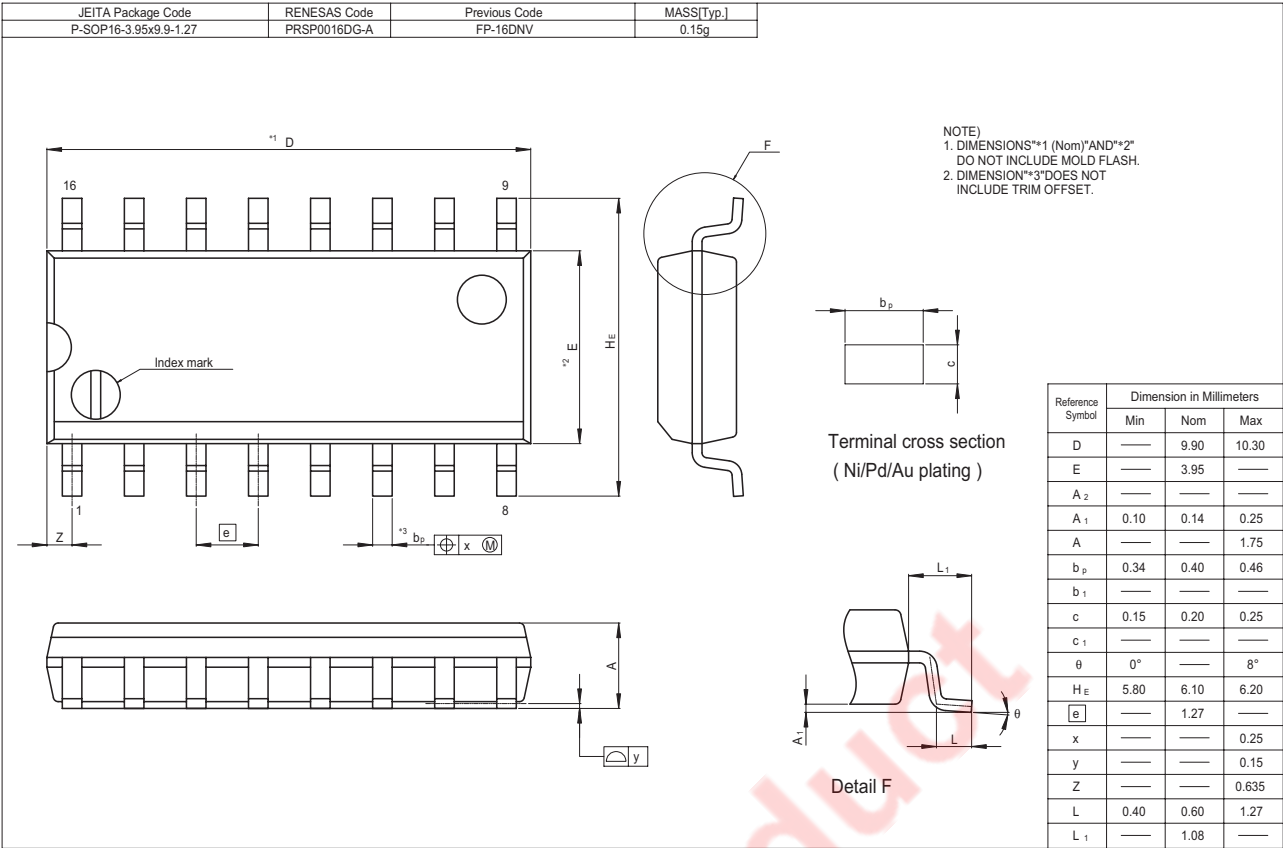
Waveform



Note: Input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, and: for  $f_{max}$ ,  $t_{TLH} = t_{THL} \leq 2.5$  ns.

# Package Dimensions





## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



### RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

#### **Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A.  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

#### **Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

#### **Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

#### **Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

#### **Renesas Technology (Shanghai) Co., Ltd.**

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

#### **Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

#### **Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

#### **Renesas Technology Malaysia Sdn. Bhd.**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510