

HD74HC668, HD74HC669

Synchronous UP/Down Decade Counter Synchronous Up/Down 4-bit binary Counter

REJ03D0638-0200
(Previous ADE-205-520)
Rev.2.00
Mar 30, 2006

Description

This synchronous presettable decade counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters.

A buffered clock input triggers the four master-slave flip-flops on the rising (positive going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\bar{P}$ and $\bar{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. when the input is high, the counter counts up; when low, it counts down. Input $\bar{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\bar{P}$ or $\bar{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable $\bar{P}$, Enable $\bar{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

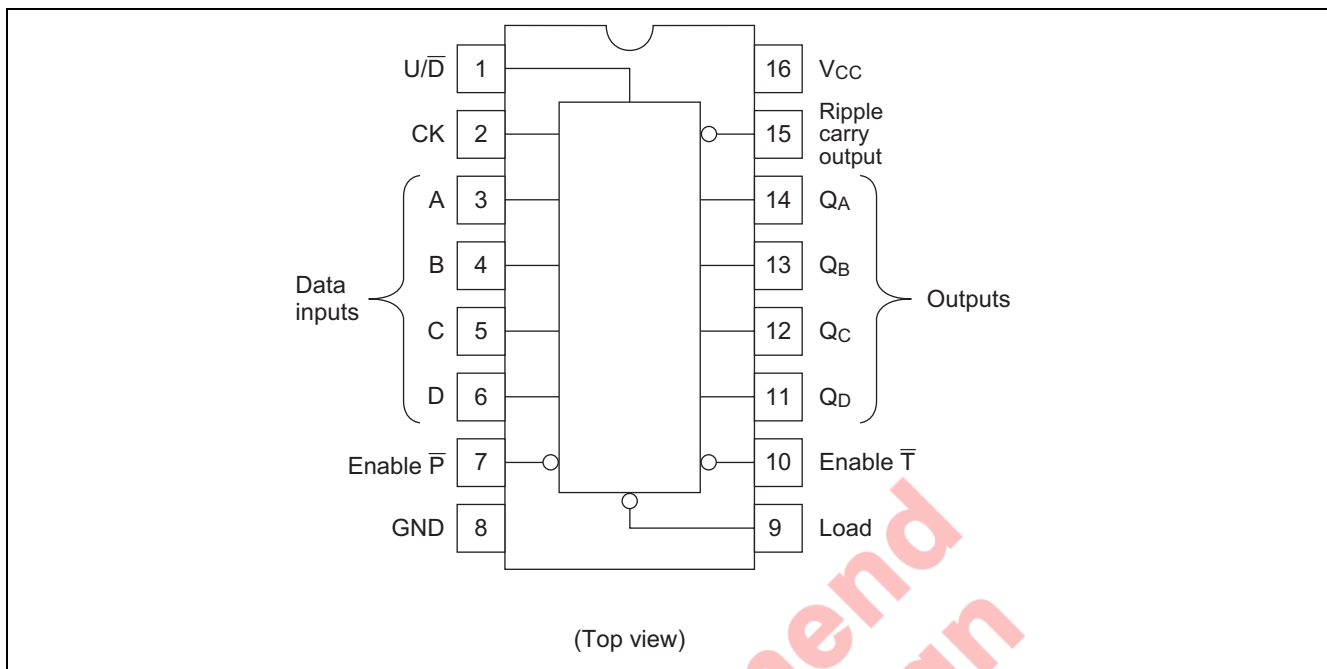
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max ($T_a = 25^\circ C$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC669P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC669FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC668RPEL HD74HC669RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (1,000 pcs/reel)

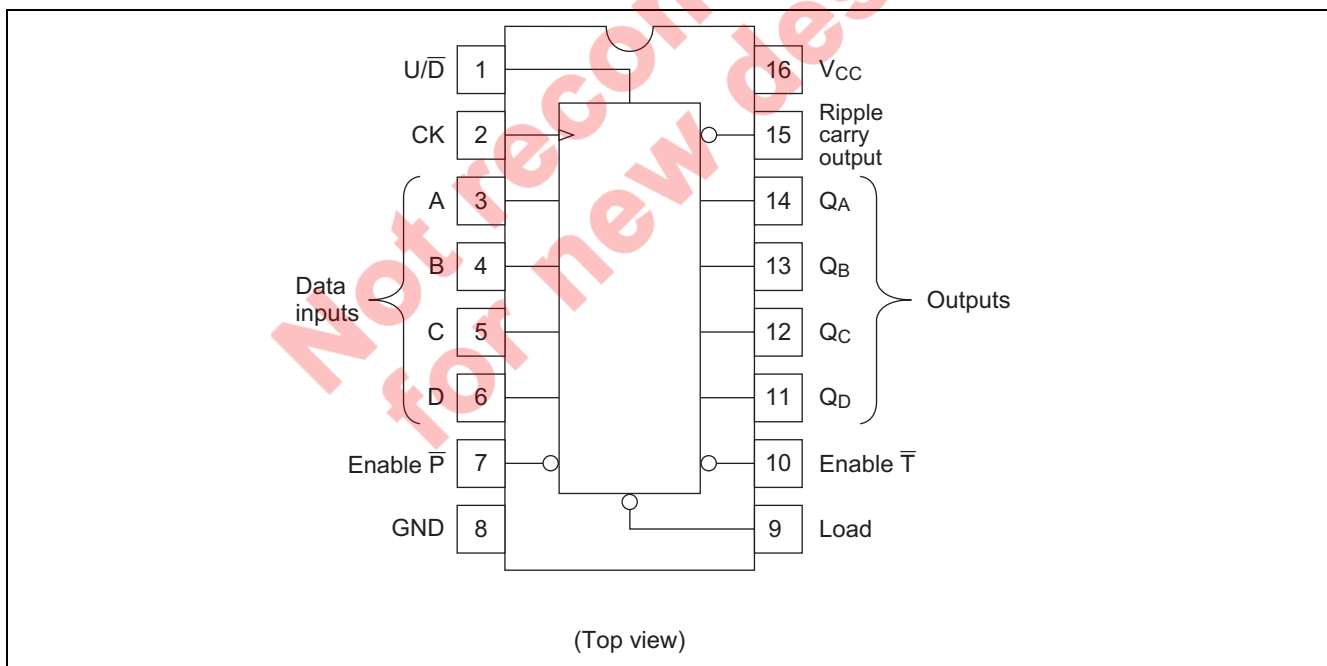
Note: Please consult the sales office for the above package availability.

Pin Arrangement

HD74HC668

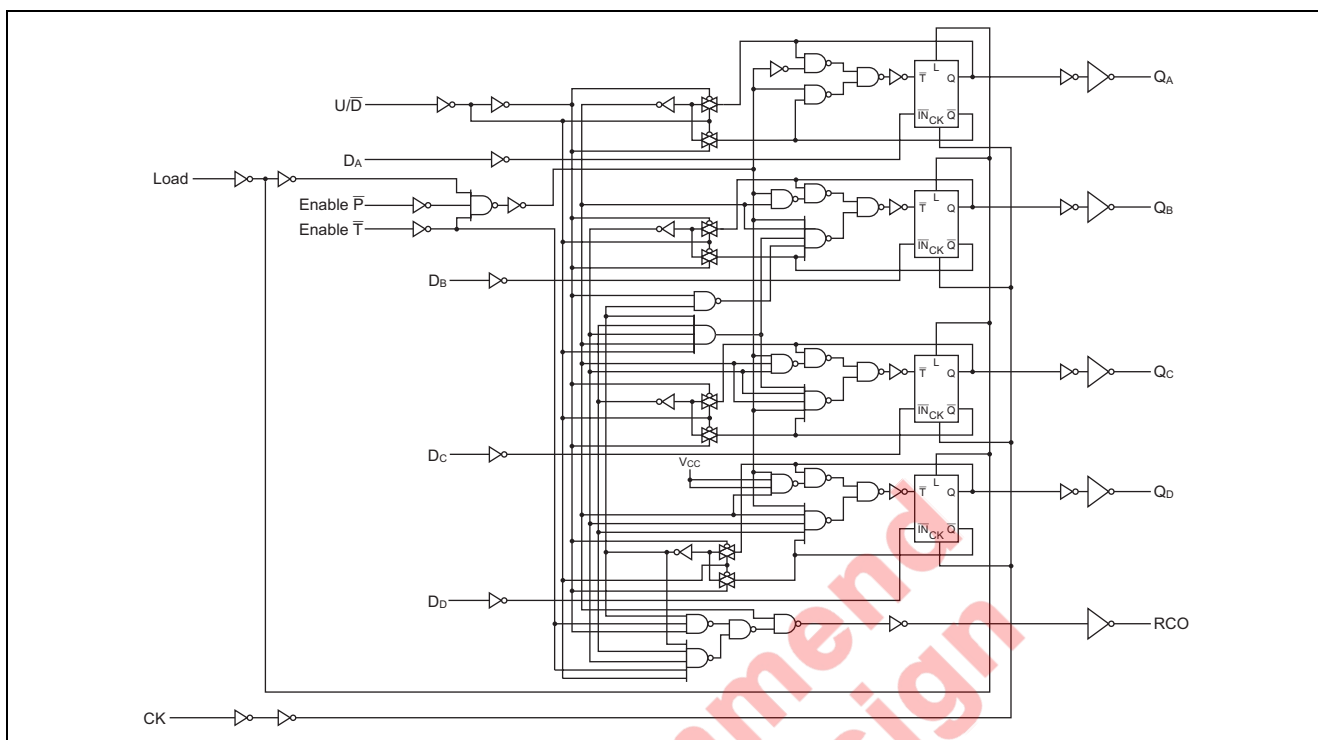


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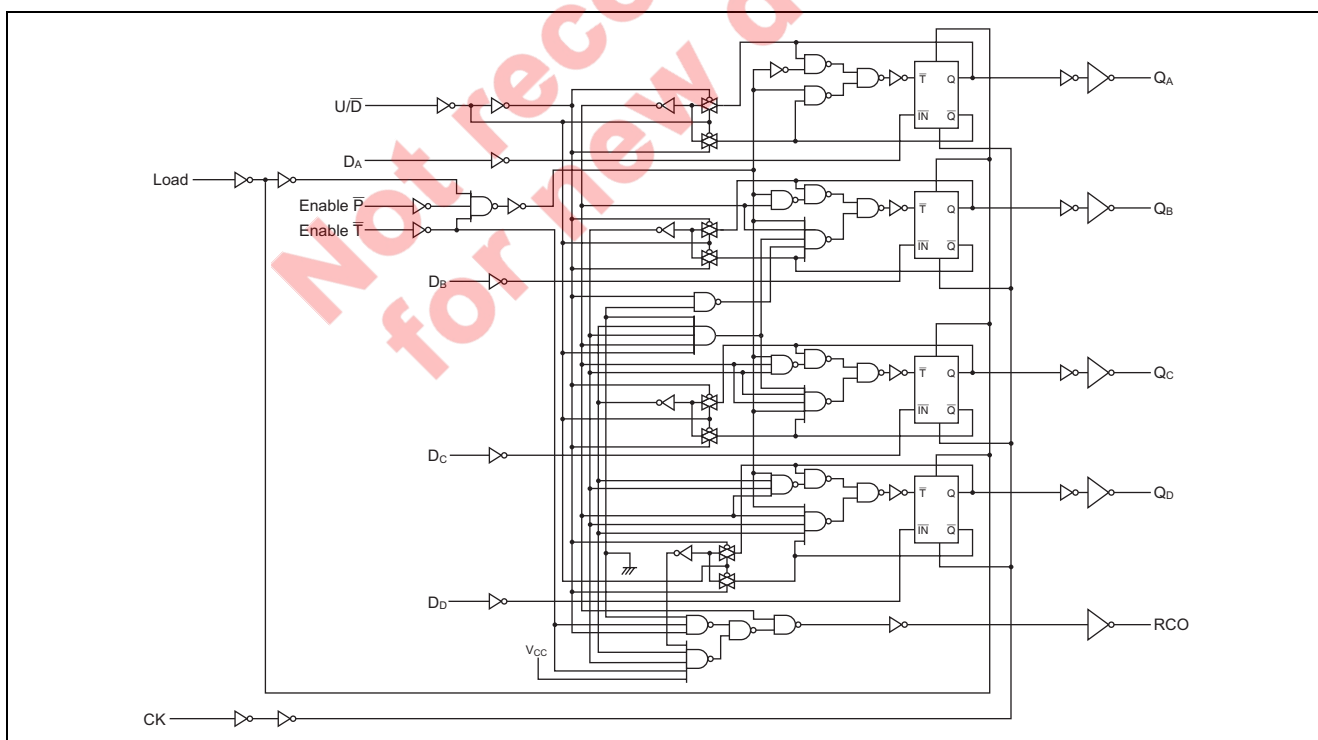


Logic Diagram

HD74HC668

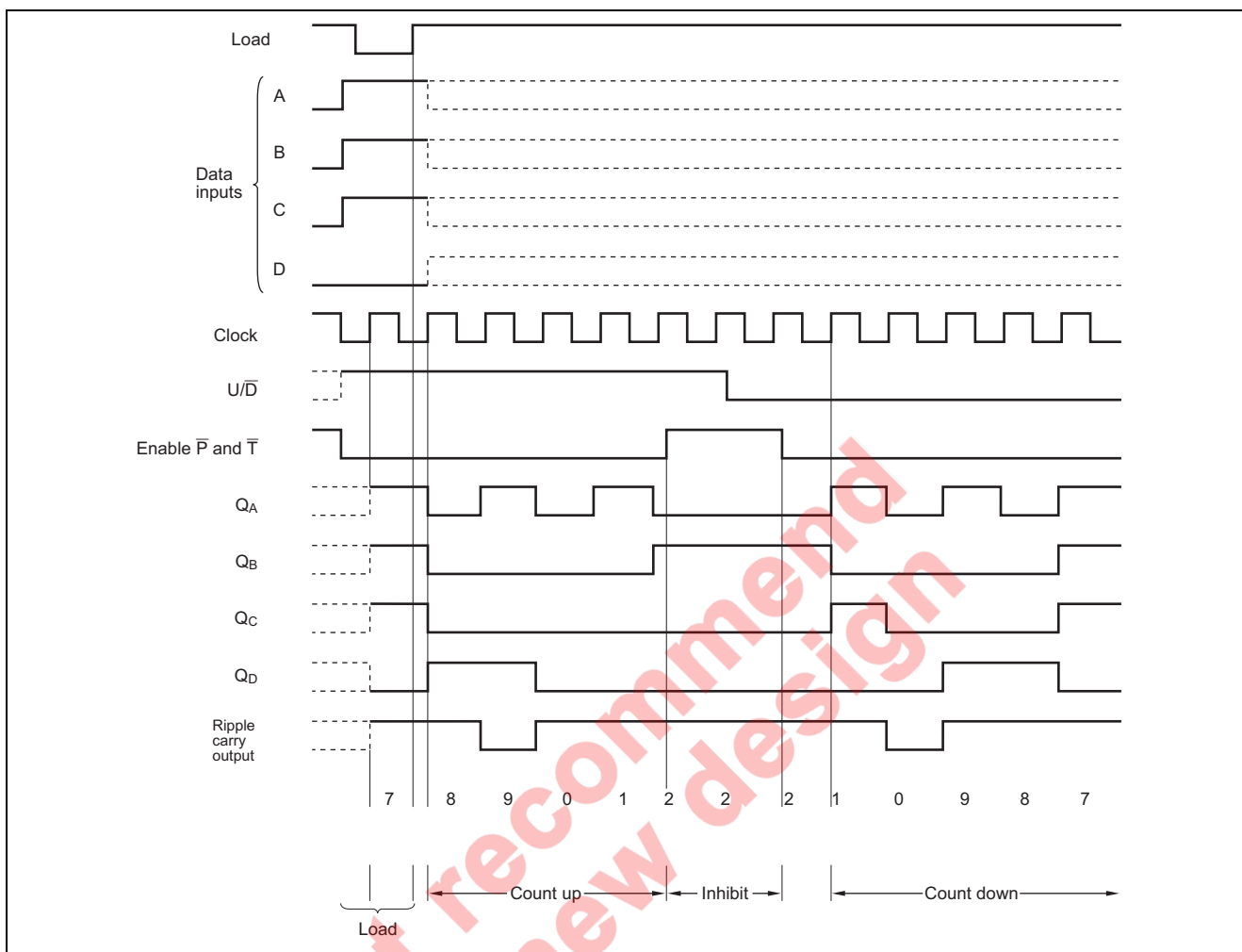


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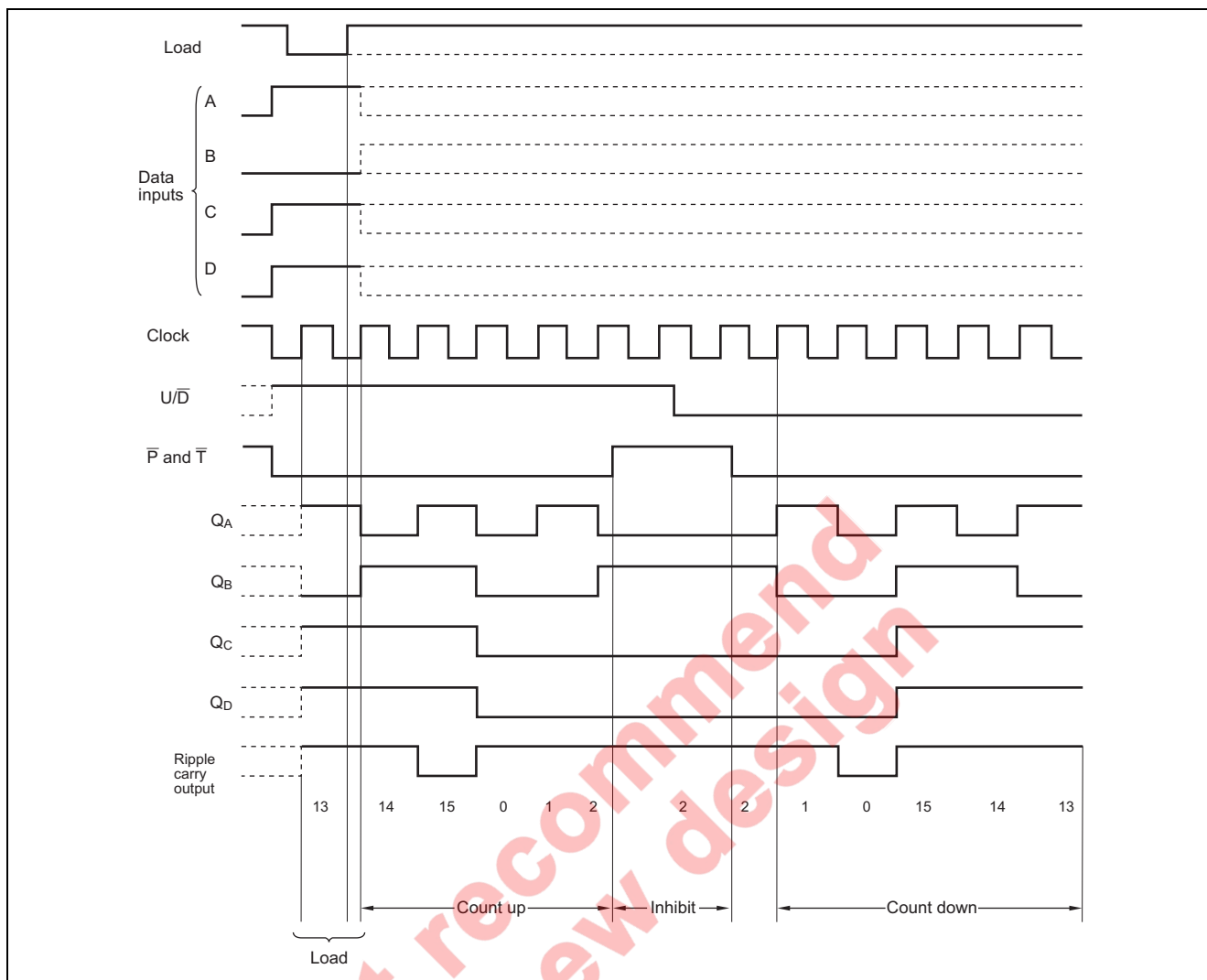


Timing Chart

HD74HC668



HD74HC669



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

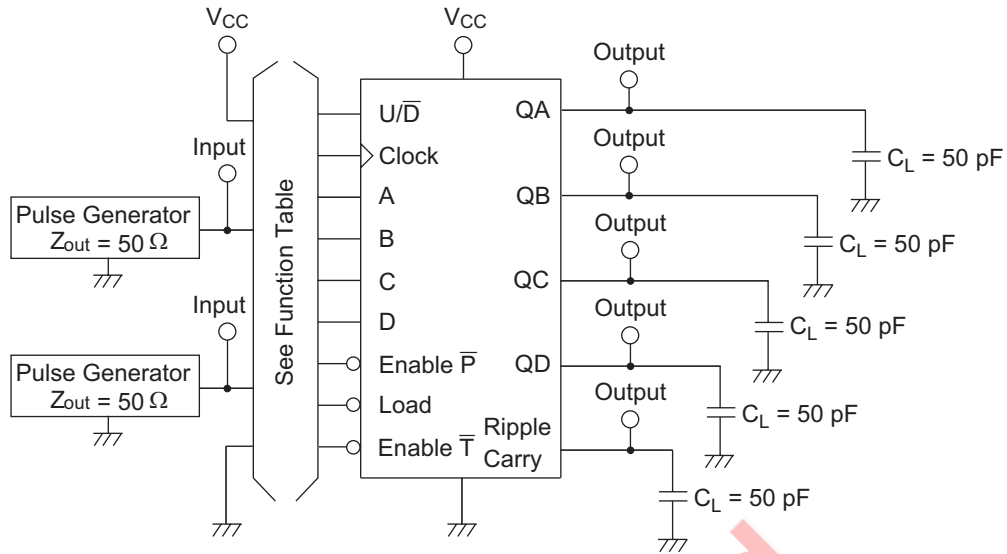
Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = VIH or VIL	IOH = -20 μA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—	IOH = -4 mA		
		6.0	5.68	—	—	5.63	—	IOH = -5.2 mA		
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = VIH or VIL	IOL = 20 μA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33	IOL = 4 mA		
		6.0	—	—	0.26	—	0.33	IOL = 5.2 mA		
Input current	Iin	6.0	—	—	±0.1	—	±1.0	μA	Vin = VCC or GND	
Quiescent supply current	ICC	6.0	—	—	4.0	—	40	μA	Vin = VCC or GND, Iout = 0 μA	

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock Frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	Clock to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	225	—	280	ns	Clock to Q
		4.5	—	—	45	—	56		
		6.0	—	—	38	—	48		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	190	ns	Enable $\bar{T}$ to Ripple carry out
		4.5	—	—	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	$U/\bar{D}$ to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	150	—	—	190	—	ns	Enable $\bar{P}$, $\bar{T}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	t_{su}	2.0	150	—	—	190	—	ns	Loadk to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	t_{su}	2.0	150	—	—	190	—	ns	$U/\bar{D}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

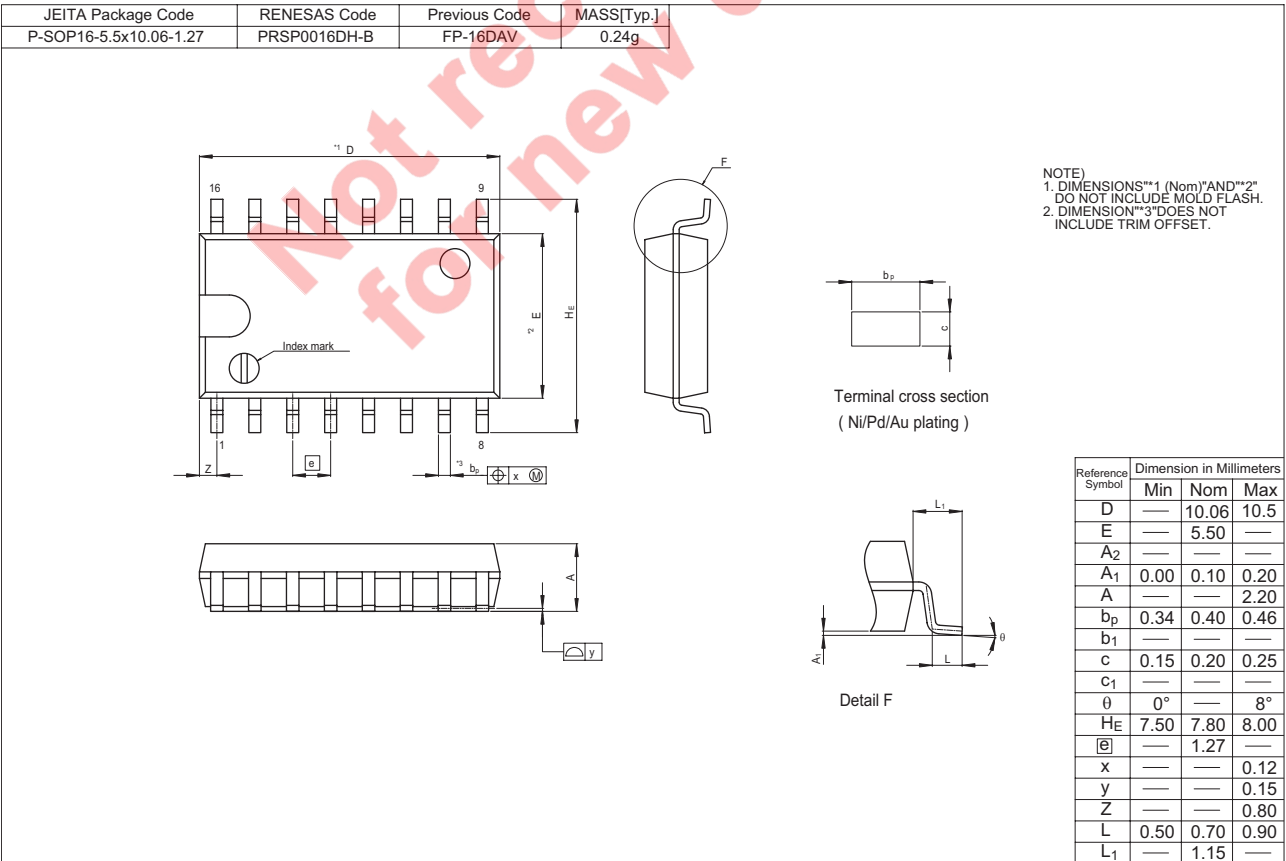
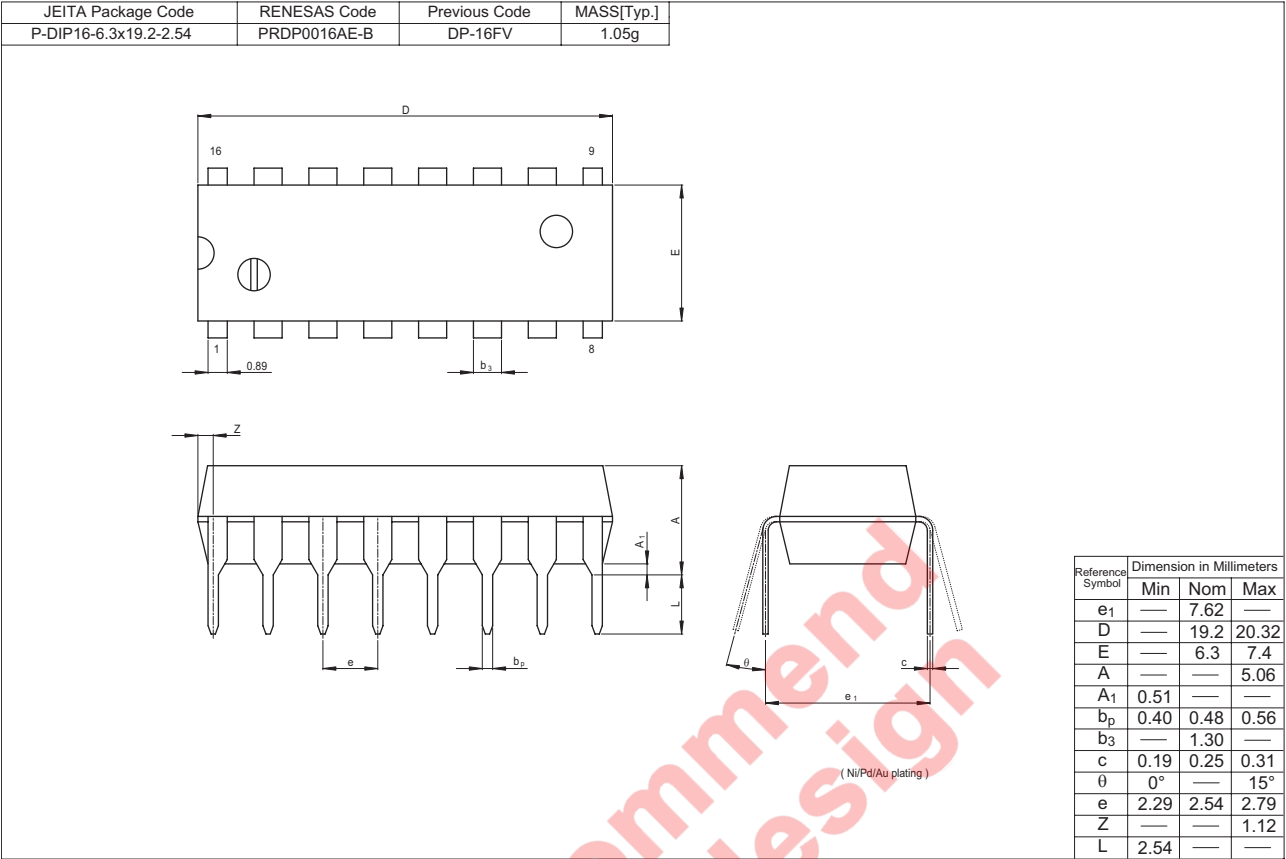
Test Circuit



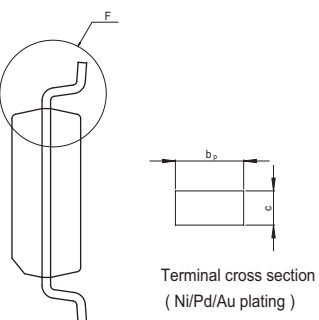
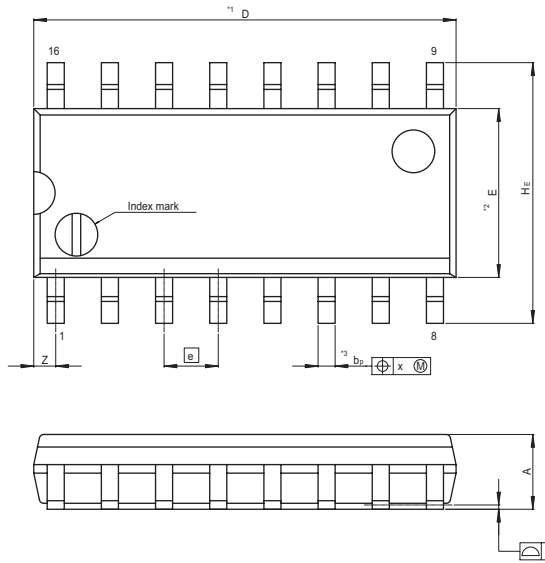
Note : 1. C_L includes probe and jig capacitance.

Not recommended
for new design

Package Dimensions



JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)
1. DIMENSIONS**1 (Nom)**AND**2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A ₂	—	—	—
A ₁	0.10	0.14	0.25
A	—	—	1.75
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
C ₁	—	—	—
θ	0°	—	8°
HE	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L ₁	—	1.08	—

Not recommended
for new design

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Renesas Technology America, Inc.

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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510