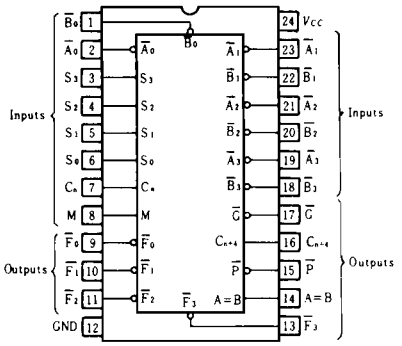
HD74HC181 ● Arithmetic Logic Unit/Function Generator

Preliminary

■ FEATURES

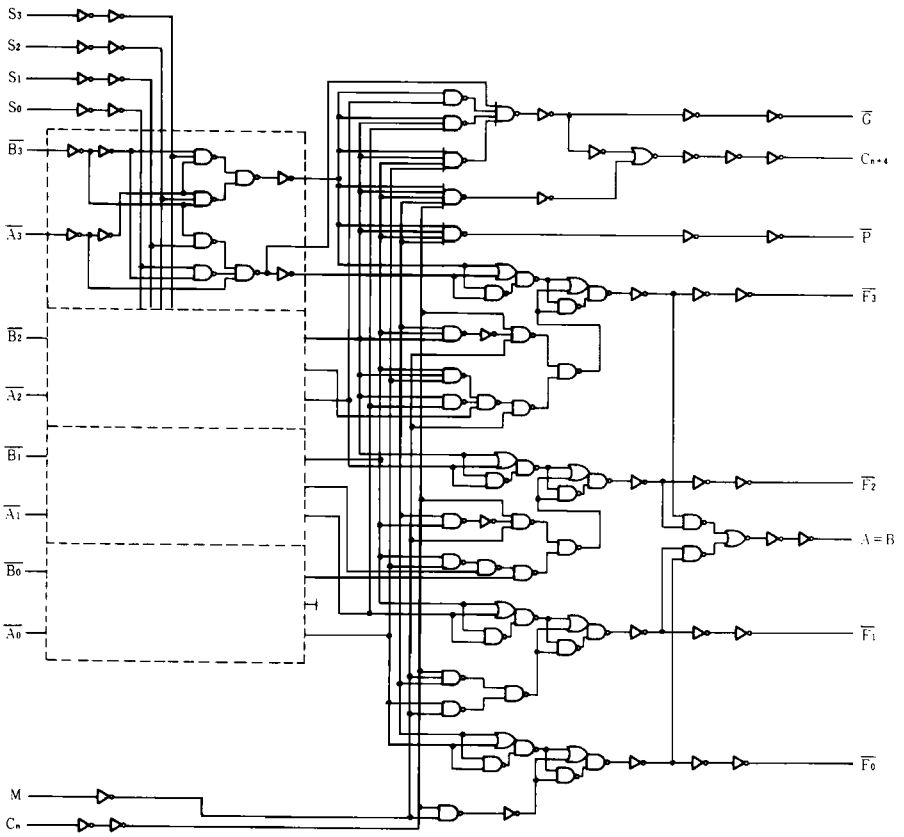
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



NOTE

The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

The HD74HC181 is arithmetic logic unit (ALU)/function generator that have a complexity of 75 equivalent gates. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Function Table (Table 1 and 2).

These operations are selected by the four function-select lines (S_0, S_1, S_2, S_3) and include addition, subtraction, decrement, and straight transfer.

When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M).

A full carry look-ahead scheme is made available in this device for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the HD74HC182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The HD74HC181 will accommodate active-high or active-low data if the pin designations are interpreted as follows.

Pin No.	2	1	23	22	21	20	19	18
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3
Active-low data (Table 2)	$\bar{A}_0$	$\bar{B}_0$	$\bar{A}_1$	$\bar{B}_1$	$\bar{A}_2$	$\bar{B}_2$	$\bar{A}_3$	$\bar{B}_3$
Pin No.	9	10	11	13	7	16	15	17
Active-high data (Table 1)	F_0	F_1	F_2	F_3	$\bar{C}_n$	$\bar{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	C_n	C_{n+4}	$\bar{P}$	$\bar{G}$

The HD74HC181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing this comparison. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively.

Input Cn	Output C_{n+4}	Active-high data (Table 1)	Active-low data (Table 2)
H	H	A ≦ B	A ≧ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≧ B	A ≦ B

This circuit have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Table 1 and 2 and include exclusive-OR, NAND, AND NOR, and OR functions.

- Signal Designations

The HD74HC181 together with the HD74HC182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators and the bars over the terminal letter symbols (e.g. $\bar{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\bar{C}$ means "do carry" while a high means "to not carry". The logic functions and arithmetic operations of Figure 2 are given in Table 2.

Figure 1

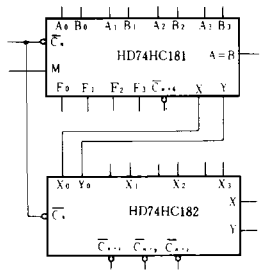
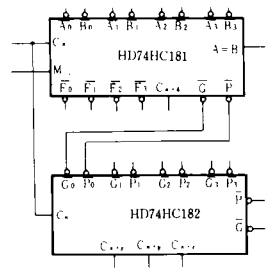


Figure 2



■PIN DESIGNATIONS

Item	Functions
$\bar{A}_3$, $\bar{A}_2$, $\bar{A}_1$, $\bar{A}_0$	Word A Inputs
B_3, B_2, B_1, B_0	Word B Inputs
S_3, S_2, S_1, S_0	Function-Select Inputs
C_n	Ripple-Carry Input
M	Mode Control Input
F_3, F_2, F_1, F_0	Function Outputs
A = B	Comparator Output
$\bar{P}$	Carry Propagate Output
$\overline{C_{n+4}}$	Ripple-Carry Output
$\bar{G}$	Carry Generate Output

■FUNCTION TABLE

● Table 1

S Inputs				Active-high data		
				M="H"	M="L" : Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	$\overline{C}_n$="H" (no carry)	$\overline{C}_n$="L" (with carry)
L	L	L	L	$F=\overline{A}$	F=A	F=A plus 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) plus 1
L	L	H	L	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ plus 1
L	L	H	H	F=0	F=minus 1 (2's compl)	F=Zero
L	H	L	L	$F=\overline{AB}$	$F=A$ plus $A\overline{B}$	$F=A$ plus $A\overline{B}$ plus 1
L	H	L	H	$F=\overline{B}$	$F=(A+B)$ plus $A\overline{B}$	$F=(A+B)$ plus $A\overline{B}$ plus 1
L	H	H	L	$F=A\oplus B$	F=A minus B minus 1	F=A minus B
L	H	H	H	$F=A\overline{B}$	$F=A\overline{B}$ minus 1	$F=A\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A plus AB	F=A plus AB plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	$F=(A+\overline{B})$ plus AB	$F=(A+\overline{B})$ plus AB plus 1
H	L	H	H	F=AB	F=AB minus 1	F=AB
H	H	L	L	F=1	F=A plus A*	F=A plus A plus 1
H	H	L	H	$F=A+\overline{B}$	$F=(A+B)$ plus A	$F=(A+B)$ plus A plus 1
H	H	H	L	F=A+B	$F=(A+\overline{B})$ plus A	$F=(A+\overline{B})$ plus A plus 1
H	H	H	H	F=A	F=A minus 1	F=A

Notes) H; high level, L; low level

* Each bit is shifted to the next more significant position.

● Table 2

S Inputs				Active-low data		
				M="H"	M="L" : Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	C_n="L" (no carry)	C_n="H" (with carry)
L	L	L	L	$F=\overline{A}$	F=A minus 1	F=A
L	L	L	H	$F=\overline{AB}$	F=AB minus 1	F=AB
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ minus 1	$F=A\overline{B}$
L	L	H	H	F=1	F=minus 1 (2's compl)	F=0
L	H	L	L	$F=\overline{A+B}$	F=A plus $(A+\overline{B})$	F=A plus $(A+\overline{B})$ plus 1
L	H	L	H	$F=\overline{B}$	F=AB plus $(A+\overline{B})$	F=AB plus $(A+\overline{B})$ plus 1
L	H	H	L	$F=\overline{A\oplus B}$	F=A minus B minus 1	F=A minus B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	$F=(A+\overline{B})$ plus 1
H	L	L	L	$F=\overline{A}B$	F=A plus $(A+B)$	F=A plus $(A+B)$ plus 1
H	L	L	H	$F=A\oplus B$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	$F=A\overline{B}$ plus $(A+B)$	$F=A\overline{B}$ plus $(A+B)$ plus 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) plus 1
H	H	L	L	F=0	F=A plus A*	F=A plus A plus 1
H	H	L	H	$F=A\overline{B}$	F=AB plus A	F=AB plus A plus 1
H	H	H	L	F=AB	$F=A\overline{B}$ plus A	$F=A\overline{B}$ plus A plus 1
H	H	H	H	F=A	F=A	F=A plus 1

* Each bit is shifted to the next more significant position.

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	C_n to C_{n+4}	—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
		2.0	C_n to any F	—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
		2.0	A or B to G $S_0=S_3=V_{CC}$, $S_1=S_2=$GND	—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
		2.0	A or B to G $S_0=S_3=$GND, $S_1=S_2=V_{CC}$	—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	23	
		2.0	A or B to P	—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
		2.0	A_1 or B_1 to F_1 $S_0=S_3=V_{CC}$, $S_1=S_2=$GND	—	—	240	—	300	ns
		4.5		—	—	48	—	60	
		6.0		—	—	41	—	51	
		2.0	A or B to C_{n+4} $S_0=S_3=V_{CC}$, $S_1=S_2=$GND	—	—	250	—	315	ns
		4.5		—	—	50	—	63	
		6.0		—	—	43	—	54	
		2.0	A_1 or B_1 to F_1 $S_1=S_2=V_{CC}$ or M=V_{CC}	—	—	275	—	345	ns
		4.5		—	—	55	—	69	
		6.0		—	—	47	—	59	
		2.0	A or B to A=B	—	—	280	—	350	ns
		4.5		—	—	56	—	70	
		6.0		—	—	48	—	60	
		2.0	A or B to C_{n+4} $S_0=S_3=$GND, $S_1=S_2=V_{CC}$	—	—	280	—	350	ns
		4.5		—	—	56	—	70	
		6.0		—	—	48	—	60	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	—	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF