

# HD74CBT3257

4-bit 1-of-2 FET Multiplexer / Demultiplexer

HITACHI

ADE-205-624B (Z)

Rev. 2  
Nov. 2001

## Description

The HD74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer / demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output enable ( $\overline{OE}$ ) and select control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

## Features

- Minimal propagation delay through the switch.
- 5  $\Omega$  switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.  
-Ideally suited for notebook applications.
- Package type

Product code example: HD74CBT3257TELL

Package type	Package code	Package suffix	Taping code
TSSOP-16pin	TTP-16DA	T	ELL(2000pcs / Reel)

Notes: 1. As for the Pb-free package is attached the “V” to the end of package code.  
2. As for the Pb-free product is attached the “-E” to the end of product code.



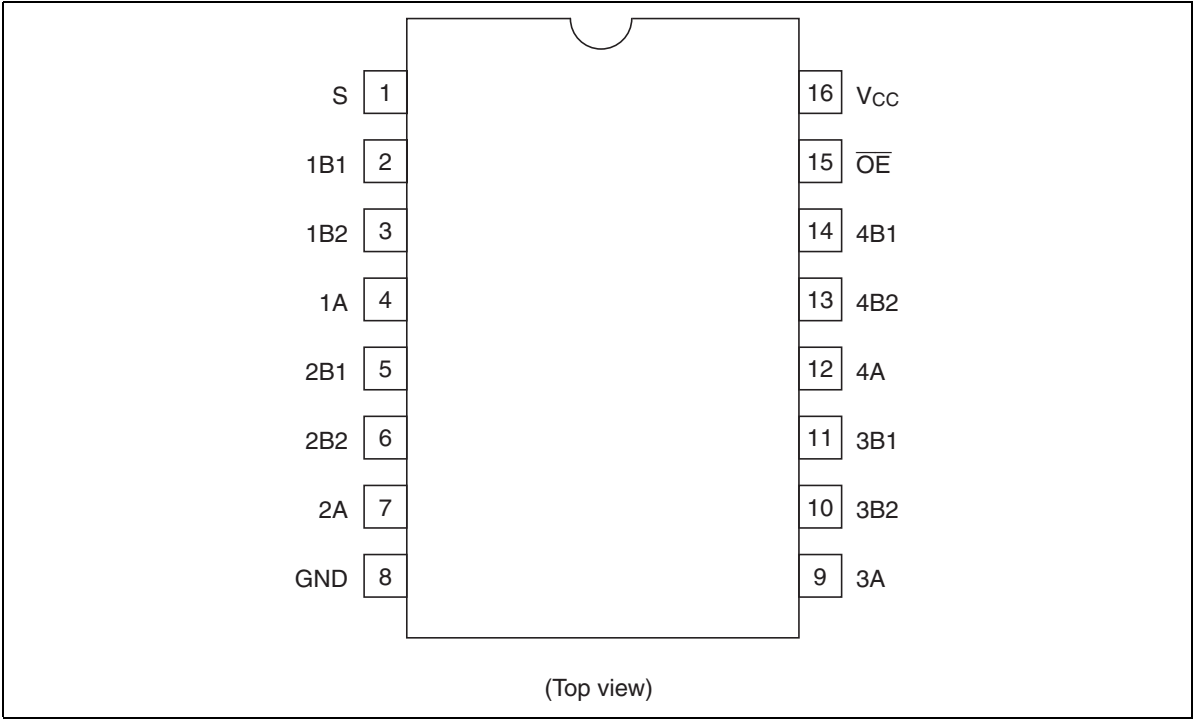
Function Table

Inputs

$\overline{OE}$	S	Function
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

H: High level  
L: Low level  
X: Immaterial

Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	−0.5 to 7.0	V	
Input voltage range <sup>*1</sup>	$V_I$	−0.5 to 7.0	V	
Input clamp current	$I_{IK}$	−50	mA	$V_I < 0$
Continuous output current	$I_O$	128	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	±100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) <sup>*2</sup>	$P_T$	500	mW	TSSOP
Storage temperature	$T_{stg}$	−65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

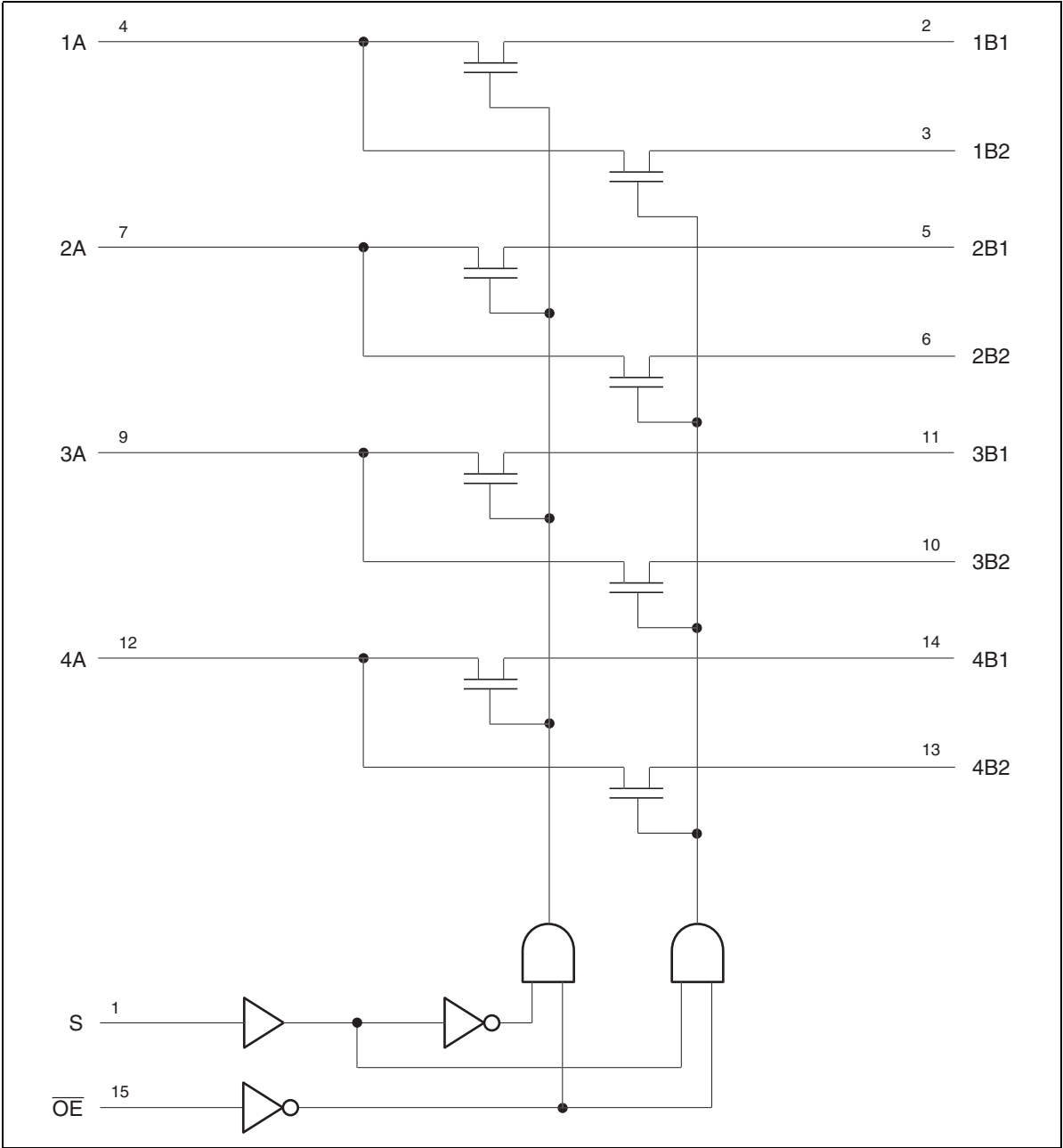
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	4.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_{IO}$	0	5.5	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	5	ns / V	$V_{CC} = 4.5$ to $5.5$ V
Operating free-air temperature	$T_a$	−40	85	°C	

Note: Unused or floating inputs must be held high or low.

Block Diagram



## DC Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>cc</sub> (V)	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Clamp diode voltage	V <sub>IK</sub>	4.5	—	—	-1.2	V	I <sub>IN</sub> = -18 mA
Input voltage	V <sub>IH</sub>	4.0 to 5.5	2.0	—	—	V	
	V <sub>IL</sub>	4.0 to 5.5	—	—	0.8		
On-state switch resistance <sup>*2</sup>	R <sub>ON</sub>	4.0	—	14	20	Ω	V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA Typ at V <sub>CC</sub> = 4.0 V
		4.5	—	5	7		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA
		4.5	—	5	7		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA
		4.5	—	10	15		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1.0	μA	V <sub>IN</sub> = 5.5 V or GND
Off-state leakage current	I <sub>OZ</sub>	5.5	—	—	±1.0	μA	0 ≤ A, B ≤ V <sub>CC</sub>
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	3	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 mA
Increase in I <sub>CC</sub> per input <sup>*3</sup>	ΔI <sub>CC</sub>	5.5	—	—	2.5	mA	One input at 3.4 V, other inputs at V <sub>CC</sub> or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## Capacitance

(Ta = 25°C)

Item	Symbol	V <sub>cc</sub> (V)	Min	Typ	Max	Unit	Test conditions
Control input capacitance	C <sub>IN</sub>	5.0	—	3.5	—	pF	V <sub>IN</sub> = 0 or 3 V
Input / output capacitance	A port	C <sub>I/O (OFF)</sub>	5.0	9	—	pF	V <sub>O</sub> = 0 or 3 V
	B port		5.0	5	—		OE = V <sub>CC</sub>

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

(Ta = -40 to 85°C)

- V<sub>CC</sub> = 4.0 V

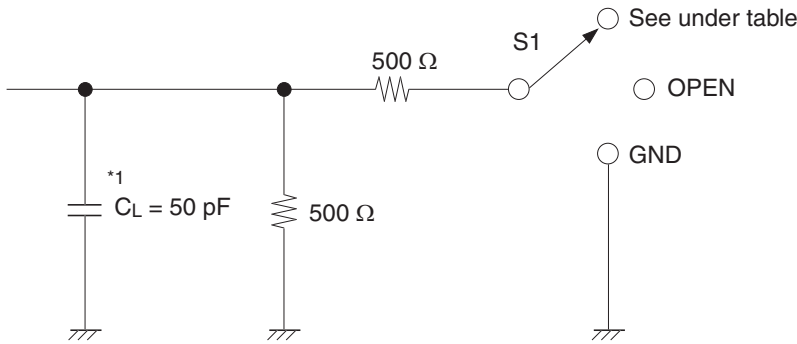
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time <sup>1)</sup>	t <sub>PLH</sub> t <sub>PHL</sub>	—	0.35	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	A or B	B or A
Propagation delay time	t <sub>PLH</sub> t <sub>PHL</sub>	—	5.5	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A
Enable time	t <sub>ZH</sub>	—	5.7	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	B
	t <sub>ZL</sub>	—	5.6			$\overline{\text{OE}}$	A or B
Disable time	t <sub>HZ</sub>	—	5.2	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	B
		—	5.5			$\overline{\text{OE}}$	A or B
	t <sub>LZ</sub>	—	5.2			S	B
		—	6.4			$\overline{\text{OE}}$	A or B

- V<sub>CC</sub> = 5.0±0.5 V

Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time <sup>1)</sup>	t <sub>PLH</sub> t <sub>PHL</sub>	—	0.25	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	A or B	B or A
Propagation delay time	t <sub>PLH</sub> t <sub>PHL</sub>	1.6	5.0	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A
Enable time	t <sub>ZH</sub>	1.6	5.2	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	B
	t <sub>ZL</sub>	1.8	5.1			$\overline{\text{OE}}$	A or B
Disable time	t <sub>HZ</sub>	1.0	5.0	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	B
		2.2	5.5			$\overline{\text{OE}}$	A or B
	t <sub>LZ</sub>	1.0	5.0			S	B
		2.2	6.8			$\overline{\text{OE}}$	A or B

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Test Circuit

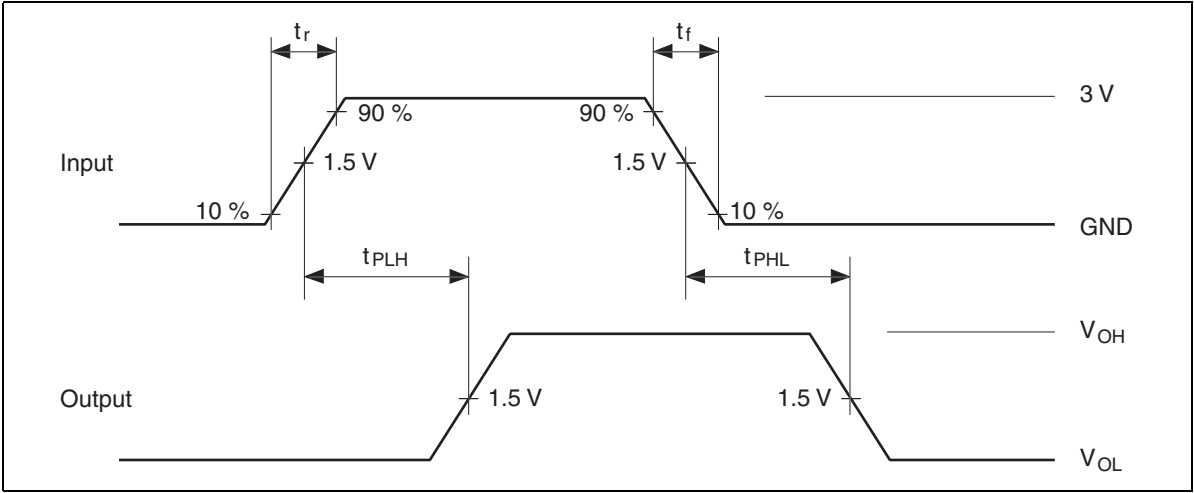


Load circuit for outputs

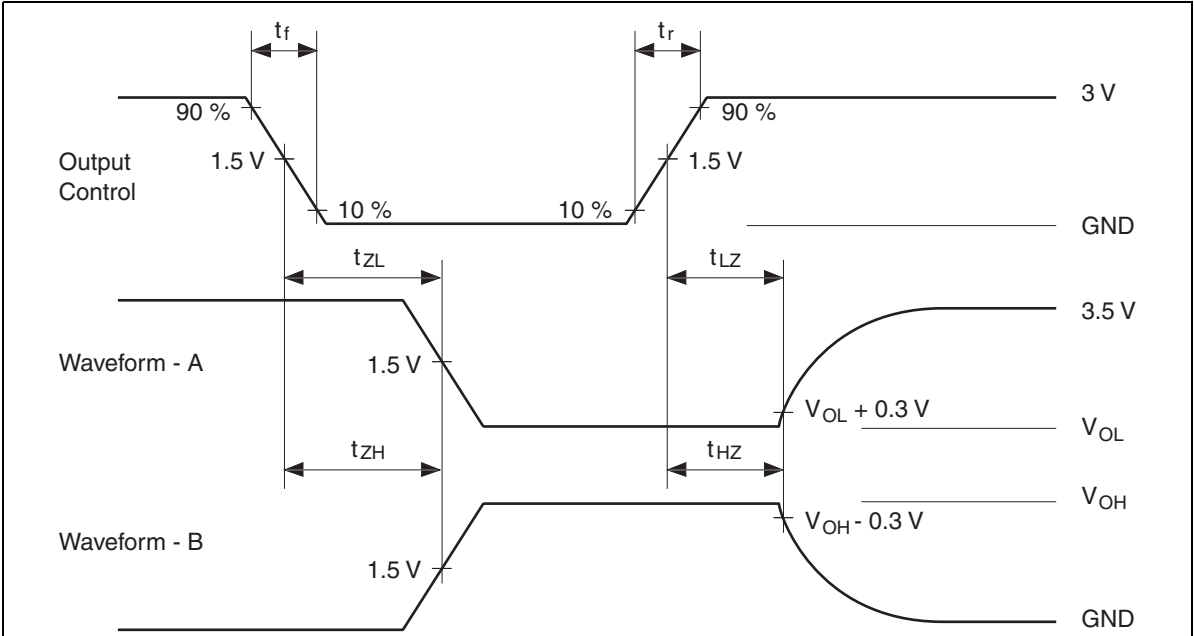
Symbol	S1
t <sub>PLH</sub> / t <sub>PHL</sub>	OPEN
t <sub>ZH</sub> / t <sub>HZ</sub>	OPEN
t <sub>ZL</sub> / t <sub>LZ</sub>	7 V

Note: 1. C<sub>L</sub> includes probe and jig capacitance.

Waveforms – 1



Waveforms – 2

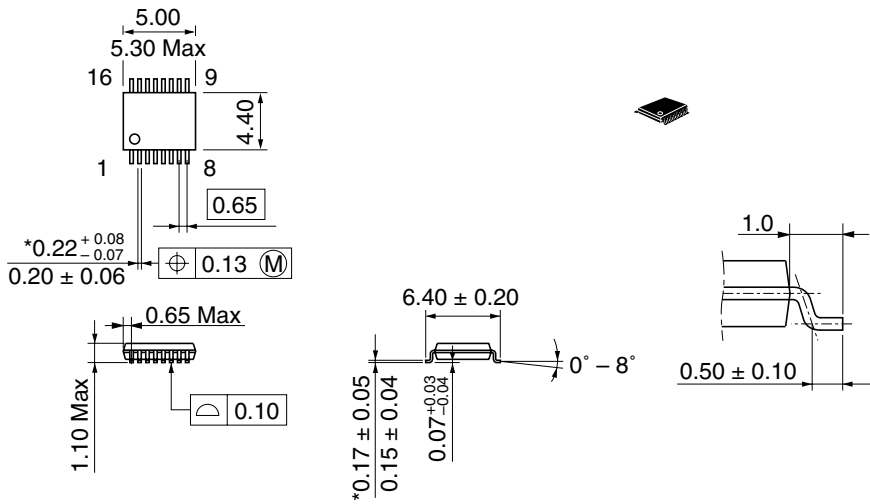


- Notes:
1. All input pulses are supplied by generators having the following characteristics :  
PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.



Package Dimensions

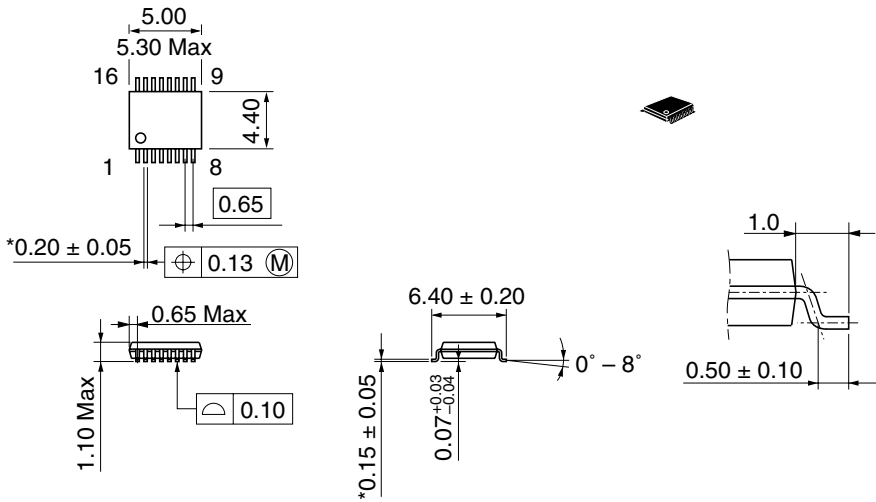
As of July, 2001  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

As of July, 2001  
Unit: mm



\*Pd plating

Hitachi Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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