
HD74ALVCH162500

18-bit Universal Bus Transceivers with 3-state Outputs

HITACHI

ADE-205-181 (Z)
Preliminary
1st. Edition
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Description

Data flow in each direction is controlled by output enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A to B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ is high. When $\overline{\text{LEAB}}$ is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If $\overline{\text{LEAB}}$ is low, the A bus data is stored in the latch flip flop on the high to low transition of $\overline{\text{CLKAB}}$. Output enable $\overline{\text{OEAB}}$ is active high. When $\overline{\text{OEAB}}$ is high, the B port outputs are active. When $\overline{\text{OEAB}}$ is low, the B port outputs are in the high impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$. The output enables are complementary ($\overline{\text{OEAB}}$ is active high, and $\overline{\text{OEBA}}$ is active low). Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- $V_{\text{CC}} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ ($@V_{\text{CC}} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ ($@V_{\text{CC}} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 12 \text{ mA}$ ($@V_{\text{CC}} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

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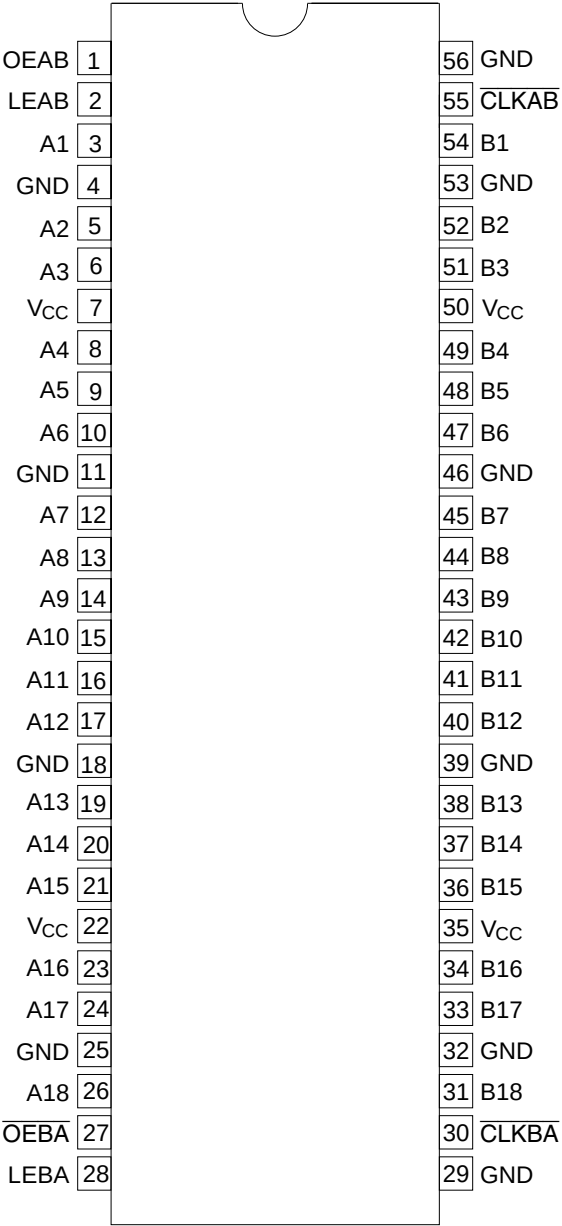
Function Table ^{*3}

Inputs				Output B
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ^{*1}
H	L	L	X	B ₀ ^{*2}

H : High level
L : Low level
X : Immaterial
Z : High impedance
↓ : High to low transition

- Notes:
- 1. Output level before the indicated steady state input conditions were established.
 - 2. Output level before the indicated steady state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.
 - 3. A to B data flow is show; B to A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	−0.5 to 4.6	V	
Input voltage ^{*1, 2}	V_I	−0.5 to 4.6	V	Except I/O ports
		−0.5 to $V_{CC} + 0.5$		I/O ports
Output voltage ^{*1, 2}	V_O	−0.5 to $V_{CC} + 0.5$	V	
Input clamp current	I_{IK}	−50	mA	
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
		±100		
Maximum power dissipation at $T_a = 55^{\circ}\text{C}$ (in still air) ^{*3}	P_T	1	W	TSSOP
Storage temperature	T_{stg}	−65 to 150	$^{\circ}\text{C}$	

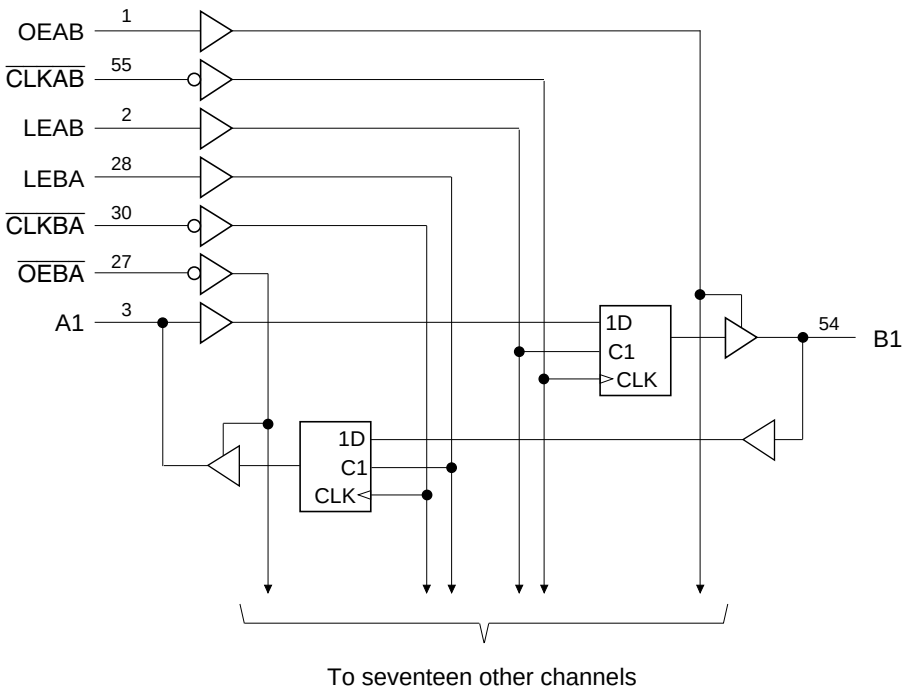
- Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	−6	mA	$V_{CC} = 2.3\text{ V}$
		—	−8		$V_{CC} = 2.7\text{ V}$
		—	−12		$V_{CC} = 3.0\text{ V}$
Low level output current	I_{OL}	—	6	mA	$V_{CC} = 2.3\text{ V}$
		—	8		$V_{CC} = 2.7\text{ V}$
		—	12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	−40	85	$^{\circ}\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics (Ta = –40 to 85°C)

Item	Symbol	V _{CC} (V) ^{*1}	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V _{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V _{OH}	Min to Max	V _{CC} –0.2	—	V	I _{OH} = –100 µA
		2.3	1.9	—		I _{OH} = –4 mA, V _{IH} = 1.7 V
		2.3	1.7	—		I _{OH} = –6 mA, V _{IH} = 1.7 V
		3.0	2.4	—		I _{OH} = –6 mA, V _{IH} = 2.0 V
		2.7	2.0	—		I _{OH} = –8 mA, V _{IH} = 2.0 V
		3.0	2.0	—		I _{OH} = –12 mA, V _{IH} = 2.0 V
	V _{OL}	Min to Max	—	0.2		I _{OL} = 100 µA
		2.3	—	0.4		I _{OL} = 4 mA, V _{IL} = 0.7 V
		2.3	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.7 V
		3.0	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.8 V
		2.7	—	0.6		I _{OL} = 8 mA, V _{IL} = 0.8 V
		3.0	—	0.8		I _{OL} = 12 mA, V _{IL} = 0.8 V
Input current	I _{IN}	3.6	—	±5	µA	V _{IN} = V _{CC} or GND
	I _{IN (hold)}	2.3	45	—		V _{IN} = 0.7 V
		2.3	–45	—		V _{IN} = 1.7 V
		3.0	75	—		V _{IN} = 0.8 V
		3.0	–75	—		V _{IN} = 2.0 V
		3.6	—	±500		V _{IN} = 0 to 3.6 V
Off state output current ^{*2}	I _{OZ}	3.6	—	±10	µA	V _{OUT} = V _{CC} or GND
Quiescent supply current	I _{CC}	3.6	—	40	µA	V _{IN} = V _{CC} or GND
	ΔI _{CC}	3.0 to 3.6	—	750	µA	V _{IN} = one input at (V _{CC} –0.6) V, other inputs at V _{CC} or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics (Ta = -40 to 85°C)

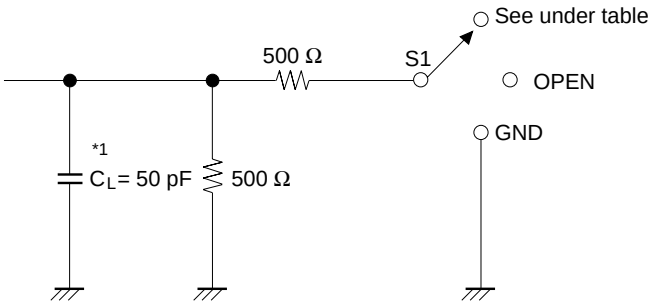
Item	Symbol	V _{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t _{PLH}	2.5±0.2	1.0	—	6.2	ns	A or B	B or A
		2.7	—	—	5.4			
		3.3±0.3	1.0	—	4.5			
	t _{PHL}	2.5±0.2	1.0	—	7.0		LEAB or LEBA	A or B
		2.7	—	—	6.2			
		3.3±0.3	1.0	—	5.3		CLKAB or CLKBA	A or B
		2.5±0.2	1.0	—	7.7			
		2.7	—	—	7.3			
		3.3±0.3	1.1	—	6.1			
Output enable time	t _{ZH}	2.5±0.2	1.0	—	6.7	ns	OEAB	B
		2.7	—	—	6.1			
		3.3±0.3	1.0	—	5.2			
	t _{ZL}	2.5±0.2	1.0	—	7.2		OEBA	A
		2.7	—	—	6.9			
		3.3±0.3	1.0	—	5.8			
Output disable time	t _{HZ}	2.5±0.2	1.7	—	6.8	ns	OEAB	B
		2.7	—	—	6.2			
		3.3±0.3	1.5	—	5.5			
	t _{LZ}	2.5±0.2	1.0	—	6.1		OEBA	A
		2.7	—	—	5.1			
		3.3±0.3	1.0	—	4.8			
Input capacitance	C _{IN}	3.3	—	4.0	—	pF	Control inputs	
Output capacitance	C _{IN / O}	3.3	—	8.0	—	pF	A or B ports	

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Switching Characteristics (Ta = −40 to 85°C) (Cont)

Item	Symbol	V _{cc} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t _{su}	2.5±0.2	1.7	—	—	ns	Data before $\overline{\text{CLK}}\downarrow$
		2.7	1.4	—	—		
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.1	—	—		Data before LE $\downarrow$
		2.7	1.0	—	—		$\overline{\text{CLK}}$ “H”
		3.3±0.3	1.0	—	—		
		2.5±0.2	1.9	—	—		Data before LE $\downarrow$
		2.7	1.6	—	—		$\overline{\text{CLK}}$ “L”
		3.3±0.3	1.4	—	—		
Hold time	t _h	2.5±0.2	1.7	—	—	ns	Data after $\overline{\text{CLK}}\downarrow$
		2.7	1.6	—	—		
		3.3±0.3	1.3	—	—		
		2.5±0.2	2.0	—	—		Data after LE $\downarrow$
		2.7	1.8	—	—		$\overline{\text{CLK}}$ “H”
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.6	—	—		Data after LE $\downarrow$
		2.7	1.5	—	—		$\overline{\text{CLK}}$ “L”
		3.3±0.3	1.2	—	—		
Pulse width	t _w	2.5±0.2	3.3	—	—	ns	LE “H”
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		$\overline{\text{CLK}}$ “H” or “L”
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

• Test Circuit

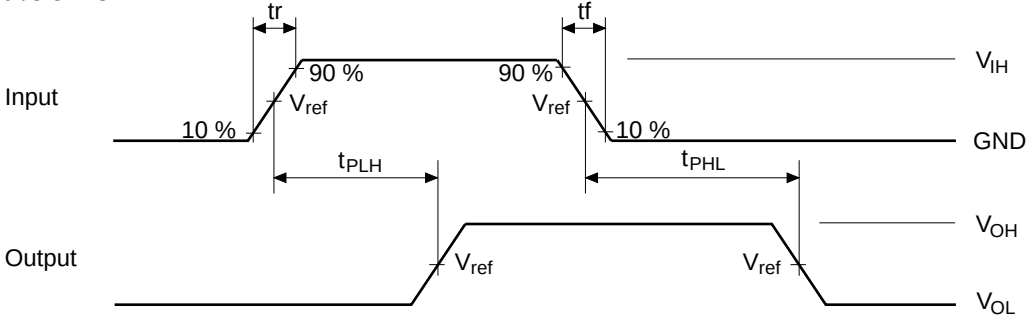


Load Circuit for Outputs

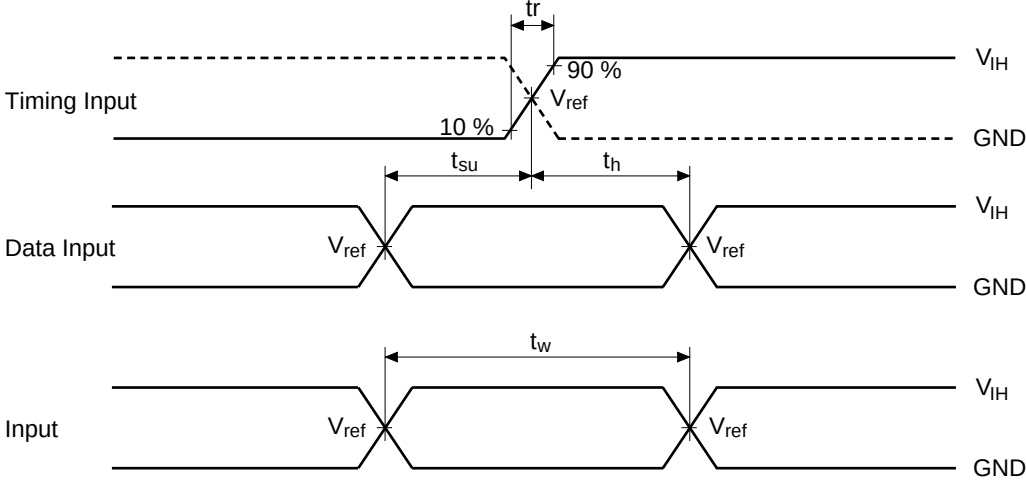
Symbol	$V_{CC}=2.5\pm0.2V$	$V_{CC}=2.7V, 3.3\pm0.3V$
t_{PLH}/t_{PHL}	OPEN	OPEN
$t_{su}/t_h/t_w$		
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

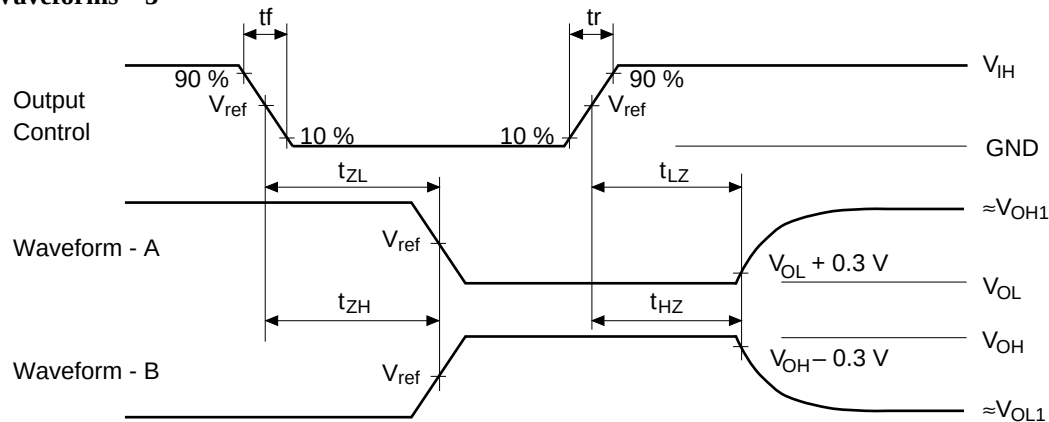
• Waveforms – 1



• Waveforms – 2



• Waveforms – 3

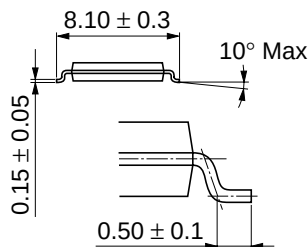
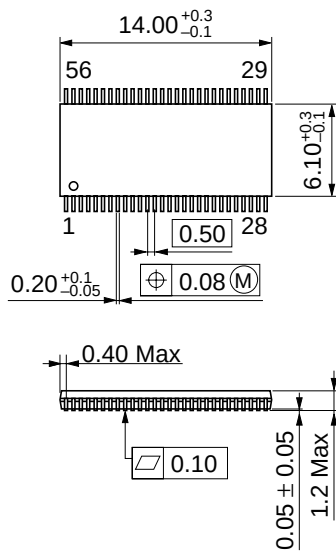


TEST	$V_{CC}=2.5\pm0.2\text{V}$	$V_{CC}=2.7\text{V}, 3.3\pm0.3\text{V}$
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:
PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



Hitachi code	TTP-56D
EIAJ code	—
JEDEC code	—

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