HD68562

DUSCC (Dual Universal Serial Communications Controller)

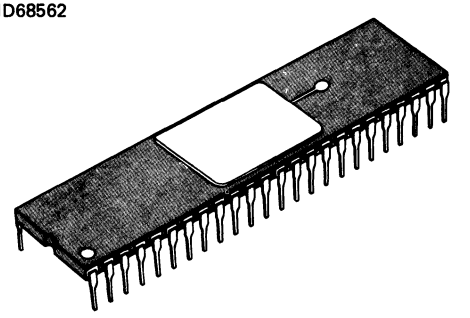
—ADVANCE INFORMATION—

The HD68562 Dual Universal Serial Communications Controller (DUSCC) transforms parallel data which is transferred from central processing unit into serial data. It is a single chip MOS-LSI communications device designed to be a foundation of universal high-performance data-communication subsystems, particularly for the 68000 family microprocessors.

The DUSCC provides two independent, multi-protocol, full duplex receiver/transmitter channels in a single package. Since the DUSCC supports a wide range of protocols, it handles data communications with the minimum intervention, usually just a few commands from its host processor. The controller's data rate is maximum 4M bits/s which meets the requirement of the presently most powerful systems. A high-speed, high-performance communication system is realized with minimum external logic at low cost through a variety of functions provided by the chip: 16-bit multi-function counter/timer, a digital phase locked loop (DPLL), a parity/CRC generator and checker, and baud rate generator.

The DUSCC is useful for communication between host computer and terminals, electric mail, VIDEOTEX, local area network (LAN), communications network among personal computers, etc.

HD68562

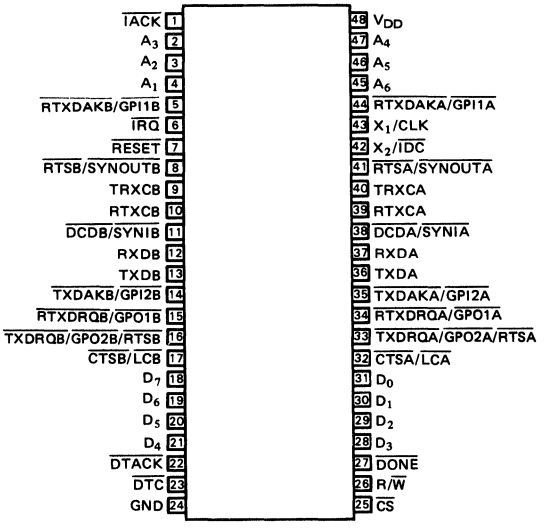


(DC-48)

■ FEATURES

- Channel data rate: 4M bps maximum
- Receiver/Transmitter: Two channels, dual full-duplex synchronous/asynchronous
- Multi-protocol operation: BOP (Bit Oriented Protocol) BCP (Byte Controlled Protocol) COP (Character Oriented Protocol) ASYNC (Asynchronous)
- High data transfer efficiency: Four-character receiver/transmitter FIFOs
- Parity and FCS (Frame Check Sequence): VRC, LRC-8, CRC-16, CRC-CCITT
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- DMA interface: Compatible with Hitachi HD68450/HD-63450 DMAC and other DMA controllers
- Multi-function programmable 16-bit C/T: Baud rate generator, etc.
- Clock oscillator: On-chip oscillator for crystal
- Power supply: Single +5V

■ PIN ARRANGEMENT



■ MAJOR FUNCTIONS OF DUSCC

Item	FUNCTION
Maximum operating frequency	4 MHz
Maximum data transfer rate	4 Mbits/s
Data length	5-8 bits
Bus interface	Compatible with HD68000 (8 bits bus)
FIFO	4 bytes for each receiver/transmitter
Number of channels	2 channels
Error check	Parity, framing, over run, under run, FCS
Channel mode	Half-duplex, full-duplex, auto-echo, local loopback
Data transfer mode	Polled, interrupt, DMA, wait
Protocol operation	ASYNC : 5-8 bits plus optional parity COP : BISYNC, X.21 BCP : DDCMP BOP : HDLC/ADCCP, SDLC, SDLC Loop, Link Level, X.75 Link Level
Baud rate generator	Built-in
Selection of baud rate	(1) 16 fixed rates: 50 to 38.4K baud. (2) Optional baud rate by timer.
Encoding/Decoding	NRZ, NRZI, FM0, FM1, Manchester
Digital phase locked loop	Built-in
DMA interface	Compatible with HD68450/HD63450 Half or full duplex operation Single or dual address data transfer
Interrupt capabilities	(1) Daisy chain option (2) Vector output (fixed or modified by status) (3) Maskable interrupt conditions (4) Programmable internal priorities
Model control	RTS, CTS, DCD Four general purpose I/O pins per channel
16-bit counter timer	Built-in
Oscillator	Built-in
Package	Ceramic DIP 48-pin
Power supply	5V ± 10% Ta = 0 to 70°C
Power dissipation	Typ. 1 W

■ INTERNAL BLOCK DIAGRAM

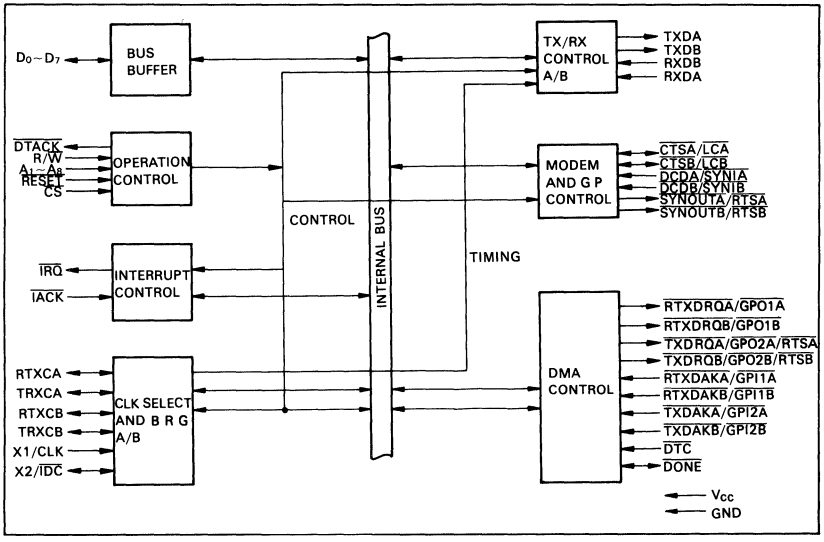


Figure 1 DUSCC Block Diagram

■ SYSTEM CONFIGURATION

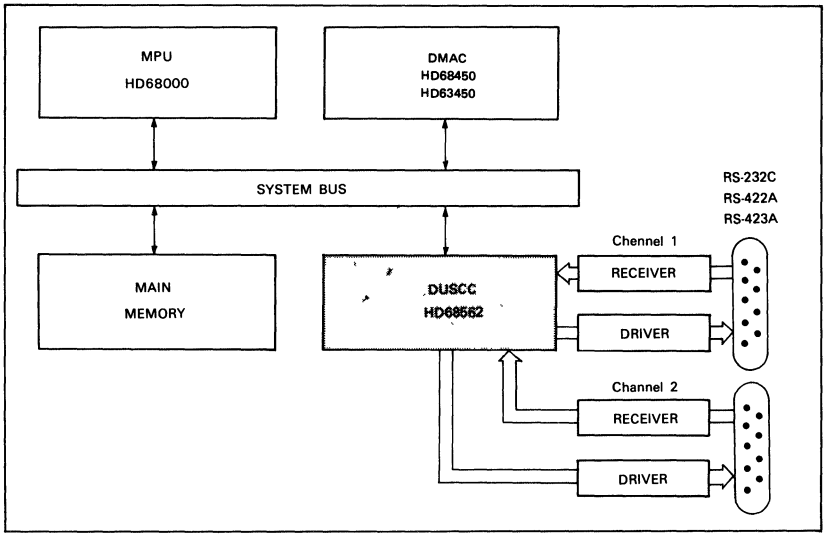


Figure 2 System Configuration Example