HD66780 (LCD-IIA)

(Dot Matrix Liquid Crystal Display Controller and Driver)

Description

The LCD-IIA (HD66780) a dot matrix liquid crystal display controller and driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcontroller or microprocessor control. All the functions required for driving a dot matrix liquid crystal display are internally provided on one chip.

Designers can complete dot matrix liquid crystal display systems with low chipcount by using the LCD-IIA (HD66780). If a driver LSI (HD44100H or HD66100F) is connected to the HD66780, up to 80 characters can be displayed.

The LCD-IIA is produced by the CMOS process. Therefore, the combination of the LCD-IIA with a CMOS microcontroller or microprocessor can complete a portable battery-driven device with low power dissipation.

Features

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Can interface to 4-bit or 8-bit MPU
- Display data RAM: 80 × 8 bits (80 characters, max)
- Character generator ROM: 12000 bits; Character font 5×10 dots: 240 characters
- Character generator RAM: 64 × 8 bits; Character font 5×8 dots: 8 characters or character font 5 × 11 dots: 4 characters
- Both display data and character generator RAMs can be read from the MPU
- Internal liquid crystal display driver
  −16 common signal drivers
  −40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H or HD66100F)
- Duty factor selection (selectable by program)
  −1/8 duty: 1 line of 5 × 7 dots + cursor
  −1/11 duty: 1 line of 5 × 10 dots + cursor
  −1/16 duty: 2 lines of 5 × 7 dots + cursor
- Maximum number of display characters as shown in table 1
- Wide range of instruction functions: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Internal automatic reset circuit at power on (internal reset circuit)
- Internal oscillation circuit
  −External resistor or ceramic filter
  −External clock operation possible
- CMOS process
- Single +5 V logic power supply (excluding power for liquid crystal display drive)
- Operation temperature range: -20°C to +75°C (-40°C to +85°C device available upon request)
- 80-pin plastic flat package (FP-80B, FP-80A)
- Low power consumption

Ordering Information

Type No.	Package
HD66780FS	80-pin plastic QFP (FP-80B)
HD66780FH	80-pin plastic QFP (FP-80A)

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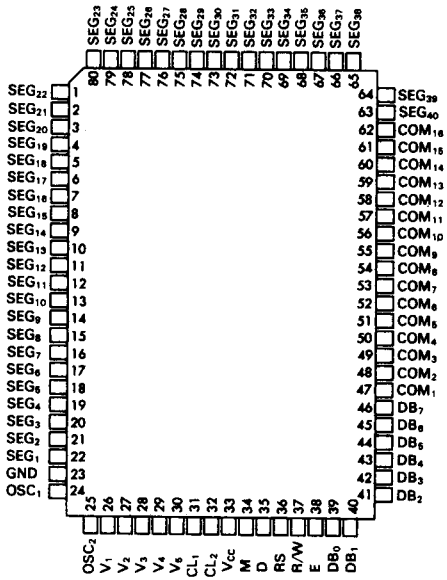
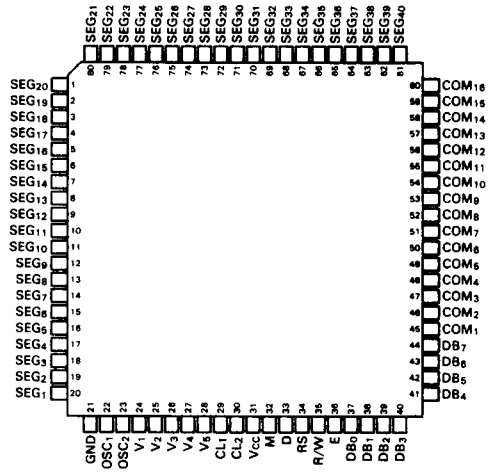
Pin Arrangement



(FP-80)



(FP-80A)

(Top-View)

Pin Description

Signal	No. of Lines	I/O	Connected to	Function
RS	1	Input	MPU	Selects register
R/W	1	Input	MPU	Selects read or write
E	1	Input	MPU	Starts data read or write
DB_7-DB_0	8	I/O	MPU	Bidirectional data bus
CL_1	1	Output	Driver LSI	Serial data latch clock
CL_2	1	Output	Driver LSI	Serial data shift clock
M	1	Output	Driver LSI	LCD waveform AC switch signal
D	1	Output	Driver LSI	Character pattern data
COM_1-COM_{16}	16	Output	LCD	Common signals
SEG_1-SEG_{40}	40	Output	LCD	Segment signals
V_1-V_5	5		Power supply	LCD drive voltages
V_{CC}, GND	2		Power supply	+5 V and ground
OSC_1-OSC_2	2			System clock

Pin Function

RS (Register Select)

RS selects the register that the MPU is accessing. RS = 0 selects the instruction register for MPU writes, and the busy flag and address counter for reads. RS = 1 selects the data register for MPU reads and writes.

R/W (Read/Write)

R/W selects whether the MPU will read from (R/W = 1) or write to (R/W = 0) the LCD-IIA.

E (Enable)

The MPU sets the E input high to signal the start of the read/write operation.

DB_7–DB_0 (Data Bus)

The bidirectional, three-state data bus, DB_0-DB_7, transfers data between the MPU and the LCD-IIA. DB_7 can be used as the busy flag. The lower-order four lines, DB_0-DB_4, are not used in four-bit interface operation.

CL_1, CL_2 (Clock 1, Clock 2)

The CL_1 output signals the HD44100H or HD66100F driver LSI to latch the serial data sent on line D. The CL_2 output signals it to shift the data.

M (Master AC Signal)

The HD44100H or HD66100F driver LSIs use the M output to convert the LCD drive waveform to AC.

D (Serial Data)

The LCD-IIA outputs serial character pattern data corresponding to the common signals to the HD44100H or HD66100F driver LSIs on D.

COM_1–COM_{16} (Common)

COM_1-COM_{16} are the LCD common lines. Common signals that are not used are deselected. At 1/8 duty factor COM_9-COM_{16} are not used, so they output non-selected waveforms. At 1/11 duty factor COM_{12}-COM_{16} are not used, so they output non-selected waveforms.

SEG_1–SEG_{40} (Segment)

SEG_1-SEG_{40} are the LCD segment lines.

V_1–V_5 (LCD Voltages)

The LCD-IIA requires the V_1-V_5 voltages to output LCD-driving waveforms.

V_{CC}, GND (Power Supply, Ground)

V_{CC} is the LCD-IIA's logic power supply. GND is the power supply ground.

OSC_1, OSC_2 (Oscillator 1, Oscillator 2)

OSC_1 and OSC_2 are the connections for the LCD-IIA system clock. The LCD-IIA can use its internal oscillator if OSC_1 and OSC_2 are connected to a resistor or ceramic filter. An external clock can be input to OSC_1.

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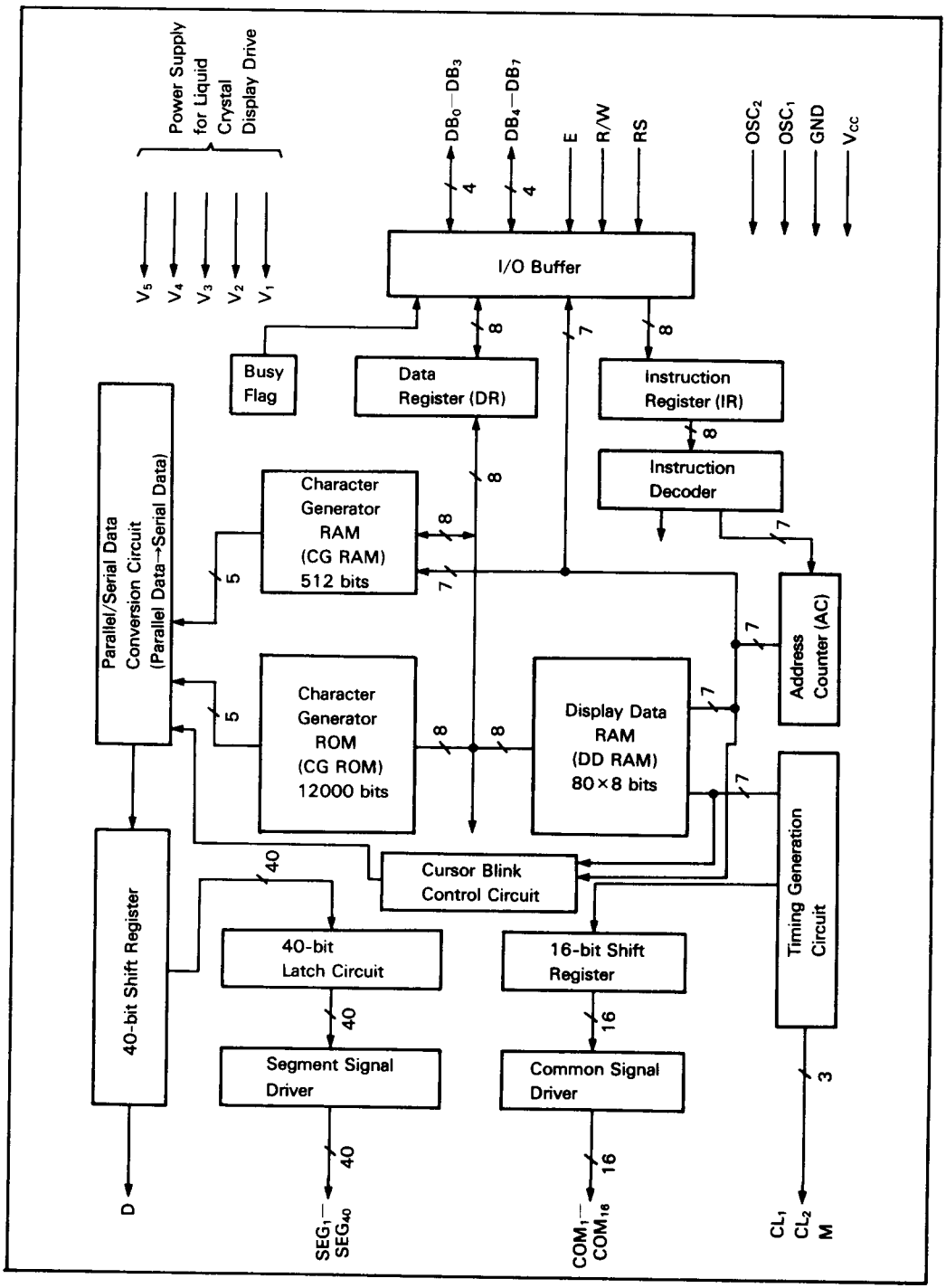
Table 1 Number of Display Characters

No. of Display Lines	Duty factor	Extension	HD44100H	HD66100F	No. of Display Characters
1-line display	1/8, 1/11 duty	Not provided	–	–	8 characters × 1 line
		Provided	9 pcs. (8 characters/pc.)	5 pcs. (16 characters/pc.)	80 characters × 1 line
2-line display	1/16 duty	Not provided	–	–	8 characters × 2 lines
		Provided	4 pcs.(8 characters × 2 lines/pc.)	2 pcs.(16 characters × 2 lines/pc.)	40 characters × 2 lines

HD66780 Block Diagram



Block Function

Registers

The HD66780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM internally. The MPU also uses the DR for data storage when reading data from the DD RAM or the CG RAM. When the MPU writes address information into the IR, the LCD-IIA sends data to the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, the LCD-IIA sends data in the DD RAM or CG RAM at the next address to the DR for the next read from the MPU. Register selector (RS) signals select these two registers (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66780 is in the internal operation mode, and instructions will not be accepted. As table 2 shows, the busy flag is output to DB $_7$ when RS = 0 and R/W = 1. The next instruction must be written after confirming that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD and CG RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1 (or decremented by 1). AC contents are output to DB_0-DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Display Data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown in figure 1.

The DD RAM adress (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

When there are fewer then 80 display characters, the display begins at the head positon. For example, 8 characters using an HD66780 are displayed as shown in figure 2.

When the display shift operation is performed, the DD RAM address moves as shown in figure 3.

A 16-character display using an HD66780 and an HD44100H is shown in figure 4.

The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66780 and two or more HD44100Hs can be considered an extension of figure 4.

Since the increase can be 8 digits for each

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Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

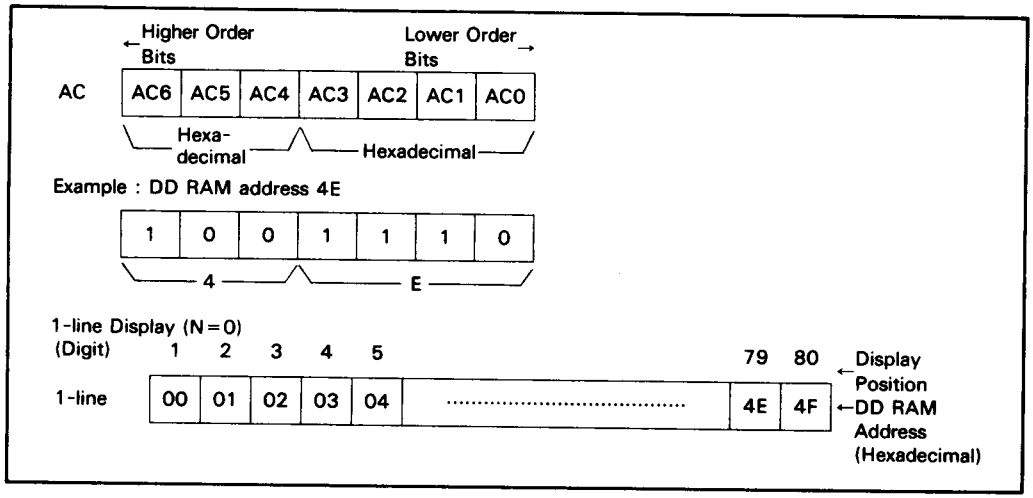

Figure 1 DD RAM Address

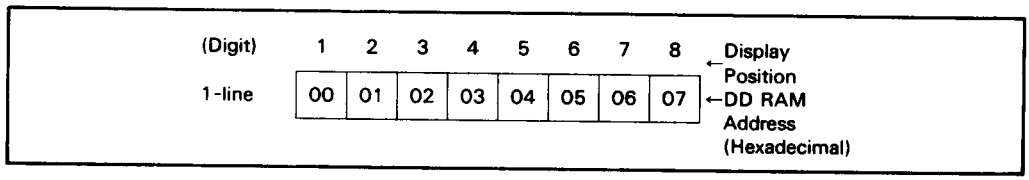

Figure 2 Eight-Character Display Example

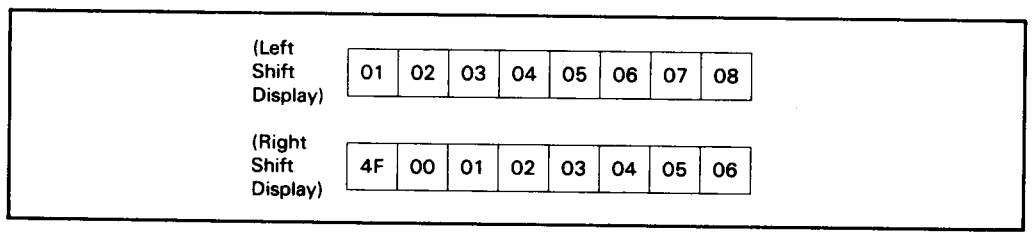

Figure 3 Display shift

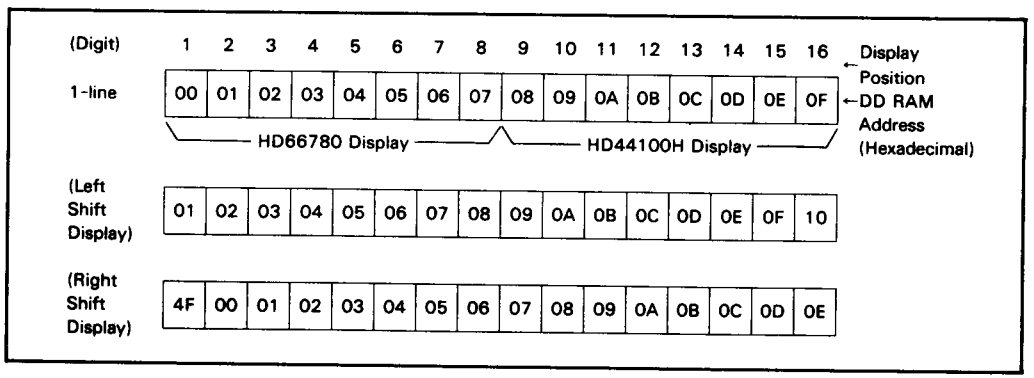

Figure 4 Sixteen-Character Display Example

additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100Hs.

The same holds when HD66100Fs are used as display drivers. Consisting of 80 outputs, one HD66100F can display 16 digits (figure 5).

When the number of display characters is fewer than 40×2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66780 is used, 8 characters × 2 lines are displayed as shown in figure 6.

When display shift is performed, the DD RAM address moves as shown in figure 7.

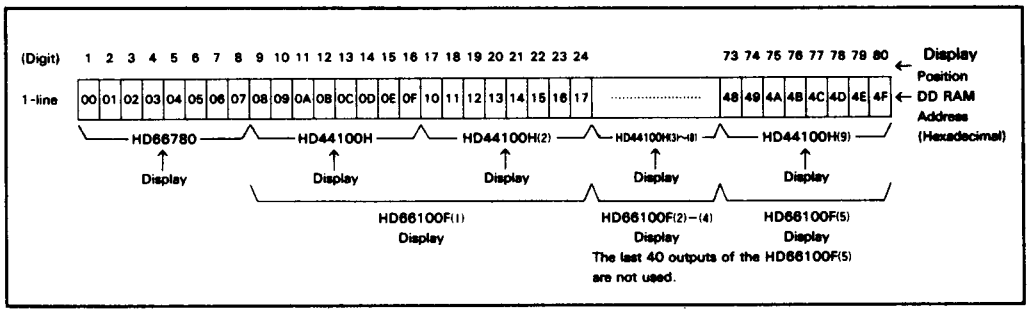

Figure 5 Extended Display

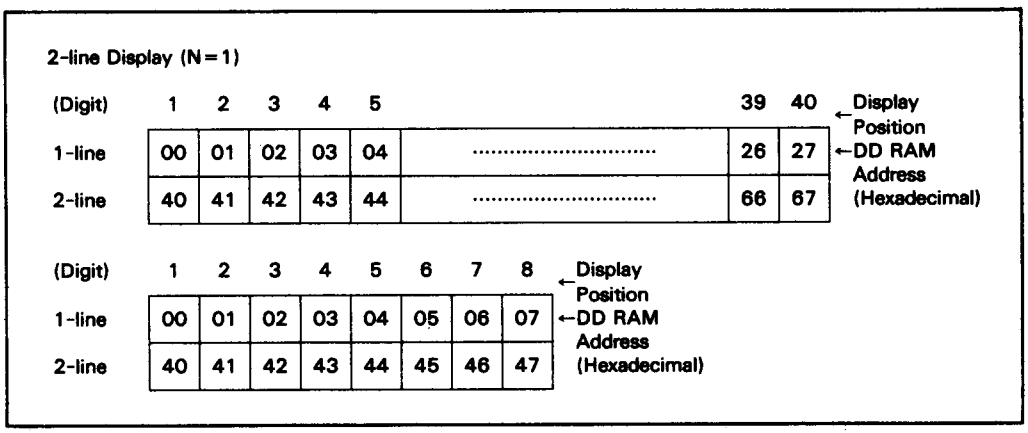

Figure 6 Two-Line by Eight-Character Display Example

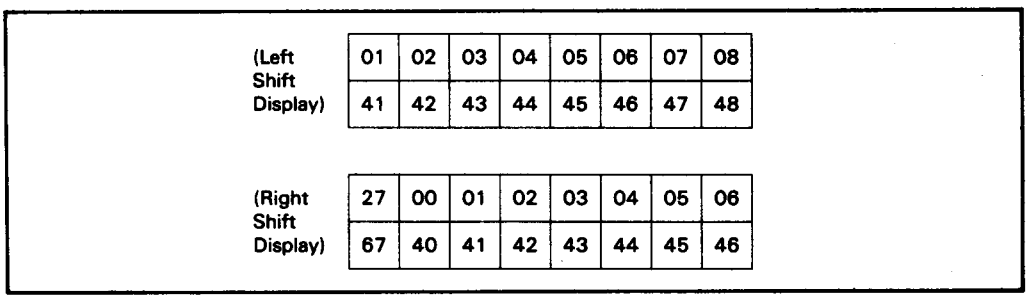

Figure 7 Two-Line Display Shift

16 characters × 2 lines are displayed as in figure 8 when an HD66780 and an HD44100H are used.

The relation between display position and DD RAM address when the number of display digits is increased by using one HD66780 and two or more HD44100Hs, can be considered an extension of figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits × 2 lines can be displayed by connecting 4 HD66780s (or 2 HD66100Fs) externally.

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. A CG ROM has 240 types of 5 × 10 dot character patterns built-in.

(Note: In a 5 × 7 dot + cursor display, only the upper part, that is, 5 × 7 dots of 5 × 10 dots, is displayed.)

Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD66780A00. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

With the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots 4 patterns can be written.

Write the character codes in the left columns of table 3 to display character patterns stored in CG RAM.

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address (Hexadecimal)
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
	HD66780 Display								HD44100H Display								
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	
(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

Figure 8 Two-Line by Sixteen-Character Display Example

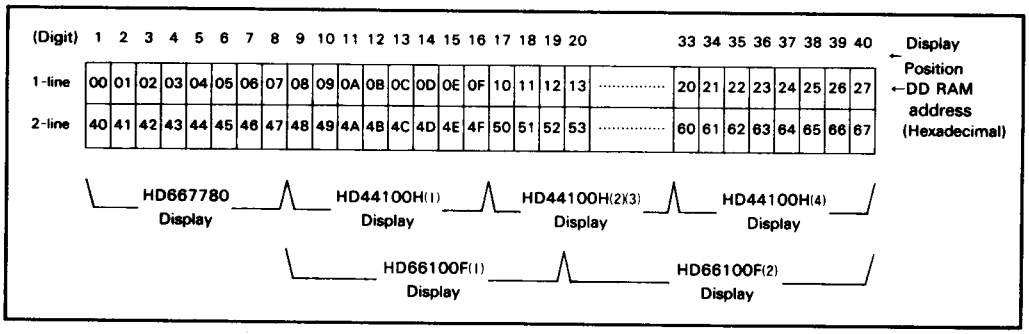

Figure 9 Two-Line Extended Display Example

Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66780A00)

Lower 4 Bits \ Higher 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
××××0000	CG* RAM (1)															
××××0001	(2)															
××××0010	(3)															
××××0011	(4)															
××××0100	(5)															
××××0101	(6)															
××××0110	(7)															
××××0111	(8)															
××××1000	(1)															
××××1001	(2)															
××××1010	(3)															
××××1011	(4)															
××××1100	(5)															
××××1101	(6)															
××××1110	(7)															
××××1111	(8)															

Note: * The user can specify any pattern for character-generator ROM.

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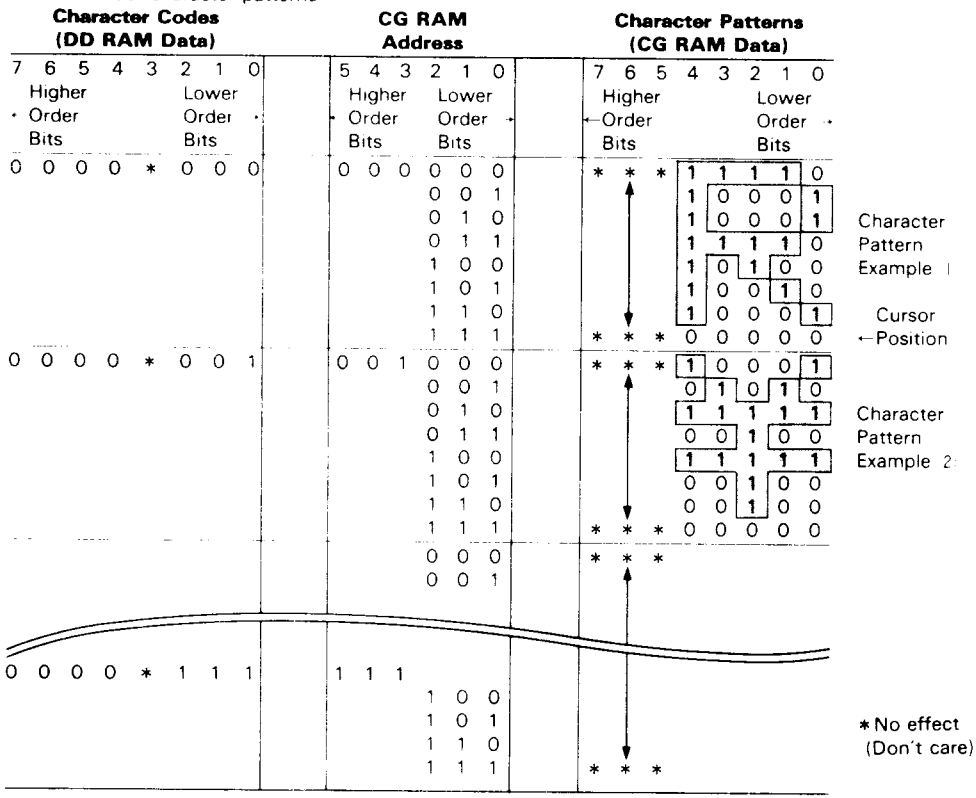
Table 4 shows the relation between CG RAM addresses and data and display patterns.

As table 4 shows, an area that is not used for display can be used as general data RAM.

Table 4 Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

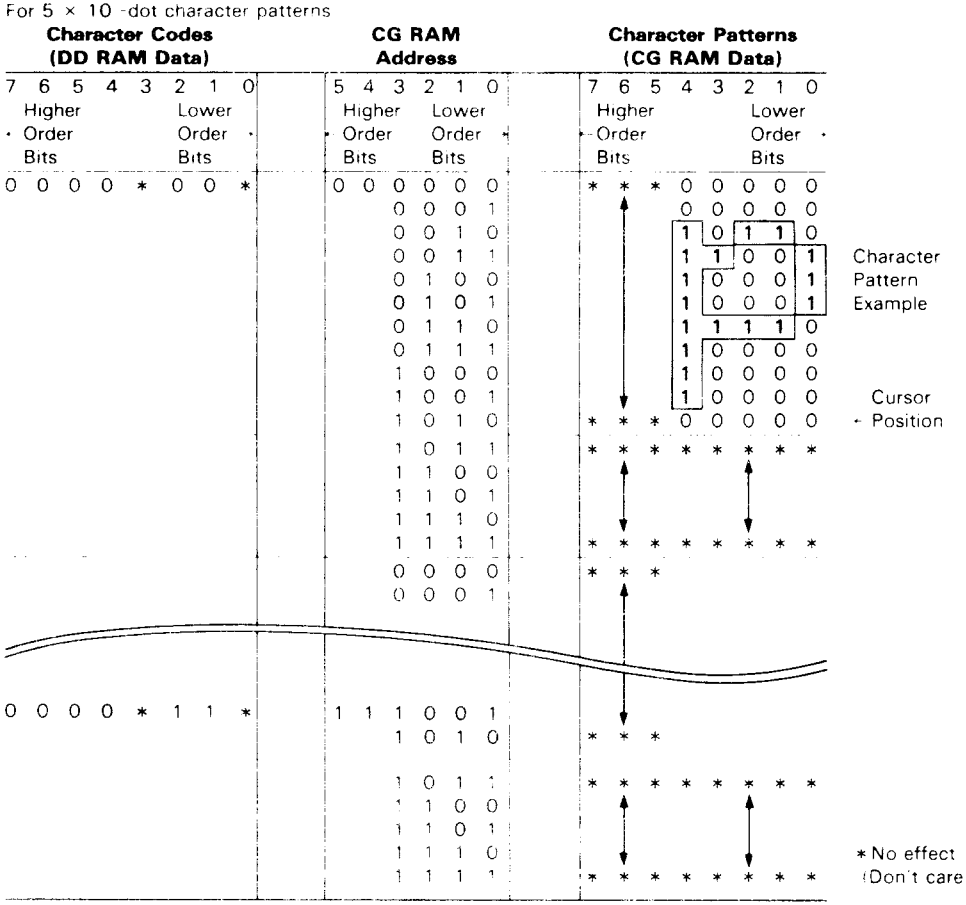
For 5 × 7-dot character patterns



Notes:
1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 characters).
2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.
4. As shown in table 3 and 4, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 is ineffective, the R display in the character pattern example, is selected by character code 00 (hexadecimal) or 08 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

Table 4 Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Cont)

For 5 × 10 -dot character patterns



Notes:
1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 characters).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is performed by logical OR with cursor.
   Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12nd-16th lines are not used for display, they can be used for the general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 are ineffective, P display in the character pattern example is selected by character code 00, 01, 08 and 09 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

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Timing generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so that they may not interfere with each other. Therefore, when writing data to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected drivers (HD44100H or HD66100F).

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms. The other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data can be sent to HD44100H or HD66100Fs, externally connected in cascade, to display an extended number of characters.

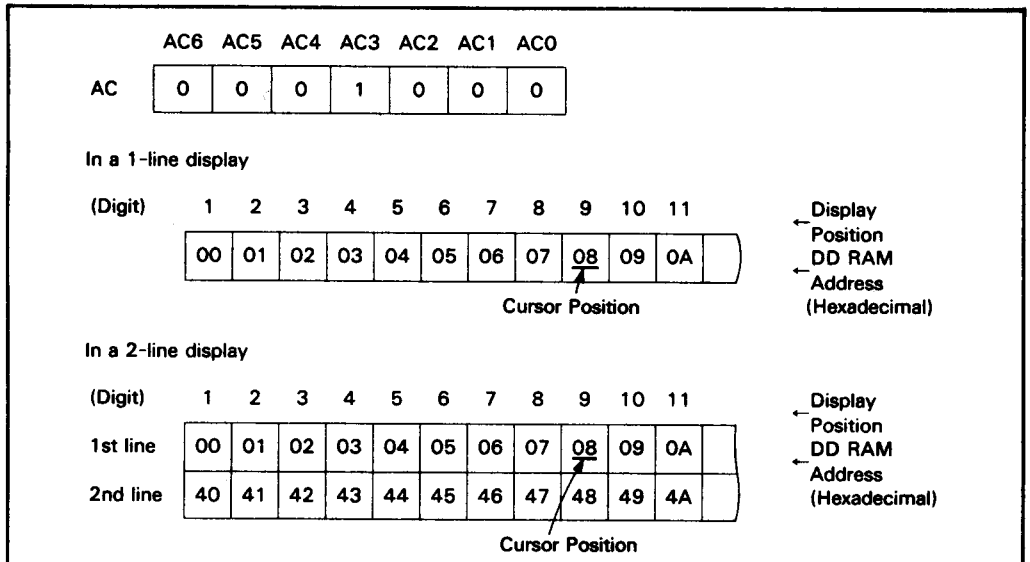
The LCD-IIA always starts sending serial data at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD66780 drives the head of the display. The rest of the display, corresponding to later addresses, are added with each additional HD44100H or HD66100F.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blinking. The cursor or blinking appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, the cursor position is as shown in figure 10.



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Figure 10 Cursor or Blink

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MPU Interface

The HD66780 can send data in either two 4-bit operations or one 8-bit operation so it can interface to both 4-and 8-bit MPU's.

When interface data is 4 bits long, data is transferred using only 4 bus lines: DB_4-DB_7. DB_0-DB_3 are not used. Data transfer between the HD66780 and the MPU completes when 4-bit data is transferred twice.

Data of the higher order 4 bits (contents of DB_4-DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0-DB_3 when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data (figure 11).

When the interface is 8 bits long, data is transferred using the 8 data bus lines DB_0-DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed at initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state lasts 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set
   a. DL = 1: 8-bit long interface data
   b. N = 0: 1-line display
   c. F = 0: 5×7-dot character font
3. Display on/off control
   a. D = 0: Display off
   b. C = 0: Cursor off
   c. B = 0: Blink off
4. Entry mode set
   a. I/D = 1: + 1(increment)
   b. S = 0: No shift

Note: When power supply conditions in the electrical characteristics are not met using internal reset circuit, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to initializing by instruction.

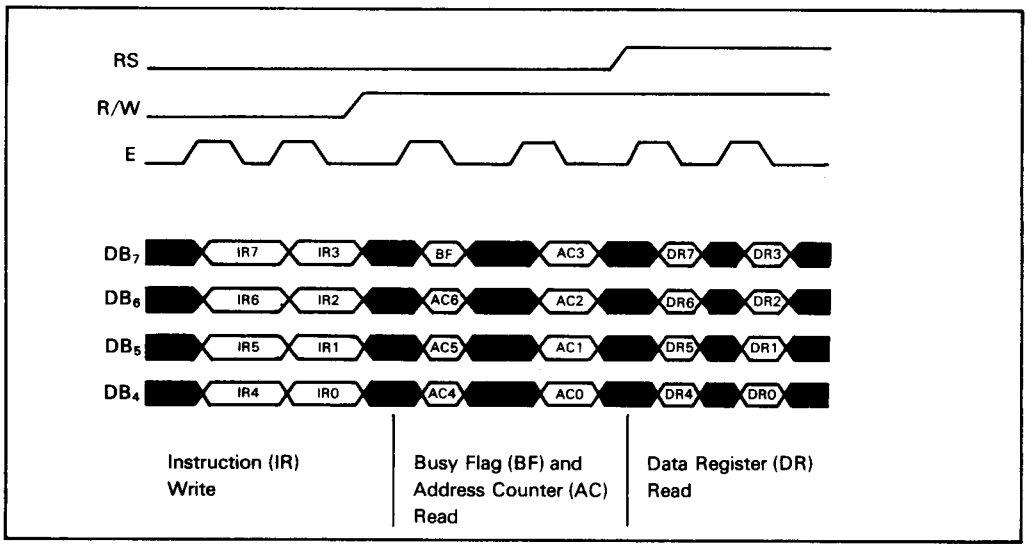

Figure 11 4-Bits Data Transfer Example

Instructions

Only two HD66780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66780 internal operation to various types of MPU's which operate at different speeds or to allow interface to peripheral control IC's. HD66780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W), and data bus signals (DB_0–DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate HD66780 functions such as display format, data length, etc
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of HD66780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

During internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is on 0 before sending an instruction from the MPU.

Note: Make sure the HD66780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction execution time. See table 5 for a list of each instruction's execution time.

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Table 5 Instructions

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (Max) (fcp or fosc 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read	40 μs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blink of cursor position character (B)	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N) and character font (F)	40 μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents	0 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	46 μs

Notes: 1.

I/D	= 1: Increment	BF	= 1: Internally operating
I/D	= 0: Decrement	BF	= 0: Can accept instruction
S	= 1: Accompanies display shift	DD RAM: Display data RAM	
S/C	= 1: Display shift	CG RAM: Character generator RAM	
S/C	= 0: Cursor move	A_{CG}: CG RAM address	
R/L	= 1: Shift to the right	A_{DD} :DD RAM address Corresponds to cursor address	
R/L	= 0: Shift to the left	AC : Address counter used for both DD and CG RAM	
DL	= 1: 8 bits, DL = 0: 4 bits		
N	= 1: 2 lines, N = 0: 1 line		
F	= 1: 5×10 dots, F = 0: 5×7 dots		

2. * No effect (Don't care)
3. Execution time changes when frequency changes.
   Example: When fcp or fosc is 270 kHz:

$$40\ \mu s \times \frac{250}{270} = 37\ \mu s$$

Clear Display

Clear display (figure 12) writes space code 20 (hexadecimal)(character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it is shifted. In other words, the display disappears and the cursor or blink goes to the left edge of the display (the first line if 2 lines are displayed). Sets I/D = 1 (increment mode) of entry mode. S of entry mode does not change.

Return Home

Return home (figure 13) sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left of the display (the first line if 2 lines are displayed).

Entry Mode Set

I/D: I/D (figure 14) increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM. Writing into or reading out of the CG RAM does not shift the display. When S = 0, the display does not shift.

Display On/Off Control

D: The display is on when D = 1 and off when D = 0 (figure 15). When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc does not

4

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Figure 12 Clear Display Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* Don't care

Figure 13 Return Home Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Figure 14 Entry Mode Set Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Figure 15 Display On/Off Control Instruction

change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7-dot is selected and 5 dots in the 11th line when the 5× 10-dot character font is selected (figure 16).

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz (figure 15). The cursor and the blink can be set to display simultaneously. (The blink time changes according to the reciprocal of fcp or fosc. For example, 409.6 × $\frac{250}{270}$ = 379.2 ms when fcp = 270 kHz.)

Cursor or Display Shift

Cursor or display shift (figure 17) shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

Table 6 shows how S/C and R/L control shifting.

Address counter (AC) contents do not change if the only action performed is shift display.

Function Set

DL: DL (figure 18) sets interface data length. Data is sent or received in 8-bit length (DB_7-DB_0) when DL = 1 and in 4-bit lengths (DB_7-

Table 6 Cursor or Display Shift Control

S/C	R/L	Function
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift
1	1	Shifts the entire display to the right. The cursor follows the display shift

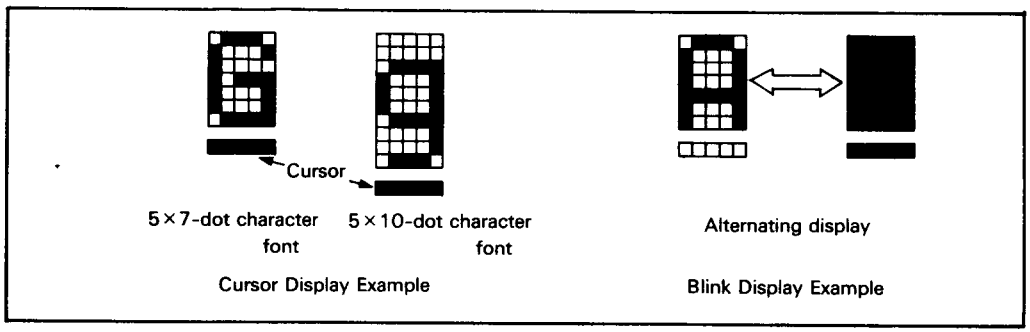

Figure 16 Cursor and Blink Display

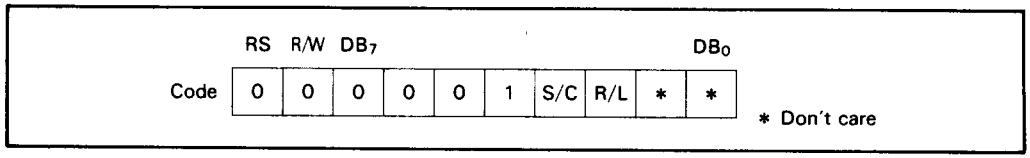

Figure 17 Corsor or Display Shift Instruction

DB_4) when DL = 0.
When the 4-bit length is selected, data must be sent or received twice.

N: N sets number of display lines.

F: F sets character font. See table 7.

Note: Perform the function set at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address (figure 19) sets the CG RAM address binary AAAAAA into the address counter. Data is then written or read from the MPU for the CG RAM.

Set DD RAM Address

Set DD RAM address (figure 20) sets the DD RAM address binary AAAAAAA into the address counter. Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is 00-4F (hexadecimal), when N = 1 (2-line display), AAAAAAA is 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

Read Busy Flag and Address

Read busy flag and address (figure 21) reads the busy flag (BF) that indicates the system is now internally operating on a previously

Table 7 Function Set N and F

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5×7 dots	1/8	
0	1	1	5×10 dots	1/11	
1	*	2	5×7 dots	1/16	Cannot display 2 lines with 5×10-dot character font

Note: * Don't care

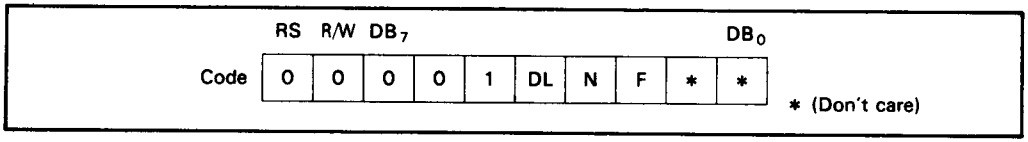

Figure 18 Function Set Instruction

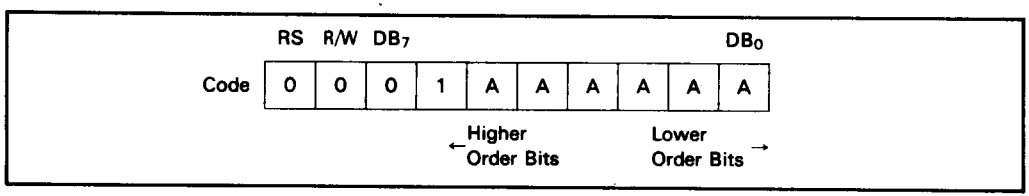

Figure 19 Set CG RAM Address Instruction

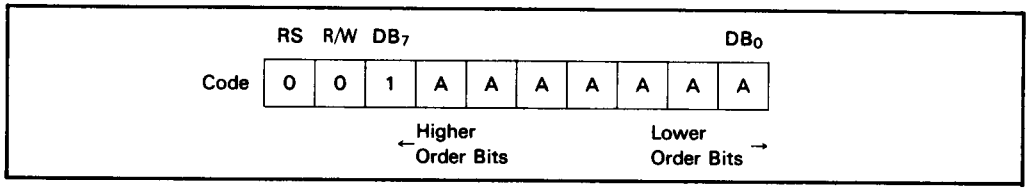

Figure 20 Set DD RAM Address Instruction

received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to 0. Check the BF status before the next write operation (figure 22).

At the same time, the value of the address counter expressed in binary (AAAAAAA) is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in set CG RAM address and set DD RAM address.

Write Data to CG or DD RAM

Write data to CG or DD RAM (figure 23) writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After writing, the LCD-IIA automatically increments or decrements the address by 1, according to entry mode.

Read Data from CG or DD RAM

Read data from CG or DD RAM (figure 24) reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you do not the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift

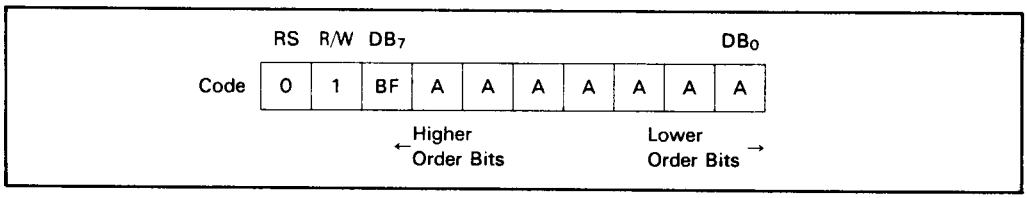

Figure 21 Read Busy Flag and Address Instruction

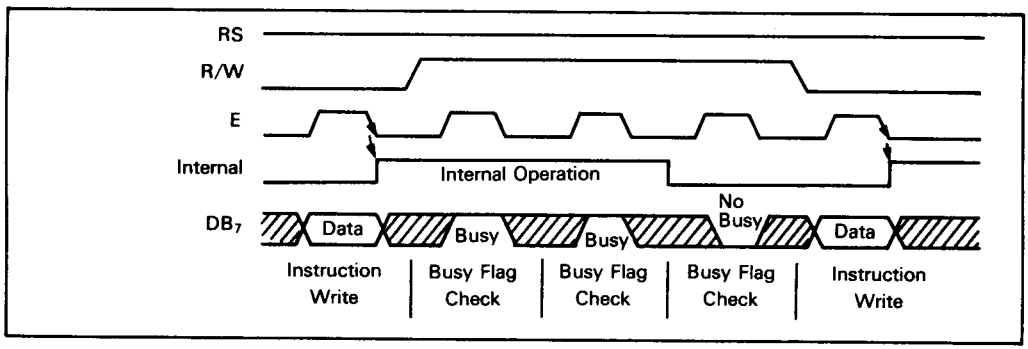

Figure 22 Example of Busy Flag Check Timing Sequence

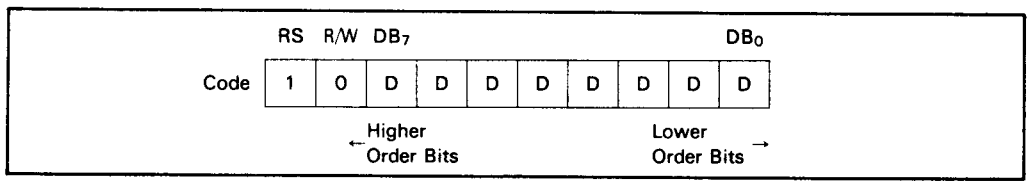

Figure 23 Write Data to CG or DD RAM Instruction

instruction (when reading out of DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display is not shifted no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out, execute the read instruction from the second time the read instruction is sent.

How to Use the HD66780

Interface to 8-Bit MPU

When Connecting to 8-Bit MPU Through PIA: Figure 25 is an example of using a PIA or I/O port (for a microcontroller) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

Connecting Directly to the 8-Bit MPU Bus: Figure 26 shows the LCD-IIA connected directly to an HD6800.

Example of Interfacing to the HD6805: Figure 27 shows the LCD-IIA connected directly to an HD6805.

4

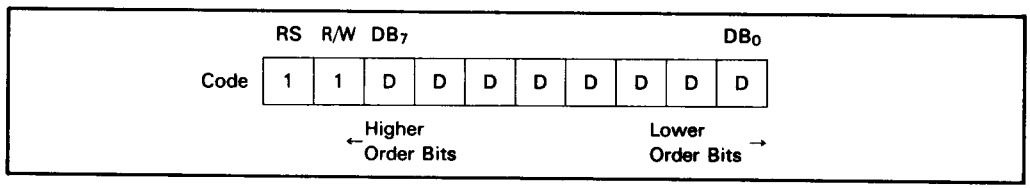

Figure 24 Read Data from CG or DD RAM Instruction

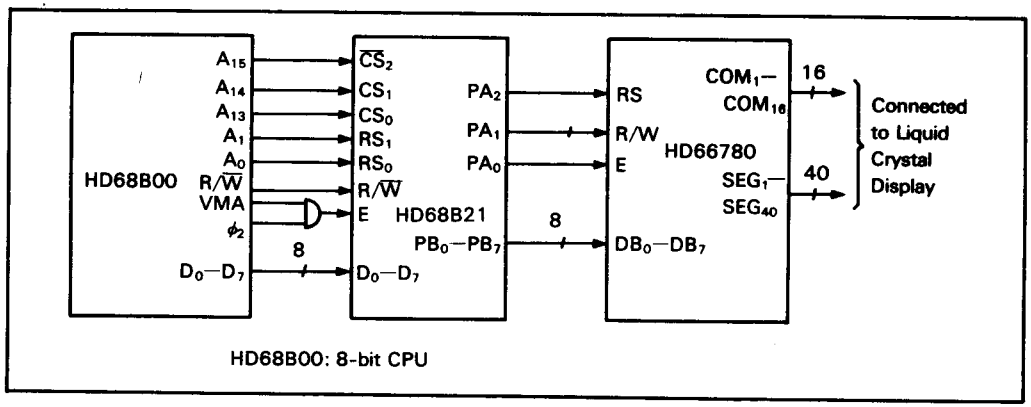

Figure 25 Example of Interface to HD68B00 using PIA (HD68B21)

Example of Interfacing to the HD6301: Figure 28 shows the LCD-IIA connected directly to an HD6301.

Interface to 4-Bit MPU

The HD66780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port, If the I/O port has enough bits, data can be transferred in 8-bit length, but if there aren't enough bits, the transfer is made in two operations of 4 bits each (designating the interface data length as 4 bits). In the latter case, the timing sequence becomes somewhat complex. (see figure 29).

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

Figure 30 shows an example of an interface to the 400 series.

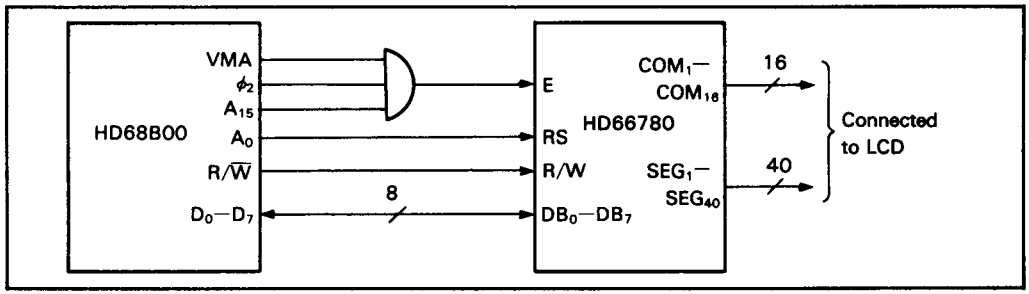

Figure 26 Direct Connection to HD68B00

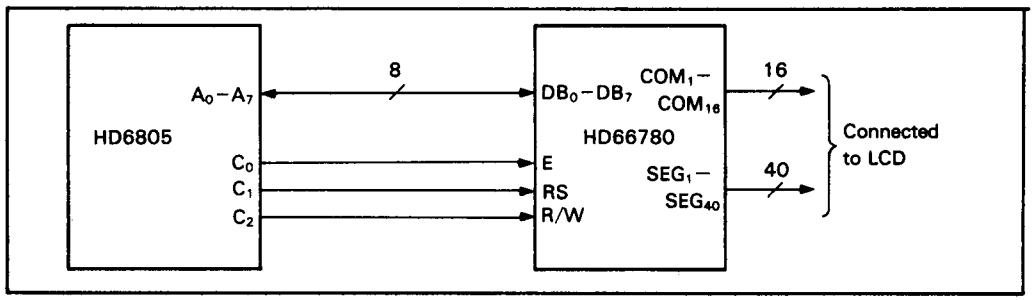

Figure 27 Direct Connection to HD6805

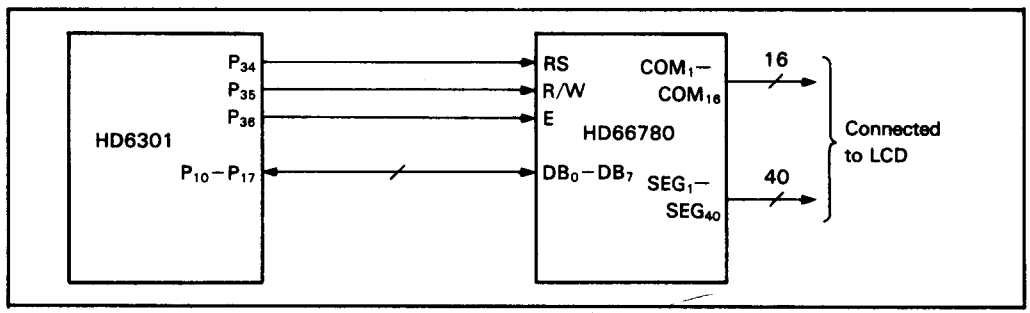

Figure 28 Direct Connection to HD6301

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66780 can perform 2 types of display, using 5 × 7 dots or 5 × 10 dots for the character font, with a cursor on each.

Up to 2 lines can be displayed with 5 × 7 dots and 1 line with 5 × 10 dots.

Therefore, three types of common signals are available (table 8).

Number of lines and font types can be selected by program (see table 5).

Connection to HD66780 and Liquid Crystal Display: Figure 31 shows connection examples. Since 5 SEG signal lines can display one digit, one HD66780 can display up to 8 digits

Table 8 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16

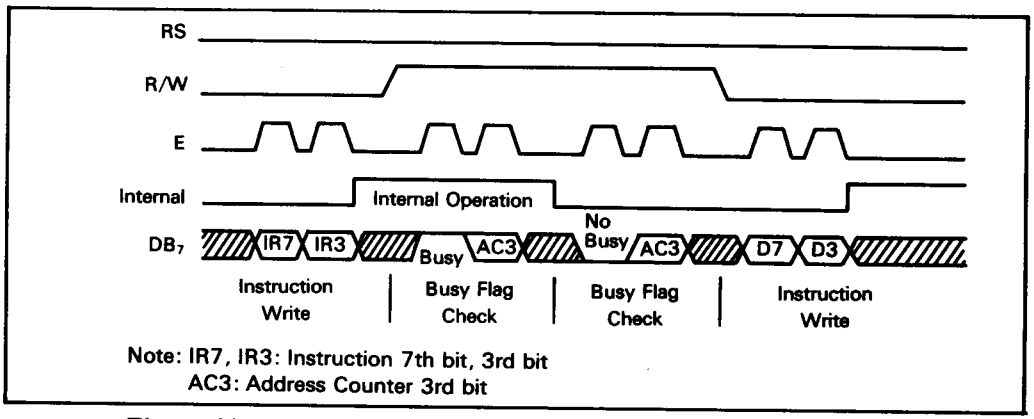

Figure 29 An Example of 4-Bit Data Transfer Timing Sequence

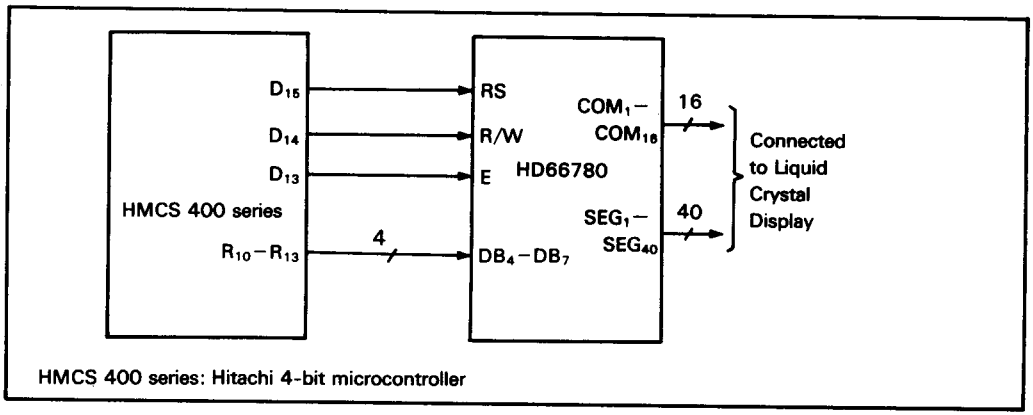

Figure 30 Example of Interface to the 400 Series

for a 1-line display and 16 digits for a 2-line display.

In figure 31 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals (figure 32).

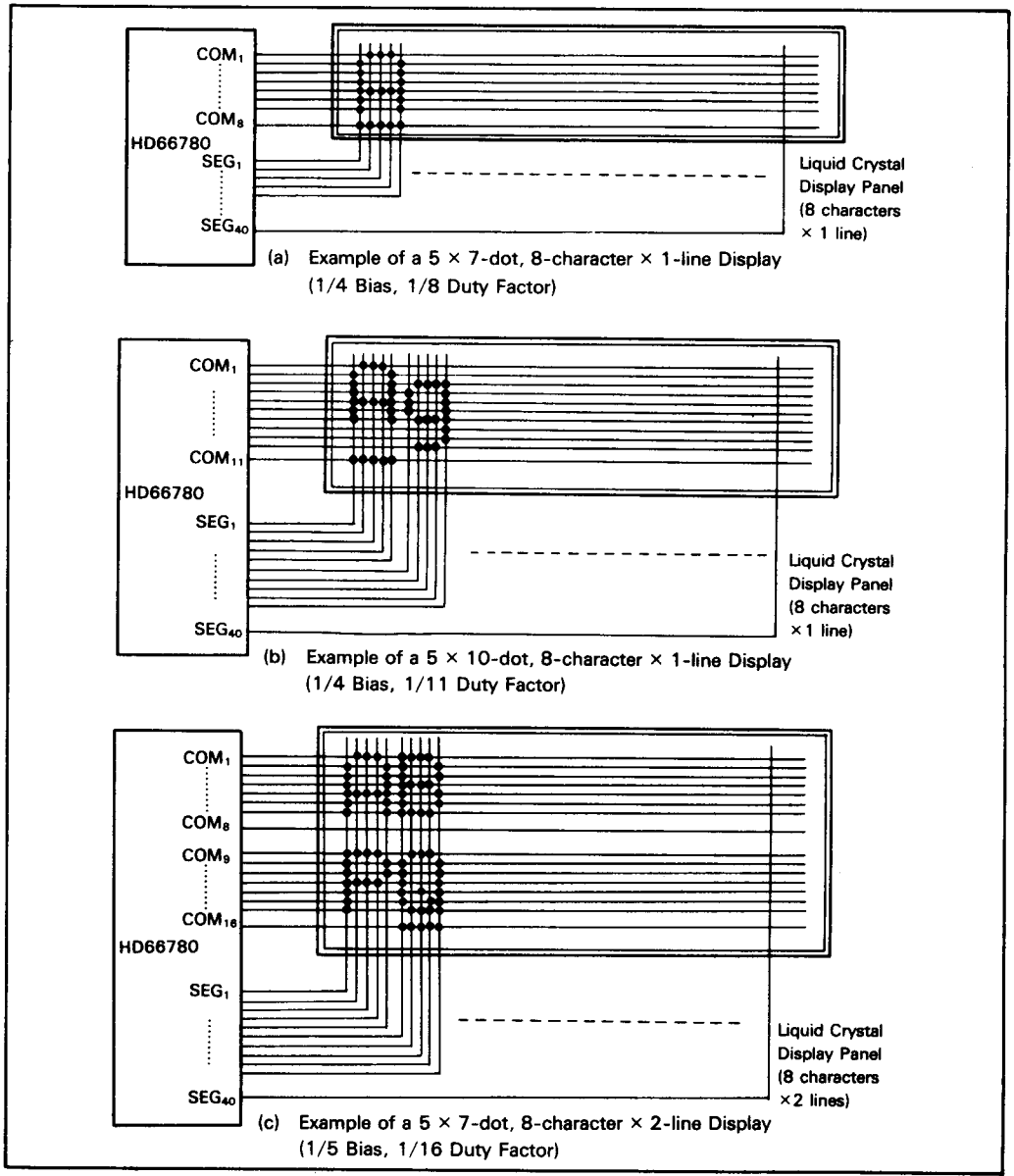

Figure 31 Liquid Crystal Display and Connections to HD66780

Connection for Changed Matrix Layout: In the preceding examples, the number of lines was matched to the number of scanning lines. The display types in figure 33 are possible by changing the matrix layout in the liquid crystal display panel.

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) address for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 31.

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factors. Table 9 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 34.

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

Figure 35 shows examples of liquid crystal display frame frequency when the oscillation frequency is 250 kHz (1 clock = 4 μs).

Connection with Driver LSI HD44100H or HD66100F

You can increase the number of display characters by externally connecting liquid crystal display driver LSI's HD44100H or HD66100F to the HD66780.

When connected to the HD66780, the HD44100H or HD66100F is used as a segment signal driver. The HD44100H and the HD66100F can be connected to the HD66780 directly since they supply CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figures 36 and 37 show connection examples.

Note: Connection of voltage supply terminals V_1 through V_6 for the liquid crystal display drive is complicated.

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Table 9 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor	Bias	Power Supply V_1	V_2	V_3	V_4	V_5
1/8,1/11	1/4	V_{CC} - (1/4)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (3/4)V_{LCD}	V_{CC} - V_{LCD}
1/16	1/5	V_{CC} - (1/5)V_{LCD}	V_{CC} - (2/5)V_{LCD}	V_{CC} - (3/5)V_{LCD}	V_{CC} - (4/5)V_{LCD}	V_{CC} - V_{LCD}

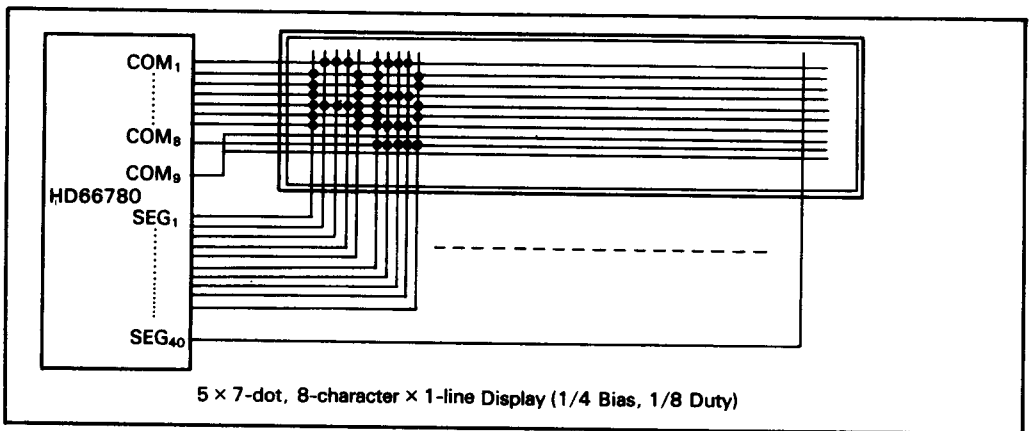


Figure 32 Using COM_9 to Avoid Cross-Talk on Unneeded Scanning Line

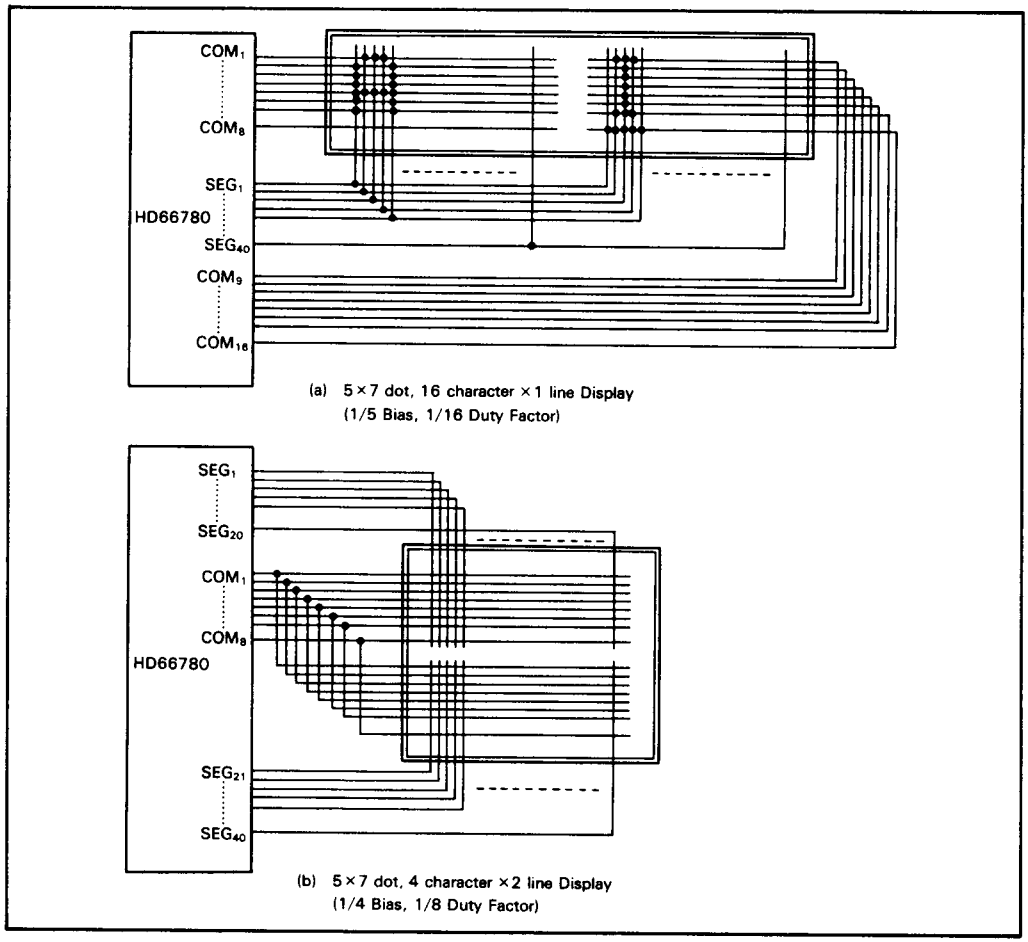


Figure 33 Changed Matrix Layout Displays

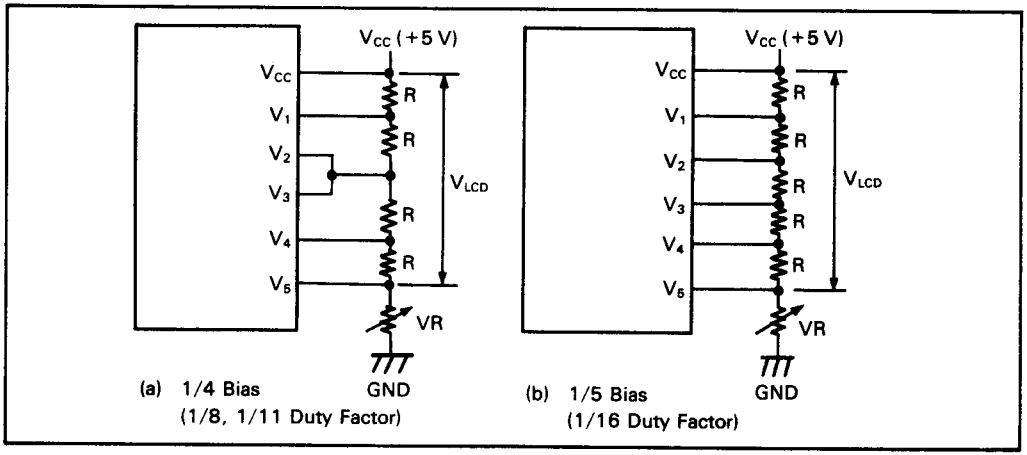
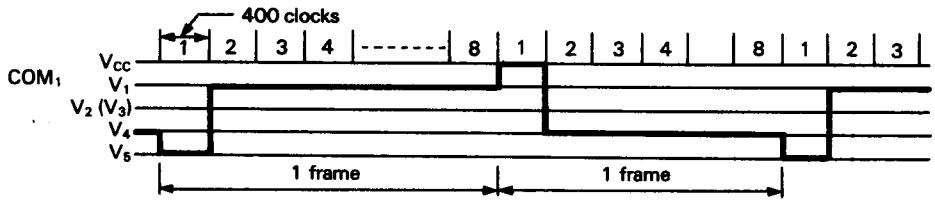


Figure 34 Drive Voltage Supply Example

Up to 9 HD44100Hs can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to 4 for a 2-line display (duty factor 1/16). (For the HD66100F, 5 and 2 units respectively.) RAM size limits the HD66780 to a maximum of 80 character diaplay digits. The connection method in figures 36 and 37 remains unchanged for both 1-line and 2-line display and both 5 × 7-and 5 × 10-dot character fonts.

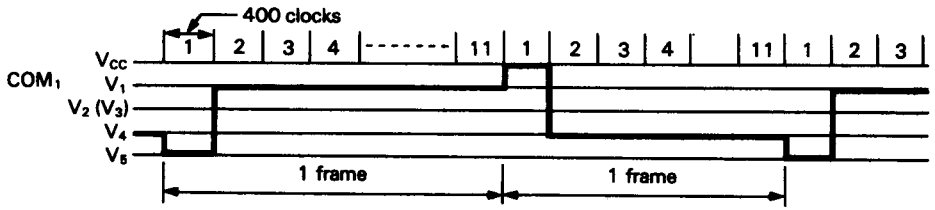
(1) 1/8 Duty Factor



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

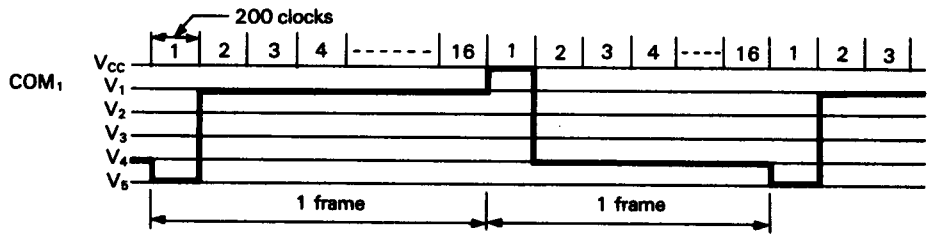
(2) 1/11 Duty Factor



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty Factor



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

Figure 35 Liquid Crystal Display Waveforms (at f_{osc} = 250kHz)

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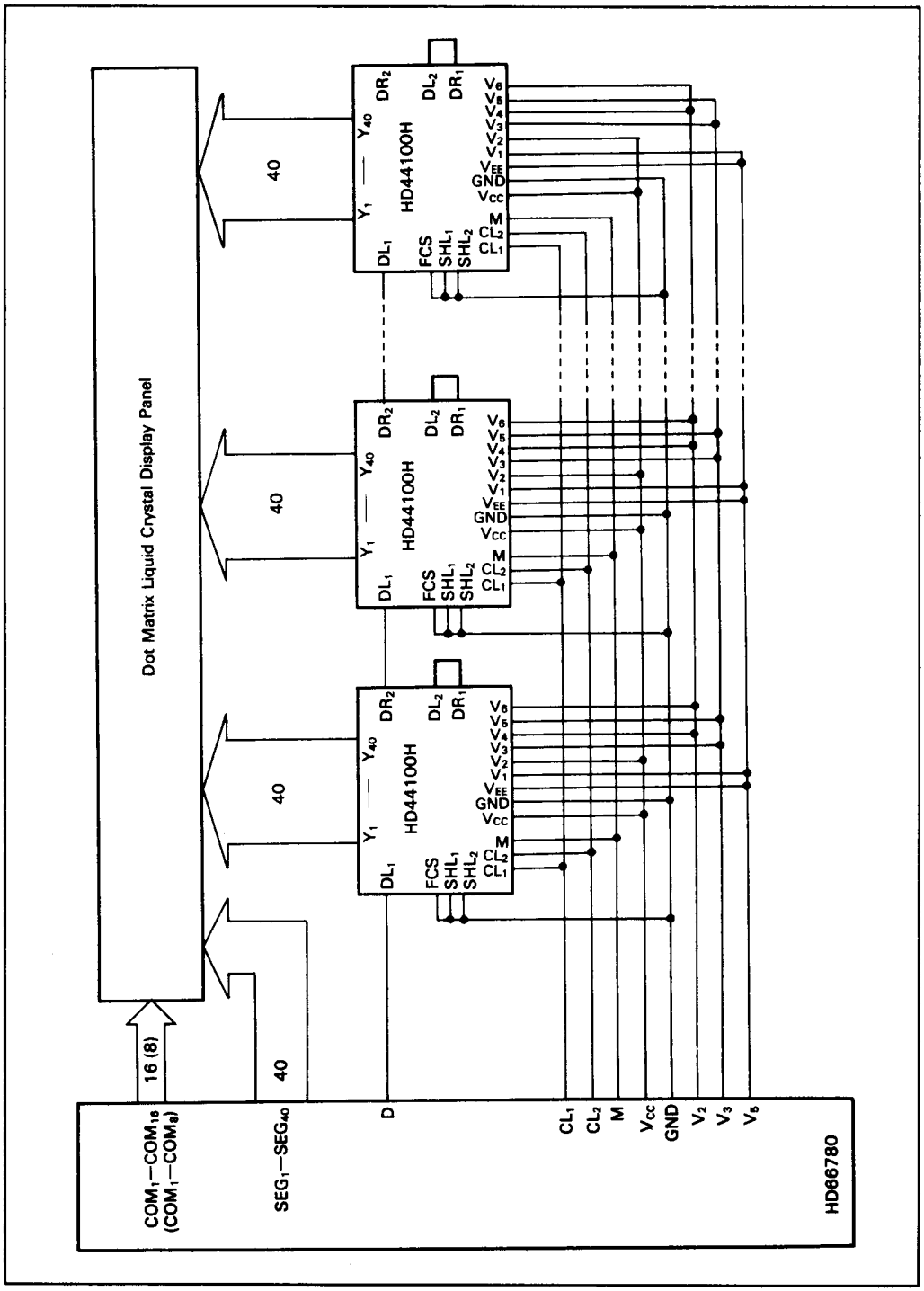

Figure 36 Example of Connecting HD44100H to HD66780

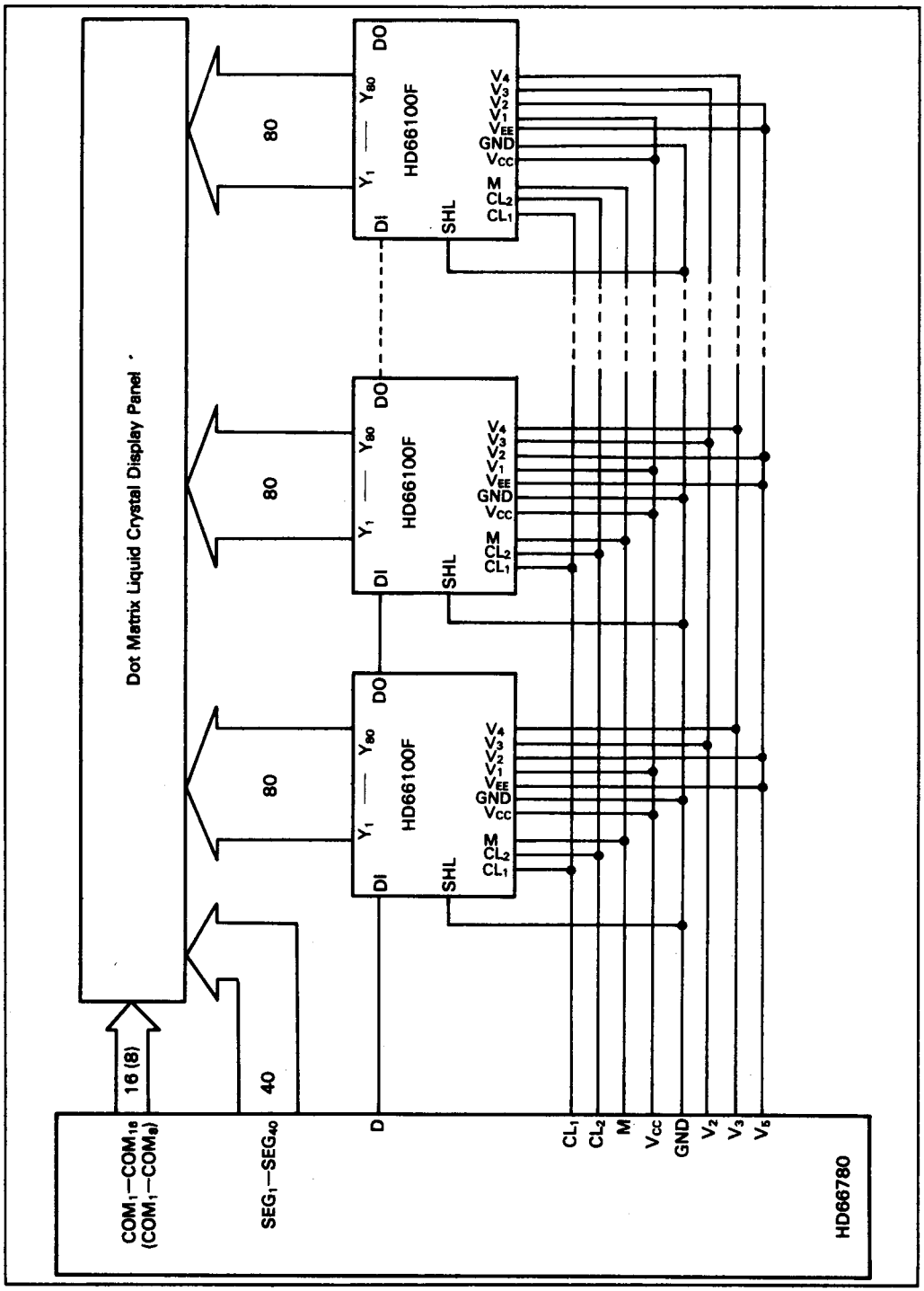

Figure 37 Example of Connecting HD66100F to HD66780

Instruction and Display Correspondence
8-bit Operation, 8-digit × 1-line Display (Using Internal Reset): Table 10 shows an example of an 8-bit × 1-line display in 8-bit operation. The HD66780 functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

4-bit Operation, 8-digit × 1-line Display (Using Internal Reset): The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the LCD-IIA attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two 4-bit accesses, a rewrite is needed to set the functions (see table 11 step 3).

Thus, DB_4-DB_7 of the function set is written twice.

8-bit Operation, 8-digit × 2-line Display: For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set after the eighth character is completed (see table 12). Note that the first and second lines of the display are shifted.

In the example, the display is shifted when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD66780 must be initialized by instruction. (See "Initializing by Instruction")

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the LCD-IIA must be initialized by instruction.
When interface is 8 bits long, use the initialization procedure in figure 38.

When interface is 4 bits long, use the initialization procedure in figure 39.

Table 10 8-Bit Operation, 8-Character × 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

4

Table 11 4-Bit Operation, 8-Character × 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed after this.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

After this, control is the same as 8-bit operation.

Table 12 8-Bit Operation, 8-Character × 2-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and one of the three character fonts.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI	Sets RAM address so that the cursor may be positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the left. The first and second lines' shift is operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

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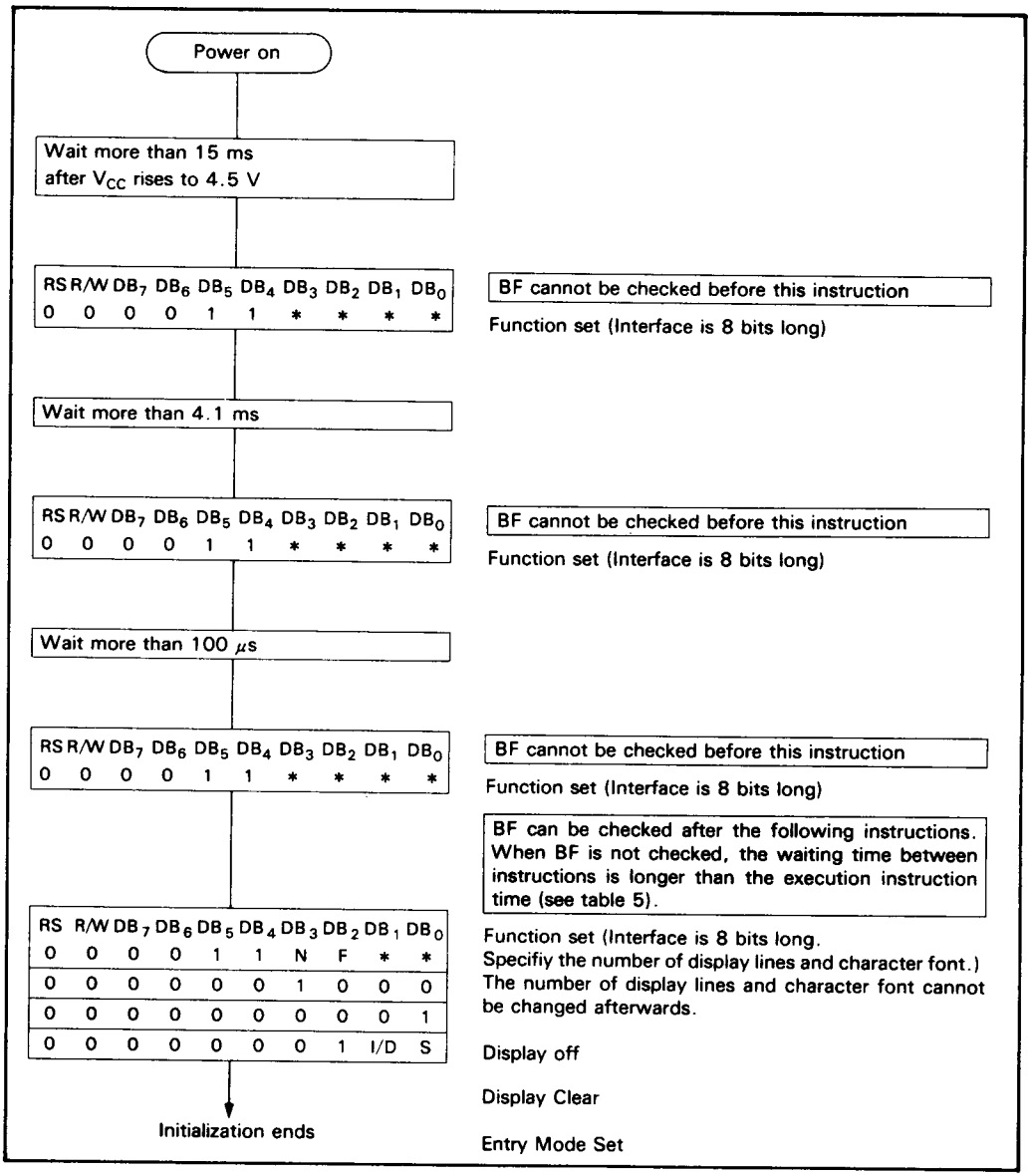


Figure 38 Initialization by Instruction, Eight-Bit Interface

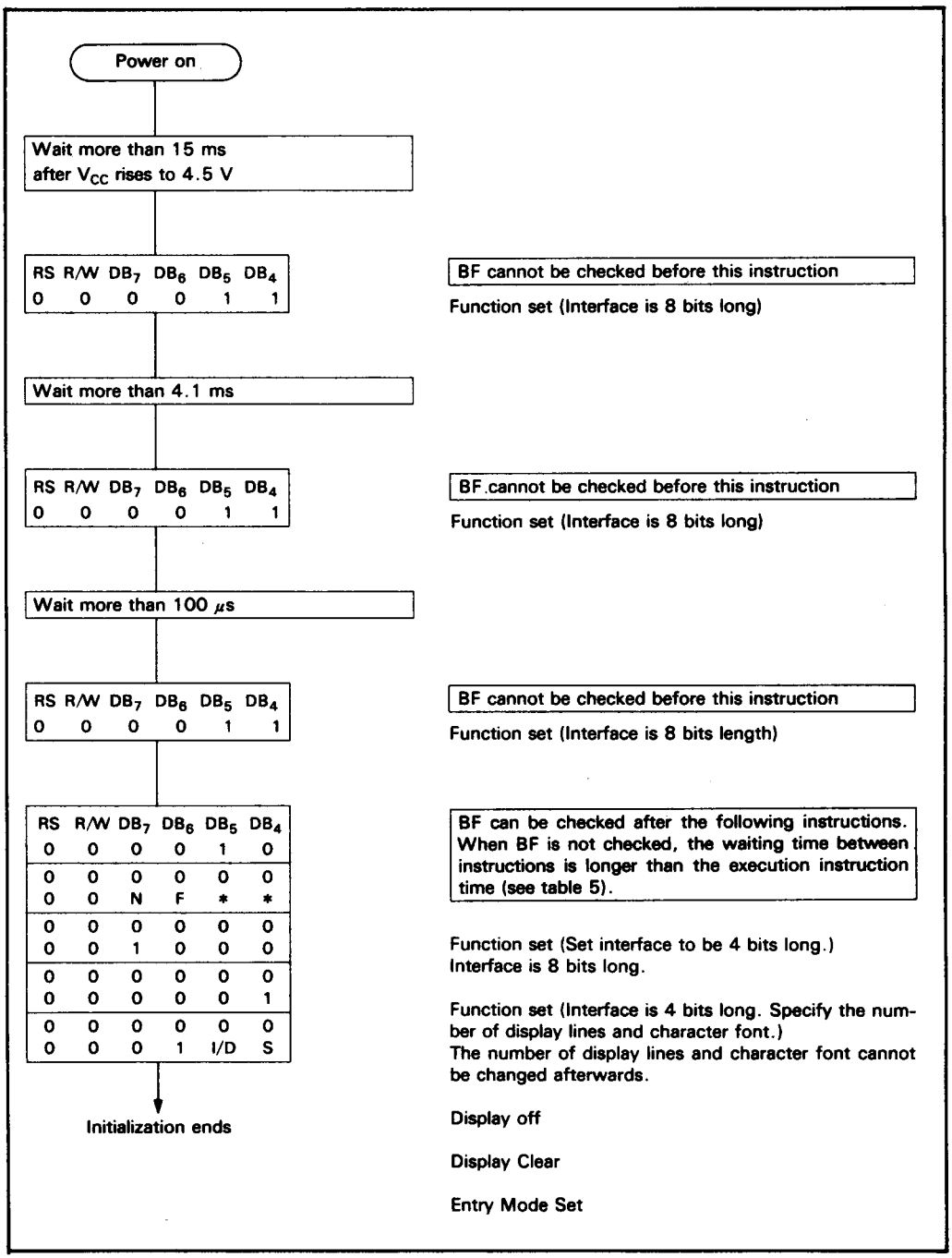


Figure 39 Initialization by Instruction, Four-Bit Interface

LCD-II and LCD-IIA

Table 13 shows the differences between the LCD-II and LCA-IIA.

There are two types of multiplex waveforms for LCD driving: A and B. A type, shown in figure 40, is used for alternation in 1 frame, and B type, shown in figure 41, for alternation in 2 frames. B type has better display quality in highly multiplexed drive.

Table 13 Functions Comparison between LCD-II and LCD-IIA

Item		LCD-II (HD44780)	LCD-IIA (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
*Character generator ROM (Kinds of characters)		7200 bits 192 characters 5×7: 160 characters 5×10: 32 characters	12000 bits 240 characters 5×10: 240 characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COMs 40 SEGs (16 characters)	Same as LCD-II	
Character font (with a cursor)		5×8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16		
*LCD driving voltage	1/4 bias	3.0 to 11 (v)	3.0 to V_{CC} (V)	V_{CC} to V_5 (V)
	1/5 bias	4.6 to 11 (v)	3.0 to V_{CC} (v)	
*LCD driving waveform		A waveform	B waveform	See figures 40,41
*Bus timing		1, 1.5 MHz	2 MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	
Pin arrangement		Refer to p.98	Same as LCD-II	

Note: * indicates the modified items on LCD-IIA.

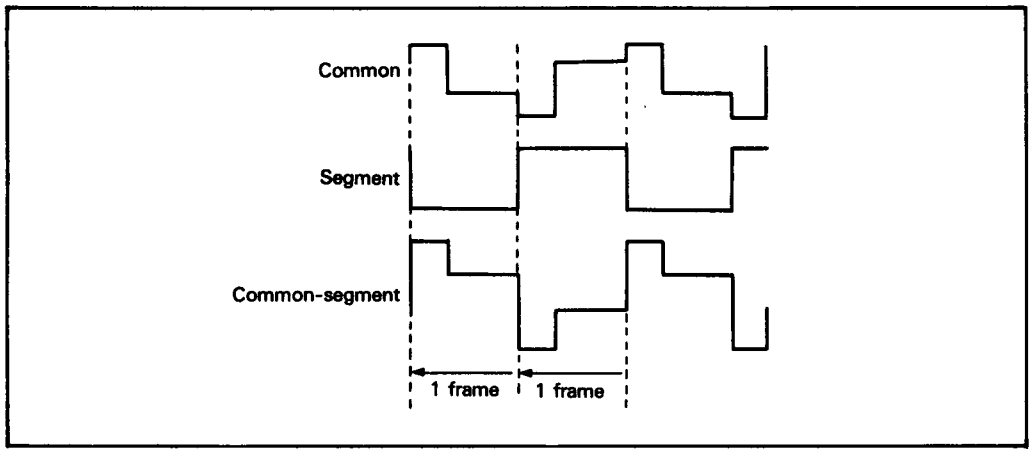


Figure 40 A-Type Waveforms (1/3 Duty Factor, 1/3 Bias)

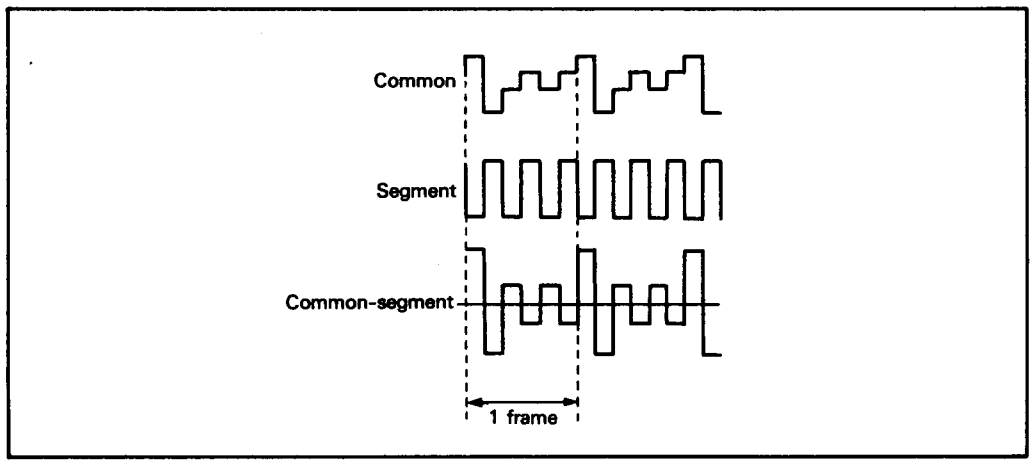


Figure 41 B-Type Waveforms (1/3 Duty Factor, 1/3 Bias)

Character Pattern Development Procedure

The numbers in the above figure correspond to the following operations:

1. Determime the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program character patterns in the EPROM.
4. Send the EPROM to Hitachi.
5. Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.
6. If there is no problem in the character pattern listing, Hitachi creates trial LSIs and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

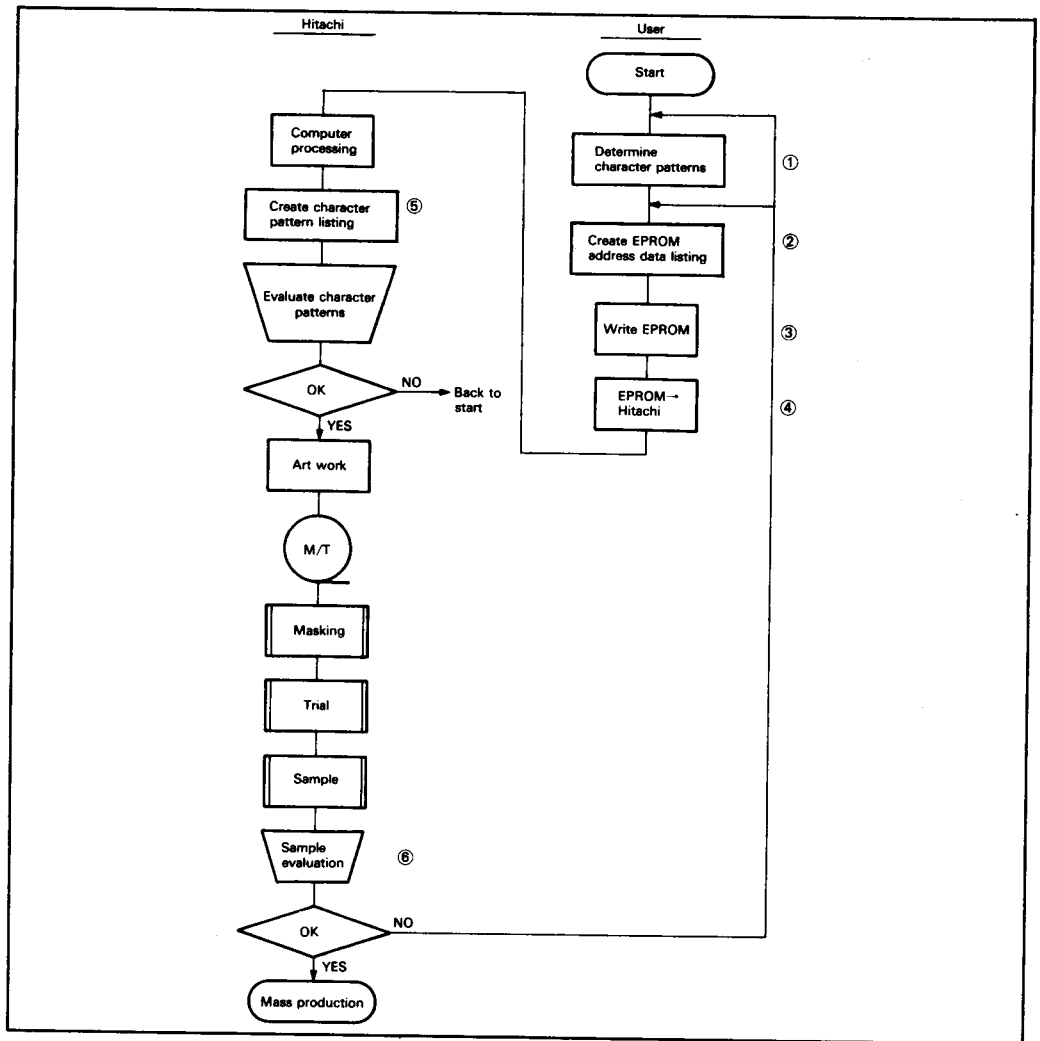


Figure 42 Character Pattern Development Procedure

Character Pattern Program Method

The relationship between the EPROM address and character pattern is shown in table 14.

In order to evaluate ROM patterns, we recommend to use our LCD controller HD61830. We also supply LCD control board (CB1026R).

Table 14 Character Data in EPROM

EPROM Address												Data							
(right sile up)												(LSB)							
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
								0	0	0	0	0	0	0	0	0			
								0	0	0	1	0	0	0	0	0			
								0	0	1	0	0	1	1	0	1			
								0	0	1	1	1	0	0	1	1			
								0	1	0	0	1	0	0	0	1			
1	1	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1			
								0	1	1	0	0	1	1	1	1			
								0	1	1	1	0	0	0	0	1			
								1	0	0	0	0	0	0	0	1			
								1	0	0	1	0	0	0	0	1			
								1	0	1	0	0	0	0	0	0			
								1	0	1	1								
								1	1	0	0								
								1	1	0	1								
								1	1	1	0								
								1	1	1	1								

Character code — Line code

Notes: 1. EPROM Data O_5-O_7 are invalid
2. Data "0" must be programed at 11th line (cursor position).
3. Data at 12-16th line are invalid
4. Data at O_0 locate at the left side of screen. (The relation between the bit number and position is reversed, compared with HD44780.)

Handling Unused Character Patterns

1. EPROM data outside the character pattern area

   Ignored by the character generator ROM for display operation so it can be 0 or 1.

2. EPROM data in CG RAM area

   Ignored by the character generator ROM for display operation so it can be 0 or 1.

3. EPROM data used when the user does not use any LCD-II character pattern

   Handled in one of the two ways explained below. Select one of two ways according to the user application.

   a. When unused character patterns are not programed

      If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because the EPROM is filled with 1 when the EPROM is erased.)

   b. Program 0 for unused character patterns

      Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C

Notes: 1. If LSIs are used above the absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to V1 to V5. The relation: $V_{CC} \geqq V1 \geqq V3 \geqq V4 \geqq V5 \geqq GND$ must be maintained.
(high to low)

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, Ta = -20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition		Note
Input High Voltage (1)	V_{IH1}	2.3	–	V_{CC}	V			(2)
Input Low Voltage (1)	V_{IL1}	–	–	0.6	V			(2)
Input High Voltage (2)	V_{IH2}	V_{CC} - 1.0	–	V_{CC}	V			(12)
Input Low Voltage (2)	V_{IL2}	–	–	1.0	V			(12)
Output High Voltage (1)(TTL)	V_{OH1}	2.4	–	–	V	$-I_{OH}$ = 0.205 mA		(3)
Output Low Voltage (1)(TTL)	V_{OL1}	–	–	0.4	V	I_{OL} = 1.6 mA		(3)
Output High Voltage (2)(CMOS)	V_{OH2}	0.9V_{CC}	–	–	V	$-I_{OH}$ = 0.04 mA		(4)
Output Low Voltage (2)(CMOS)	V_{OL2}	–	–	0.1V_{CC}	V	I_{OL} = 0.04 mA		(4)
Driver On Resistance (COM)	R_{COM}	–	–	20	kΩ	±Id = 0.05 mA to each COM Pin		(10)
Driver On Resistance (SEG)	R_{SEG}	–	–	30	kΩ	±Id = 0.05 mA to each SEG Pin		(10)
Input Leakage Current	I_{IL}	-1	–	1	μA	V_{in} = 0 to V_{CC}		(5)
Pull up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V		
Power Supply Current (1)	I_{CC1}	–	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz		(6)
Power Supply Current (2)	I_{CC2}	–	0.35	0.6	mA	Rf oscillation, External clock operation V_{CC} = 5 V, f_{OSC} = fcp = 270 kHz		(6) (11)
External Clock Operation								
External Clock Frequency	f_{cp}	125	250	350	kHz			(7)
External Clock Duty	Duty	45	50	55	%			(7)
External Clock Rise Time	t_{rcp}	–	–	0.2	μs			(7)
External Clock Fall Time	t_{fcp}	–	–	0.2	μs			(7)
Internal Clock Operation (Rf Oscillation)								
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 82 kΩ±2%		(8)
Internal Clock Operation (Ceramic Filter Oscillation)								
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter		(9)
LCD Voltage	V_{LCD1}	3.0	–	V_{CC}	V	V_{CC} - V_5	1/5 bias	(13)
	V_{LCD2}	3.0	–	V_{CC}	V		1/4 bias	(13)

Notes:
1. Figure 43 shows the I/O pin configurations except for liquid crystal display output.
2. Input pins and I/O pins. Excludes OSC_1 pin.
3. I/O pins.
4. Output pins.
5. Current flowing through pull-up MOS's and output drive MOS's is excluded.
6. Input/output current is excluded. When input is at an intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.
7. External clock operation as shown in figure 44.
8. Internal oscillator operation using oscillation resistor Rf (figure 45).
9. Internal oscillator operation using a ceramic filter (figure 46).
10. R_{COM} applies to the resistance between power supply pin (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).
    R_{SEG} applies to the resistance between power supply pin (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

4

11. Relation between operation frequency and current consumption is shown in figure 47. (V_{CC} = 5 V)
12. Applied to OSC_1 pin.
13. When each COM and SEG output voltage is within ±0.15 V of LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

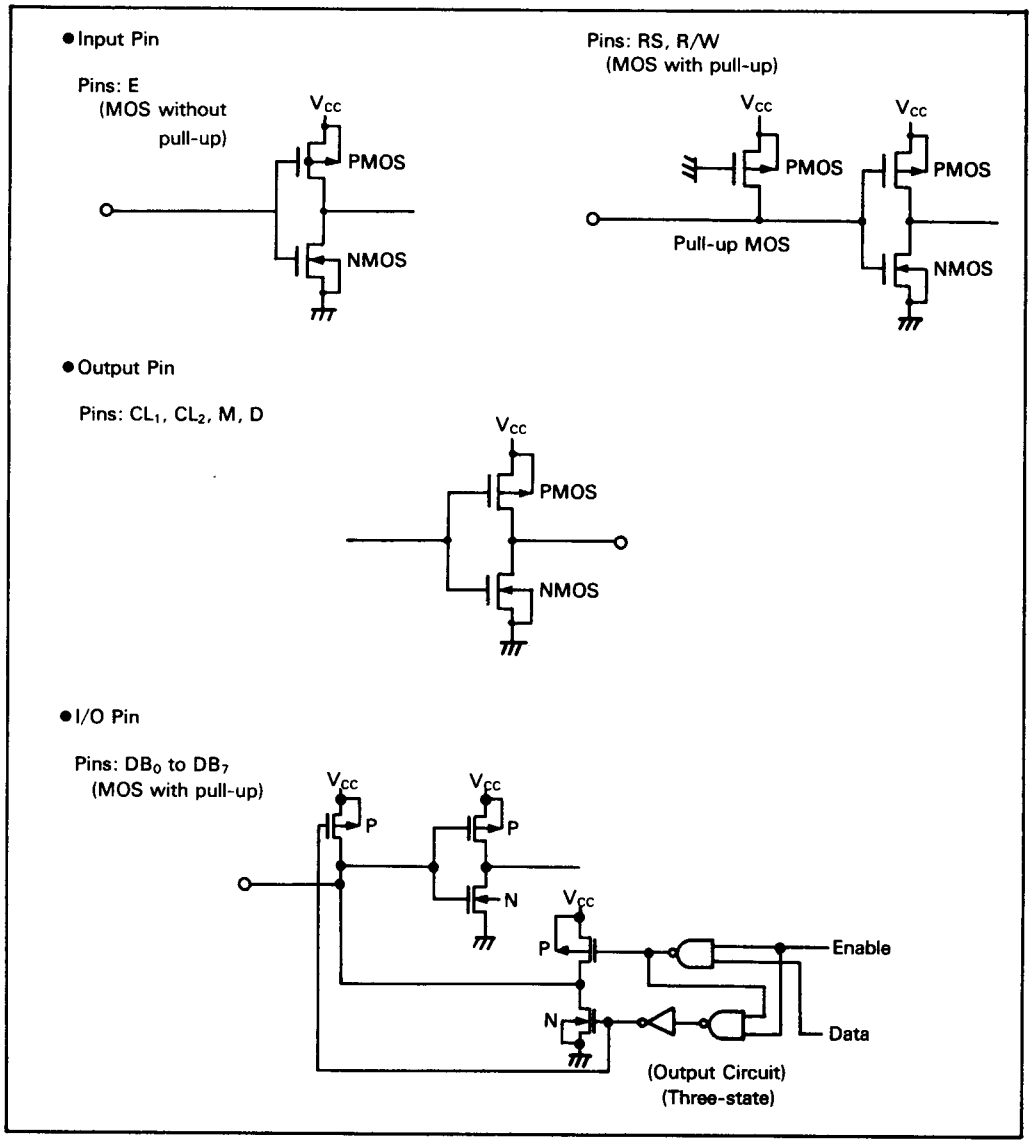


Figure 43 Pin Configuration

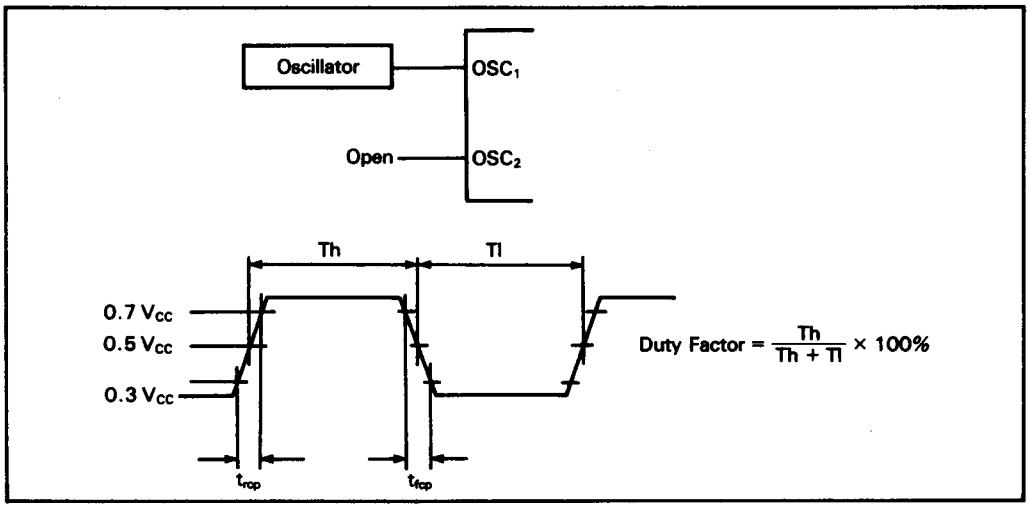


Figure 44 External Clock

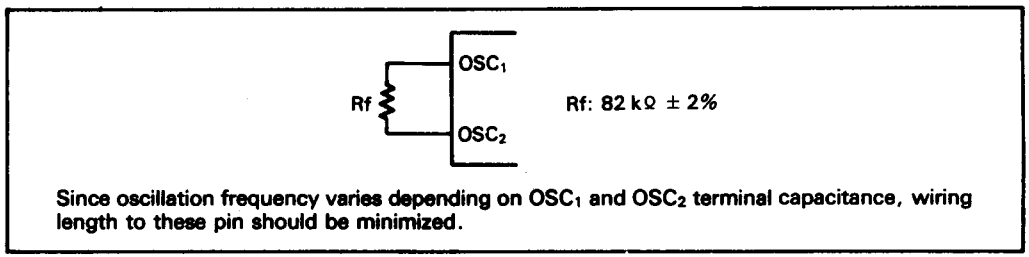


Figure 45 Internal Oscillator, Resistor

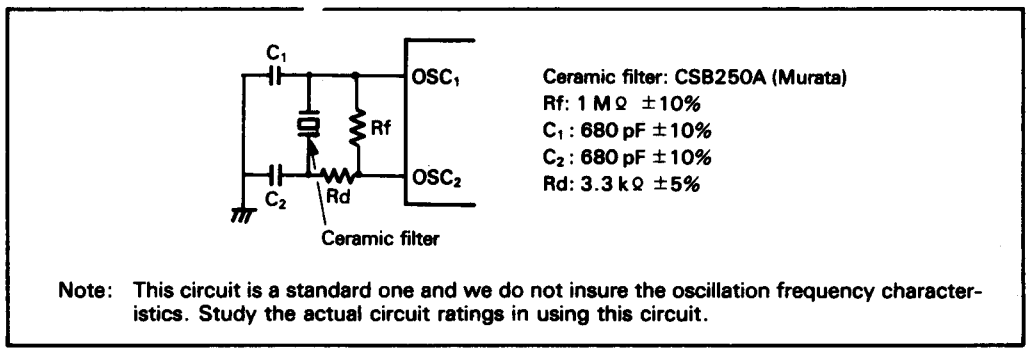


Figure 46 Internal Oscillator, Ceramic Filter

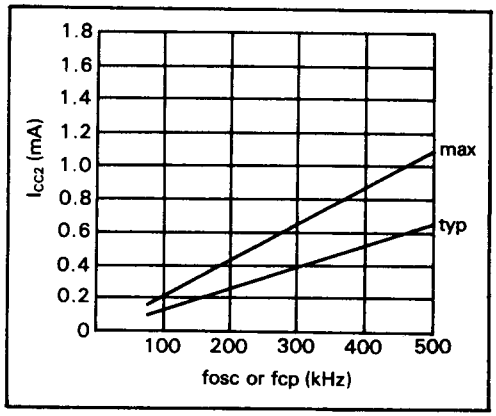
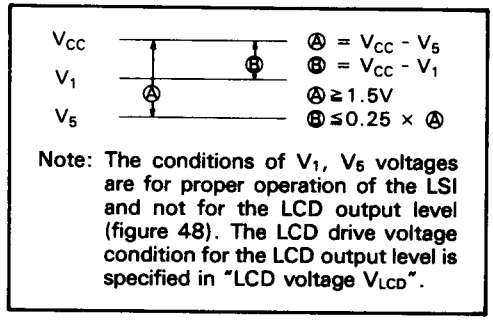


Figure 47 Frequency vs Current



Note: The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level (figure 48). The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Figure 48 V_1, V_5 Voltages

Bus Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Write Operation (Writing Data from MPU to HD66780)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 52
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 52
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 52
Address Set-up Time (RS, R/W–E)	t_{AS}	40	–	ns	Fig. 52
Address Hold Time	t_{AH}	10	–	ns	Fig. 52
Data Set-up Time	t_{DSW}	60	–	ns	Fig. 52
Data Hold Time	t_H	10	–	ns	Fig. 52

Read Operation (Reading Data from HD66780 to MPU)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 53
Enable Pulse Width (High level)	PW_{EH}	250	–	ns	Fig. 53
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 53
Address Set-up Time (RS, R/W–E)	t_{AS}	40	–	ns	Fig. 53
Address Hold Time	t_{AH}	10	–	ns	Fig. 53
Data Delay Time	t_{DDR}	–	250	ns	Fig. 53
Data Hold Time	t_{DHR}	20	–	ns	Fig. 53

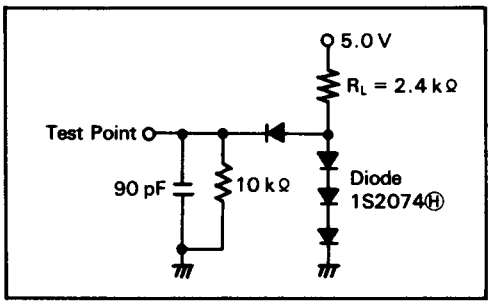


Figure 49 Load Circuit (DB_0–DB_7)

Interface Signal with HD44100H or HD66100F Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Item		Symbol	Min	Max	Unit	Test Condition
Clock Pulse Width	(High level)	t_{CWH}	800	–	ns	Fig. 54
Clock Pulse Width	(Low level)	t_{CWL}	800	–	ns	Fig. 54
Clock Set-up Time		t_{CSU}	500	–	ns	Fig. 54
Data Set-up Time		t_{SU}	300	–	ns	Fig. 54
Data Hold Time		t_{DH}	300	–	ns	Fig. 54
M Delay Time		t_{DM}	-1000	1000	ns	Fig. 54
Clock Rise/Fall Time		t_{ct}	–	100	ns	Fig. 54

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Max	Unit	Test Condition
Power Supply Rise Time	t_{rCC}	0.1	10	ms	Fig. 51
Power Supply Off Time	t_{OFF}	1	–	ms	Fig. 51

Note: The internal reset circuit will not operate normally unless the preceding conditions are met. In that case, initialize by instruction. (Refer to Initializing by Instruction)

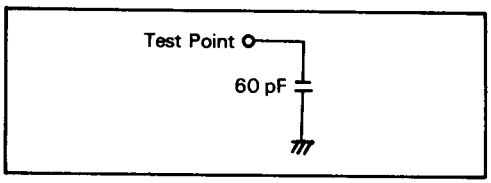


Figure 50 Interface Signal Load Circuit

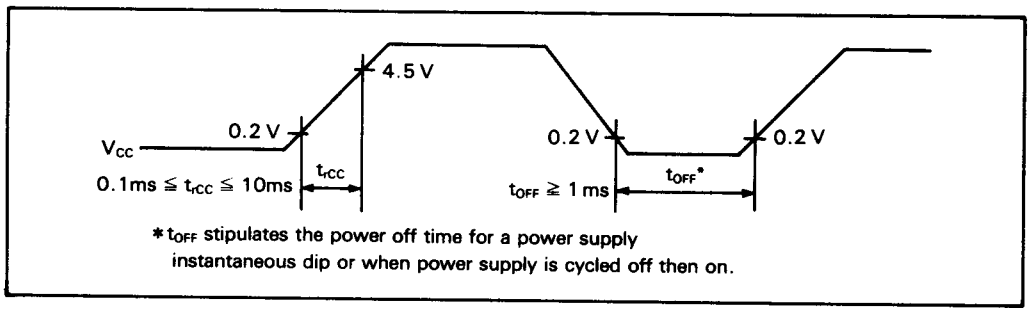


Figure 51 Power Supply Timing

Timing Characteristics

Write Operation

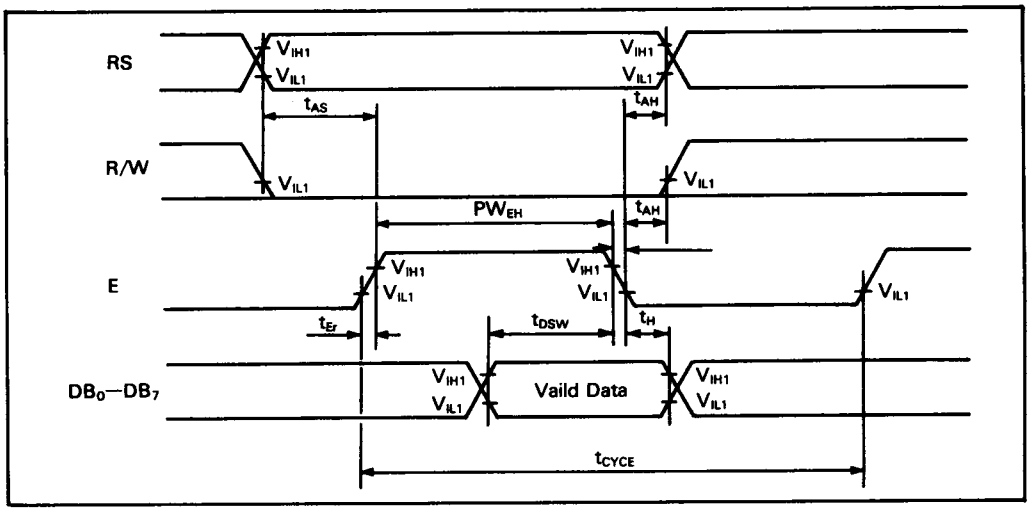


Figure 52 Bus Write Operation Sequence (Writing Data from MPU to HD66780)

Read Operation

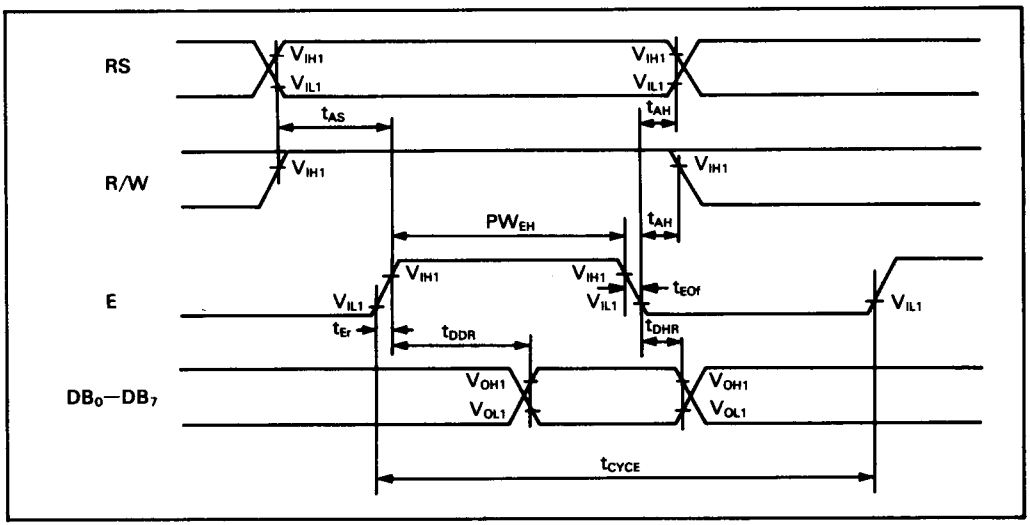


Figure 53 Bus Read Operation Sequence (Reading Data from HD66780 to MPU)

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Interface Signal with Driver LSI HD44100H or HD66100F

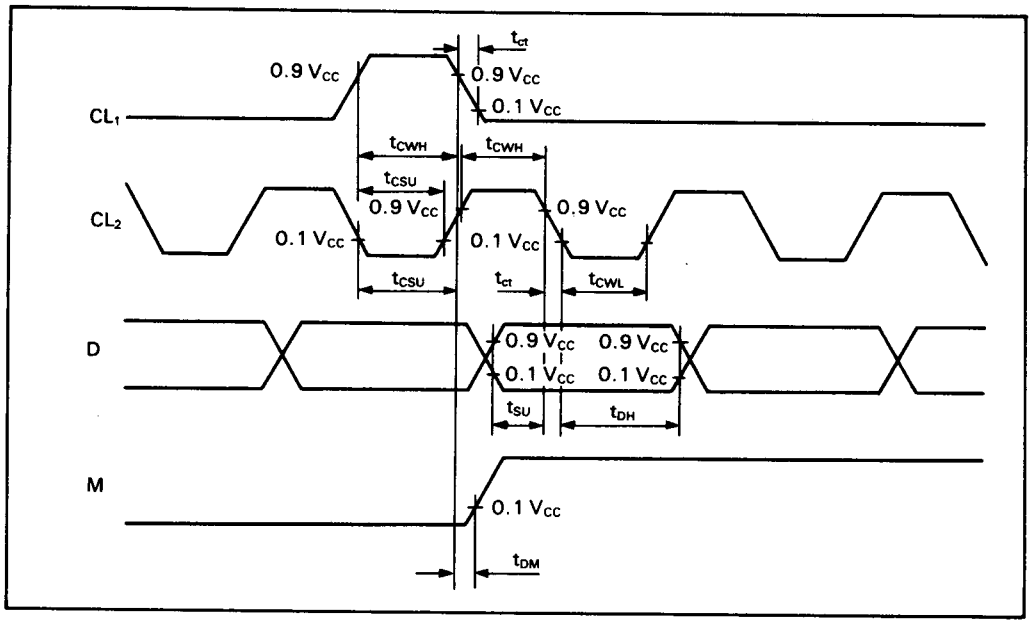

Figure 54 Sending Data to Driver LSI HD44100H or HD66100F