HD66215T

(Common Driver for a Dot Matrix Liquid Crystal Graphic Display with 100-Channel Outputs)

HITACHI

Description

The HD66215T is a common driver for a large dot matrix liquid crystal graphic display (LCD). The driver's 100 channels can be divided into two groups of 50 channels by selecting data input/output pins. Outputs X_1 to X_{10} and X_{91} to X_{100} can be disabled by mode selection. Unused output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. A 101-channel output mode can also be selected for an application to various display panels. The driver is powered by about 3V, making it suitable for battery-driven portable equipment featuring the low power dissipation of liquid crystal elements.

The HD66215T, packaged in a micro-tape carrier package (micro-TCP), allows design of a compact LCD system with a frame (an area peripheral to the LCD panel) about half the width of conventional systems.

Features

- Duty cycle: About 1/64 to 1/240
- 100 internal LCD drive circuits (101-channel mode can be selected for a 101-output version)
- High output voltage for driving the LCD: 10 to 28 V
- Output division function (50 × 2-output)
- 10-output through modes
- 101-output mode
- Display off function
- Internal 100-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- Micro-TCP with 3-sprocket-hole width
- Operating voltage: 2.5 to 5.5 V

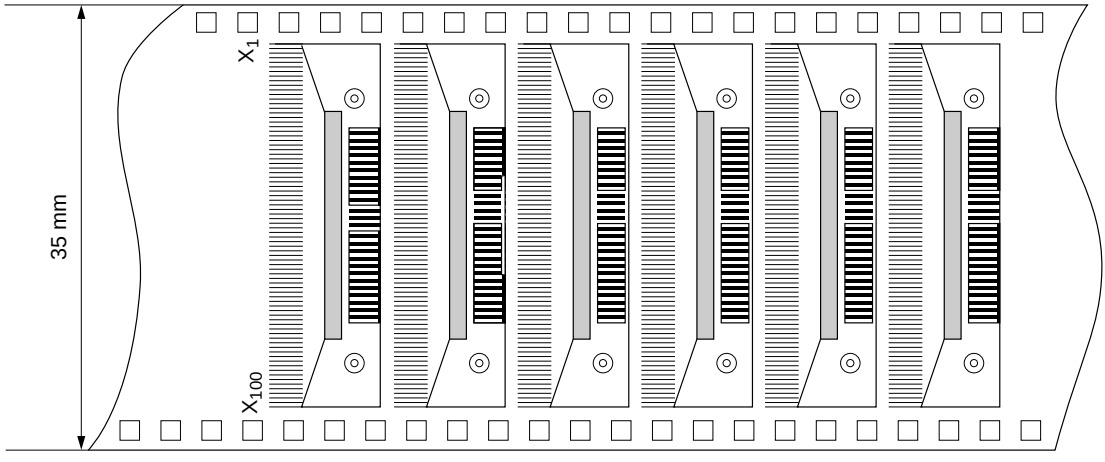
Ordering Information

Type No.	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66215TA0	0.23 mm	1.20 mm	3 sprocket holes
HD66215TA1	0.22 mm	1.00 mm	3 sprocket holes
HD66215TA2	0.18 mm	0.85 mm	3 sprocket holes

Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in "The Information of TCP."

Hitachi semiconductor

Tape Carrier Package



Pin Arrangement

1	V_1L
2	V_6L
3	V_5L
4	$V_{EE}L$
5	MODE1
6	DIO4
7	$\overline{\text{DISPOFF}}$
8	V_{CC}
9	SHL/R
10	DIO3
11	DIO2
12	GND
13	M
14	CL
15	DIO1
16	MODE2
17	$V_{EE}R$
18	V_5R
19	V_6R
20	V_1R

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	8	V_{CC}	—	Power supply
GND	12	GND		
V_1L, V_1R	1, 20	V_1L, V_1R	Input	
V_6L, V_6R	2, 19	V_6L, V_6R		
V_5L, V_5R	3, 18	V_5L, V_5R		
$V_{EE}L$, $V_{EE}R$	4, 17	$V_{EE}L$, $V_{EE}R$		
CL	14	Clock		Control signal
M	13	M		
SHL/R	9	Shift left/right		
DIO1	15	Data	Input/output	
DIO2	11			
DIO3	10			
DIO4	6			
$\overline{DISPOFF}$	7	Display off	Input	
MODE1, MODE2	5, 16	Mode1, Mode2		
X_1–X_{100}	21–120	X_1–X_{100}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_1L, V_1R, V_5L, V_5R, V_6L, V_6R, $V_{EE}L$, $V_{EE}R$: Supply different levels of power to drive the LCD. V_1 and V_{EE} are selected levels, and V_5 and V_6 are non-selected levels. See figure 1.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes LCD drive outputs to AC.

SHL/R: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1–DIO4: Input or output data. DIO1 and DIO2 are data input/output pins for X_1–X_{50}, and DIO3 and DIO4 are input/output pins for X_{51}–X_{100} (X_{101}) in 50 × 2-output modes. In a 100-output mode, DIO2 and DIO3 must be short-circuited, and DIO1 and DIO4 are used as data input/output pins.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets LCD drive outputs X_1–X_{100} (X_{101}) to V_1 level.

MODE1, MODE2: Select an LCD output mode (table 1). In 10-output through modes, ten unused output pins are made invalid. These ten pins must be open in these modes since they output M signals.

LCD Drive Outputs

X_1–X_{100}: Each X outputs one of the four voltage levels, V_1, V_5, V_6, or V_{EE}, depending on a combination of the M signal and data levels. See figure 3.

Table 1 Selection of LCD Output

MODE1	MODE2	Selected Mode
0	0	Normal (100-output)
0	1	10-output through (X_1–X_{10})
1	0	(X_{91}–X_{100})
1	1	101-output

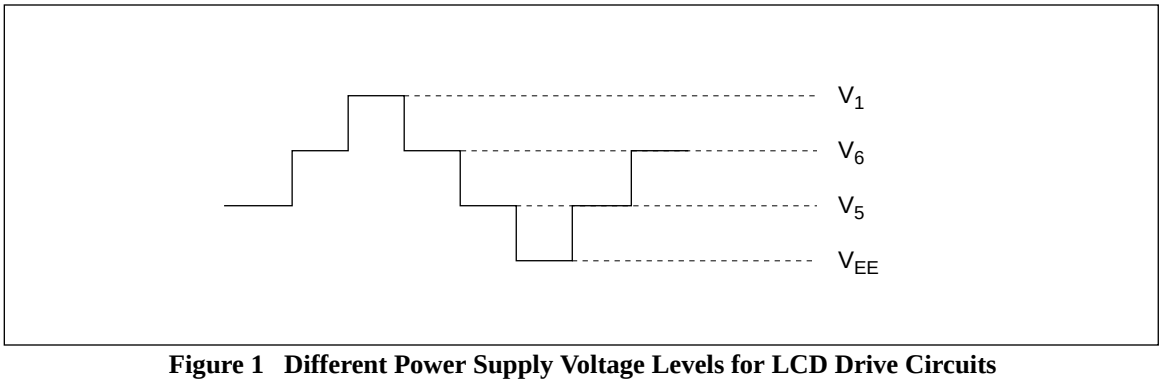


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 100 × 1-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 100 × 1-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{100} \rightarrow X_{51}$

For 10-output through modes and 101-output mode, see Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Each Mode.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Normal Mode (100-Output Mode)

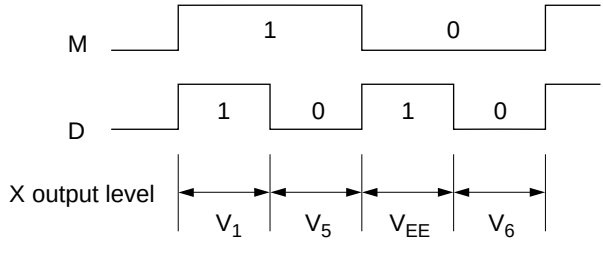
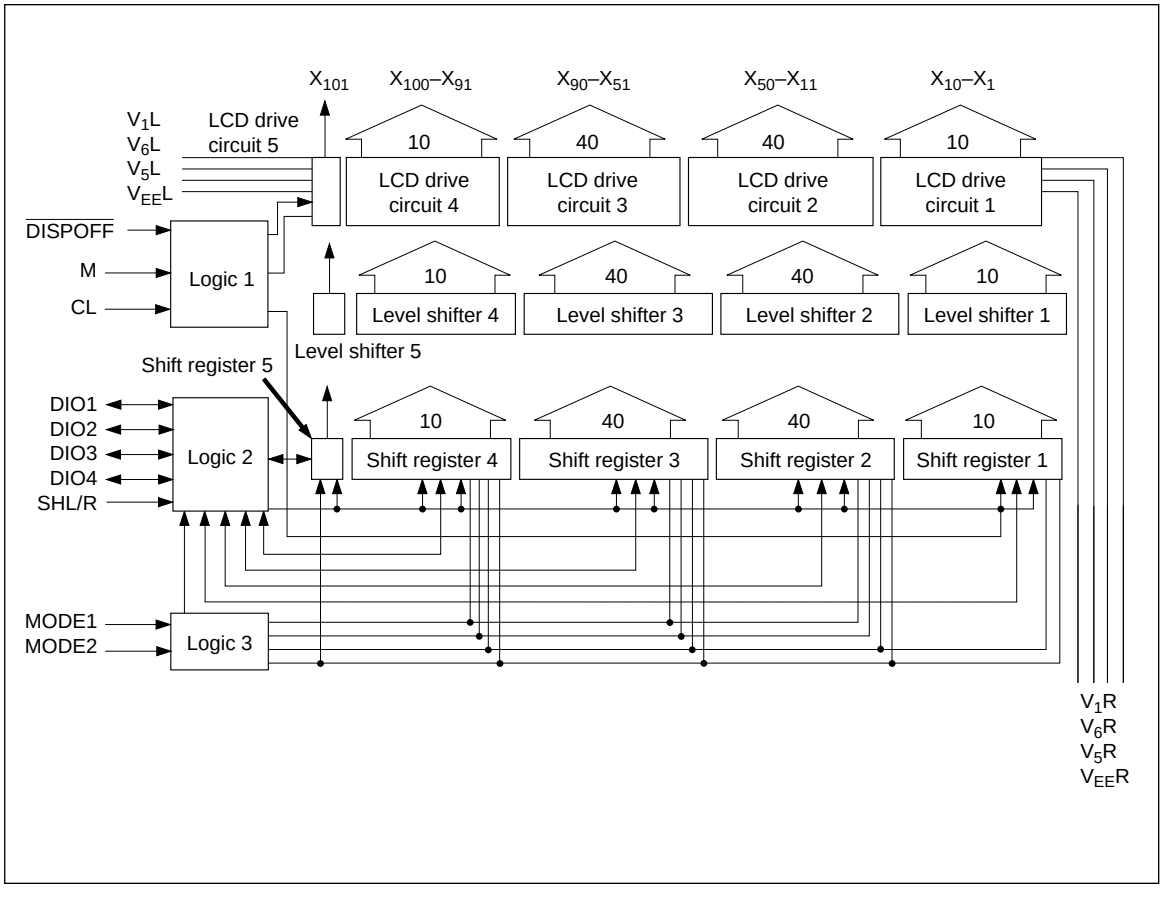


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuits

The 100-bit LCD drive circuits generate four voltage levels, V_1, V_5, V_6, and V_{EE}, which drive an LCD panel. One of the four levels is output to the corresponding X pin, depending on a combination of the M signal and the data in the shift register.

Level Shifters

The level shifters change logic control signals (2.5 to 5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Registers

The 100-bit shift registers shift data input via the DIO pin by one bit. The bit that is shifted out is output from the DIO pin to the next driver IC. Both shifting and output occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL/R pin selects the data shift direction.

Logic 3

Logic 3 selects which shift register operates depending on the settings of MODE1 and MODE2.

Data Shift and Common Signal Scan Direction

Figure 4–7 show the data shift direction and common signal scan direction selected by SHL/R and DIO pins in each mode.

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 100 × 1-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 100 × 1-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{100} \rightarrow X_{51}$

Figure 4 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 100-Output Mode (MODE1 = 0 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 90-output mode				
	Input	Short-circuited		Output	$X_{11} \rightarrow X_{100}$
	In 40- and 50-output mode				
	Input	Output	Input	Output	$X_{11} \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 90-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_{11}$
	In 40- and 50-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_{11}$
					$X_{100} \rightarrow X_{51}$

Figure 5 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO pins in 10-Output (X_1–X_{10}) Through Mode (MODE1 = 0 and MODE 2 = 1)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 90-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{90}$
	In 50- and 40-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{90}$
High	In 90-output mode				
	Output	Short-circuited		Input	$X_{90} \rightarrow X_1$
	In 50- and 40-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{90} \rightarrow X_{51}$

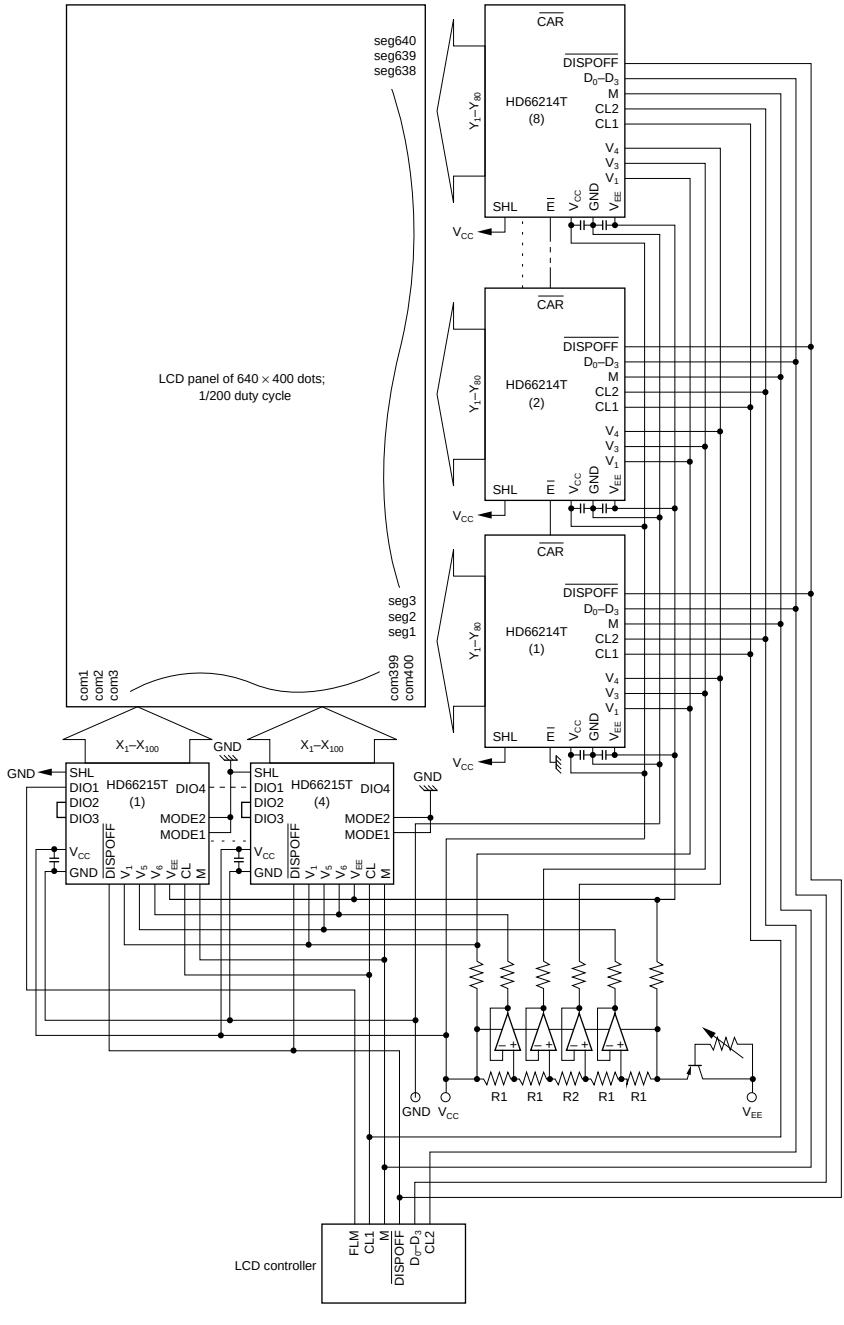
Figure 6 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 10-Output (X_{91}–X_{100}) Through Mode (MODE1 = 1 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 101-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{101}$
	In 50- and 51-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{101}$
High	In 101-output mode				
	Output	Short-circuited		Input	$X_{101} \rightarrow X_1$
	In 50- and 51-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{101} \rightarrow X_{51}$

In 101-output mode, any 10-output through mode cannot be used.

Figure 7 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 101-Output Mode (MODE1 = 1 and MODE2 = 1)

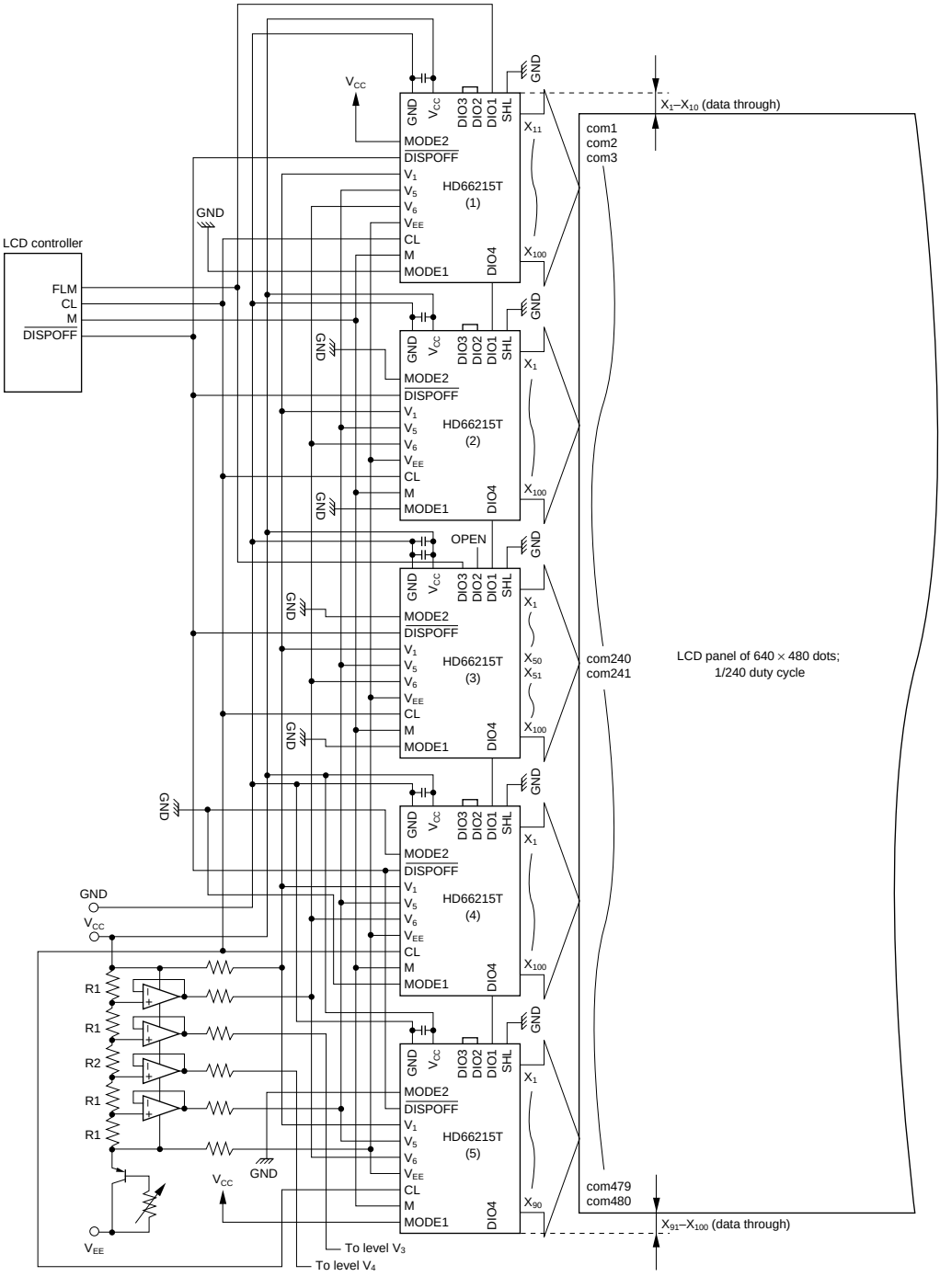
Application Examples



Notes: 1. The resistances of R1 and R2 depend on the type of LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 8 LCD Panel of 640 × 400 Dots, 1/200 Duty Cycle



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2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 9 LCD Panel of 640 × 480 Dots, 1/240 Duty Cycle

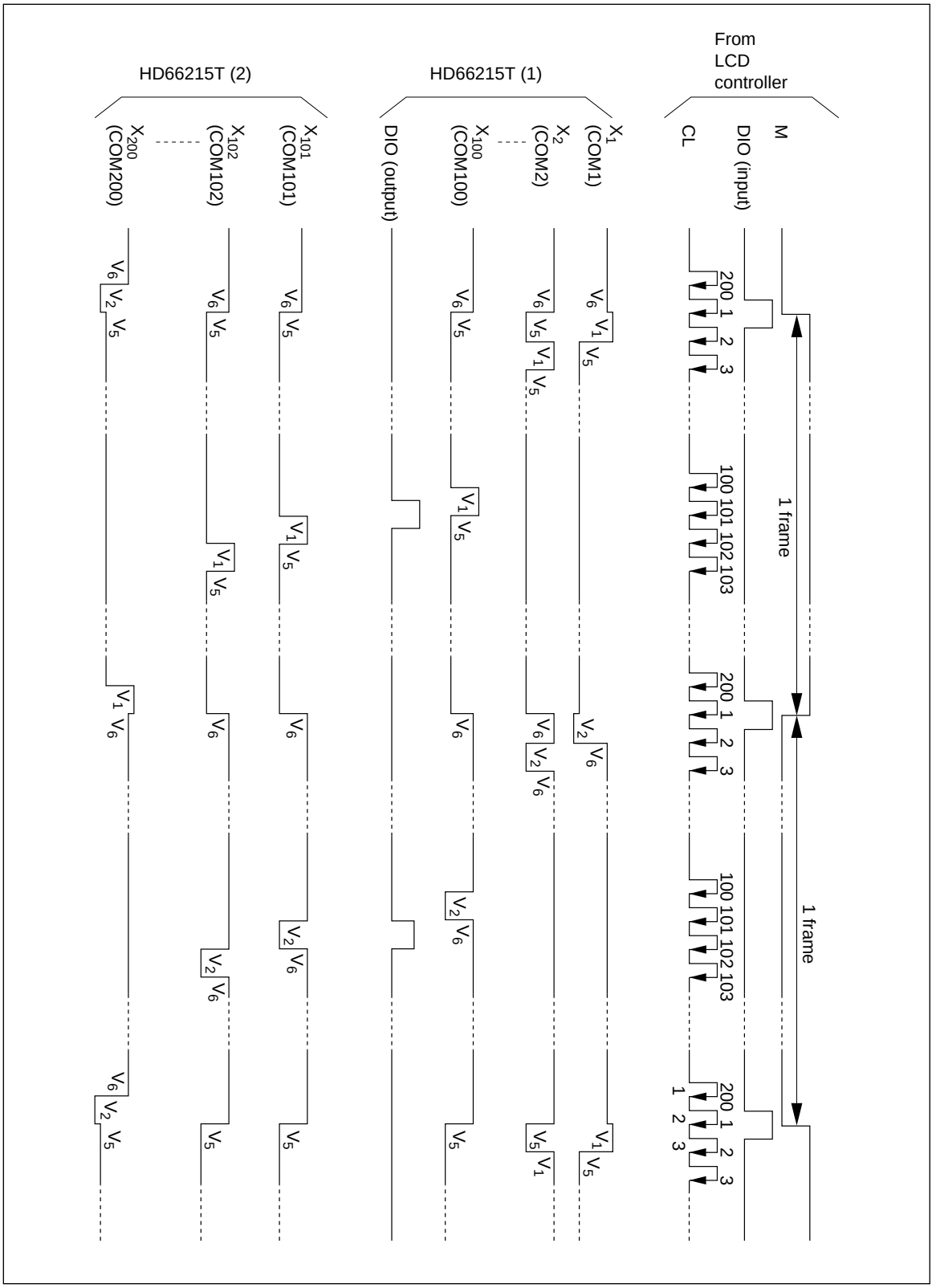

Figure 10 Operational Timing in Normal Mode (100-Output Mode, 1/200 Duty Cycle)

HD66215T Connection Examples

Figure 11 shows an example of an HD66215T driving a 480-line LCD panel with a 1/240 to 1/250 duty cycle. Here, selecting MODE1 and MODE2 disables outputs X_1–X_{10} of driver IC1 and outputs X_{91}–X_{100} of driver IC5. As a result, unused driver output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. In addition, since the 100 channels of the driver can be divided into two groups of 50 channels by selecting data input/output pins, data input is divided at the center of the panel (IC3).

Figure 12 shows an example of an HD66215T driving a 400-line LCD panel with a 1/200 to 1/210 duty cycle.

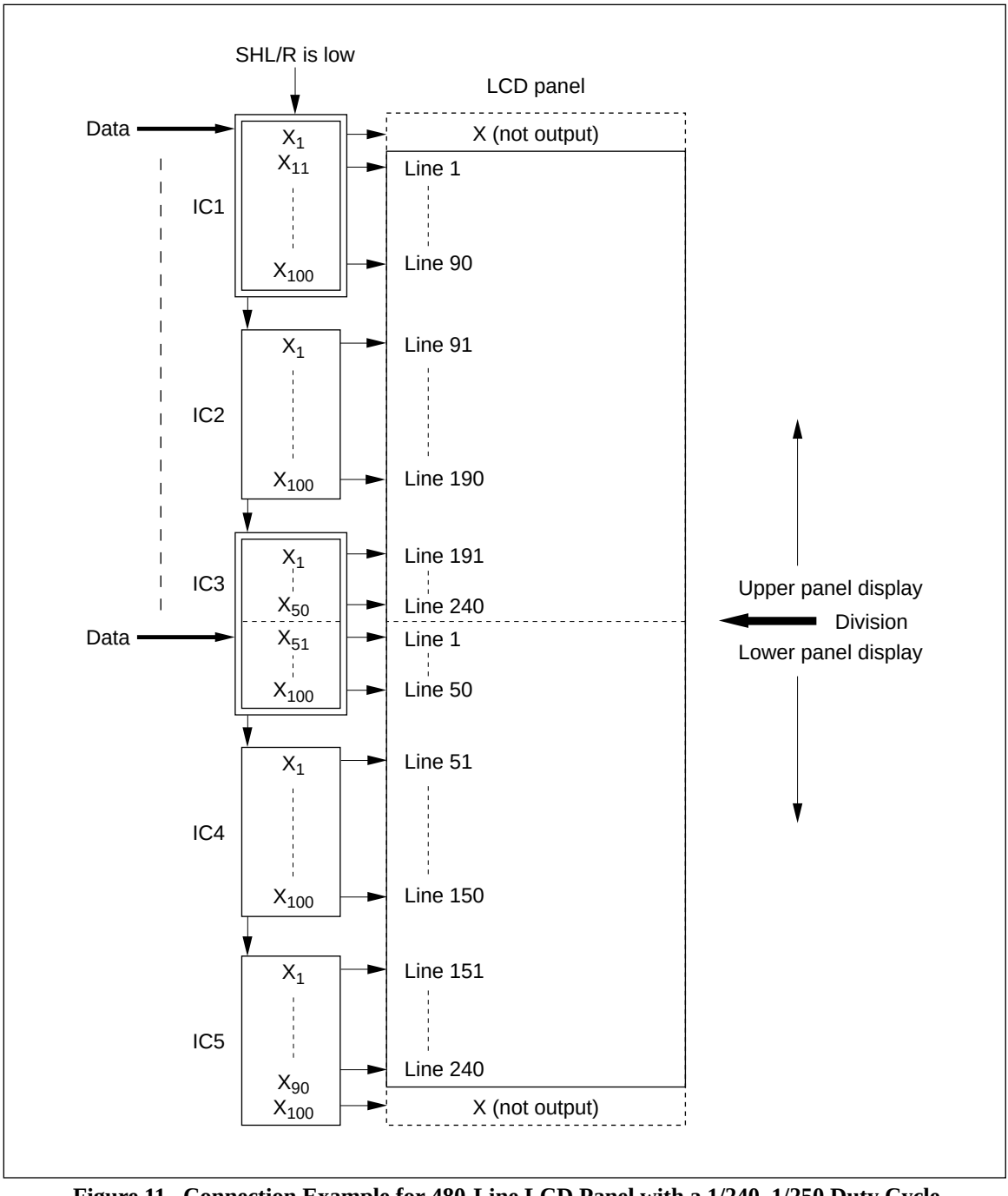

Figure 11 Connection Example for 480-Line LCD Panel with a 1/240–1/250 Duty Cycle

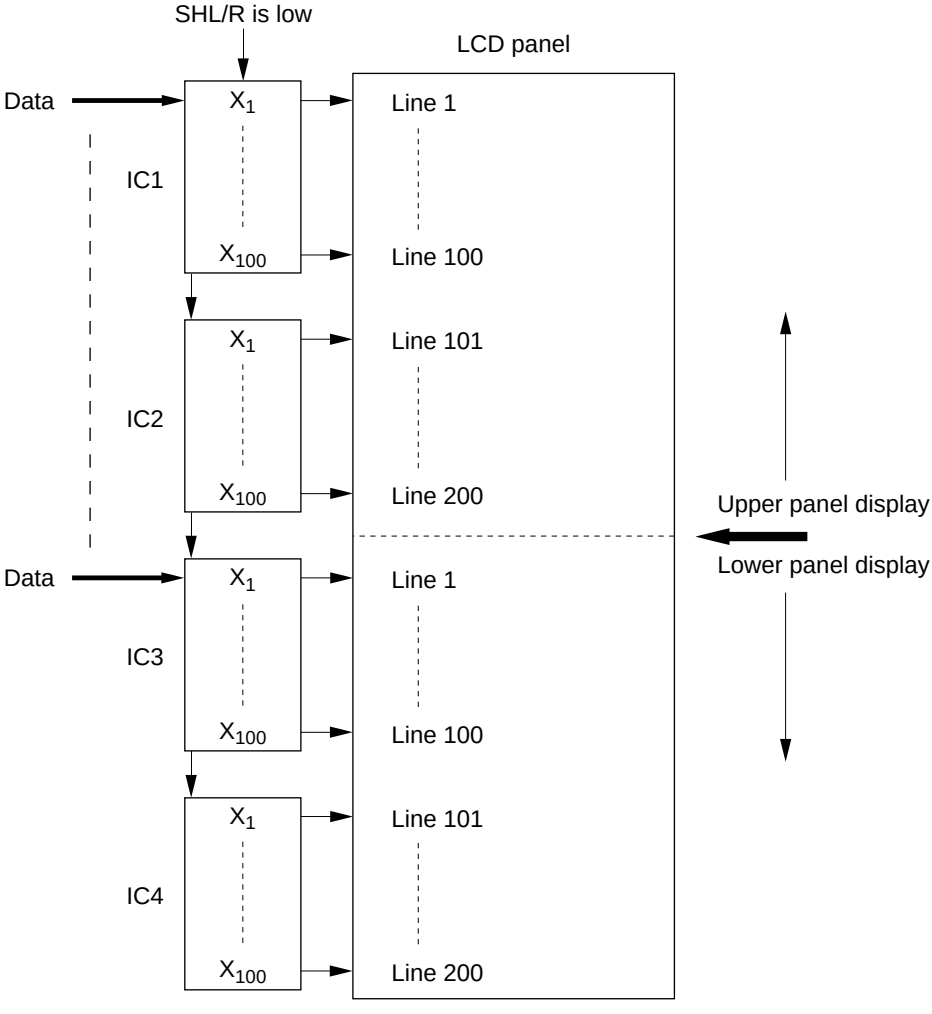

Figure 12 Connection Example for 400-Line LCD Panel with a 1/200–1/210 Duty Cycle

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits		V_{CC}	–0.3 to +7.0	V	2
Power supply voltage for LCD drive circuits		V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage	1	V_{T1}	–0.3 to V_{CC} + 0.3		2, 3
	2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3		2, 4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125		

Notes: 1. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunction or unreliability.

2. The reference point is GND (0 V).
3. Applies to pins CL, M, SHL/R, DIO1–DIO4 (input), $\overline{\text{DISPOFF}}$.
4. Applies to pins V_1, V_5, and V_6.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item		Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage		V_{IH}	1	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low voltage		V_{IL}	1	0	—	$0.3 \times V_{CC}$			
Output high voltage		V_{OH}	2	V_{CC} – 0.4	—	—		I_{OH} = –0.4 mA	
Output low voltage		V_{OL}	2	—	—	0.4		I_{OL} = 0.4 mA	
Vi–Xj on resistance		R_{ON}	3	—	0.5	1.0	kΩ	I_{ON} = 100 µA	1
Input leakage current	1	I_{IL1}	4	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
	2	I_{IL2}	5	–25	—	25		V_{IN} = V_{CC} to V_{EE}	
	3	I_{IL3}	2	–5.0	—	5.0		V_{IN} = V_{CC} to GND	
Current consumption	(5 V)	I_{GND}	—	—	—	100		f_{CL} = 19.2 kHz	2
		I_{EE}	—	—	—	250		V_{CC} – V_{EE} = 28 V f_{FLM} = 80 Hz V_{CC} – GND = 5 V	
	(3 V)	I_{GND}	—	—	—	50		f_{CL} = 19.2 kHz	2
		I_{EE}	—	—	—	250		V_{CC} – V_{EE} = 28 V f_{FLM} = 80 Hz V_{CC} – GND = 3 V	

Pins:
1. CL, M, SHL/R, $\overline{\text{DISPOFF}}$, DIO1–DIO4 (input)
2. DIO1–DIO4 (input)
3. X_1–X_{100}, V_1, V_5, V_6
4. CL, M, SHL/R, MODE1, MODE2, $\overline{\text{DISPOFF}}$
5. V_1, V_5, V_6

Notes:
1. Indicates the resistance between one pin from X_1–X_{100} and another pin from V_1, V_5, V_6, and V_{EE}, when load current is applied to the X pin. Defined under the following conditions:
   V_{CC} – V_{EE} = 28 V
   V_1, V_6 = V_{CC} – {1/10 (V_{CC} –V_{EE})}
   V_5 = V_{EE} + {1/10 (V_{CC} –V_{EE})}
   V_1 and V_6 should be near V_{CC} level, and V5 should be near V_{EE} level (figure 4). All voltage must be within Δ V. Δ V is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that Δ V depends on power supply voltages V_{CC} – V_{EE} (figure 5).
2. Excludes input and output current. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

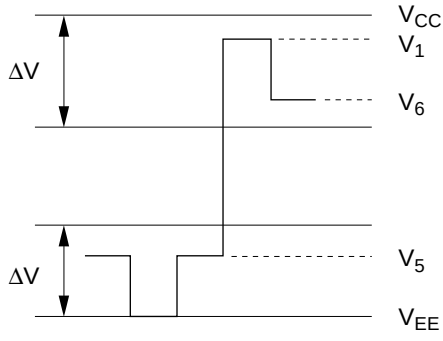

Figure 13 Relation between Driver Output Waveform and Level Voltages

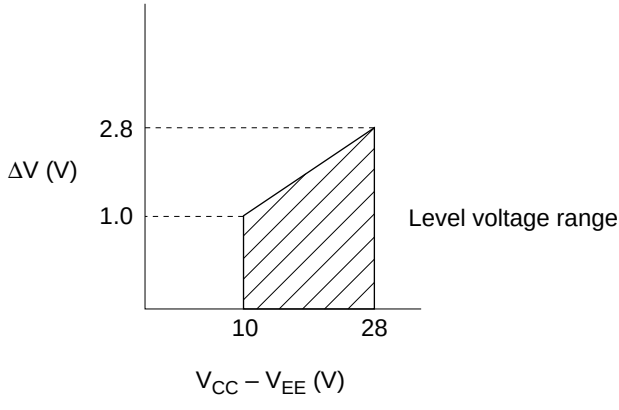

Figure 14 Relation between $V_{CC} - V_{EE}$ and Δ V

AC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL	10	—	µs
Clock high-level width	t_{CWH}		65	—	ns
Clock low-level width	t_{CWL}		1.0	—	µs
Clock rise time	t_r		—	50	ns
Clock fall time	t_f				
Data setup time	t_{DS}	DIO1–DIO4, CL	100	—	
Data hold time	t_{DH}				
Data output delay time*	t_{DD}		—	7.0	µs
Data output hold time	t_{DHW}		100	—	ns

Note: * The load circuit is shown in figure 15 is connected.

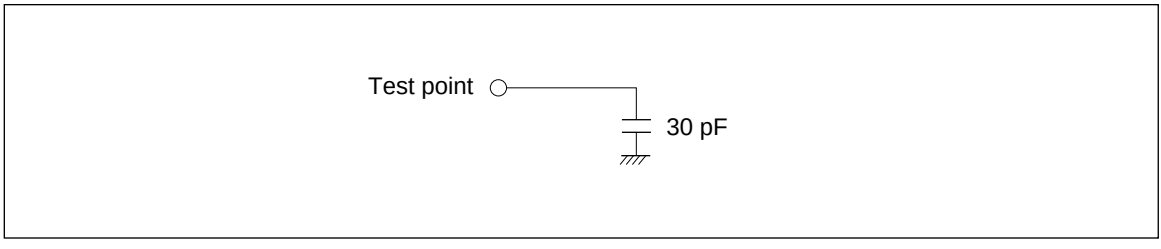

Figure 15 Load Circuit

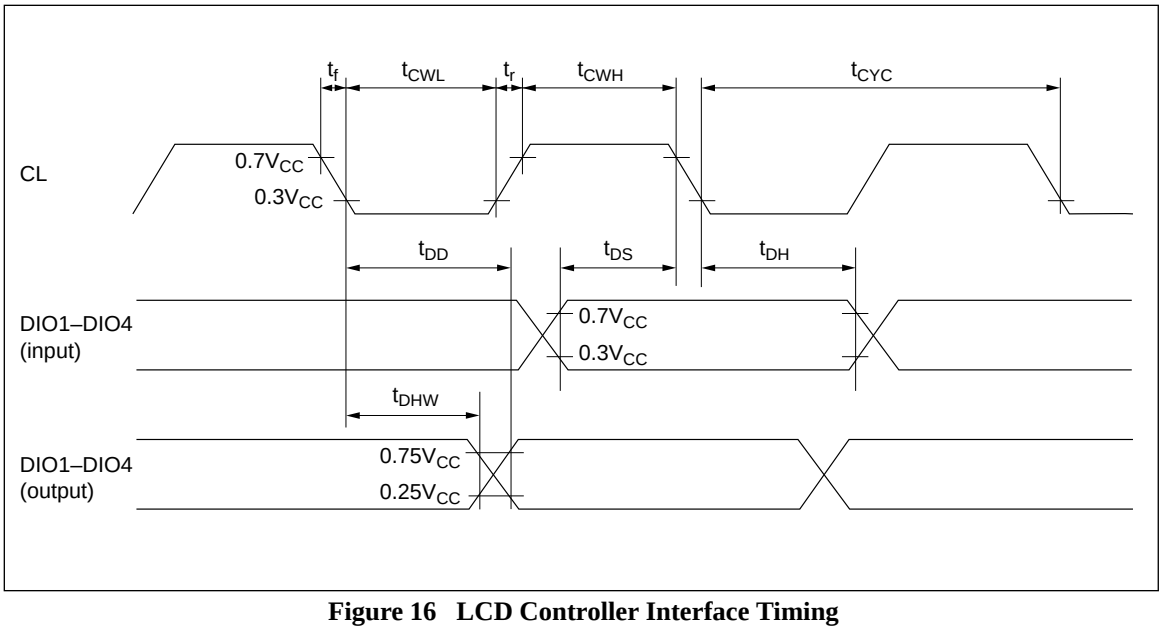

Figure 16 LCD Controller Interface Timing