Section 15. Electrical Specifications

15.1 Absolute Maximum Ratings

Table 15-1 lists the absolute maximum ratings.

Table 15-1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Programming voltage	V_{PP}	–0.3 to +14.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 15-1.

15.2 Electrical Characteristics

15.2.1 DC Characteristics

Table 15-2 lists the DC characteristics of the H8/320 series.

Table 15-2. DC Characteristics

Conditions: V_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger input voltage (1)	$P6_6$ – $P6_3$, $P6_0$, $P7_0$	V_T^-	1.0	–	–	V	
		V_T^+	–	–	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.4	–	–	V	
Input high voltage (2)	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0 EXTAL, $\overline{NMI}$	V_{IH}	V_{CC} – 0.7	–	V_{CC} + 0.3	V	
Input high voltage	Input pins other than (1) and (2)	V_{IH}	2.0	–	V_{CC} + 0.3	V	
Input low voltage (3)	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0, EXTAL	V_{IL}	–0.3	–	0.5	V	
Input low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	–	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	–	–	V	I_{OH} = –200 µA
			3.5	–	–	V	I_{OH} = –1.0 mA
Output low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	$P1_7$ – $P1_0$, $P2_7$ – $P2_0$		–	–	1.0	V	I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	–	–	10.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD_1, MD_0		–	–	1.0	µA	
Leakage current in 3-state (off state)	Ports 1 to 7	$\lvert I_{TSI} \rvert$	–	–	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 7	-Ip	30	–	250	µA	V_{in} = 0 V

Table 15-2. DC Characteristics (cont.)

Conditions: V_{CC} = AV_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	V_{in} = 0 V
	$\overline{NMI}$		–	–	30	pF	
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	f = 1 MHz Ta = 25°C
Current dissipation*	Normal operation	I_{CC}	–	12	25	mA	f = 6 MHz
			–	16	30	mA	f = 8 MHz
			–	20	40	mA	f = 10 MHz
	Sleep mode		–	8	15	mA	f = 6 MHz
			–	10	20	mA	f = 8 MHz
			–	12	25	mA	f = 10 MHz
	Standby modes		–	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

* Current dissipation values assume that $V_{IH\ min.}$ = V_{CC} – 0.5V, $V_{IL\ max.}$ = 0.5V, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 15-3. Allowable Output Current Sink Values

Conditions: V_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	–	–	80	mA
	All output pins		–	–	120	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output high current sink (total)	Total of all output	$\Sigma-I_{OH}$	–	–	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-3. In particular, when driving a Darlington pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

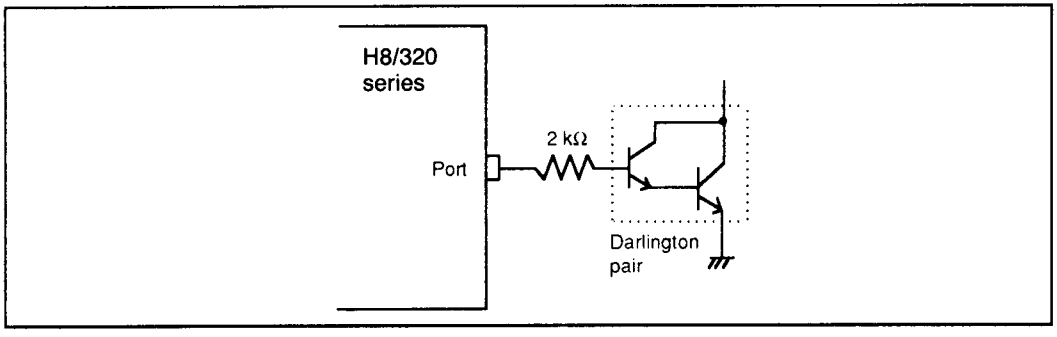

Figure 15-1. Example of Circuit for Driving a Darlington Pair

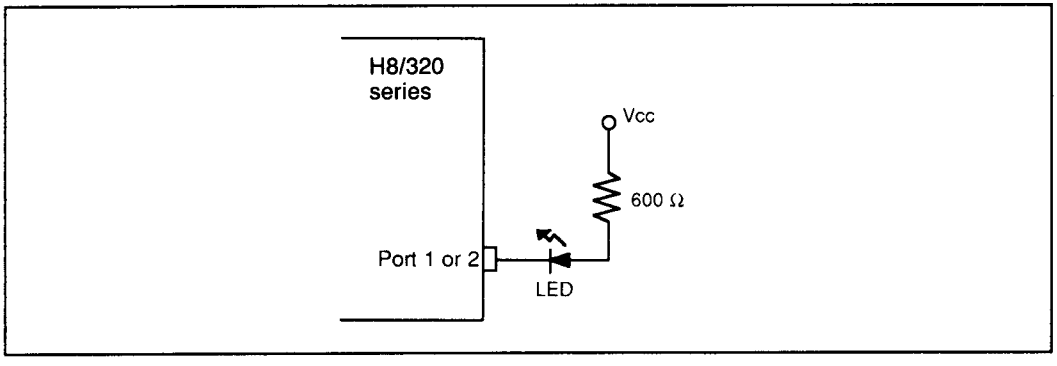

Figure 15-2. Example of Circuit for Driving a LED

15.2.2 AC Characteristics

The AC characteristics for the H8/320 series are listed in three tables. Bus timing parameters are given in table 15-4, control signal timing parameters in table 15-5, and timing parameters of the on-chip supporting modules in table 15-6.

Table 15-4. Bus Timing

Conditions: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Measurement Item	Symbol	Measurement conditions	6MHz min	6MHz max	8MHz min	8MHz max	10MHz min	10MHz max	Unit
Clock cycle time	t_{cyc}	Fig. 15-4	166.7	2000	125	2000	100	2000	ns
Clock pulse width Low	t_{CL}	Fig. 15-4	65	–	45	–	35	–	ns
Clock pulse width High	t_{CH}	Fig. 15-4	65	–	45	–	35	–	ns
Clock rise time	t_{Cr}	Fig. 15-4	–	15	–	15	–	15	ns
Clock fall time	t_{Cf}	Fig. 15-4	–	15	–	15	–	15	ns
Address delay time	t_{AD}	Fig. 15-4	–	70	–	60	–	55	ns
Address hold time	t_{AH}	Fig. 15-4	30	–	25	–	20	–	ns
Address strobe delay time	t_{ASD}	Fig. 15-4	–	70	–	60	–	40	ns
Write strobe delay time	t_{WSD}	Fig. 15-4	–	70	–	60	–	50	ns
Strobe delay time	t_{SD}	Fig. 15-4	–	70	–	60	–	50	ns
Write strobe pulse width	t_{WSW}	Fig. 15-4	200	–	150	–	120	–	ns
Address setup time 1	t_{AS1}	Fig. 15-4	25	–	20	–	15	–	ns
Address setup time 2	t_{AS2}	Fig. 15-4	105	–	80	–	65	–	ns
Read data setup time	t_{RDS}	Fig. 15-4	60	–	50	–	35	–	ns
Read data hold time	t_{RDH}	Fig. 15-4	0	–	0	–	0	–	ns
Write data delay time	t_{WDD}	Fig. 15-4	–	85	–	75	–	75	ns
Read data access time	t_{ACC}	Fig. 15-4	–	280	–	210	–	170	ns
Write data setup time	t_{WDS}	Fig. 15-4	30	–	15	–	10	–	ns
Write data hold time	t_{WDH}	Fig. 15-4	30	–	25	–	20	–	ns
Wait setup time	t_{WTS}	Fig. 15-5	45	–	45	–	45	–	ns
Wait hold time	t_{WTH}	Fig. 15-5	10	–	10	–	10	–	ns
E clock delay time	t_{ED}	Fig. 15-6	–	25	–	25	–	25	ns
E clock rise time	t_{Er}	Fig. 15-6	–	15	–	15	–	15	ns
E clock fall time	t_{Ef}	Fig. 15-6	–	15	–	15	–	15	ns
Read data hold time (for E clock)	t_{RDHE}	Fig. 15-6	0	–	0	–	0	–	ns
Write data hold time (for E clock)	t_{WDHE}	Fig. 15-6	50	–	40	–	30	–	ns

Table 15-5. Control Signal Timing

Conditions: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10 MHz, V_{SS} = 0 V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Measurement Item	Symbol	Measurement conditions	6MHz min	6MHz max	8MHz min	8MHz max	10MHz min	10MHz max	Unit
$\overline{RES}$ setup time	t_{RESS}	Fig. 15-7	200	–	200	–	200	–	ns
$\overline{RES}$ pulse width	t_{RESW}	Fig. 15-7	10	–	10	–	10	–	t_{cyc}
Mode programming setup time	t_{MDS}	Fig. 15-7	4	–	4	–	4	–	t_{cyc}
$\overline{NMI}$ setup time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIS}	Fig. 15-8	150	–	150	–	150	–	ns
$\overline{NMI}$ hold time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIH}	Fig. 15-8	10	–	10	–	10	–	ns
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIW}	Fig. 15-8	200	–	200	–	200	–	ns
Crystal oscillator settling time (reset)	t_{OSC1}	Fig. 15-9	20	–	20	–	20	–	ms
Crystal oscillator settling time (software standby)	t_{OSC2}	Fig. 15-10	10	–	10	–	10	–	ms

Table 15-6. Timing Conditions of On-Chip Supporting Modules

Conditions: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

	Item	Symbol	Measurement conditions	6MHz min	6MHz max	8MHz min	8MHz max	10MHz min	10MHz max	Unit
FRT	Timer output delay time	t_{FTOD}	Fig. 15-11	–	100	–	100	–	100	ns
	Timer input setup time	t_{FTIS}	Fig. 15-11	50	–	50	–	50	–	ns
	Timer clock input setup time	t_{FTCS}	Fig. 15-12	50	–	50	–	50	–	ns
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	Fig. 15-12	1.5	–	1.5	–	1.5	–	t_{cyc}

Table 15-6. Timing Conditions of On-Chip Supporting Modules (cont.)

Conditions: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10 MHz, V_{SS} = 0 V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

	Item	Symbol	Measurement conditions	6MHz min	6MHz max	8MHz min	8MHz max	10MHz min	10MHz max	Unit
TMR	Timer output delay time	t_{TMOD}	Fig. 15-13	–	100	–	100	–	100	ns
	Timer reset input setup time	t_{TMRS}	Fig. 15-15	50	–	50	–	50	–	ns
	Timer clock input setup time	t_{TMCS}	Fig. 15-14	50	–	50	–	50	–	ns
	Timer clock pulse width (single edge)	t_{TMCWH} t_{TMCWL}	Fig. 15-14	1.5	–	1.5	–	1.5	–	t_{cyc}
	Timer clock pulse width (both edges)		Fig. 15-14	2.5	–	2.5	–	2.5	–	t_{cyc}
SCI	Input clock cycle (Async)	t_{Scyc}	Fig. 15-16	2	–	2	–	2	–	t_{cyc}
	(Sync)	t_{Scyc}	Fig. 15-16	4	–	4	–	4	–	t_{cyc}
	Transmit data delay time (Sync)	t_{TXD}	Fig. 15-16	–	100	–	100	–	100	ns
	Receive data setup time (Sync)	t_{RXS}	Fig. 15-16	100	–	100	–	100	–	ns
	Receive data hold time (Sync)	t_{RXH}	Fig. 15-16	100	–	100	–	100	–	ns
	Input clock pulse width	t_{SCKW}	Fig. 15-17	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}
Ports	Output data delay time	t_{PWD}	Fig. 15-18	–	100	–	100	–	100	ns
	Input data setup time	t_{PRS}	Fig. 15-18	50	–	50	–	50	–	ns
	Input data hold time	t_{PRH}	Fig. 15-18	50	–	50	–	50	–	ns

Table 15-6. Timing Conditions of On-Chip Supporting Modules (cont.)

Conditions: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10 MHz, V_{SS} = 0 V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

	Item	Symbol	Measurement conditions	6MHz min	6MHz max	8MHz min	8MHz max	10MHz min	10MHz max	Unit
Parallel handshake interface	Handshake input strobe pulse width	t_{HISW}	Fig. 15-19	1.5	–	1.5	–	1.5	–	t_{cyc}
	Handshake input data setup time	t_{HIS}	Fig. 15-19	10	–	10	–	10	–	ns
	Handshake input data hold time	t_{HIH}	Fig. 15-19	120	–	120	–	120	–	ns
	Handshake output strobe delay time	t_{HOSD1}	Fig. 15-20	–	80	–	80	–	80	ns
		t_{HOSD2}	Fig. 15-20	–	80	–	80	–	80	ns
	Busy output delay time	t_{HBSOD1}	Fig. 15-21	–	150	–	150	–	150	ns
		t_{HBSOD2}	Fig. 15-21	–	150	–	150	–	150	ns

- **Measurement Conditions for AC Characteristics**

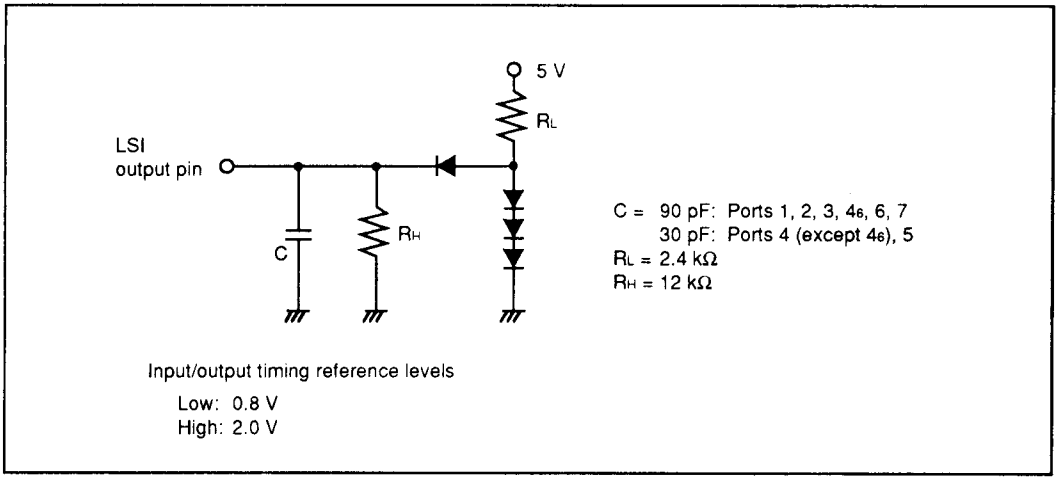

Figure 15-3. Output Load Circuit

15.3 MCU Operational Timing

This section provides the following timing charts:

15.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

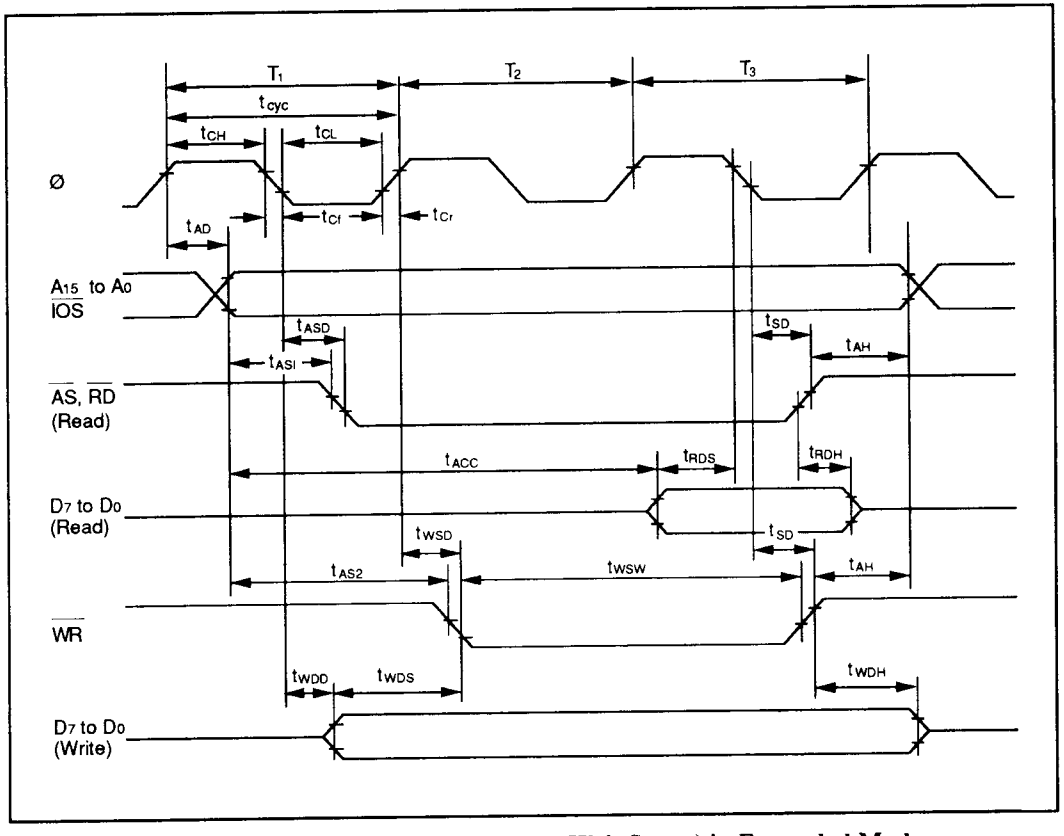

Figure 15-4. Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

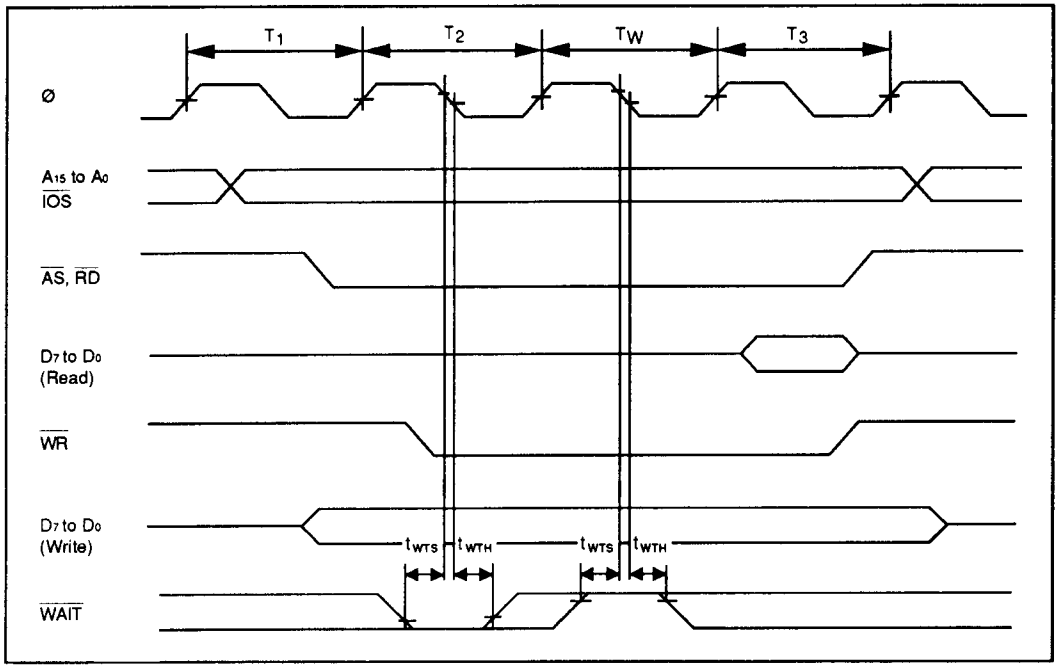

Figure 15-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

(3) E Clock Bus Cycle

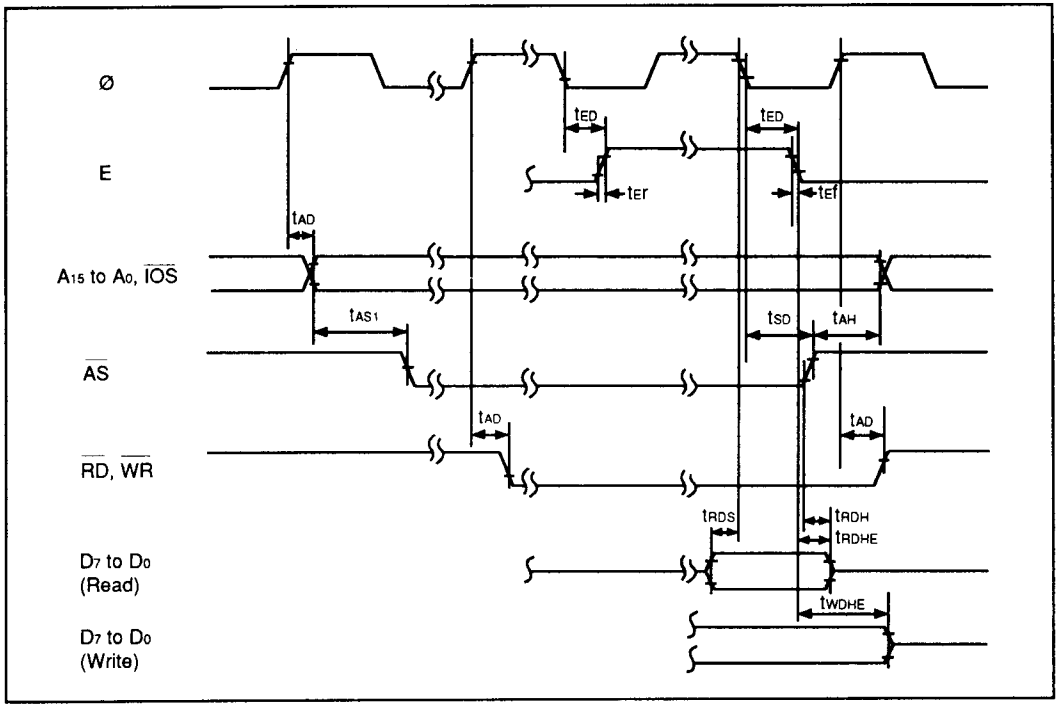

Figure 15-6. E Clock Bus Cycle

15.3.2 Control Signal Timing

(1) Reset Input Timing

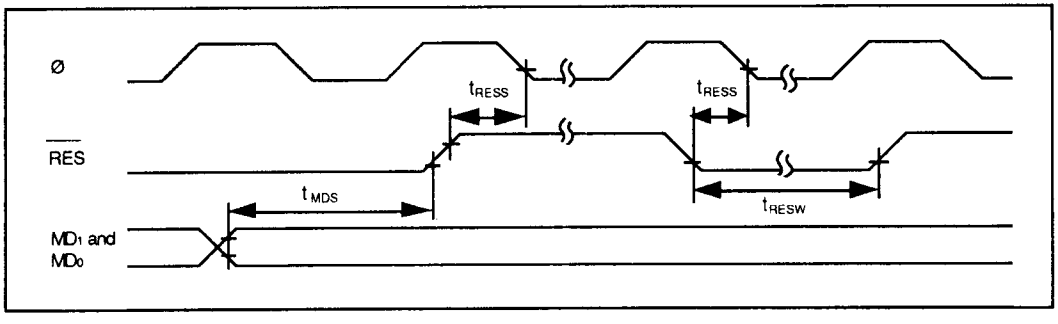

Figure 15-7. Reset Input Timing

(2) Interrupt Input Timing

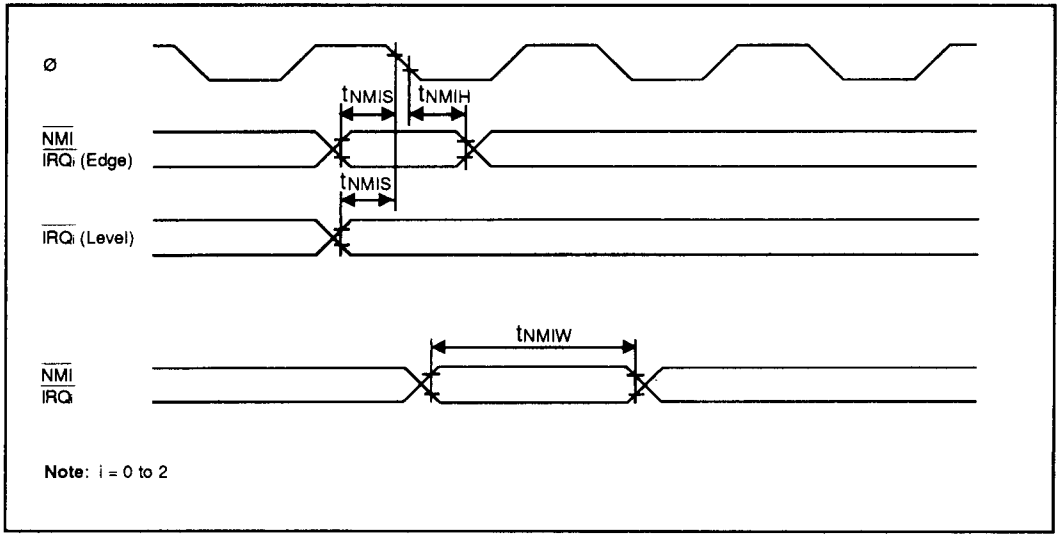

Figure 15-8. Interrupt Input Timing

(3) Clock Settling Timing

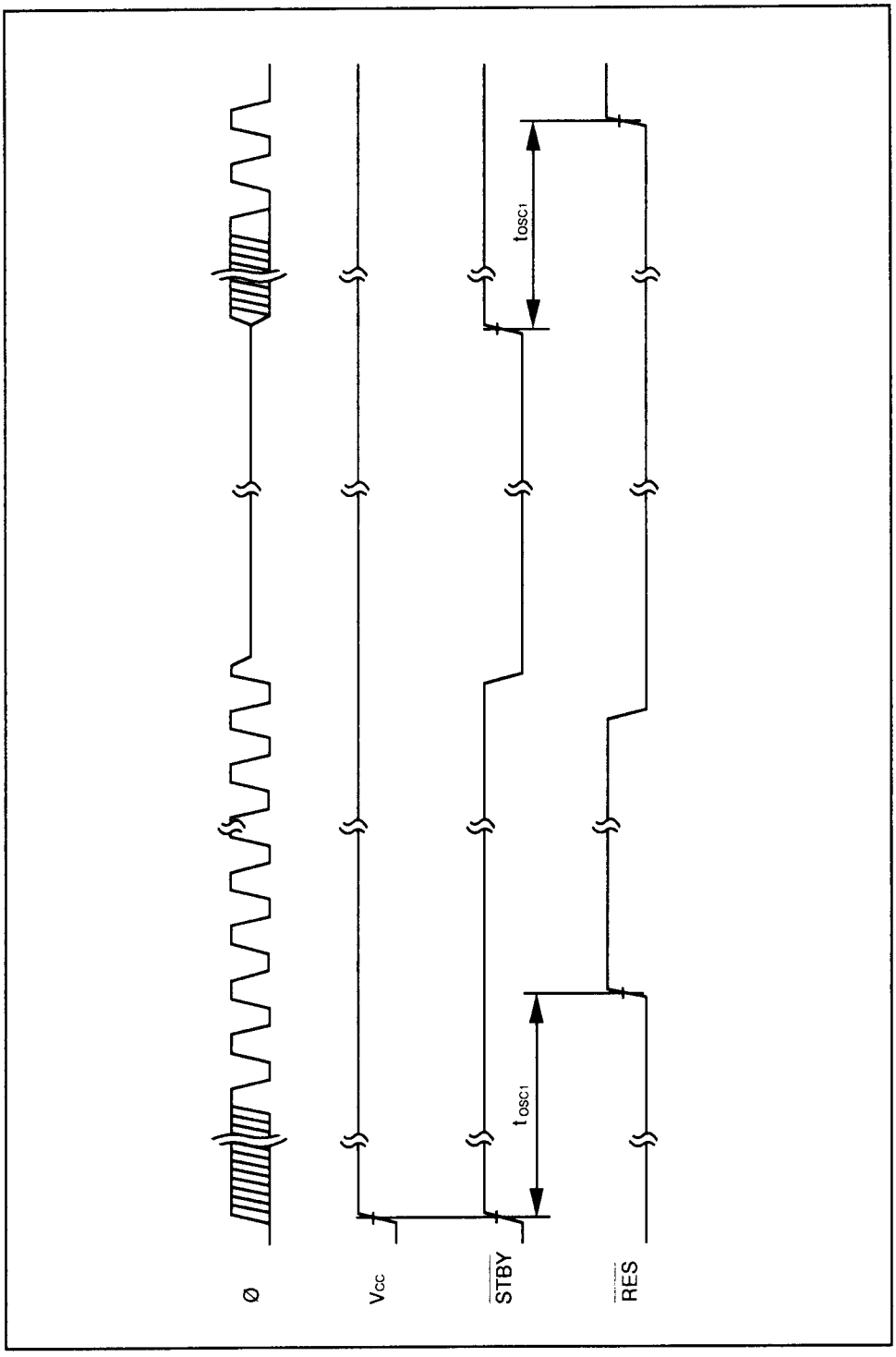

Figure 15-9. Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

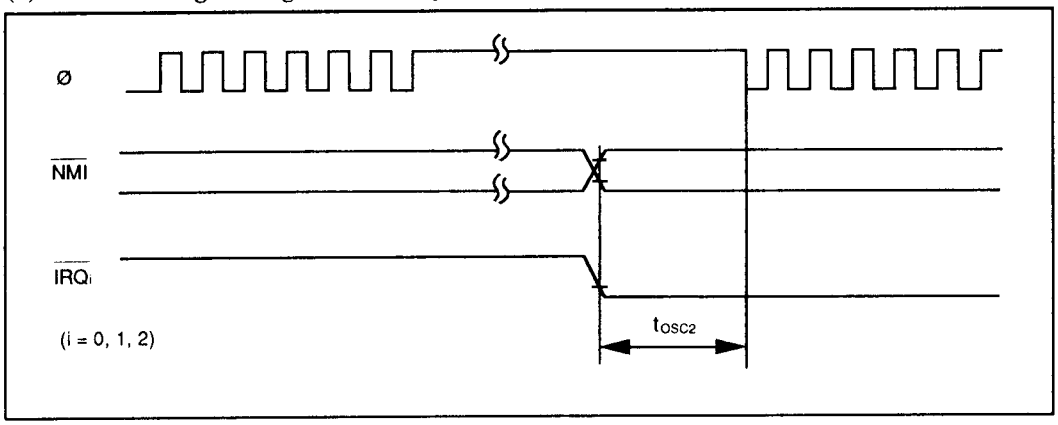

Figure 15-10. Clock Settling Timing for Recovery from Software Standby Mode

15.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

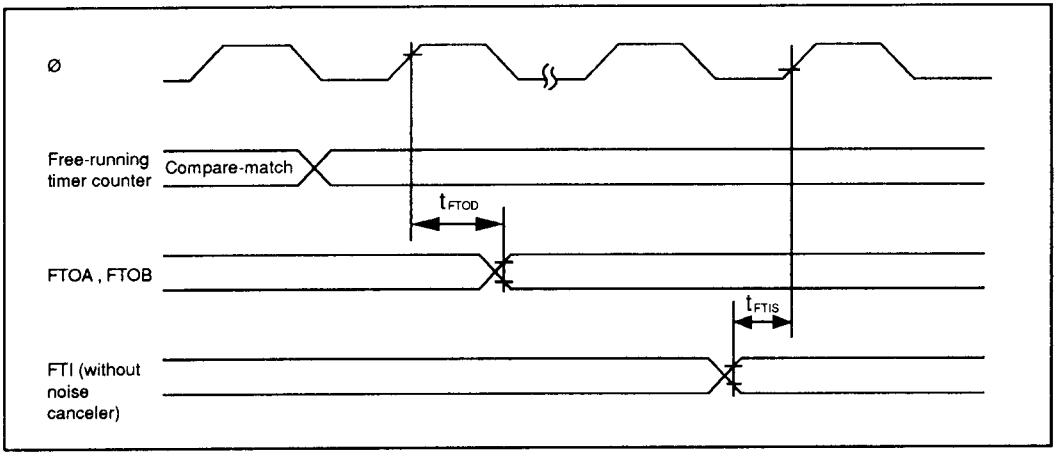

Figure 15-11. Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

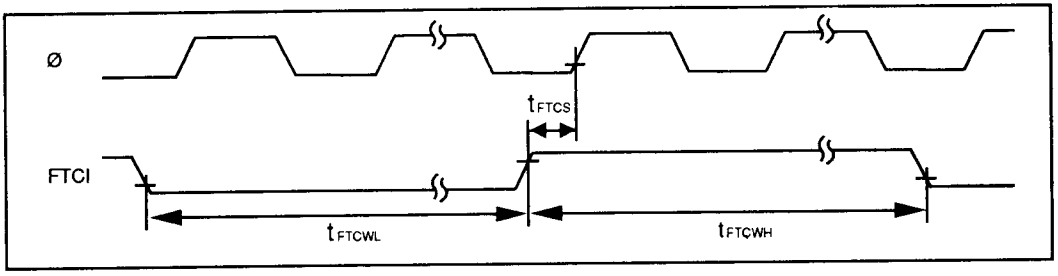

Figure 15-12. External Clock Input Timing for Free-Running Timer

15.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

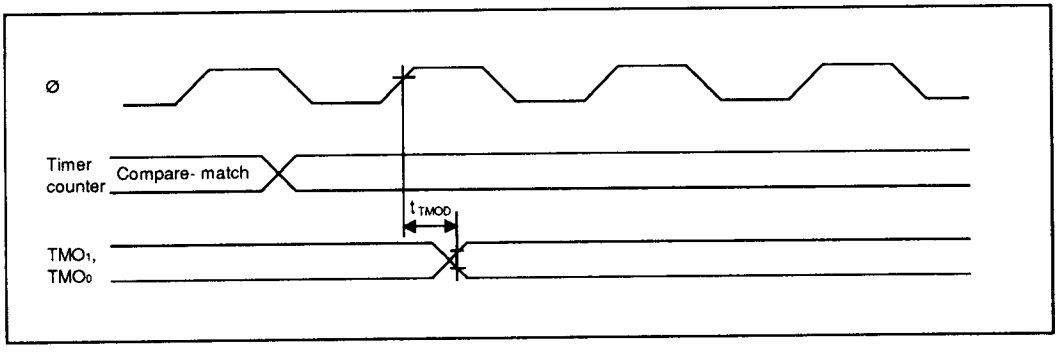

Figure 15-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

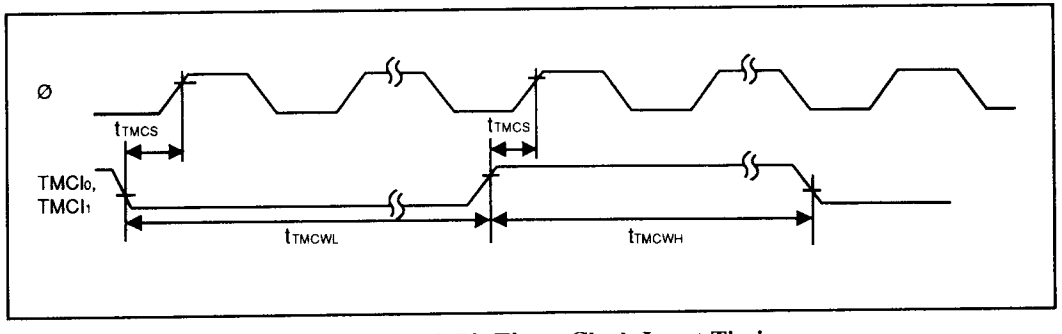

Figure 15-14. 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

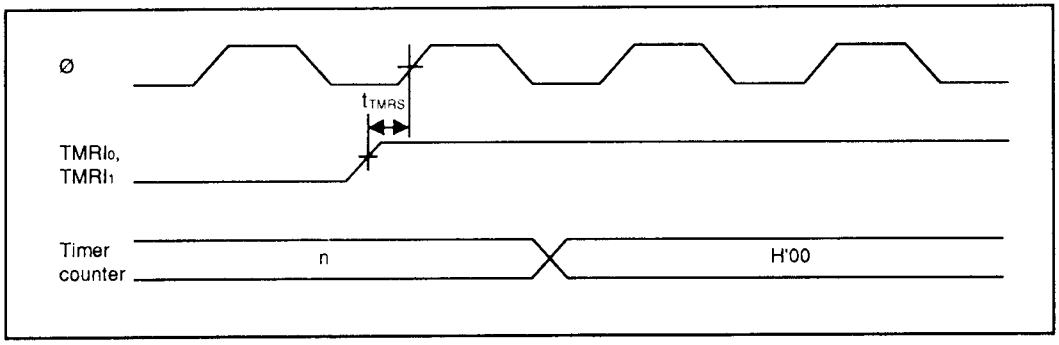

Figure 15-15. 8-Bit Timer Reset Input Timing

15.3.5 Serial Communication Interface Timing

(1) SCI Input/Output Timing

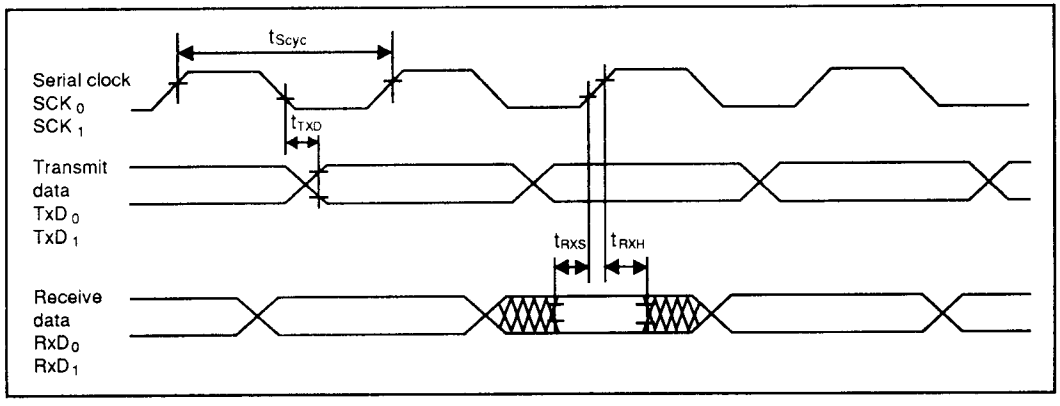

Figure 15-16. SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

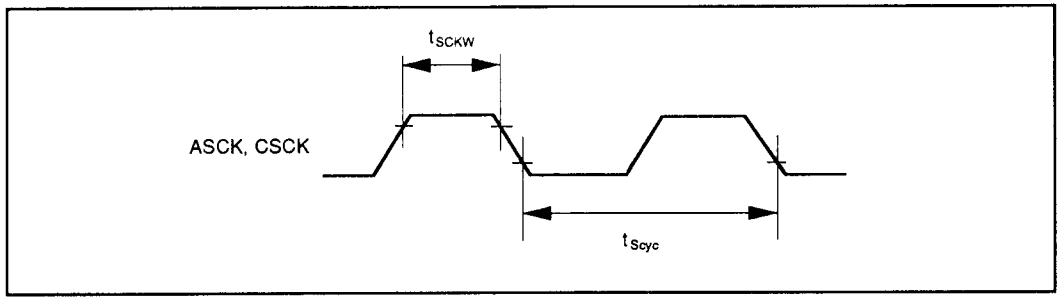

Figure 15-17. SCI Input Clock Timing

15.3.6 I/O Port Timing

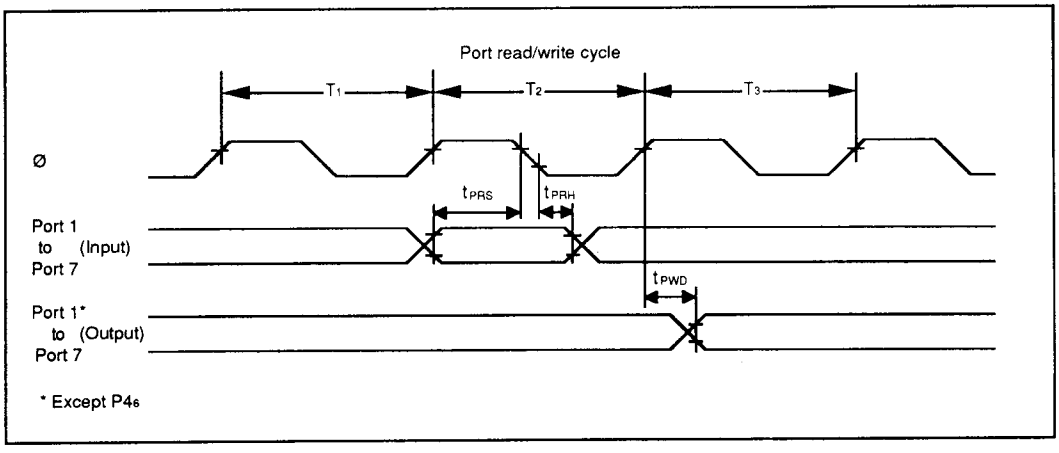

Figure 15-18. I/O Port Input/Output Timing

15.3.7 Parallel Handshake Interface Timing

(1) Input Strobe Input Timing

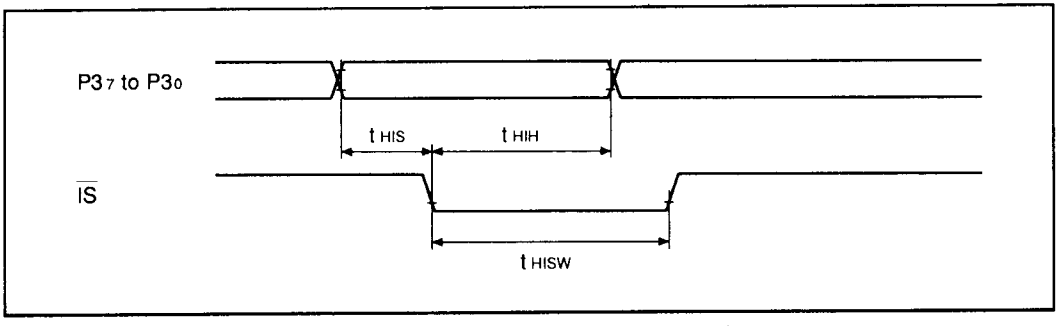

Figure 15-19. Input Strobe Input Timing

(2) Output Strobe Output Timing

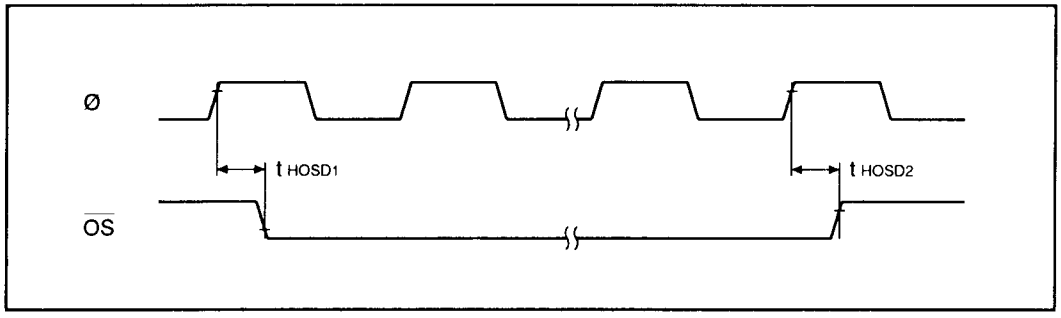

Figure 15-20. Output Strobe Output Timing

(3) Busy Output Timing

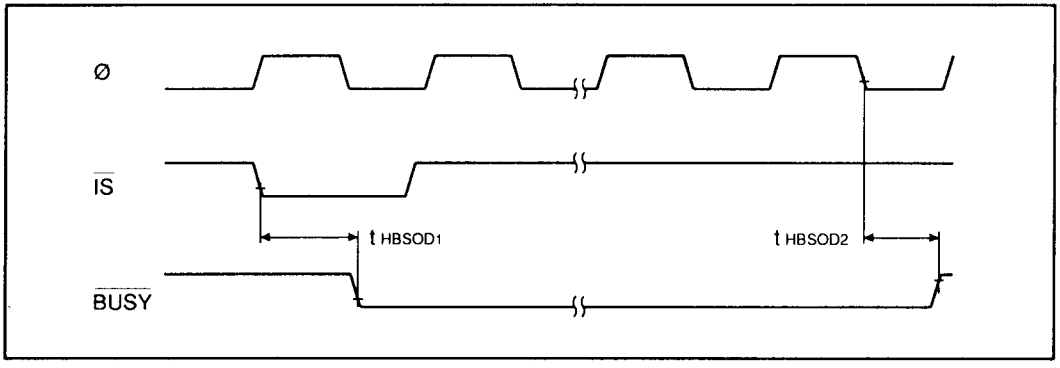

Figure 15-21. Busy Output Timing

Table C-1. Pin States (cont.)

T-90-01

Pin Name	MCU Mode	Reset	Hardware Standby	Software Standby	Sleep Mode	Normal Operation
P55 to P50,	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3					
P66 to P60,	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3					
P77/$\overline{\text{WAIT}}$	1	3-State	3-State	3-state	3-state	$\overline{\text{WAIT}}$
	2					
	3			Prev. state	Prev. state	I/O port
P76 to P74,	1	High	3-State	High	High	$\overline{\text{AS}}$, $\overline{\text{WR}}$,
$\overline{\text{AS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$,	2					$\overline{\text{RD}}$
	3	3-State		Prev. state	Prev. state	I/O port
P73 to P70,	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2					
	3					

Notes:

1. 3-state: High-impedance state
2. Prev. state: Previous state. Input ports are in the high-impedance state (with the MOS pull-up on if DDR = 0 and DR = 1). Output ports hold their previous output level.
3. On-chip supporting modules are initialized, so these pins revert to I/O ports according to the DDR and DR bits.
4. I/O port: Direction depends on the data direction (DDR) bit. Note that these pins may also be used by the on-chip supporting modules.

See section 5, I/O Ports for further information.

Appendix D. Package Dimensions

T-90-20

Figure D-1 shows the dimensions of the DC-64S package. Figure D-2 shows the dimensions of the DP-64S package. Figure D-3 shows the dimensions of the FP-64A package.

Unit: mm (inch)

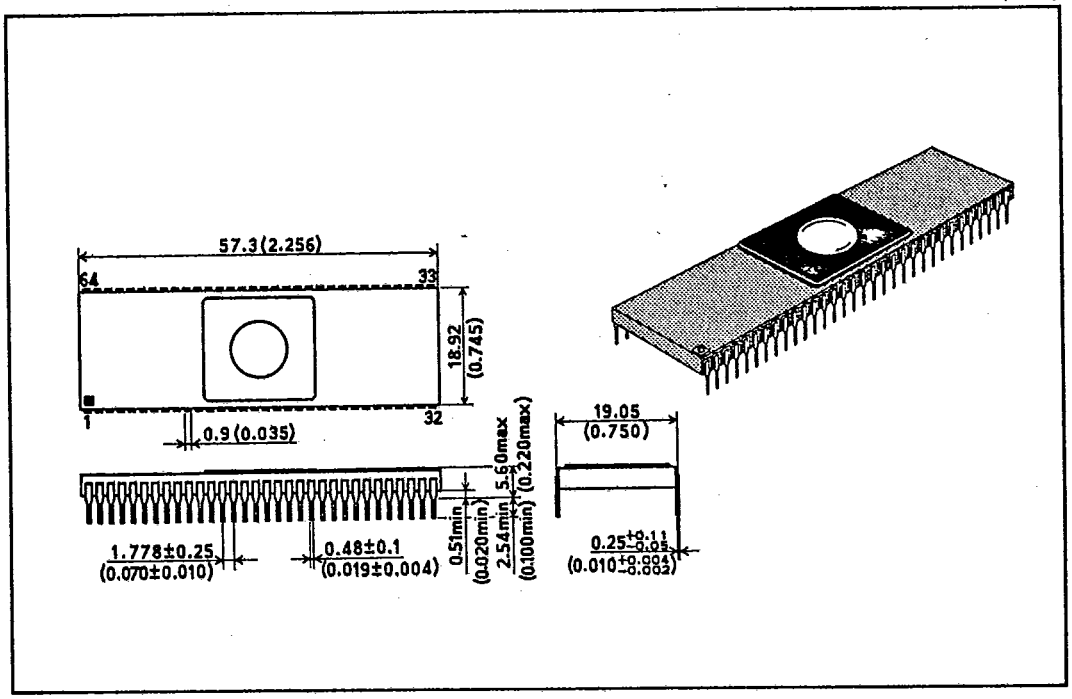

Figure D-1. Package Dimensions (DC-64S)

Unit: mm (inch)

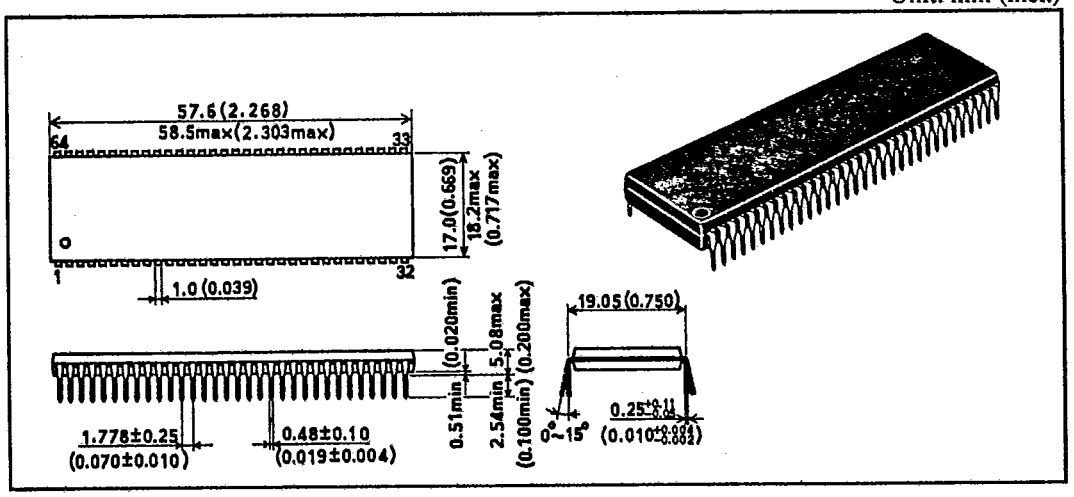

Figure D-2. Package Dimensions (DP-64S)

Appendix E. Package Dimensions

T-90-20

Figure D-1 shows the dimensions of the DC-64S package. Figure D-2 shows the dimensions of the DP-64S package. Figure D-3 shows the dimensions of the FP-64A package. Figure D-4 shows the dimensions of the CP-68 package.

Unit: mm

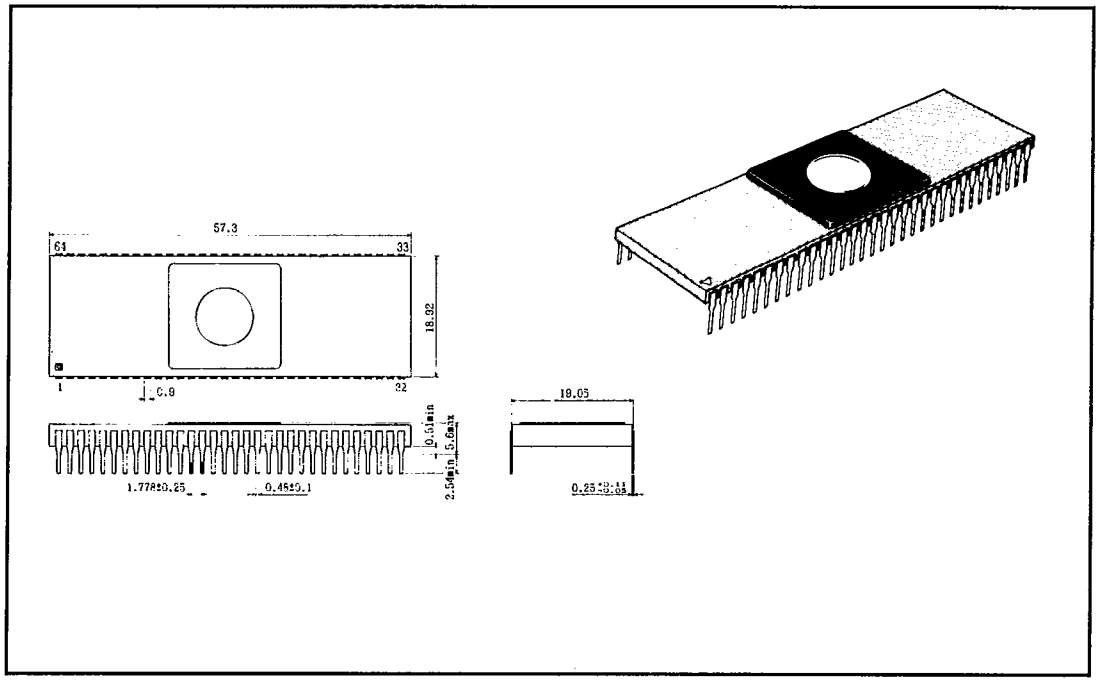

Figure E-1. Package Dimensions (DC-64S)

Unit: mm

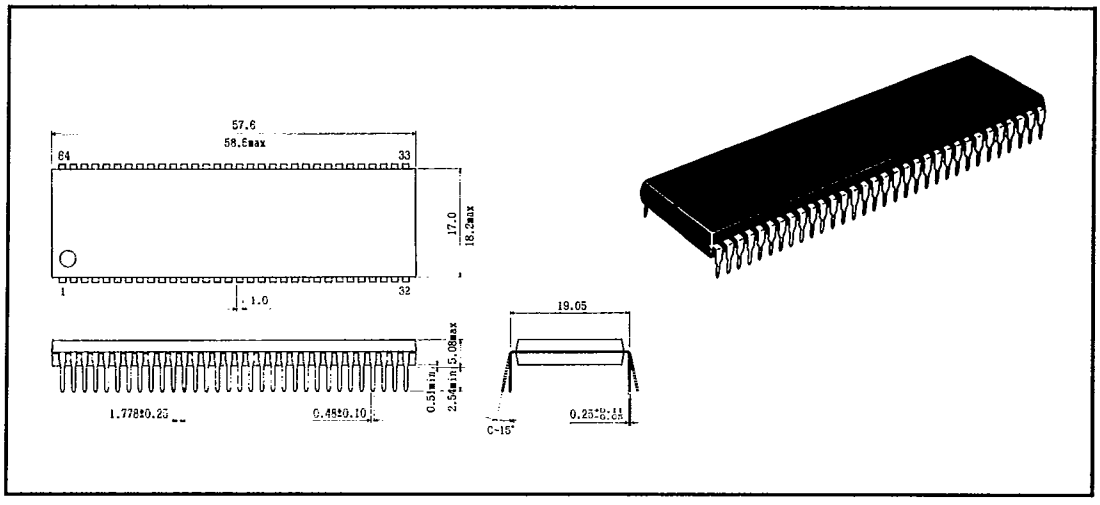

Figure E-2. Package Dimensions (DP-64S)

Unit: mm

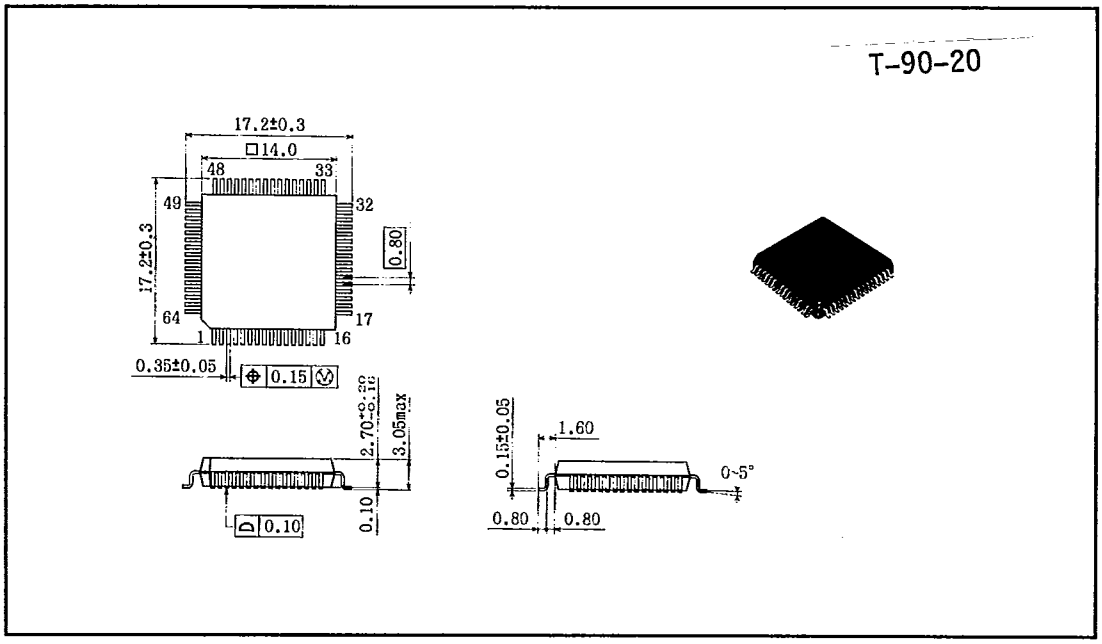

Figure E-3. Package Dimensions (FP-64A)

Unit: mm

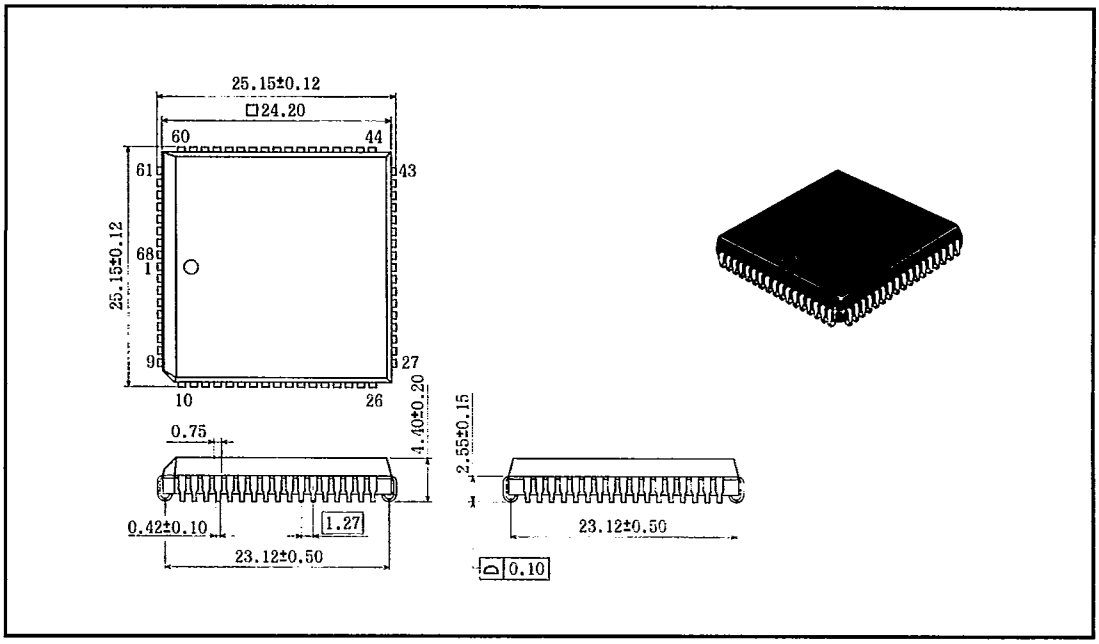

Figure E-4. Package Dimensions (CP-68)