HD63463

HDC (Hard Disk Controller)

DESCRIPTION

The HD63463 (HDC: Hard Disk Controller) is a CMOS device developed for use as a peripheral LSI for the 16-bit microprocessor HD68000 (MPU: Microprocessing Unit). The HDC connects the host system and the Winchester type hard disk device with or without HD68450 (DMAC: Direct Memory Access Controller).

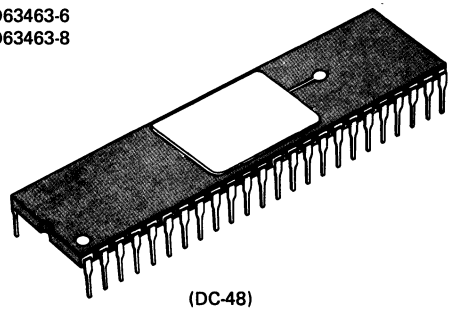
FEATURES

- Two types of disk interface, ST506/ST412/ST412HP and SMD
- Choice of data bus width – 16 or 8 bits
- Serial data transfer rate – max 20 Mbit/s [NRZ], max 10 Mbit/s [MFM]
- Step rate – max 1.1 MHz
- Internal data buffer (256 bytes x 2)
- Zero-sector interleave access
- Programmed I/O access
- Automatic error correction
- Zero pattern detector/generator, address mark detector/generator, write precompensation logic, etc internally provided
- 22 high-level function commands
- 25 error codes
- External circuit diagnosis command
- Low power dissipation – typ 250 mW

TYPE OF PRODUCTS

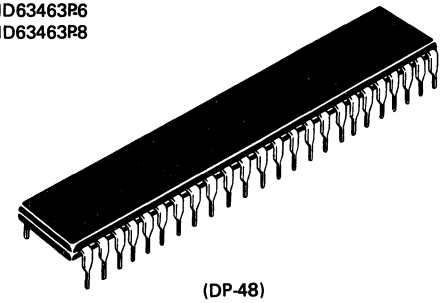
Type No.	Clock Frequency (MHz)		Package
	Host	Drive	
HD63463-6	6.0	15.0	DC-48
HD63463-8	8.0	20.0	
HD63463P6	6.0	15.0	DP-48
HD63463P8	8.0	20.0	
HD63463CP6	6.0	15.0	CP-52
HD63463CP8	8.0	20.0	

HD63463-6
HD63463-8



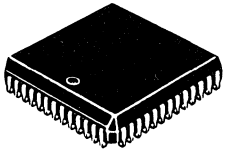
(DC-48)

HD63463P6
HD63463P8



(DP-48)

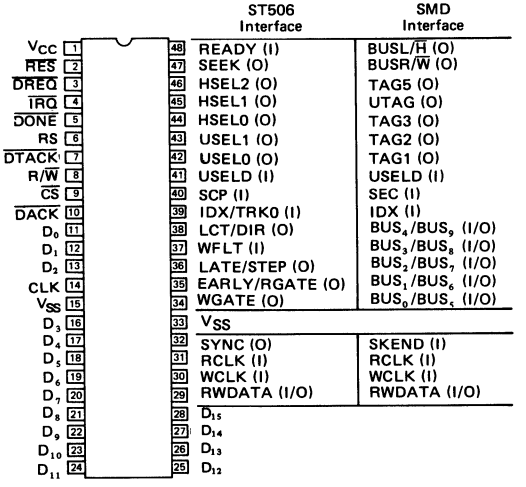
HD63463CP6
HD63463CP8



(CP-52)

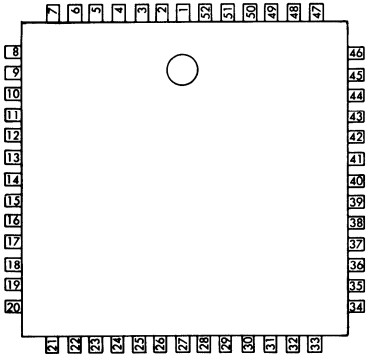
PIN ARRANGEMENT

DC-48, DP-48



(Top View)

CP-52



(Top View)

Pin No.	ST506 Interface	SMD Interface	Pin No.	ST506 Interface	SMD Interface
1	V_{CC}		27	V_{CC}	
2	V_{CC}		28	D_{12} (I/O)	
3	$\overline{RES}$ (I)		29	D_{13} (I/O)	
4	$\overline{DREQ}$ (O)		30	D_{14} (I/O)	
5	$\overline{IRQ}$ (O)		31	D_{15} (I/O)	
6	$\overline{DONE}$ (I)		32	RWDATA (I/O)	RWDATA (I/O)
7	RS (I)		33	WCLK (I)	WCLK (I)
8	$\overline{DTACK}$ (O)		34	RCLK (I)	RCLK (I)
9	R/$\overline{W}$ (I)		35	SYNC (O)	SKEND (I)
10	CS (I)		36	V_{SS}	
11	$\overline{DACK}$ (I)		37	V_{SS}	
12	D_0 (I/O)		38	WGATE (O)	BUS_0/BUS_5 (I/O)
13	D_1 (I/O)		39	EARLY/RGATE (O)	BUS_1/BUS_6 (I/O)
14	D_2 (I/O)		40	LATE/STEP (O)	BUS_2/BUS_7 (I/O)
15	CLK (I)		41	WFLT (I)	BUS_3/BUS_8 (I/O)
16	V_{SS}		42	LCT/DIR (O)	BUS_4/BUS_9 (I/O)
17	V_{SS}		43	IDX/TRK0 (I)	IDX (I)
18	D_3 (I/O)		44	SCP (I)	SEC (I)
19	D_4 (I/O)		45	USELD (I)	USELD (I)
20	D_5 (I/O)		46	USEL0 (O)	TAG1 (O)
21	D_6 (I/O)		47	USEL1 (O)	TAG2 (O)
22	D_7 (I/O)		48	HSEL0 (O)	TAG3 (O)
23	D_8 (I/O)		49	HSEL1 (O)	UTAG (O)
24	D_9 (I/O)		50	HSEL2 (O)	TAG5 (O)
25	D_{10} (I/O)		51	SEEK (O)	BUSR/$\overline{W}$ (O)
26	D_{11} (I/O)		52	READY (I)	BUSL/$\overline{H}$ (O)

SIGNAL LINES

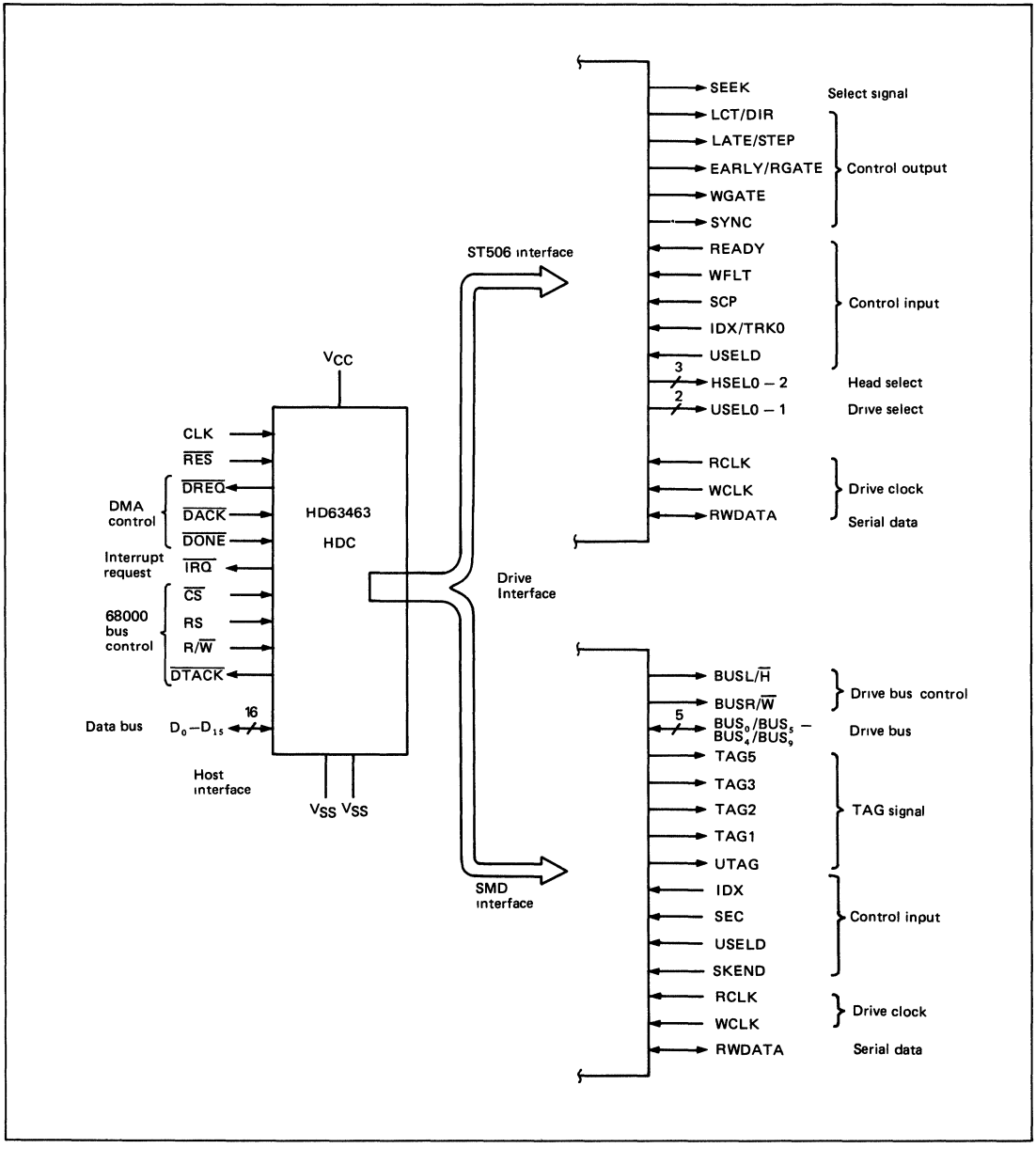


Figure 1 Input/Output Signals

HITACHI
Hitachi America Ltd. • 2210 O'Toole Avenue • San Jose, CA 95131 • (408) 435-8300

MAJOR FUNCTIONS OF HDC

Drive Interface	ST506*	Number of Heads	Max 8
		Number of Drives	Max 4
		Write Precompensation	Controlled
		High-Speed Seek	Step rate min 875 ns (CLK: 8 MHz)
	Storage Module Drive (SMD)	Number of Heads	Max 32
		Number of Drives	Max 8
		Track Offset	Controlled
		Data Strobe	Controlled
	Serial Data Format	NRZ or MFM (selectable)	
	Serial Data Transfer Rate	Max 20 Mbps (NRZ), max 10 Mbps (MFM)	
	Multiple Sector Access	Multiple sector, multiple track	
	Parallel Seek	Possible	
	Diagnosis	External circuit diagnosis	
Disk Format	Data Length	256, 512, 1024, 2048, or 4096 bytes (selectable)	
	Number of Sectors	Max 255 (hard sector), max 128 (soft sector)	
	Number of Cylinders	Max 1024	
	Sector Format	Hard sector or soft sector (selectable)	
Error Processing	Processing Code	16-bit CRC (error detection), 2 types	
		32-bit ECC (error detection or correction)	
	Error Correction Capability	Automatic correction of single burst error (up to 11 bits)	
On-Chip Data Buffer	Capacity	256 bytes x 2	
	Data Transfer	Simultaneous transfer on host side and drive side	
	Addressing	Stack type (pointer can be updated)	
Host Interface	Operation Cycle Time	Max 8 MHz	
	Data Bus Width	16 or 8 bits (selectable)	
	DMA Transfer	Burst or cycle steal mode (selectable)	
	Programmed I/O	Possible	
Commands	Seek	2 commands	
	Disk Read/Write	8 commands	
	Data Buffer	4 commands	
	Drive Check	2 commands	
	Others	6 commands	

*ST506/ST412/ST412HP is referred to as "ST506" in this document.

HARDWARE DESCRIPTION

SYSTEM CONFIGURATION

An HDC-based system configuration is illustrated in figure 2. The HDC is used to connect more than one hard disk drives (also called "drive" in this manual) to the host system. The host system consists of the MPU (Microprocessing Unit), the main memory and the DMAC (Direct Memory Access Controller). The HDC requires minimum number of external circuits that are connected to the host system including the HD68000 (MPU) and the HD68450 (DMAC).

If the host system does not require a high throughput, then the DMAC is not necessary. A few additional external circuits allow the HDC to be connected to another host system other than the HD68000.

The HDC may control either up to four ST506 drives or up to eight SMD drives.

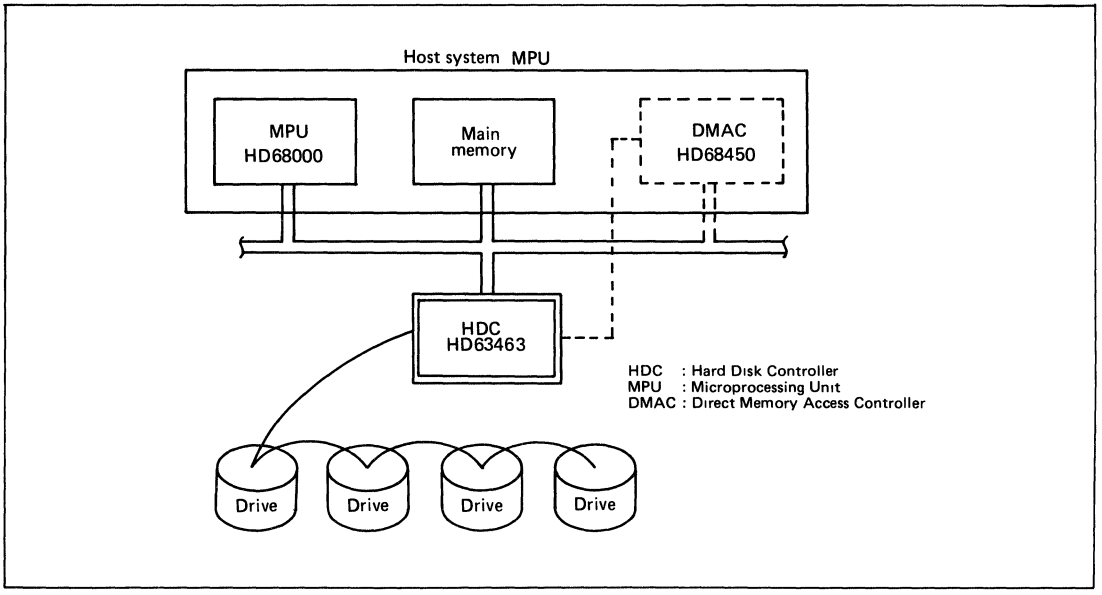


Figure 2 System Configuration Example

SIGNAL LINES

The input/output signal lines of the HDC are shown in figure 1 which covers both ST506 and SMD drive interface.

Each signal is described in the following tables and descriptions.

Host Interface

Category	Signal	I/O
Clock, Reset	CLK	I
	$\overline{RES}$	I
DMA Control (HD68450 Compatible)	$\overline{DREQ}$	O
	$\overline{DACK}$	I
	$\overline{DONE}$	I
Interrupt Request	$\overline{IRQ}$	O
Bus Control (HD68000 Compatible)	$\overline{CS}$	I
	RS	I
	R/$\overline{W}$	I
	$\overline{DTACK}$	O
Data Bus (HD68000 Compatible)	$D_0 - D_{15}$	I/O

CLK – Clock signal from the host system.

$\overline{RES}$ – Reset signal from the host system.

$\overline{DREQ}$ – Asserted when a DMA data transfer is requested to the DMAC. Receiving this signal, the DMAC obtains the bus mastership from the MPU.

$\overline{DACK}$ – Transfer acknowledge signal from the DMAC. Receiving this signal, the HDC transfers data through the host bus in the DMA mode. When $\overline{RES}$ signal is at "0", HDC data bus configuration change from 16 bits to 8 bits when $\overline{DACK}$ = 0.

$\overline{DONE}$ – Receiving this signal from the DMAC, the DMA data transfer through the host bus stops immediately.

$\overline{IRQ}$ – Interrupt request signal sent to the MPU (open drain output).

$\overline{CS}$ – Chip select signal generated by decoding address, address strobe, and data strobe of the host.

RS – Register select signal of the HDC. It selects registers when set to "0", data buffers when set to "1".

R/$\overline{W}$ – Signal that indicates the data transfer direction.

$\overline{DTACK}$ – Acknowledge signal that indicates the end of data transfer in the host bus. The host waits until the HDC asserts this signal to terminate the transfer.

D_0–D_{15} – 16-bit bi-directional data bus. When used as an 8-bit data bus, D_8–D_{15} must be open.

ST506 Interface

Category	Signal	I/O
Select Signal	SEEK	O
Control Output	LCT/DIR	O
	LATE/STEP	O
	EARLY/RGATE	O
	WGATE	O
	SYNC	O
	HSEL0–HSEL2	O
	USEL0–USEL1	O
Control Input	READY	I
	WFLT	I
	SCP	I
	IDX/TRK0	I
	USELD	I
Drive Clock	RCLK	I
	WCLK	I
Drive Data	RWDATA	I/O

SEEK – Used to decode multiplexed signals. SEEK signal remains high during the head positioning operation of the HDC.

LCT/DIR – When SEEK is at "1", this signal indicates the head direction: the head moves toward the spindle if the LCT/DIR signal is at "1". When SEEK is at "0", write current is reduced if this signal is at "1".

LATE/STEP – When SEEK is at "1", this signal serves as step pulses output for head positioning. When SEEK is at "0", this signal requests write precompensation (LATE).

EARLY/RGATE – When the WGATE signal is at "1", this signal requires write precompensation (EARLY). Otherwise, it serves as a read gate signal that requests reading data from the drive.

WGATE – Write gate signal that requests writing data to the drive.

SYNC – Signal to select the loop gain of the external data separator. SYNC is at "1" when RGATE is at "1" and one byte of $00 is detected in the disk data. SYNC is at "0" when RGATE is at "0".

HSEL0–HSEL2 – 3-bit signal that selects up to eight heads in the drive.

USEL0- USEL1 – 2-bit signal that selects one of four drives.

READY – Signal indicating that the selected drive is ready.

WFLT – Signal indicating that the drive has detected a fault which may cause a write error.

SCP – Signal indicating that head positioning (seek operation) has been completed in the drive.

IDX/TRK0 – When SEEK is at "1", this signal indicates that the head in the drive is positioned at the outermost track (track 0). When SEEK is at "0", this signal serves as an index signal that indicates the beginning of a track.

USELD – Response signal from the drive indicating that the drive is selected.

RCLK – Disk read clock from the external data separator. Its frequency is twice the serial transfer rate.

WCLK – Disk write clock from the external oscillator. Its frequency is twice the serial transfer rate.

RWDATA – Disk read/write serial data is input/output as modified frequency modulation code. This pin is normally in read state.

SMD Interface

Category	Signal	I/O
Drive Bus Control	BUSL/$\overline{H}$	O
	BUSR/$\overline{W}$	O
Drive Bus	BUS_0/BUS_5 – BUS_4/BUS_9	I/O
Tag	TAG5	O
	TAG3	O
	TAG2	O
	TAG1	O
	UTAG	O
Control Input	IDX	I
	SEC	I
	USELD	I
	SKEND	I
Drive Clock	RCLK	I
	WCLK	I
Drive Data	RWDATA	I/O

BUSL/$\overline{H}$ – When this signal is at high, lower 5 bits of 10-bit drive bus are being transferred.

BUSR/$\overline{W}$ – When this signal is at high, BUS_0/BUS_5–BUS_4/BUS_9 are in input state.

BUS_0/BUS_5 – BUS_4/BUS_9 – 5-bit bi-directional bus that is used to control the drive. When the data is output from 10-bit drive bus, the high-order 5 bits are output first and then the low-order 5 bits. When the data is input to the bus, higher 3 bits of the 8-bit status are fetched first, then the lower 5 bits.

TAG5 – Together with TAG2, used as a status input select signal.

TAG3 – Tag signal indicating that the drive bus contains information such as disk read/write instruction.

TAG2 – Tag signal indicating that the drive bus contains the address for head selection. When drive status is read from the drive bus, TAG2 and TAG5 are decoded to select the status.

TAG1 – Tag signal indicating that the drive bus contains the destination cylinder address.

UTAG – Tag signal indicating that the drive bus contains a 3-bit drive number.

IDX – Index signal indicating the beginning of a track.

SEC – Signal indicating the beginning of a sector.

USELD – Response signal from the drive indicating that the drive is selected.

SKEND – Signal that is generated when the servo circuit in the disk drive terminates seek operation and the head is placed on the track.

RCLK – Disk read clock from the drive. Its frequency is the same as the serial data transfer rate.

WCLK – Disk write clock from the drive. Its frequency is the same as the serial data transfer rate.

RWDATA – Disk read/write serial data that is input/output as Non-Return to Zero code.

HOST INTERFACE

The HDC can be directly connected to the HD68000 (MPU) and the HD68450 (DMAC), so that the HDC data is transferred asynchronously with the host system. The HDC data bus is 16-bit wide, in addition, an 8-bit configuration is available by asserting the $\overline{DACK}$ signal externally during reset. The minimum access time that is required for communication between the HDC and the MPU, or between the HDC and the DMAC is listed in Table 1 (wait cycles are not included).

Table 1 Host Interface Minimum Access Time

Transfer Direction \ Data Bus	8-Bit Data Bus (cycles)	16-Bit Data Bus (cycles)
MPU read (HDC to MPU)	3	4
MPU write (MPU to HDC)	3	3
DMA write (memory to HDC)	3	3
DMA read (HDC to memory)	3	4

DRIVE INTERFACE

The HDC can interface with two different types of drives. DIF mode of the Operation Mode register 0 (OM0) selects the drive interface. ST506 interface is selected when DIF is at "0", and SMD interface when DIF is at "1". The external circuits required for HDC drive interface vary according to which interface is used. Figures 3 and 4 show the interface circuits which connect ST506 device and SMD device respectively.

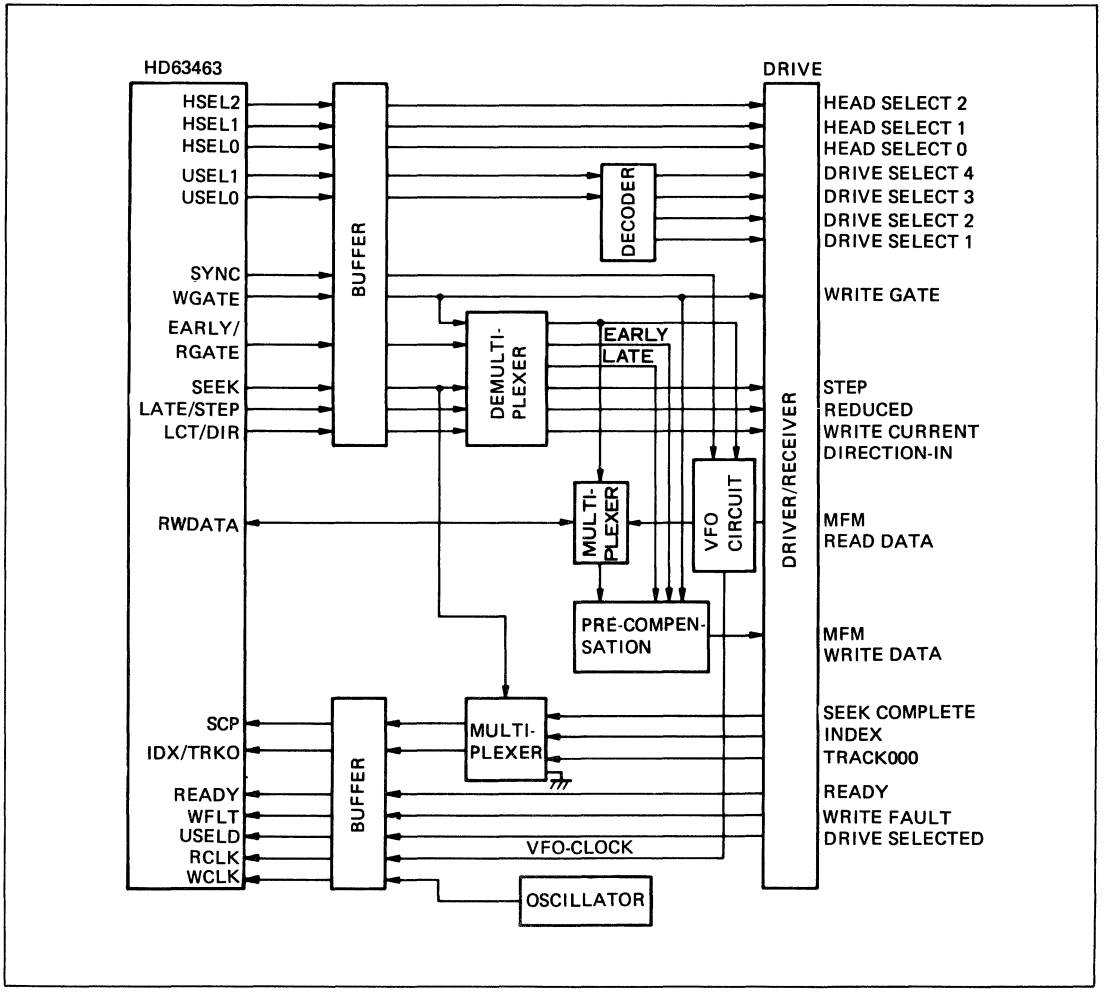


Figure 3 ST506 Interface Circuit

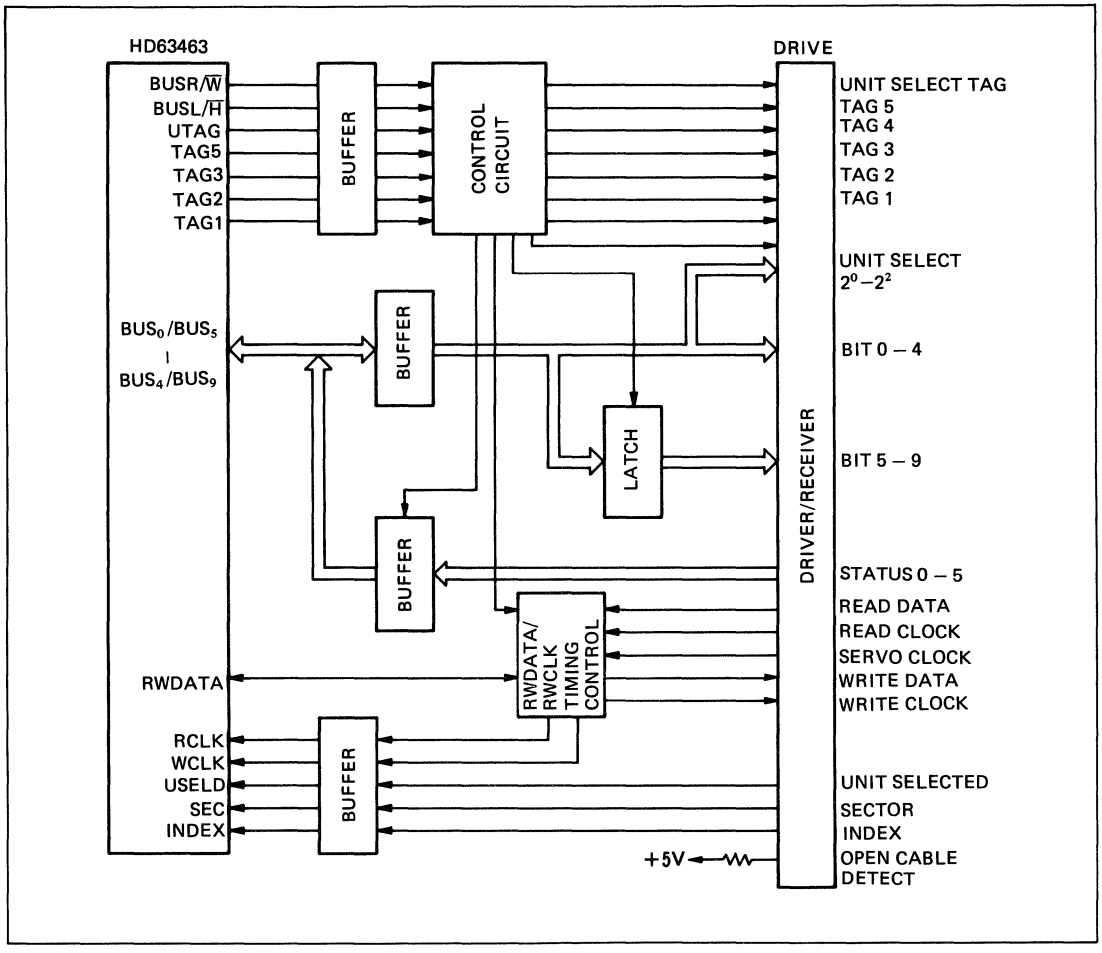


Figure 4 SMD Interface Circuit

SOFTWARE INTERFACE

The HDC is furnished with 22 commands, which are classified into 6 categories; specification, head positioning, disk access, data transfer, drive check, and others.

Table 2 List of Commands

Category	Command	Mnemonic
Specifications	Specify	SPC
Head Positiong	Recalibrate	RCLB
	Seek	SEK
Disk Access	Read Data	RD
	Read Erroneous Data	RED
	Read ID	RID
	Read ID Skew (Note 1)	RIS
	Find ID	FID
	Check Data	CKD
	Compare Data	CMPD
	Write Data	WD
	Write Format	WFM
	Write Format Skew (Note 1)	WFS
Data Transfer	Memory to Buffer	MTB
	Buffer to Memory	BTM
	Open Buffer Write	OPBW
	Open Buffer Read	OPBR
Drive Check	Polling	POL
	Check Drive	CKV
Others	Abort	ABT
	Check ECC	CKE
	Polling Disable	POD
	Recall	RCAL
	Test	TST

(Note 1) Valid only for the hard sector. Disabled for the soft sector.

Specify – Specifies the HDC's operation mode, data transfer mode, etc.

Recalibrate – Moves the drive head to the outermost track (track 0).

Seek – Moves the drive head onto a track specified by the Next Cylinder Address.

Read Data – Reads the data of specified sectors and stores it in the data buffer.

Read Erroneous Data – Reads disk data and stores it in the data buffer no matter a CRC error occurs or not in ID area.

Read ID – Reads ID areas from specified number of sectors.

Read ID Skew – Reads ID area of a sector formatted by Write Format Skew command.

Find ID – Reads ID areas and stores the data in data buffers. ID area containing a CRC error is skipped reading, and the subsequent ID area without any CRC error is searched for.

Check Data – Checks if there is any ECC or CRC error in DATA area of specified sectors. No data is transferred to data buffers or to the main memory while checking.

Compare Data – Compares the data in data buffers and the data read from specified sectors.

Write Data – Writes the data stored in data buffers into DATA area of specified sectors.

Write Format – For the hard sector, formats a specified number of sectors starting with a specified physical sector address. For the soft sector, formats a track.

Write Format Skew – Formats a sector specified by a physical sector address by skewing ID area by 64 bytes.

Memory to Buffer – Transfers data from the main memory to the data buffer by DMA transfer.

Buffer to Memory – Transfers data stored in the data buffer to the main memory by DMA transfer.

Open Buffer Write – Provides initialization of pointer to write data into the data buffer starting from an address specified by Pointer Offset. The data buffer is written in the PIO mode after the command execution ends.

Open Buffer Read – Provides initialization to read the data stored in the data buffer from an address specified by Pointer Offset. The data buffer is read in the PIO mode after the command execution ends.

Polling – Monitors drive status including seek end.

Check Drive – Sets result parameters indicating status of a specified drive to Parameter Block.

Abort – Stops all operations being executed by the HDC.

Check ECC – For ECC errors occurred during RD and RED command execution, reports result parameters indicating addresses and patterns of erroneous data.

Polling Disable – Stops Polling command execution.

Recall – Clears all bits of the status register and sets a buffer pointer to the start address of parameter block so that command parameters can be accepted.

Test – Makes the output pins of the HDC's drive interface three-stated.

Table 3 Command Code, Interrupt Request, and DMA Data Transfer

Command Name	Command Code		Interrupt Factor Bits			DMA Transfer	
	Binary	HEX	CED	SED	DER	DTM = 0	DTM = 1
Specify	1110 1000	E8					
Recalibrate	1100 1000	C8	o	o	o		
Seek	1100 0000	C0	o	o	o		
Read Data	0100 0000	40	o	o	o		o
Read Erroneous Data	0111 0000	70	o	o	o		o
Read ID	0110 0000	60	o	o	o		o
Read ID Skew	0110 1000	68					
Find ID	0110 0001	61	o	o	o		o
Check Data	0100 1000	48	o	o	o		
Compare Data	1000 1000	88	o	o	o		o
Write Data	1000 0111	87	o	o	o		o
Write Format	1010 0011	A3	o	o	o		o
Write Format Skew	1010 1011	AB					
Memory to Buffer	1001 0000	90	o			o	o
Buffer to Memory	0101 0000	50	o			o	o
Open Buffer Read	0011 0000	30					
Open Buffer Write	0011 1000	38					
Polling	0001 0000	10		o	o		
Check Drive	0010 1000	28			o		
Abort	1111 ****	F0-FF	o				
Check ECC	0010 0000	20					
Test	1110 0000	E0					
Polling Disable	0001 1000	18		o	o		
Recall	0000 1000	08					
Inhibited	1101 ****	D0-DF					

o: Set at the end of command execution.

o: DMA transfer is performed.

DMA: Direct Memory Access
DTM: Data Transfer Mode
*: don't care

PROGRAMMING MODEL

Figure 5 shows the internal configuration of the HDC and a programming model. The HDC internally provides an 8-bit STR (Status register), an 8-bit CMR (Command register), a 16-byte PB (Parameter Block) and two 256-byte data buffers (DBUF0 and DBUF1). The data can be written to/read from PB, DBUF0 and DBUF1 by externally accessing DTR (Data Transfer register). Their address are specified by a pointer, and is incremented for each access. Internal processors set pointer value, or select one of PB, DBUF0 and DBUF1 to be connected to DTR. These internal processors are initialized by writing a command from the MPU to CMR. The result of command execution is reflected in the STR.

At the beginning of the command execution, internal processors read command parameters in PB written by the MPU and determine the command operation mode. At the end of the command execution, the MPU reads result parameters in PB written by internal processors.

When the HDC writes data to a disk, the host system sends disk write data to DBUF, then internal processors write the contents of DBUF into the disk. When the HDC reads data from a disk, internal processors read the contents of the disk and stores them into DBUF, then the host system reads data from DBUF. The MPU can access STR, CMR, and DTR while the DMAC can access only DTR in the single addressing mode.

When used in 8-bit mode, the HDC requires 2-byte address space. One byte (RS (Resister Select signal) = 0) is an 8-bit read only STR or an 8-bit write only CMR. Another byte (RS = 1) is an 8-bit DTR.

When used in a 16-bit mode, the HDC requires 2-word address space. One word (RS = 0) consists of an 8-bit CMR and an 8-bit read only STR. Another word (RS = 1) serves as a 16-bit DTR.

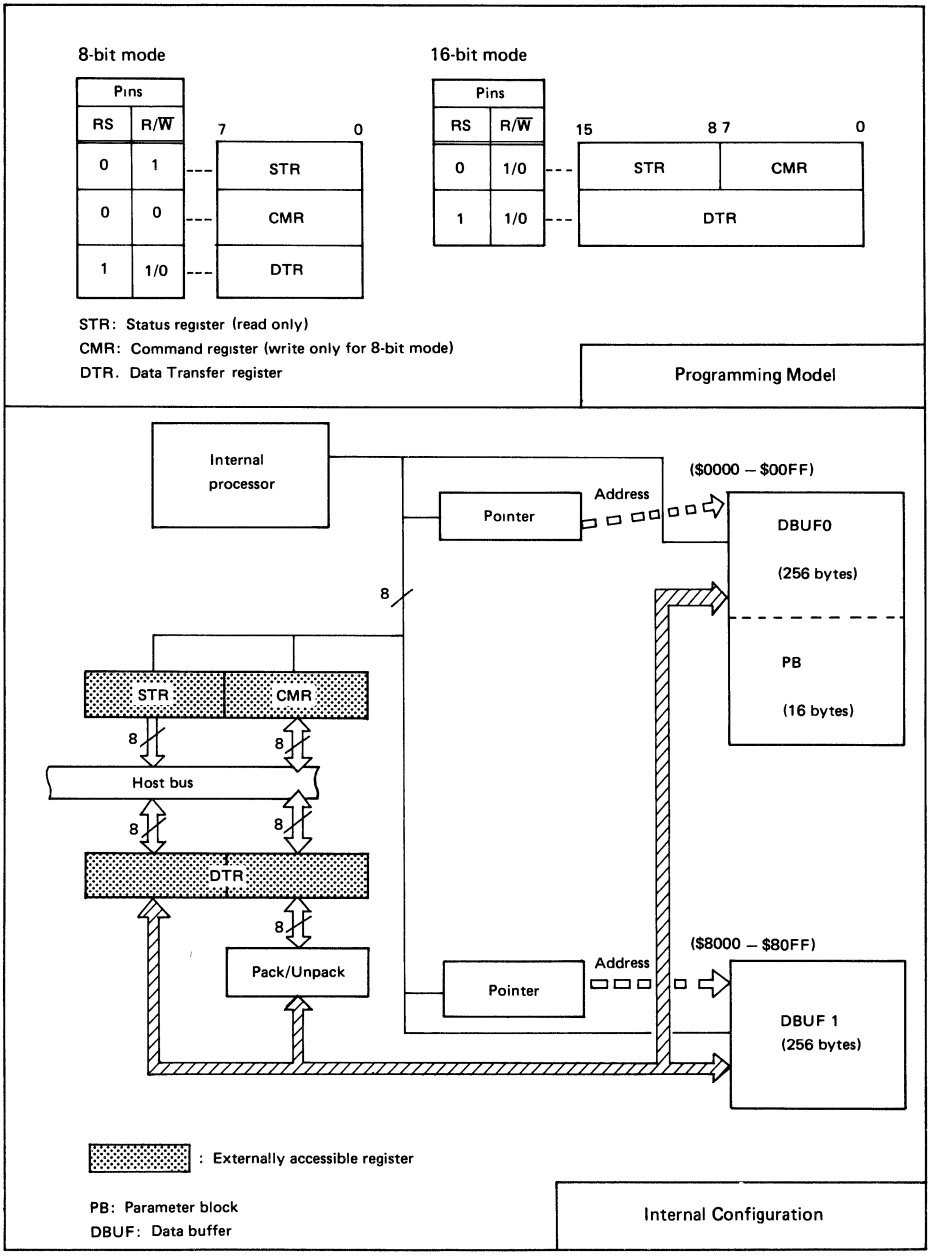


Figure 5 Internal Configuration and Programming Model

When the HDC is either in idle state or command execution end state, the MPU can access PB by accessing DTR. While the HDC is executing a command (during data transfer), DBUF0 or DBUF1 can be accessed by accessing DTR. Before accessing DBUF0 or DBUF1, the MPU must issue a command to open the buffer.

STATUS REGISTER

The bit configuration of the Status register is shown in the figure below, and each bit is described in Table 4.

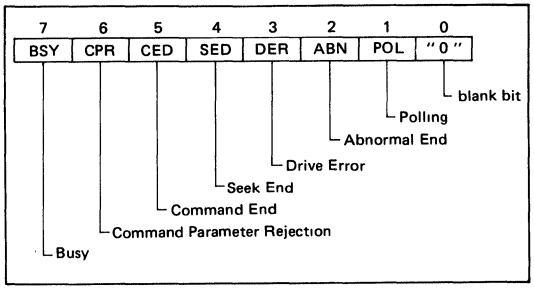


Table 4 Status Register Bit Description

Bit	Abbr.	Bit Name	Set "1" Condition	Reset "0" Condition	Interrupt Source Bit	Description
7	BSY	Busy	Command acknowledged	Command execution end (except for POL command)		While HDC is executing a command, BSY bit is set to "1".
6	CPR	Command Parameter Rejection	Command execution	RCAL command received		With this bit reset to "0", command parameters can be written.
5	CED	Command End	Command execution end	RCAL command received	○	Set to "1" when command shown in table 3 ends. When this bit is set, HDC asserts $\overline{IRQ}$ signal.
4	SED	Seek End	Drive seek end detected	RCAL command received	○	If detecting drive seek end during execution of command shown in table 3, HDC sets "1" in this bit at the end of command execution.
3	DER	Drive Error	Drive error detected	RCAL command received	○	If detecting drive error during execution of command shown in table 3, HDC sets "1" in this bit at the end of command execution.
2	ABN	Abnormal End	Error detected	RCAL command received		If acknowledging errors such as illegal command, drive faults, data over/under run, the HDC sets "1" to ABN at the end of command execution. The SSB contains the error code.
1	POL	Polling	POL command received	POD command received, seek operation end detected, drive error detected		Set to "1" during execution of POL command.
0						Blank bit, always set to "0".

○: An interrupt is generated when this bit is set.

HDC CONTROL PROCEDURE

The MPU's procedure to control the HDC is shown in figure 6. To control the HDC, the MPU must read STR of the HDC. The MPU may issue command parameters to PB in the HDC only when both BSY and CPR bits are cleared.

This enables the HDC to change its status from idle state to command wait state. Although a data buffer pointer does not indicate the start address of PB under command wait state, STR has the same contents as in the idle state. It is impossible to distinguish these two internal HDC states externally.

After this, the MPU issues a command. The HDC executes a command after setting BSY bit to "1". At the end of command execution, result parameters are stored in PB, the CPR bit is set to "1", and BSY bit is cleared. Under this condition, the MPU reads result parameters from PB. Issuing Recall command after this enables the HDC state to change from command execution end state to idle state.

Some commands do not require either or both of the command parameter and result parameter. For some commands, the CED bit, SED bit, or DER bit is set to "1", which enables the HDC to generate an interrupt request to the MPU.

In the DMA (direct memory access) mode, data transfer takes place between the main memory and the HDC when a disk access command is received. For this reason, the MPU must initialize the DMAC before issuing a disk access command to the HDC. Data such as system memory address and number of transfer words are written into the DMAC register.

When the MPU writes data into internal control register in the DMAC, the DMAC state changes from the idle state to transfer request wait state. Upon reception of a transfer request signal ($\overline{\text{DREQ}}$) from the HDC, the DMAC transfers data to/from the HDC and system memory until specified number of words are transferred. The DMAC may generate an interrupt request to the MPU when the transfer is completed.

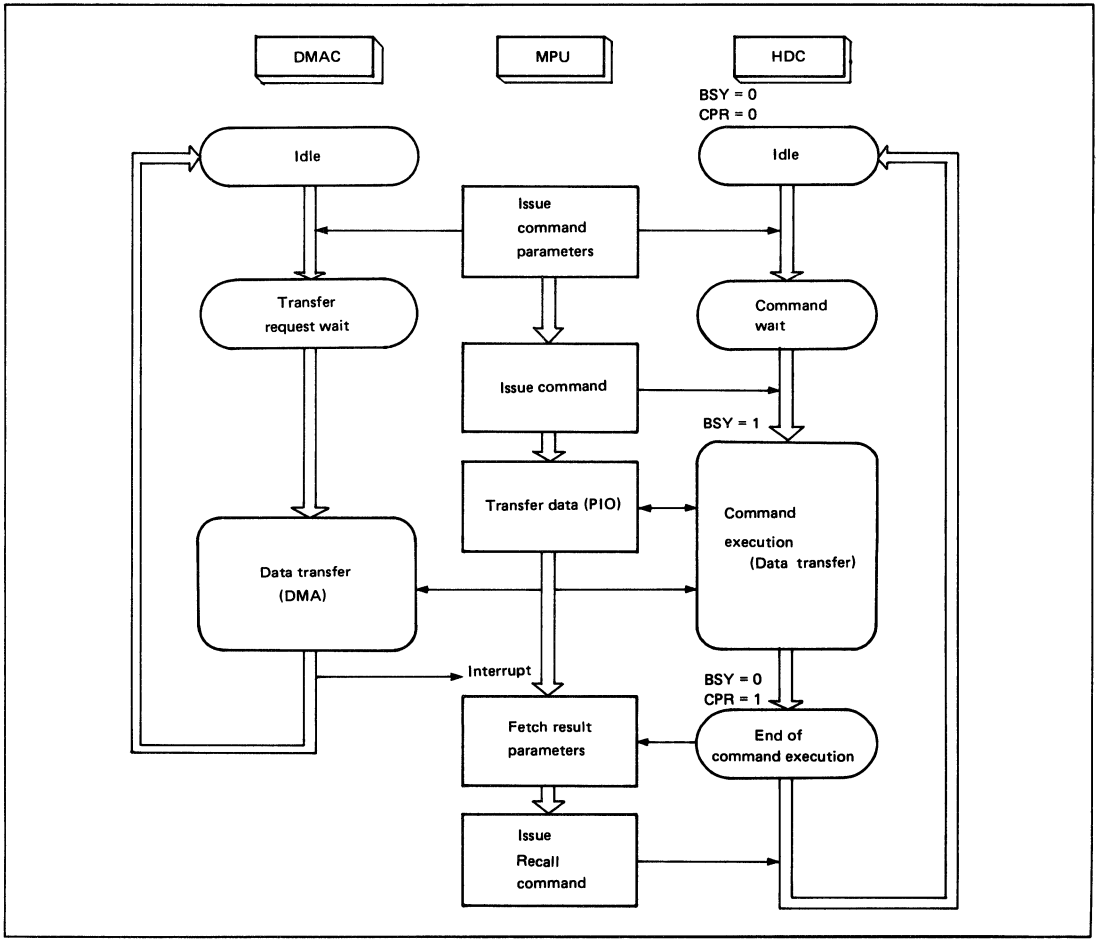


Figure 6 HDC Control Procedure

COMMAND PARAMETERS

Command parameters are listed in Table 5. Command parameters used by the HDC to control ST506 type hard disk drive are listed in the upper row of each command, and those for the SMD type in the lower row.

Table 5 Command Parameter (byte organization)

Commands	Parameters (Upper row: ST506 / Lower row: SMD)
Specify	OM0 OM1 OM2 CUL TO/NCH NCL NH NS SH/RL GPL1 GPL2 GPL3 LCCH LCCL PCCH PCCL OM0 OM1 OM2 CUL TO/NCH NCL NH NS SH/RL GPL1 GPL2 RGTLT
Recalibrate	US $00 US $00
Seek	US $00 NCAH NCAL US $00 NCAH NCAL
Read Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Read Erroneous Data	US PHA SCNTH SCNTL US PHA $00 PSA SCNTH SCNTL
Read ID Read ID Skew (Note 1)	US PHA $00 OFFSET $00 SCNTL US PHA $00 PSA $00 SCNTL
Find ID	US PHA $00 OFFSET $00 SCNTL US PHA $00 PSA $00 SCNTL
Check Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Compare Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Format Write Format Skew (Note 1)	US PHA SCNTH SCNTL US PHA $00 PSA SCNTH SCNTL
Memory to Buffer	POFFH POFFL POFFH POFFL
Buffer to Memory	POFFH POFFL POFFH POFFL
Open Buffer Read	POFFH POFFL POFFH POFFL
Open Buffer Write	POFFH POFFL POFFH POFFL
Polling	None
Check Drive	US $00 US $00
Abort	None
Check ECC	None
Test	None
Polling Disable	None
Recall	None

(Note 1) Read ID Skew and Write Format Skew are valid only for SMD interface.

SPECIFY COMMAND PARAMETERS

Parameters of SPC command may be used to specify the HDC operation mode and the disk format. Parameters are listed in Table 6. Contents of these parameters are different according to which type of drive is used: either ST506 or SMD. Each parameter is described in Tables 7 and 8. Table 7 lists parameters which are specified by a bit, and Table 8 lists parameters which are specified by 3–16 bits.

The HDC supports soft sector format (in ST506 interface) and hard sector format (in SMD interface) which are shown in Figure 7.

Table 6 Specify Command Parameter Organization

	Bit 7	6	5	4	3	2	1	0
OM0	SECT	MOD	DIF	PADP	ECD	CRCP	CRCI	ACOR
OM1	DTM	BRST	CEDM	SEDM	DERM	0	AMEX	PSK
OM2	SL (ST506)							
	CUL							
	TO						NCH	
	NCL							
	NH							
	NS							
	SH					RL		
	GPL1							
	GPL2							
	GPL3							
	LCC High (LCCH)							
	LCC Low (LCCL)							
	PCC High (PCCH)							
	PCC Low (PCCL)							
(SMD)								
OM2	0	0	0	0	SOFM	SOFP	STBL	STBE

Table 7 Specify Command Parameters (a)

Abbreviation	Name	0	1	ST506	SMD
SECT	Sector Organization	Soft Sector	Hard Sector	0	1
MOD	Data Modulation	MFM	NRZ	0	1
DIF	Drive Interface	ST506	SMD	0	1
PADP	PAD Pattern	$00	$4E	*	0
ECD	Error Check Code	CRC	ECC	*	*
CRCP	CRC Polynomial	$X^{16} + 1$	$X^{16} + X^{12} + X^5 + 1$	*	*
CRCI	CRC Initial Value	$0000	$FFFF	*	*
ACOR	Automatic Correction	Disabled	Enabled	*	*
DTM	Data Transfer Mode	PIO	DMA	*	*
BRST	DMA Burst Mode	Cycle Steal	Burst	*	*
CEDM	Command End Mask	Unmasked	Masked	*	*
SEDM	Seek End Mask	Unmasked	Masked	*	*
DERM	Drive Error Mask	Unmasked	Masked	*	*
AMEX	Address Mark Exclude	Included	Not Included	*	*
PSK	Parallel Seek	Normal	Parallel	*	1
SOFM	Servo Offset Minus	Normal	Minus	None	*
SOFP	Servo Offset Plus	Normal	Plus	None	*
STBL	Strobe Late	Normal	Late	None	*
STBE	Strobe Early	Normal	Early	None	*

* Either 0 or 1

Table 8 Specify Command Parameters (b)

Abbreviation	Name	ST506	SMD
SL	Step Pulse Low	8 bits	None
CUL	Connecting Unit List	4 bits	8 bits
TO	Read/Write Time-over	6 bits	6 bits
NC	Number of Cylinders	10 bits	10 bits
NH	Number of Heads	3 bits	5 bits
NS	Number of Sectors	8 bits	8 bits
SH	Step Pulse High	5 bits	None
RL	Record Length	3 bits	3 bits
GPL1	Gap Length 1 (8 bits)	GAP1	HEAD SCAT
GPL2	Gap Length 2 (8 bits)	PLO SYNC	PLO SYNC
GPL3	Gap Length 3 (8 bits)	GAP3	RGATE Latency
LCC	Low Current Cylinder	16 bits	None
PCC	Precompensation Cylinder	16 bits	None

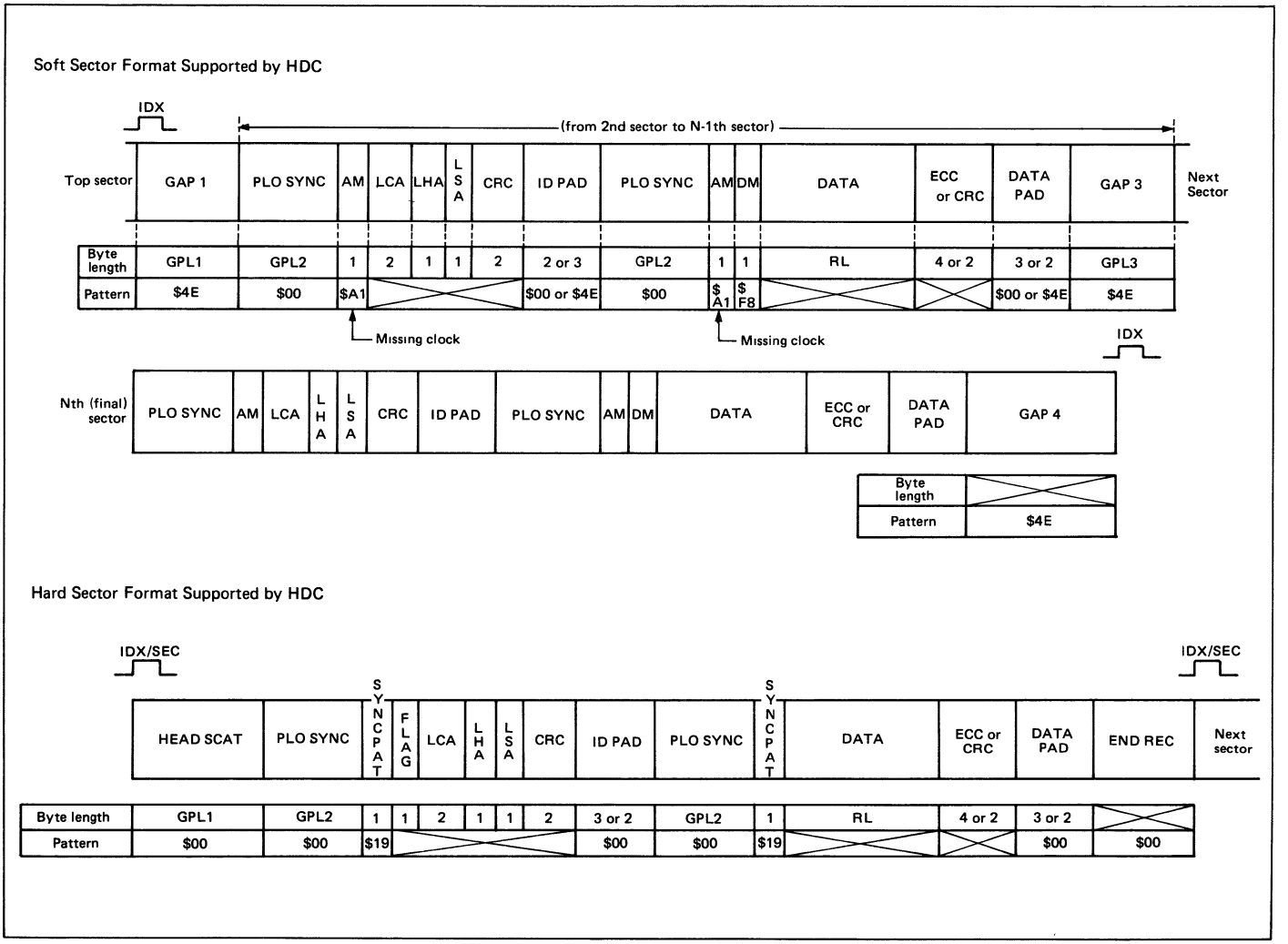


Figure 7 Disk Format

OM0 (Operation Mode 0)

(1) SECT (Sector Format) bit

This bit specifies the format of the drive to be connected to the HDC. There are two drive formats available: hard sector and soft sector.

SECT = 1: Hard Sector Format
SECT = 0: Soft Sector Format

(2) MOD (Modulation) bit

This bit specifies modulation mode for data written to/read from the drive.

MOD = 1: NRZ (Non Return to Zero)
MOD = 0: MEM (Modified FM)

(3) DIF (Drive Interface) bit

This bit specifies the type of drive interface: either ST506 or SMD. The pin function of the HDC changes according to the interface type.

DIF = 1: SMD Interface
DIF = 0: ST506 Interface

In SMD interface, the HDC performs seek instruction, head specification, drive status check, etc to the drive through 5-bit bi-directional buffer BUS_0/BUS_5–BUS_4/BUS_9.

In ST506 interface, the HDC makes the drive perform seek operation by issuing step pulses.

(4) PADP (PAD Pattern) bit

This bit specifies the data pattern of PAD area that follows ID and DATA areas. The value of the PADP bit gives the data pattern of PAD area that is written into the drive by WFM or WD command execution.

	Hard Sector	Soft Sector
PADP = 1	Prohibited	$4E
PADP = 0	$00	$00

(5) ECD (Error Check Code) bit

This bit specifies the error check code which is added to the end of the DATA area. CRC code is always specified for the ID area regardless of ECD bit.

ECD = 1: ECC (Error Correction Code)
ECD = 0: CRC (Cyclic Redundancy Check Code)

ECC enables error detection and correction. A 4-byte ECC code is added to the end of DATA area. A generation polynominal G(x) of ECC is as follows (the initial value is fixed to "00").

$$G(x) = (x^{21} + 1)(x^{11} + x^2 + 1)$$
$$= x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$$

CRC enables error detection, but not error correction. A 2-byte CRC code is added to the end of DATA area. A generation polynominal G(x) of CRC is specified by the CRCP bit.

(6) CRCP (CRC Polynominal) bit

This bit determines the polynominal G(x) that generates CRC of ID and DATA areas when ECD = 0.

CRCP = 1: $G(x) = x^{16} + x^{12} + x^5 + 1$
CRCP = 0: $G(x) = x^{16} + 1$

(7) CRCI (CRC Initial) bit

This bit sets the initial value of CRC.

CRCI = 1: Initial value = $FFFF
CRCI = 0: Initial value = $0000

(8) ACOR (Automatic Correction) bit

This bit selects whether or not the HDC will automatically correct an error detected in DATA area during RD command execution.

ACOR = 1: Automatic correction is performed.
ACOR = 0: Automatic correction is not performed.

Automatic correction mode is valid when ECC is specified as the error check code of DATA area and the sector length is 256 bytes (RL = $01, ECD = 1). For any other cases specify "0" to the ACOR bit.

OM1 (Operation Mode 1)

(1) DTM (Data Transfer Mode) bit

This bit is used to specify data transfer operation between the HDC and the main memory during the execution of the following commands:

RD	RED	RID
RIS	FID	WD
CMPD	WFM	WFS

These commands normally perform transfer between drive and memory via HDC data buffers. However, it is possible to cease transfer between the HDC and memory during these command execution by utilizing DTM bit.

DTM = 1: DMA mode
DTM = 0: PIO mode

In DMA mode, the HDC performs transfer between drive and memory via HDC data buffer. In this case, DMA transfer is performed between the HDC and memory, and transfer mode is specified by BRST bit.

In PIO mode, the HDC performs transfer between drive and the HDC. In this case, transfer between the HDC and main

memory must be supported by the host system using one of four buffer access commands of the HDC: MTB, BTM, OPBR, and OPBW.

(2) BRST (DMA Burst) bit
This bit specifies DMA transfer mode of buffer access commands and drive access commands which perform transfer between the HDC and the main memory.

BRST = 1: Burst mode
BRST = 0: Cycle Steal mode

(3) CEDM, SEDM, DERM bits
CEDM (Command End Mask), SEDM (Seek End Mask), and DERM (Drive Error Mask) bits specify whether the $\overline{IRQ}$ signal is to be asserted or not. CEDM, SEDM, and DERM correspond to CED (Command End), SED (Seek End), and DER (Drive Error) bits in STR (Status register).

1: $\overline{IRQ}$ is masked (not asserted).
0: $\overline{IRQ}$ is not masked (asserted).

Mask bit	Corresponding bits in STR	
CEDM	CED	bit 5
SEDM	SED	bit 4
DERM	DER	bit 3

(4) AMEX (Address Mark Excluded) bit
This bit specifies whether or not the byte-synchronization pattern marking the beginning of ID area or DATA area (AM in soft sector, SYNCPAT in hard sector) is to be included in the CRC or ECC error detection span. The AMEX bit affects the byte length of ID PAD area and DATA PAD area.

	AM or SYNCPAT	PAD Length
AMEX = 1	Excluded	2 bytes
AMEX = 0	Included	3 bytes

(5) PSK (Parallel Seek) bit
This bit specifies seek operation mode, and is valid only in ST506 interface (in SMD interface, PSK must be fixed to "1"). The HDC specifies step pulse issue timing by utilizing the value of OM2, SH, and PSK bits.

PSK = 0: Normal Seek mode
PSK = 1: Parallel Seek mode

In Normal Seek mode, the HDC issues step pulses in long cycle (0.1–32 ms). SEK and RCLB command execution ends when the HDC issues step pulses and then detects seek end.

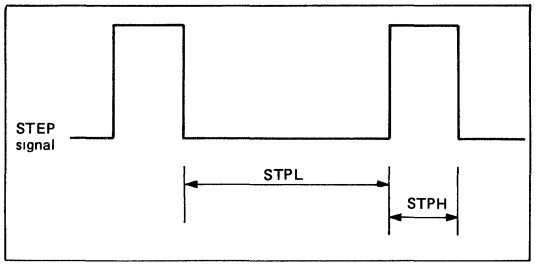
In Parallel Seek mode, the HDC issues step pulses in short cycle (0.5–115 μs). SEK and RCLB command execution ends when the HDC issues step pulses. Since the HDC does not check the seek end, parallel seek operation in multiple drives is realized by issuing SEK or RCLB command to these drives. Seek end is to be checked by using POL command.

OM2 (Operation Mode 2)
This 8-bit register specifies step pulse low width in ST506 interface, and specifies drive control output signal during disk read command execution in SMD interface.

In ST506 interface, OM2 indicates SL which specifies step pulse low width (STPL: Step Pulse Low). Low-speed seek mode (Normal Seek mode) is selected when PSK = 0, and high-speed seek mode (Parallel Seek mode) is selected when PSK = 1. Highest seek speed is realized when PSK = 1 and SL = $FF. The relation between step pulse low width and SL is shown in the following Table (see Step Pulse High/Record Length register to specify step pulse high width).

7	6	5	4	3	2	1	0
Step Pulse Low (SL)							

Seek Mode	SL	STPL (step pulse low)
Normal seek (PSK = 0)	SL = $00	STPL = 988 CLK
	$01 ≦ SL ≦ $FE (1) (254)	STPL = (SL − 1) x 1280 + 2364 CLK (2364 CLK ≦ STPL ≦ 326204 CLK)
	SL = $FF	Disabled
Parallel seek (PSK = 1)	SL = $00	STPL = 27CLK
	$01 ≦ SL ≦ $FE (1) (254)	STPL = SL x 6 + 28 CLK (34CLK ≦ STPL ≦ 1152 CLK)
	SL = $FF	STPL = 5CLK



In SMD interface, OM2 specifies drive control output signal from the HDC during data read command execution. In data write command (all the commands that assert WGATE signal) and SEK, RCLB command execution, outputs of drive control signals are low regardless of the contents of OM2. Bits 4–7 in OM2 are to be set to "0".

SOFM bit: With SOFM = 1, the drive head is offset from the normal position away from the spindle.
SOFP bit: With SOFP = 1, the drive head is offset from the normal position towards the spindle.
STBL bit: With STBL = 1, the data from the drive PLO data separator is strobed later than usual.
STBE bit: With STBE = 1, the data from the drive PLO data separator is strobed earlier than usual.

7	6	5	4	3	2	1	0
0	0	0	0	SOFM	SOFP	STBL	STBE

Strobe Early
Strobe Late
Servo Offset Plus
Servo Offset Minus

CUL (Connecting Unit List)
This register stores bit-map information indicating which drive is connected to the HDC.

In ST506 interface, bits 0–3 correspond to drives 0–3 respectively. To connect a drive, write "1" into the corresponding bit (up to 4 drives can be connected).

7	6	5	4	3	2	1	0
0	0	0	0				

Drive Unit 0
Drive Unit 1
Drive Unit 2
Drive Unit 3

In SMD interface, bits 0–7 correspond to drives 0–7 respectively. To connect a drive, write "1" into the corresponding bit (up to 8 drives can be connected).

7	6	5	4	3	2	1	0

Drive Unit 0
Drive Unit 1
Drive Unit 2
Drive Unit 3
Drive Unit 4
Drive Unit 5
Drive Unit 6
Drive Unit 7

TO/NCH, NCL (Read/Write Time Over, Number of Cylinders High/Low)
NCH and NCL registers specify the number of cylinders in disk drive, and time-over during disk access command execution.

(1) TO (Read/Write Time Over)
The high-order 6 bits in TO/NCH are used to assign the ID search time: time-over (t_{over}). According to the value of TO, the HDC sets time-over period as follows.
$\$01 \leqq TO \leqq \$3F$ (TO = $00 is prohibited.)
$TO \times 8 \times 10^4\ CLK \leqq t_{over} \leqq (TO + 1) \times 8 \times 10^4\ CLK$

(2) NC (Number of Cylinders)
The low-order 2 bits of TO/NCH and 8 bits of NCL specify the number of cylinders (NC). NC is 1023 at a maximum. Its value is number of cylinders minus 1.

The HDC uses NC to issue NC + 10 step pulses during RCLB command execution (ST506 interface), or to check whether or not the command parameter NCA (Next Cylinder Address) exceeds NC during SEK command execution.

15	14	13	12	11	10	9	8
Read/Write Time Over						NCH	

Number of Cylinders High

7	6	5	4	3	2	1	0
Number of Cylinders Low							

NH (Number of Heads)
This register indicates the number of heads. Its value is to be number of drive heads minus 1.

In disk access command execution, the HDC checks whether or not PHA (Physical Head Address) specified by command parameters exceeds NH. When PHA exceeds NH, the HDC sets IPH (Invalid Physical Head Address) to result parameter SSB (Sense Status Byte) and abnormally terminates the execution.

To select a head during multiple track operation in disk access command execution, the HDC checks whether PHA exceeds NH or not. When PHA exceeds NH, the HDC sets IPH to SSB and abnormally terminates the execution.

7	6	5	4	3	2	1	0
Number of Heads							

In ST506 interface, up to 8 heads can be selected ($00 ≦ NH ≦ $07). Bits 3–7 must be fixed to "0".

7	6	5	4	3	2	1	0
0	0	0	0	0	2^2	2^1	2^0

In SMD interface, up to 32 heads can be selected ($00 ≦ NH ≦ $1F). Bits 5–7 must be fixed to "0".

7	6	5	4	3	2	1	0
0	0	0	2^4	2^3	2^2	2^1	2^0

NS (Number of Sectors)
This register indicates the number of sectors. Its value is number of sectors/track minus 1 ($00 ≦ NS ≦ $FE).

In data read/write command execution, the HDC checks whether LSA (Logical Sector Address) exceeds NS or not.

In multiple sector operation in data read/write command execution, the HDC checks whether LSA exceeds NS or not each time LSA is incremented after one sector operation. If LSA exceeds NS, the HDC sets "0" to LSA, increments LHA and PHA, and compares NH and PHA. If NH exceeds PHA, the HDC executes multiple track operation. If PHA exceeds NH, the HDC sets IPH (Invalid Physical Head Address) to result parameter SSB and abnormally terminates the execution.

7	6	5	4	3	2	1	0
Number of Sectors							

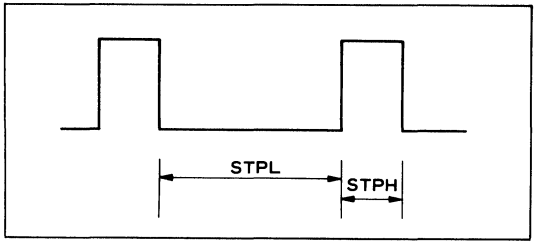
SH/RL (Step Pulse High/Record Length)

7	6	5	4	3	2	1	0
Step Pulse High (SH)					Record Length (RL)		

(1) SH (Step Pulse High)
The high-order 5-bit SH/RL indicates step pulse high width (STPH: Step Pulse High) in ST506 interface.

STPH is fixed to 2CLK in highest speed seek mode (PSK = 1 and SL = $FF). Otherwise, SH sets STPH regardless of the PSK bit. The relation between STPH and SH is shown in the following table. SH is ignored when maximum speed seek mode is selected in ST506 interface.

In SMD interface, the high-order 5 bits are to be fixed to "0".



SH	STPH (step pulse high)
SH = * * : don't care	STPH = 2 CLK (Note 1)
SH = $00	STPH = 3 CLK
$01 ≦ SH ≦ $1F (1) (31)	STPH = SH x 3 + 1 CLK (4 CLK ≦ STPH ≦ 94 CLK)

(Note 1) Highest-speed seek mode (PSK = 1, SL = $FF)

(2) RL (Record Length)
The low-order 3-bit SH/RL indicates record length per sector.

RL			Record Length
Bit 2	Bit 1	Bit 0	
0	0	0	Inhibited
0	0	1	256 bytes
0	1	0	512 bytes
0	1	1	1024 bytes
1	0	0	2048 bytes
1	0	1	4096 bytes
1	1	0	Inhibited
1	1	1	Inhibited

GPL1, 2 (Gap Length 1, 2)
These registers specify the length of gap and SYNC area in the sector during WD and WFM command execution.

GPL1 specifies the length of gap areas (GAP1 in soft sector, HEAD SCAT in hard sector) that follow an index or a sector pulse by byte. It is used for WFM command execution. These areas are formatted 6 bytes longer than the value set to GPL1 during the command execution. [$00 ≦ GPL1 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 1							

GPL2 specifies the length of SYNC area located at the beginning of ID and DATA areas by byte. It is used for WD and WFM commands. This area is formatted 3 bytes longer than the value set to GPL2 during the command execution. [$08 ≦ GPL2 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 2							

GPL3/RGTLT (Gap Length 3, Read Gate Latency)
GPL3/RGTLT specifies the length of GAP3 for the soft sector and read gate latency delay for the hard sector by byte.

GPL3 specifies the length of GAP3 located at the end of a sector in soft sector format by byte. It is used for WFM command. This area is formatted 3 bytes longer than the value set to GPL3. [$09 ≦ GPL3 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 3							

RGTLT specifies the time period between the detection of an index or a sector pulse and the assertion of RGATE in unit of byte. It is used for disk read commands. RGATE is asserted 5 bytes later than the value set to RGTLT. RGTLT must be set to assert RGATE at the beginning of or before PLO SYNC area in the ID field. During RIS command execution, 64 bytes are added to the amount of latency automatically. [$00 ≦ RGTLT ≦ $FF]

7	6	5	4	3	2	1	0
RGATE Latency							

LCCH, LCCL (Low Current Cylinder High/Low)
For the inner cylinders of the drive, it is necessary to reduce write current during WFM and WD command execution. These registers specify address of the outermost cylinder from where write current is reduced. This is valid only in ST506 interface. When a disk write command is executed to any cylinder whose address is equal to or greater than LCC, the HDC asserts the LCT pin to high. [$0000 ≦ LCC ≦ NC (Number of Cylinders)]

15	14	13	12	11	10	9	8
Low Current Cylinder High							

7	6	5	4	3	2	1	0
Low Current Cylinder Low							

PCC (Precompensation Cylinder)
This register specifies the address of the outermost cylinder from where compensation of the bit data timing is required. This is valid only in ST506 interface. When a disk write command is executed to any cylinder whose address is equal to or greater than PCC, either EARLY or LATE signal is generated in accordance with the bit data timing. [$0000 ≦ PCC ≦ NC]

15	14	13	12	11	10	9	8
Pre-compensation Cylinder High							

7	6	5	4	3	2	1	0
Pre-compensation Cylinder Low							

OTHER COMMAND PARAMETERS
The following describes command parameters other than SPC command parameters in alphabetical order.

(1) FLAG
This parameter is used to specify the FLAG byte of ID area of a hard sector that the HDC will access. If the FLAG given by the command parameter does not match the FLAG read from ID area of the disk, the HDC will not access the sector.

(2) LCA (Logical Cylinder Address)
This parameter is used to specify the logical cylinder address of ID area (16 bits: the high-order 8 bits for LCAH and the low-order 8 bits for LCAL) of a sector that the HDC will access. If LCA given by the command parameter does not match LCA read from ID area, the HDC will not access the sector. In soft sector format, it is prohibited to specify $F8 to the high-order 8 bits (LCAH).

(3) LHA (Logical Head Address)
LHA is used to specify the logical head address of ID area of a sector that the HDC will access. If LHA given by the command parameter does not match the LHA read from ID area, the HDC will not access that sector. In multiple track operation, LHA is automatically incremented by one. Since LHA is logical, it may exceed the number specified by the parameter NH (number of heads).

(4) LSA (Logical Sector Address)
LSA is used to specify the logical sector address of ID area that the HDC will access. If LSA given by the command parameter does not match LSA read from ID area, the HDC will not access the sector. In multiple sector operation, LSA is automatically incremented by one. Since LSA is compared with the control register NS (number of sectors) for switching of heads, the LSA must not exceed the NS.

(5) NCA (Next Cylinder Address)
This parameter is used to specify the physical address (10 bits) of a cylinder to which the head will move when a SEK command is issued. The outermost cylinder address is $0000. The high-order 8 bits of NCA are used for NCAH and the low-order 8 bits for NCAL. The high-order 6 bits of NCAH must be fixed to "0". If NCA exceeds NC, com-

mand execution abnormally terminates.

(6) OFFSET
OFFSET specifies how many sectors to be skipped reading after an index pulse. Then the HDC reads ID fields, and stores them into the data buffer.

(7) PHA (Physical Head Address)
The MPU specifies PHA when issuing a disk access command. Unlike LHA, PHA is physical, and the bit status of PHA is directly output as HSEL signals. The high-order 5 bits of PHA must be fixed to "0" for ST506 interface, and the high-order 3 bits for SMD interface. In multiple track operation, PHA is automatically incremented by one within the HDC if another head switching is required. If PHA exceeds the value given by NH, the command execution will abnormally terminate.

(8) POFF (Pointer Offset)
The MPU specifies a transfer start address (16 bits) when issuing a command for accessing the data buffer. The MSB of the high-order 8 bits (POFFH) selects one of two data buffers, and the remaining 7 bits must be fixed to "0". The low-order 8 bits (POFFL) specifies a transfer start address of the selected data buffer (256 bytes). For the 16-bit data bus, POFF is limited to an even address only.

(9) PSA (Physical Sector Address)
This parameter is used to specify a physical address of a hard sector at which the execution of RID, RIS, FID, WFM, or WFS starts. If PSA is $00, the sector following an index pulse is specified.

(10) SCNT (Sector Count)
This parameter is used to specify the number of sectors (16 bits) that the HDC will continuously access in a disk access command execution. Upper 8 bits are SCNTH, and lower 8 bits are SCNTL. Up to 1024 sectors are specified in ST506 interface (128 sectors x 8 heads), and up to 8160 sectors are specifiable in SMD interface (255 sectors x 32 heads). For commands relating to the ID (RID and WFM), they perform no multiple track operation. In addition, maximum number of sectors that can be formatted at a time by WFM command is 128 for soft sector, and 102 for hard sector.

(11) US (Unit Select)
The MPU specifies the address (8 bits) of a target drive when issuing a head positioning, disk access or drive check command. The contents of US are directly output from USEL signals. The high-order 6 bits of US must be fixed to "0" for ST506 interface, and the high-order 5 bits for SMD interface. US is the high-order 8 bits of a 16-bit word, and the low-order 8 bits of the word are PHA or $00. It is not necessary to issue $00 to the low-order 8 bits when CKV or RCLB command is issued.

RESULT PARAMETERS

Result parameters are listed in Table 9. In this table, result parameters used by the HDC to control ST506 type hard disk drive are found in the upper row of each command, and those for SMD type in the lower row.

Table 9 Result Parameters (Byte-organized)

Command	Parameter (Upper row: ST506 / Lower row: SMD)
Recalibrate	$00 SSB US VUL $00 SSB US VUL
Specify	($00 SSB) ($00 SSB)
Seek	$00 SSB US VUL $00 SSB US VUL
Read Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Read Erroneous Data	$00 SSB US PHA SCNTH SCNTL $00 SSB US PHA $00 PSA SCNTH SCNTL
Read ID Read ID Skew (Note 1)	$00 SSB US PHA $00 SCNTL $00 SSB US PHA $00 PSA $00 SCNTL
Find ID	$00 SSB US PHA $00 SCNTL $00 SSB US PHA $00 PSA $00 SCNTL
Check Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Compare Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Format Write Format Skew (Note 1)	$00 SSB US PHA SCNTH SCNTL $00 SSB US PHA $00 PSA SCNTH SCNTL
Memory to Buffer	($00 SSB) ($00 SSB)
Buffer to Memory	($00 SSB) ($00 SSB)
Open Buffer Read	($00 SSB) ($00 SSB)
Open Buffer Write	($00 SSB) ($00 SSB)
Polling	$00 SSB US VUL $00 SSB US VUL
Check Drive	$00 SSB US $00 DST0 $00 $00 SSB US $00 DST0 DST1 DST2 DST3
Abort	$00 SSB $00 SSB
Check ECC	$00 SSB EA0 EA1 EP0 EP1 EP2 $00 $00 SSB EA0 EA1 EP0 EP1 EP2 $00
Test	($00 SSB) ($00 SSB)
Polling Disable	($00 SSB US VUL) ($00 SSB US VUL)
Recall	($00 SSB US VUL) ($00 SSB US VUL)

(Note 1) Read ID Skew and Write Format Skew are valid only for SMD.
(Note 2) Parenthesized parameters are reported when a command is issued under the illegal condition.

DST (Drive Status)

Table 10 Drive List (DST)

Bit		7	6	5	4	3	2	1	0
ST506	DST0	READY	SCP	TRK0	0	WFLT	0	0	0
SMD	DST0	*	*	*	WPRT	FLT	SKERR	OCYL	URDY
	DST1	*	*	SELER	WERR3	WERR2	WERR1	SERR2	SERR1
	DST2	*	*	SAD32	SAD16	SAD8	SAD 4	SAD 2	SAD 1
	DST3	*	*	DTP32	DTP16	DTP8	DTP4	DTP2	DTP1

* Depends on the state of BUS_1/BUS_6 – BUS_4/BUS_9.

Each bit of DST indicates drive interface input signal level. DST0 (1 byte) is reported in ST506 interface, and DST0–3 (4 bytes) are reported in SMD interface.

In ST506 interface, the WFLT bit in DST0 indicates the signal level of WFLT pin. Even if WFLT signal is momentarily asserted, the internal latch memorizes this and reflects its state on WFLT bit. When WFLT signal is negated, the latch read operation by the HDC clears this latch.

In SMD interface, the HDC reads 8 bits by 4 words of the drive status signal which is selected by signals TAG2 and TAG5.

TAG2	TAG5	Status
0	0	DST0
0	1	DST1
1	0	DST2
1	1	DST3

Following (1) through (5) are read during CKV command execution and checked during disk access command execution. DST1 through DST3 are referred to during CKV command execution.

Status that each bit in DST1–3 indicates may vary according to the drive connected to the HDC. Following descriptions indicate DST bit function when the HDC is connected to a Hitachi 8″ disk drive, DK-812S.

(1) URDY (Unit Ready)
This bit indicates that a selected drive is in ready state.

(2) OCYL (On Cylinder)
This bit indicates that a head is positioned correctly on a track.

(3) SKERR (Seek Error)
This bit indicates that errors have been detected in a drive during seek operation.

(4) FLT (Fault)
This bit indicates that errors relevant to disk access have been detected in the drive. Result parameter DST1 indicates what type of error has occurred. See (6) through (11) for DST bits indicating error status.

(5) WPRT (Write Protected)
This bit indicates that a selected drive is write protected.

(6) SERR1 (Status Error 1)

(7) SERR2 (Status Error 2)

(8) WERR1 (Write Error 1)

(9) WERR2 (Write Error 2)

(10) WERR3 (Write Error 3)

(11) SELER (Select Error)

(12) SAD1–32 (Sector Address)

(13) DTP1–32 (Drive Type)

EA (Error Address)
Reports the start address (16 bits) of a byte from where the burst error that is detected during CKE command execution exists. The high-order 8 bits are EA0, and the low-order 8 bits are EA1. As the HDC corrects up to 11 bits of burst error, the MPU corrects contiguous 3 bytes starting from a byte specified by EA. EA = $0000 indicates a start address of sector data.

EP (Error Pattern)
Reports EP0, EP1, and EP2 as the pattern required for error correction as a result of CKE command execution. The MPU exclusive-OR 3-byte data containing errors with EP0, EP1, and EP2.

FLAG (Flag)
Reports the same value as FLAG specified by command parameters.

LCA (Logical Cylinder Address)
Reports the same value as LCA specified by command parameters.

LHA (Logical Head Address)
Bit organization of LHA is the same as that of the command parameter LHA. In multiple track operation, LHA is incremented by one each time access to one track ends.

LSA (Logical Sector Address)
Bit organization of LSA is the same as that of the command parameter LSA. In multiple sector operation, LSA is incremented by one each time access to one sector ends.

PHA (Physical Head Address)
Bit organization of PHA is the same as that of the command parameter PHA. In multiple track operation, PHA is incremented by one each time access to one track ends.

PSA (Physical Sector Address)
Bit organization of PSA is the same as that of the command parameter PSA. In multiple sector operation, PSA is incremented by one each time access to one sector ends.

SCNT (Sector Count)
Bit organization of SCNT is the same as that of the command parameter SCNT. In multiple sector operation, SCNT is decremented by one each time access to one sector ends. When SCNT reaches "0", command execution normally terminates.

SSB (Sense Status Byte)
This is the area where 8-bit error code is set ($00 is set for normal termination). There are 25 error codes which notify what kind of error has occurred during the command execution (See Tables 11–14).

US (Unit Select)
Reports the same value as US specified by command parameters.

VUL (Valid Unit List)
VUL is a bit-mapped list which gives the address of a drive that is ready to accept a head positioning or a disk access command. Its bit organization is the same as that of CUL. This bit is set when seek operation in the drive is terminated, or when SPC command is executed. This bit is reset when seek operation starts, when drive error occurs, or when the bit in CUL corresponding to the drive is not set to "1".

Table 11 Error Codes Relevant to Host Interface

Mnemonic	Name	Error Code	Contents
ABT	Command Aborted	04	ABT command has been accepted.
IVC	Invalid Command	08	An invalid command has been accepted.
PER	Parameter Error	0C	The command parameter has not been stored in an appropriate area in PB.
NIN	Not Initialized	10	Head positioning, disk access, and drive check commands have been accepted, before SPC command is executed.
RTS	Rejected Test	14	The TST command is received after SPC command has been received.

Table 12 Error Codes Relevant to Drives

Mnemonic	Name	Error Code	Contents
NUS	No USELD	18	USELD signal for a selected drive has not been returned.
WFL	Write Fault	1C	WFLT signal (ST506 interface) or FLT signal (SMD interface) has been detected.
NRY	Not Ready	20	READY signal has been negated.

Table 13 Error Codes Relevant to Head Positioning Commands

Mnemonic	Name	Error Code	Contents
NSC	No SCP	24	SCP signal (ST506 interface) or the SKEND signal (SMD interface) has not been returned in a certain period.
ISE	In Seek	28	SEK, or a disk access command has been issued for a drive in seek operation.
INC	Invalid NCA	2C	NCA (Next Cylinder Address) greater than NC (number of cylinders) has been specified.
ISR	Invalid Step Rate	30	The highest-speed seek has been specified in the normal seek mode.
SKE	Seek Error	34	SEK or a disk access command has been issued to a drive which is in seek error state (SMD only).

Table 14 Error Codes Relevant to Disk Read/Write Commands

Mnemonic	Name	Error Code	Contents
OVR	Over Run	38	A transfer between the main memory and data buffers has not caught up with a transfer between a drive and data buffers.
IPH	Invalid PHA	3C	PHA (Physical Head Address) greater than NH (Number of Heads) has been specified.
DEE	DATA Field ECC Error	40	A data error has been detected by ECC (Error Correction Code).
DCE	DATA Field CRC Error	44	A CRC (Cyclic Redundancy Check Code) error has occurred in DATA area.
ECR	Error Corrected	48	An ECC error detected in DATA area has been automatically corrected.
DFE	DATA Field Fatal Error	4C	A fatal ECC error has occurred in DATA area.
NDA	No DATA AM	60	The address mark in DATA area has not been detected.
NHT	Not Hit	50	In CMPD command execution, data from the host and disk data have not coincided with each other.
ICE	ID Field CRC Error	54	A CRC error in ID area has been detected in RID command execution in SMD interface.
TOV	Time Over	58	ID has not been found in the period specified by TO (Time Over).
NIA	No ID AM	5C	The ID area that begins with improper address mark has been detected.
NWR	Not Writable	64	WD command has been issued to a drive where the write protect signal is asserted (SMD interface)

CONTROL SEQUENCE FOR ST506 TYPE DRIVE

DISK READ

The ID search timing for RD or WD command execution is shown in Figure 27. (a) is the timing where AM is found. SYNC signal is negated 4-bit period (on the basis of disk data) after CRC pattern of ID area is completed. After reading CRC, the HDC switches the clock in the satellite processor from RCLK to WCLK and then negates SYNC signal.

RCLK and WCLK clock signals are independent each other. To remove the hazard during switching, the switching signal and the clock signal must be synchronized. Therefore, SYNC is normally negated 4-bit period after reading CRC to switch the clock in the satellite processor from RCLK to WCLK.

RGATE signal is usually negated 4-bit period after SYNC signal is negated, and then asserted again one to two-byte period later to read SYNC area preceding DATA area. RGATE is asserted for 1-byte period when the AMEX bit is set to "1" during SPC command execution, and for 2-byte period when set to "0".

When AM is not found as shown in (b), the HDC searches for AM again by negating both SYNC and RGATE signals. RGATE signal is usually negated 4-bit period after SYNC signal is negated, and is negated for 2-byte period.

As the MFM is specified during SPC command execution, the frequency of clock signals synchronizing with disk data (such as RCLK, WCLK) is doubled compared to the data transfer rate. Therefore, "4-bit period" or "1-byte period" description is formally expressed as "8 WCLK cycles" or "16 WCLK cycles" respectively.

After reading DATA area and ECC or CRC area by RD command execution, RGATE and SYNC signals are negated in the same timing as they are negated after reading ID CRC area (see Figure 27 (a)).

DISK WRITE

The timing of WGATE signal for WD command execution is shown in Figure 28. The HDC negates RGATE signal after reading ID area. Then WGATE signal is asserted 1 or 2-byte period after RGATE is negated (2-byte when AMEX specified by SPC command is at "0", 1-byte when AMEX is at "1"). WGATE signal is negated immediately after PAD of DATA field ends.

The relation between IDX signal and WGATE signal during WFM command execution is shown in Figure 29. WGATE signal rises almost simultaneously with IDX signal (refer to electrical characteristics), and falls 3-byte or 4-byte period after IDX signal rises. The condition of EARLY and LATE signal generation is shown in Figure 8.

HEAD POSITIONING

The relation between DIR, STEP, and SEEK signals is shown in Figure 30. The unit is the number of CLK cycles (t_{cyc}).

When 8 MHz clock signal is supplied to CLK, STEP signal is output at least 33.8 μs after DIR signal becomes valid.

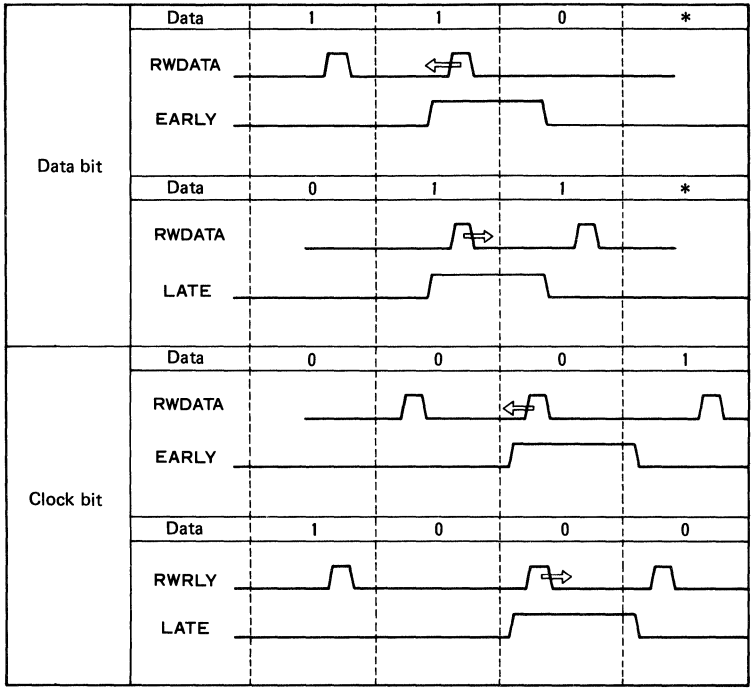


Figure 8 Write Precompensation

CONTROL SEQUENCE FOR SMD TYPE DRIVE

DRIVE SELECTION, STATUS CHECK, FAULT CLEAR

The HDC performs drive selection, status check, and Fault Clear, for all disk control command execution. Figure 35 shows the drive selection timing. The drive receives BUS_0/BUS_5 $-BUS_4/BUS_9$ from the HDC and latches them using UTAG signal. If the drive judges that its own drive number is specified, it returns USELD signal within 9 CLK after the detection of UTAG signal. Figure 36 shows the drive status check sequence. The HDC changes the direction of $BUS_0/BUS_5-BUS_4/BUS_9$ before reading the status. Then the HDC sets BUSL/$\overline{H}$ signal to high, therefore, the external circuit of the HDC can supply drive status signal to the HDC during this period. At this time, BUSL/$\overline{H}$ is in high, and lower 5 bits are input to the HDC.

The HDC resets FLT after reading the drive status which includes Fault, and the timing is shown in Figure 37. To set the high-order 5 bits of BUS outputs to low, the HDC sets $BUS_0/BUS_5-BUS_4/BUS_9$ to low, and asserts TAG3 signal with maintaining BUSL/$\overline{H}$ in low. In external circuits of the HDC, $BUS_0/BUS_5-BUS_4/BUS_9$ is latched by using TAG3 signal as a strobe signal. If BUSL/$\overline{H}$ is in low, external circuits must be used not to supply TAG3 signal of the HDC to the drive. Then, the HDC outputs the low-order 5-bit information to $BUS_0/BUS_5-BUS_4/BUS_9$, sets BUSL/$\overline{H}$ signal to high, and asserts TAG3 signal. The external circuits provide the drive with above mentioned 5-bit latch outputs, the low-order 5-bit outputs on $BUS_0/BUS_5-BUS_4/BUS_9$, and TAG3. In Fault Clear, BUSL/$\overline{H}$ signal is in high, and only BUS_4/BUS_9 is in high.

Head selection is performed by disk access commands. Figure 40 shows the head selection timing. Upper 5 bits are in low, and the head address is supplied from the low-order 5 bits of BUS. At this time, TAG2 signal is used as a strobe signal.

Further, in the execution of disk access command group, the HDC asserts TAG3 and generates RGATE or WGATE signal. Figures 41, 42 and 43 show the total sequence. When TAG3 is asserted, the high-order 5 bits of BUS output Strobe Early/Late and RTZ (it is not used for disk access). Then, the HDC outputs the low-order 5 bits. Servo offset is specified in figure 42. When TAG3 is asserted along with BUS_2/BUS_7 or BUS_3/BUS_8, servo offset is performed in the drive. Therefore, the head is moved and the HDC waits until SKEND signal is returned from the drive. Then, the HDC asserts BUS_1/BUS_6 and supplies RGATE signal to the drive to perform the read operation.

Figure 43 shows assert/negate timing of RGATE and WGATE signals which correspond to the disk format. During disk access command or ID read command execution, RGATE signal is

asserted after a time period corresponding to byte count of disk data has elapsed since IDX or SEC signal is detected. After reading CRC, the HDC itself switches the clock to WCLK signal, then negates RGATE signal with a typical delay time equivalent to 8 bits of disk data.

To read the data field, the HDC asserts RGATE again with a dwell time of 1–2 bytes period. RGATE is negated for 1-byte period when AMEX bit is set to "1" during SPC command execution, and 2-byte period when AMEX bit is set to "0". The HDC negates RGATE signal 8-bit period after reading CRC or ECC in data field.

To write the DATA field, the HDC reads ID area and asserts WGATE signal 1–2 bytes period after RGATE signal is negated. WGATE signal is to be negated when DATA PAD ends. During WFM command execution, WGATE signal rises in the same timing as IDX signal, and is negated 3–4 bytes period after IDX or SEC signal is detected.

Figure 38 shows the execution timing of RCLB command. RTZ instruction is supplied to the drive through BUS_1/BUS_6 and TAG3. Figure 39 shows the execution timing of SEK command. 10-bit cylinder address is output through $BUS_0/BUS_5-BUS_4/BUS_9$, 5 bits at a time. Strobe signal is TAG1 at this time.

Figures 44, 45, 46 and 47 shows the execution timing of CKV command. The HDC reads 8-bit drive status through $BUS_0/BUS_5-BUS_4/BUS_9$, 3 bits first and then 5 bits. Then the HDC reads status four times by switching TAG2 and TAG5 signals. Switching order is: [TAG2 = 0, TAG5 = 1], [TAG2 = 0, TAG5 = 1], [TAG2 = 1, TAG5 = 0], [TAG2 = 1, TAG5 = 1].

COMMON CONTROL

The control which is common to both ST506 and SMD interfaces is described in this section.

AUTOMATIC CORRECTION

In SPC command execution, the HDC operates in automatic correction mode if the host sets both ECD and ACOR bits in OM0 to "1". If a sector with correctable errors is detected, the erroneous data is corrected in data buffers. Automatic correction is normally performed only when the sector length is 256 bytes. Specification of the automatic correction mode is prohibited when the sector length is longer than 512 bytes because it causes the erroneous operation of the HDC.

If DTM (Data Transfer Mode) bit in OM0 is set to "1" as well as ECD and ACOR bits during SPC command execution, the HDC transfers the corrected data to the main memory in DMA mode after the automatic correction. Then, the command execution abnormally terminates. When DTM = 0, the command execution abnormally terminates after the automatic correction and data transfer is not performed. If the HDC finds the data uncorrectable, the command execution abnormally terminates without data transfer regardless of the state of DTM bit.

CORRECTION BY HOST

The host corrects erroneous data detected during RD command execution when it sets ECD and ACOR bits in OM0 to "1" and "0" respectively. When ECD bit is set to "1", the host corrects erroneous data detected during RED command execution if necessary, regardless of the status of ACOR bit. The command execution abnormally terminates when erroneous data is detected during any command execution. Then $40 is set to SSB when an error is correctable, $4C when not correctable.

When DTM = 1, the HDC sends 1-sector data including an error during RD or RED command execution and then abnormally terminates the command execution. After confirming that $40 is set to SSB, the host issues CKE command to the HDC.

When DTM = 0, the HDC abnormally terminates the command execution after 1-sector data including an error is stored in the data buffer during RD or RED command execution. After confirming that $40 is set to SSB, the host issues BTM command to the HDC after DMAC's initialization, or, issues OPBR command and reads data buffers using move and load instructions and then stores buffer data to the main memory. Then, the host issues CKE command to the HDC.

Receiving CKE command, the HDC calculates an error address (EA) and an error pattern (EP), and then sends result parameters to the host. The erroneous data exists in three contiguous bytes of the corresponding sector in main memory. EA indicates start address of this 3-byte area ($0000 indicates a start address of sector data). The host exclusive-OR the 3-byte area and EP to correct erroneous data.

The host judges CKE command execution end from status change of BSY bit from "1" to "0". When SSB is $4C, CKE command issue is prohibited as it causes the erroneous operation of the HDC. Even if errors are reported to be correctable (SSB = $40) during RD or RED command execution and the host issues CKE command, these errors may turn out to be not correctable after CKE command execution.

DMA DATA TRANSFER

In DMA data transfer, the HDC selects one of two modes: Burst mode and Cycle Steal mode. DMA transfer mode is specified by BRST (burst) bit which is a command parameter of SPC command.

In Burst mode (BRST = 1), the HDC maintains $\overline{DREQ}$ signal at low level until data transfer is terminated. $\overline{DREQ}$ signal is negated when $\overline{DONE}$ signal is input synchronously with $\overline{DACK}$ signal, or when DMA transfer of data in 256-byte internal data buffer is finished.

In Cycle Steal mode (BRST = 0), the HDC asserts $\overline{DREQ}$ signal until $\overline{DACK}$ signal is asserted. The HDC negates $\overline{DREQ}$ signal when $\overline{DACK}$ signal assertion is detected. $\overline{DREQ}$ signal will be reasserted if $\overline{DACK}$ is negated and the HDC has the transfer request. The DMA transfer conditions of Cycle Steal mode are the same as those of Burst mode.

DATA TRANSFER IN HOST INTERFACE

DMA Data Transfer in Disk Access

DMA data transfer mode, either Burst mode or Cycle Steal mode, is selected by BRST bit specified by SPC command. Figure 9 shows DMA data transfer sequence during RD and RED command execution. For 256-byte sector, (a) shows the case that the host computer reads the disk data from data buffers (DBUF0 and DBUF1) by DMA at a high speed. The capacity of two data buffers is 256 bytes for each.

If data buffers are not provided, most of high-speed host bus is occupied by transferring drive data during low-speed reading of drive data.

Internal data buffers can separate high-speed host bus timing and low-speed drive data timing, which effectively shorten drive data transfer time in host bus. Therefore, host system throughput is notably improved. The data transfer from data buffers to the main memory is performed only when the HDC is reading ID area or DATA area of the disk, but is exceptional when data in the last sector is transferred to the main memory during the multiple sector operation.

Figure 9 (b) shows the low-speed DMA transfer of the host in 256-byte sector organization. According to the figure, DBUF0 receives data of the sector 1, and DBUF1 receives that of the sector i+1. While DBUF1 is receiving the data of sector i+1, the data transfer from DBUF0 to the main memory cannot be finished because the host cannot operate promptly. Therefore, being unable to receive the data of i+2, DBUF0 waits until the disk makes one rotation (all data of DBUF0 is sent to the main manner, no data overrun occurs even if operation speed of the host is slow. Therefore, an interleave format is not required.

Figure 9 (c) indicates the sequence in 512-byte sector organization. Capacity of buffers is 256 bytes for each, and each buffer stores disk data and transfers the data to the main memory alternately. Therefore, buffers effectively operates in toggle fashion even if sector length exceeds 256 bytes, and host system throughput is improved. If operation speed of the host is too slow, data overrun may occur because data buffer cannot be emptied to receive disk data. The data transfer from data buffer to main memory must be terminated while the HDC is accessing disk data in ID or DATA area.

If the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during RD or RED command execution, the HDC immediately terminates DMA data transfer. Disk reading operation continues until the HDC finishes reading the sector which has been read when $\overline{\text{DONE}}$ signal is applied.

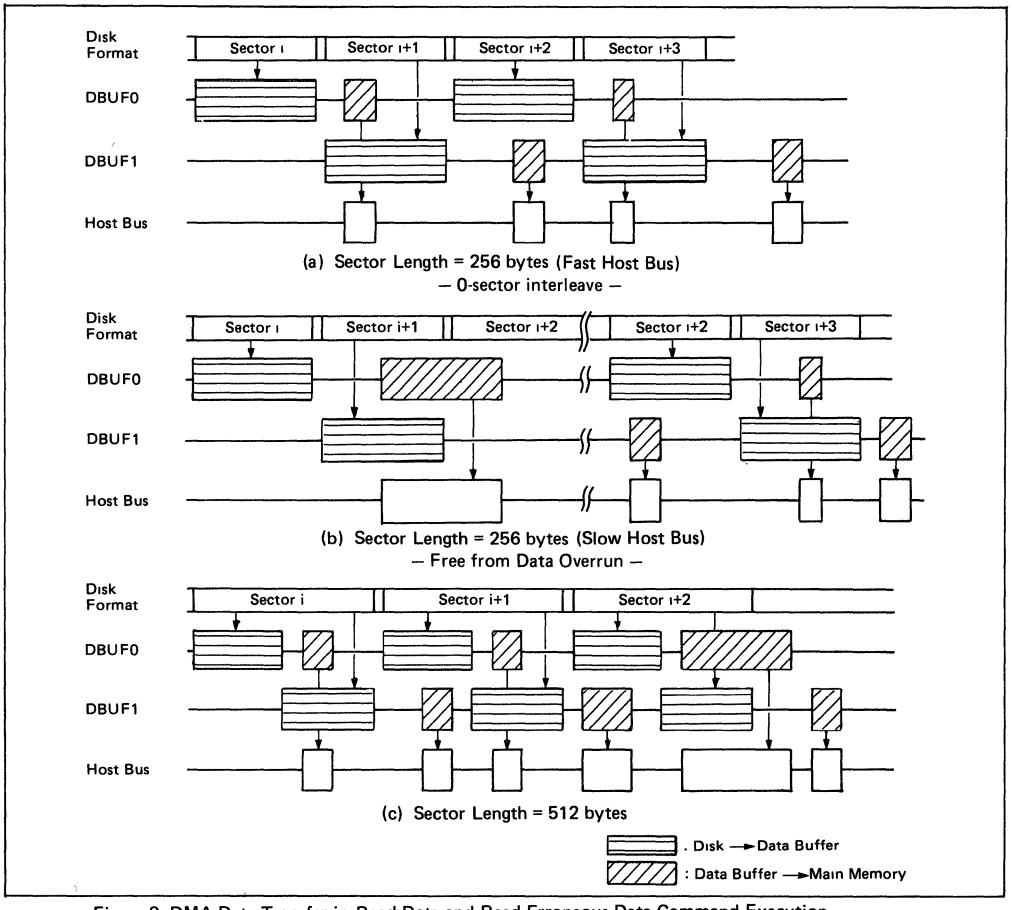


Figure 9 DMA Data Transfer in Read Data and Read Erroneous Data Command Execution

DMA data transfer during WD and CMPD command execution is shown in Figure 10. This figure differs from Figure 9 (a) in data transfer direction, DMA transfer order, and access method of first and last sectors. In Figure 10, the host is fast and sector length is 256 bytes. When the host is slow and sector length is 256 bytes, or when sector length is 512 bytes or more, data transfer sequence is the same as Figure 9.

When the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during WD command execution, the HDC immediately terminates DMA data transfer. Then all data stored in DBUF0 and DBUF1 are written to DATA area of the sector. If there is any room in DATA area after writing buffer data, the old data in buffers is written to DATA area. After DATA area is filled with buffer data, command execution terminates.

When the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during CMPD command execution, the HDC immediately terminates DMA data transfer. However, the data of the sector which has been accessed when $\overline{\text{DONE}}$ is received, is used for comparison with disk data, further, the reading operation continues until reading of the sector is finished. Therefore, $50 (Not Hit) is set to SSB in most cases when reading of the sector is finished, and then the command execution abnormally terminates.

DMA data transfer during RID or FID command execution is performed as follows (see Figure 11). When DBUF0 is filled with ID information, DBUF1 receives the succeeding ID information. DMA data transfer is not performed unless all the ID information is stored in data buffer. After DBUF0 with/without DBUF1 finishes accepting ID information from specified number of sectors, data are sent to the main memory by DMA. DMA data transfer continues until 512-byte transfer is finished.

DMA data transfer can be stopped when the DMAC sends $\overline{\text{DONE}}$ to the HDC. Therefore, the host can store only the necessary ID information to the main memory by setting the number of ID areas to be read, to the DMAC.

DMA data transfer during WFM command execution is shown in Figure 12. The HDC starts formatting operation when both DBUF1 and DBUF1 are filled with ID information from the host. The HDC writes data buffer data to the ID area of a specified sector, and writes fixed pattern to other area such as DATA area. When DBUF0 becomes empty during formatting operation, DBUF1 becomes the source in turn. When the DMAC issues $\overline{\text{DONE}}$ signal to the HDC, the HDC stops data transfer to data buffers and starts formatting. Therefore, the host can write only the necessary ID information to data buffer by setting data of how many ID areas to be transferred, to the DMAC.

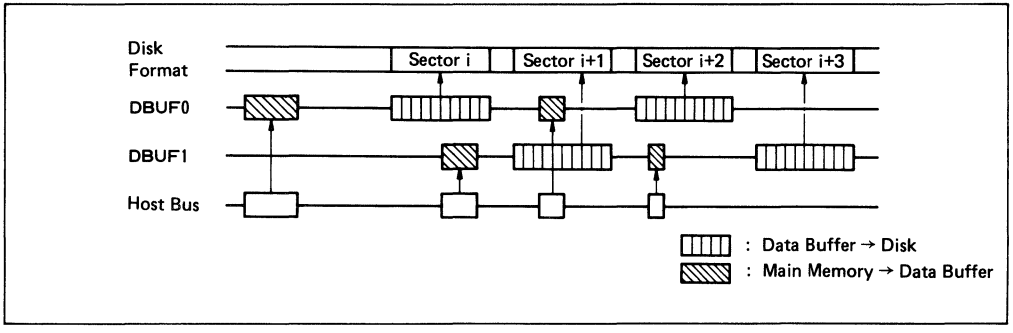


Figure 10 DMA Data Transfer in Write Data, Compare Data Command Execution (Sector Length = 256 bytes)

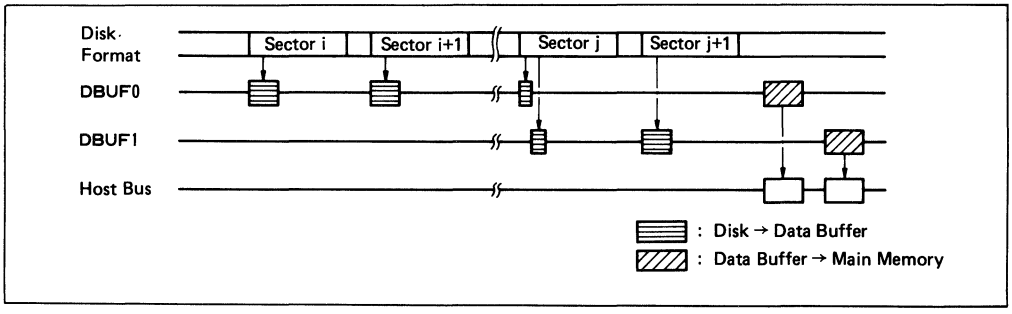


Figure 11 DMA Transfer in Read ID, Find ID Command Execution

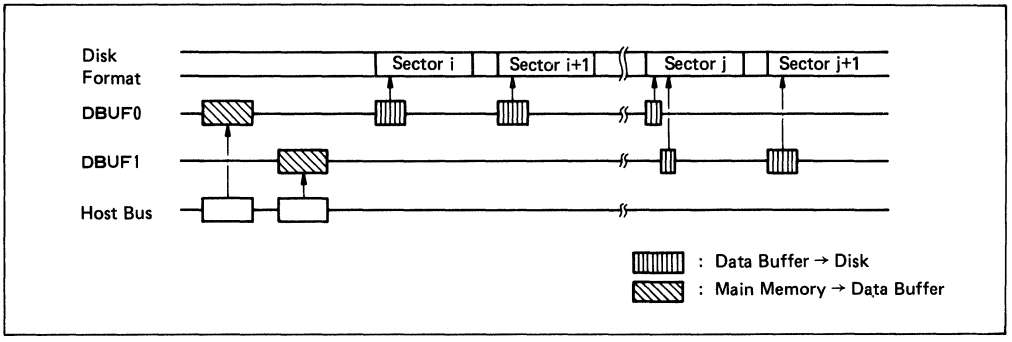


Figure 12 DMA Data Transfer in Write Format Command Execution

DMA Data Transfer by Data Transfer Commands

Accepting data transfer commands, the HDC can perform DMA data transfer between the main memory and data buffers without disk access. Either Burst mode or Cycle Steal mode is selected by the BRST bit of SPC command parameter. There are two commands available, BTM and MTB.

Selection of either DBUF0 or DBUF1, and access start address of each buffer (address 0 to 250 are specifiable), are specified by POFF (Pointer Offset). POFF is set to the data buffer pointer by command execution.

Data buffer pointer is incremented each time the DMAC accesses data buffer (+2 for 16-bit bus mode, +1 for 8-bit bus mode). Data buffer data is not guaranteed if data buffer pointer exceeds address 255. Receiving $\overline{\text{DONE}}$ signal from the DMAC, the command execution immediately terminates normally, and the CED bit in STR is set to "1". Receiving above data transfer commands, the HDC requests transfer by issuing $\overline{\text{DREQ}}$ signal to the DMAC within 150 CLK cycles.

Data Buffer Access by PIO

The host MPU can access data buffers by move or load/store instruction (Programmed I/O). In this case, the host issues OPBR or OPBW command prior to PIO access. Receiving these commands, the HDC sets BSY bit in STR to "1". Then the HDC sets data buffer pointer, sets BSY bit to "0", and terminates the command execution. It takes up to 100 CLK cycles from the command reception to BSY bit clear. Before issuing above commands, POFF must be specified by command parameters. POFF specifies either DBUF0 or DBUF1 to be accessed, and access start address (specifiable range is address 0 to 255).

The host issues move instruction to the HDC after confirming that BSY = 0. Data buffer pointer is incremented each time the HDC receives move instruction (+2 for 16-bit bus mode, +1 for 8-bit bus mode). If the pointer exceeds address 255 during data transfer in PIO mode, the buffer data is not guaranteed. The host must issue RCAL command to close the buffer.

Notes on Data Buffer

Item \ Sector Length (Byte)	256	512	1024	2048	4096
High Speed DMA (0-sector interleave)	○	○	○	○	○
PIO	○	○			
Low Speed DMA (free from overrun)	○				
Automatic Correction	○				

○ : Provided

Others

Recall command – After the host issues RCAL command, the HDC finishes the operation within up to 40 CLK cycles and clears all bits in STR.

Test command – After the host issues TST command, the HDC makes drive output pins floated within 60 CLK cycles. To cancel this state, $\overline{\text{RES}}$ signal is to be externally supplied.

Specify command – After the host issues SPC command, the HDC makes the drive interface pins fitted for either ST506 or SMD, and clears BSY bit within 250 cycles.

Abort command – After the host issues ABT command, the HDC negates all drive output pins within up to 180 CLK cycles, terminates all operation within 300 CLK cycles, and clears BSY bit. Receiving this command, the HDC clears all internal flip-flops, but the value of the control register which has been set by SPC command still remains.

Reset – Reset is not a command, but after receiving $\overline{\text{RES}}$ signal, the HDC terminates initialization within up to 150 CLK cycles and clears BSY bit.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *1	−0.3 − +7.0	V
Input Voltage	V_{in} *1	−0.3 − V_{CC} + 0.3	V
Output Current per Pin	$\|Io\|$ *2	5	mA
Total Output Current	$\|\Sigma Io\|$ *3	80	mA
Operating Temperature	T_{opr}	0 − +70	°C
Storage Temperature	T_{stg}	−55 − +150	°C

*1 This value is in reference to V_{ss} = 0V.

*2 The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.

*3 The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.

(Note) Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} *	4.75	5.0	5.25	V
Input Low Level Voltage	V_{IL} *	0	–	0.8	V
Input High Level Voltage	V_{IH} *	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

* This value is in reference to V_{SS} = 0V.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = 0 – 70°C, unless otherwise noted)

Item			Symbol	6 MHz Version HD63463-6 min	6 MHz Version HD63463-6 max	8 MHz Version HD63463-8 min	8 MHz Version HD63463-8 max	Unit	Test Condition
Input High Level Voltage	All Inputs		V_{IH}	2.2	V_{CC}	2.2	V_{CC}	V	
Input Low Level Voltage	All Inputs		V_{IL}	–0.3	0.8	–0.3	0.8	V	
Input Leak Current	R/$\overline{W}$, $\overline{CS}$, RS, $\overline{RES}$ $\overline{DACK}$, CLK $\overline{DONE}$		I_{IN}	–2.5	2.5	–2.5	2.5	μA	V_{in} = 0–V_{CC}
	ST506	SMD							
	IDX/ TRKO	IDX							
	SCP	SEC							
	USELD	USELD							
	WCLK	WCLK							
	RCLK	RCLK							
Three State (Off State) Input Current	RWDATA	RWDATA	I_{TSI}	–10	10	–10	10	μA	V_{in} = 0.4–V_{CC}
	SYNC*1	SKEND							
	WGATE*2	BUS_0/BUS_5							
	EARLY/ RGATE*1	BUS_1/BUS_6							
	LATE/ STEP*1	BUS_2/BUS_7							
	WFLT	BUS_3/BUS_8							
	LCT/DIR*1	BUS_4/BUS_9							
	READY	BUSL/$\overline{H}$*1							
	$D_0 – D_{15}$								
Output High Level Voltage	All Outputs		V_{OH}	V_{CC}–1.0	–	V_{CC}–1.0	–	V	I_{OH} = –400 μA
Output Low Level Voltage			V_{OL}	–	0.5	–	0.5	V	I_{OL} = 2.2 mA
Output Leak Current (Off State)	$\overline{IRQ}$		I_{LOH}	–	10	–	10	μA	V_{OH} = V_{CC}

(to be continued)

*1 These signals are defined when HDC is in Test mode or when drive interface is not specified. Otherwise, these signals are not defined since these are switched to output signals.

*2 This signal is defined when HDC is in test mode, otherwise this signal is not defined.

Item			Symbol	6 MHz Version HD63463-6 min	6 MHz Version HD63463-6 max	8 MHz Version HD63463-8 min	8 MHz Version HD63463-8 max	Unit	Test Condition
Signal Capacity	$\overline{RES}$ $\overline{DONE}$ RS R/$\overline{W}$ $\overline{CS}$ $\overline{DACK}$ $D_0 - D_{15}$ CLK $\overline{IRQ}$		C_{pin}	–	17	–	17	pF	V_{in} = 0 V Ta = 25°C f = 1.0 MHz
	ST506	SMD							
	RWDATA	RWDATA							
	WCLK	WCLK							
	RCLK	RCLK							
	–	SKEND							
	–	BUS_0/BUS_5							
	–	BUS_1/BUS_6							
	–	BUS_2/BUS_7							
	WFLT	BUS_3/BUS_8							
	–	BUS_4/BUS_9							
	IDX/TRK0	IDX							
	SCP	SEC							
	USELD	USELD							
	READY	–							
Current Consumption			I_{CC}	–	65	–	80	mA	• Data bus in read/write operation • Command execution in progress

AC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = 0 – 70°C, unless otherwise noted.)
Clock Timing

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
1	Clock Cycle time	tCYC	167	500	125	500	ns	See Figure 15
2	Clock Low Level Pulse Width	tPWCL	75	250	55	250	ns	
3	Clock High Level Pulse Width	tPWCH	75	250	55	250	ns	
4	Clock Rise Time	tCR	—	10	—	10	ns	
5	Clock Fall Time	tCF	—	10	—	10	ns	
6	Write Clock Cycle time	tWCYC	62.5	250	50	250	ns	
7	Write Clock Low Level Pulse Width	tPWCL	25	115	20	115	ns	
8	Write Clock High Level Pulse Width	tWCH	25	115	20	115	ns	
9	Write Clock Rise Time	tWCR	—	10	—	10	ns	
10	Write Clock Fall Time	tWCF	—	10	—	10	ns	
11	Read Clock Cycle Time	tRCYC	62.5	250	50	250	ns	
12	Read Clock Low Level Pulse Width	tRCL	25	115	20	115	ns	
13	Read Clock High Level Pulse Width	tRCH	25	115	20	115	ns	
14	Read Clock Rise Time	tRCR	—	10	—	10	ns	
15	Read Clock Fall Time	tRCF	—	10	—	10	ns	

Data Bus Configuration and $\overline{IRQ}$

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
21	$\overline{RES}$ Input Pulse Width	tRES	10	—	10	—	tcyc	See Figure 16
22	$\overline{DACK}$ Setup Time for $\overline{RES}$	tDACKSR	100	—	100	—	ns	
23	$\overline{DACK}$ Hold Time For $\overline{RES}$	tDACKHR	0	80	0	50	ns	
24	$\overline{IRQ}$ Delay Time1	tIRD1	—	200	—	150	ns	See Figure 17
26	$\overline{RES}$ Rise Time	tRESR	—	10	—	10	μs	See Figure 16

MPU Interface

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
31	R/$\overline{W}$ Setup Time for $\overline{CS}$ Assert	tRWS	60	—	50	—	ns	See Figures 18 and 19
32	R/$\overline{W}$ Hold Time	tRWH	0	—	0	—	ns	
33	RS Setup Time for $\overline{CS}$ Assert	tRSS	60	—	50	—	ns	
34	RS Hold Time	tRSH	0	—	0	—	ns	
35	$\overline{CS}$ Setup Time	tCSS	40	—	40	—	ns	
36	$\overline{CS}$ Negate Hold Time	tCSNH	40	—	40	—	ns	
37	$\overline{CS}$ Negate Width	tCSNW	80	—	80	—	ns	
38	Write Data Setup Time	tWDS	60	—	40	—	ns	
39	Write Data Hold Time	tWDH	10	—	10	—	ns	
40	$\overline{DTACK}$ Delay Time	tDTKZL	—	85	—	80	ns	
41	$\overline{DTACK}$ Hold Time	tDTKLH	—	60	—	60	ns	
43	Data Bus 3 State Recovery Time	tDBR	0	—	0	—	ns	
44	Read Data Access Time	tRDAC	—	80	—	70	ns	
45	Read Data Hold Time	tRDH	10	—	10	—	ns	
46	$\overline{CS}$ Fall Time	tCSF	—	1	—	1	tcyc	
47	$\overline{CS}$ Rise Time	tCSR	—	1	—	1	tcyc	

DMA Interface

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
50	$\overline{\text{DREQ}}$ Assert Delay Time 1	tDRAD1	—	80	—	80	ns	See Figures 20 and 21
51	$\overline{\text{DREQ}}$ Negate Delay Time 1 (Cycle Steal Mode)	tDRND1	—	80	—	80	ns	
52	$\overline{\text{DREQ}}$ Assert Delay Time 2 (Cycle Steal Mode)	tDRAD2	—	80	—	80	ns	
53	$\overline{\text{DREQ}}$ Negate Delay Time 2	tDRND2	—	80	—	80	ns	
54	$\overline{\text{DREQ}}$ Negate Delay Time 3 ($\overline{\text{DONE}}$ Assert)	tDRND3	—	80	—	80	ns	
55	DMA R/$\overline{\text{W}}$ Setup Time	tDRWS	60	—	50	—	ns	
56	DMA R/$\overline{\text{W}}$ Hold Time	tDRWH	0	—	0	—	ns	
57	$\overline{\text{DACK}}$ Setup Time	tDACKS	40	—	40	—	ns	
58	$\overline{\text{DACK}}$ Negate Hold Time	tDACKHN	40	—	40	—	ns	
59	$\overline{\text{DACK}}$ Negate Width	tDAKNW	80	—	80	—	ns	
60	DMA Write Data Setup Time	tDWDS	60	—	40	—	ns	
61	DMA Write Data Hold Time	tDWDH	10	—	10	—	ns	
62	DMA $\overline{\text{DTACK}}$ Delay Time	tDDTZL	—	85	—	80	ns	
63	DMA $\overline{\text{DTACK}}$ Hold Time	tDDTLH	—	60	—	60	ns	

(to be continued)

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
65	$\overline{\text{DONE}}$ Input Pulse Width	tPWDN	1.5	—	1.5		tcyc	See Figures 20 and 21
66	DMA Data Bus 3 State Recovery Time	tDDBR	0	—	0	—	ns	
67	DMA Read Data Access Time	tDRDAC	—	80	—	70	ns	
68	DMA Read Data Hold Time	tDRDH	10	—	10	—	ns	
69	$\overline{\text{DACK}}$ Fall Time	tDACKF	—	1	—	1	tcyc	
70	$\overline{\text{DACK}}$ Rise Time	tDACKR	—	1	—	1	tcyc	

ST506 Interface ce

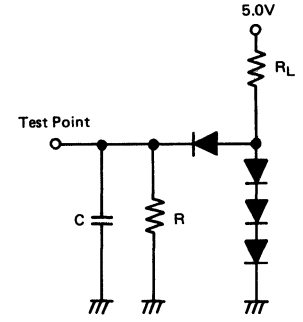
No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
110	USELD Setup Time (for USEL)	tUSLDS	—	5	—	5	tcyc	See Figure 22
111	WGATE Delay Time for Index	tWGTIDX	—	150	—	100	ns	See Figure 23
112	WFLT Pulse Width	tWFLT	2	—	2	—	tcyc	
113	Index Pulse Width	tIDXW	8tcyc 24twcyc	— —	8tcyc 24twcyc	— —	—	(Note 1) See Figure 23
114	WGATE Delay Time	tWGTD	—	130	—	125	ns	See Figure 24
116	Write Data Delay Time	tWDD	—	130	—	125	ns	
118	LATE/EARLY Delay Time	tELD	—	130	—	125	ns	
120	LATE/EARLY Setup Time (for Write Data)	tWDS	0	—	0	—	ns	
121	RGATE Delay Time	tRGTD	—	130	—	125	ns	See Figure 25
123	SYNC Delay Time	tSYND	—	130	—	125	ns	
125	Read Data Setup Time	tRDS	20	—	15	—	ns	
126	Read Data Hold Time	tRDH	20	—	15	—	ns	
127	USELD-DIR Time	tUS-DIR	70	—	70	—	tcyc	See Figure 26
128	STEP-USEL Time	tSTPUS	80	—	80	—	tcyc	
129	DIR-STEP Time	tDIRSTP	270	—	270	—	tcyc	
130	STP-DIR Time	tSTPDIR	80	—	80	—	tcyc	
131	SEEK-USEL Time	tSEKUS	1	—	1	—	tcyc	
132	SCP Wait Time	tSCP	—	1.0×10^7	—	1.0×10^7	tcyc	

(Note 1) The index pulse width must satisfy min 8 tcyc and min 24 twcyc.

SMD Interface

No.	Item	Symbol	6MHz Version HD63463-6		8MHz Version HD63463-8		Unit	Test Condition
			min	max	min	max		
150	Index Pulse Width	tIDXW	8tcyc 12twcyc	50tcyc	8tcyc 12twcyc	50tcyc	—	(Note 2) See Figure 32
151	USELD Setup Time	tUSLDS	—	7	—	7	tcyc	See Figure 31
152	Sector Pulse Width	tPWSET	8tcyc 12twcyc	50tcyc	8tcyc 12twcyc	50tcyc	—	(Note 2) See Figure 32
153	WGATE Delay Time for SEC/IDX	tWGTSEC	—	150	—	125	ns	See Figure 32
156	REGATE Delay Time	tRGTD	—	130	—	125	ns	See Figure 33
158	Read Data Setup Time	tRDS	20	—	15	—	ns	
159	Read Data Hold Time	tRDH	20	—	15	—	ns	
165	WGATE Delay Time	tWGTD	—	130	—	125	ns	See Figure 34
169	Write Data Delay Time	tWDD	—	130	—	125	ns	

(Note 2) The index sector pulse width must satisfy min 8 tcyc and min 12 twcyc.



Signal		Load Condition
$D_0 - D_{15}$ $\overline{DTACK}$ $\overline{DREQ}$ RWDATA		RL = 1.8 kΩ
ST506	SMD	C = 40 pF
SYNC	–	
WGATE	BUS_0/BUS_5	R = 10 kΩ
EARLY/ RGATE	BUS_1/BUS_6	
LATE/ STEP	BUS_2/BUS_7	All diodes are
–	BUS_3/BUS_8	1S2074 Ⓗ's or
LCT/DIR	BUS_4/BUS_9	the equivalent.
USEL0	TAG1	
USEL1	TAG2	
HSEL0	TAG3	
HSEL1	UTAG	
HSEL2	TAG5	
SEEK	BUSR/$\overline{W}$	
–	BUSL/$\overline{H}$	

Figure 13 Test Load Circuit A

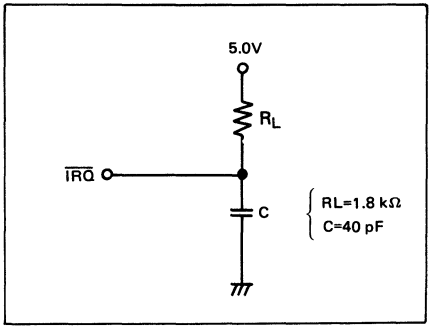


Figure 14 Test Load Circuit B

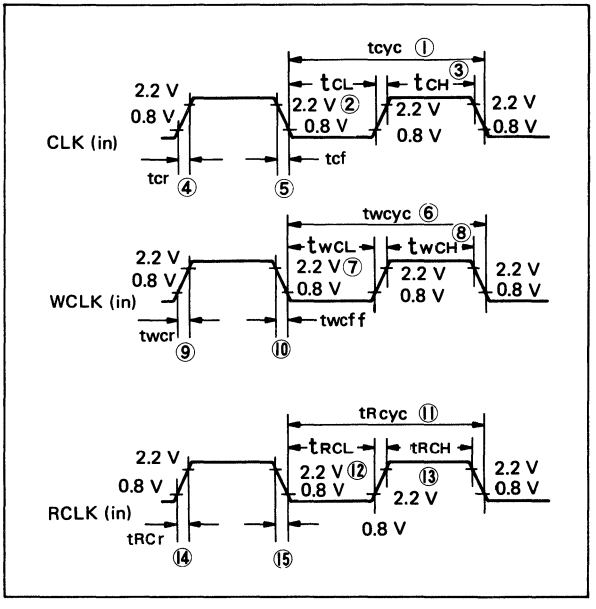


Figure 15 CLOCK

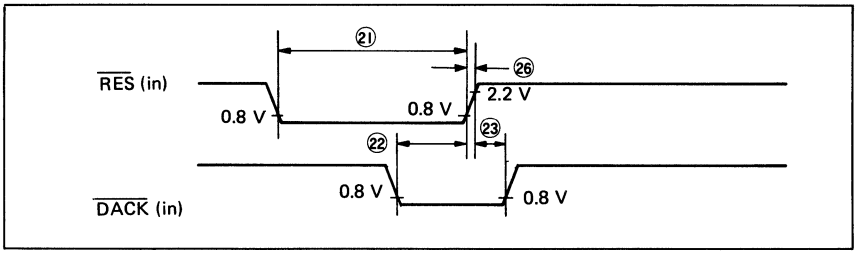


Figure 16 RES – DACK Input Timing (Data Bus Width Selection)

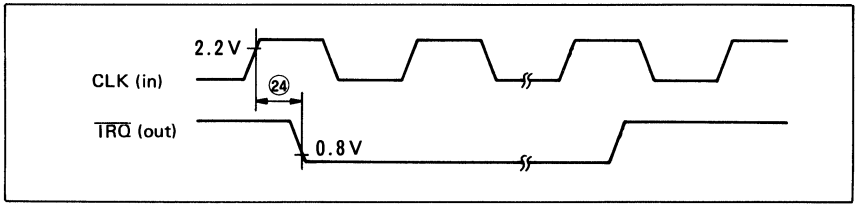
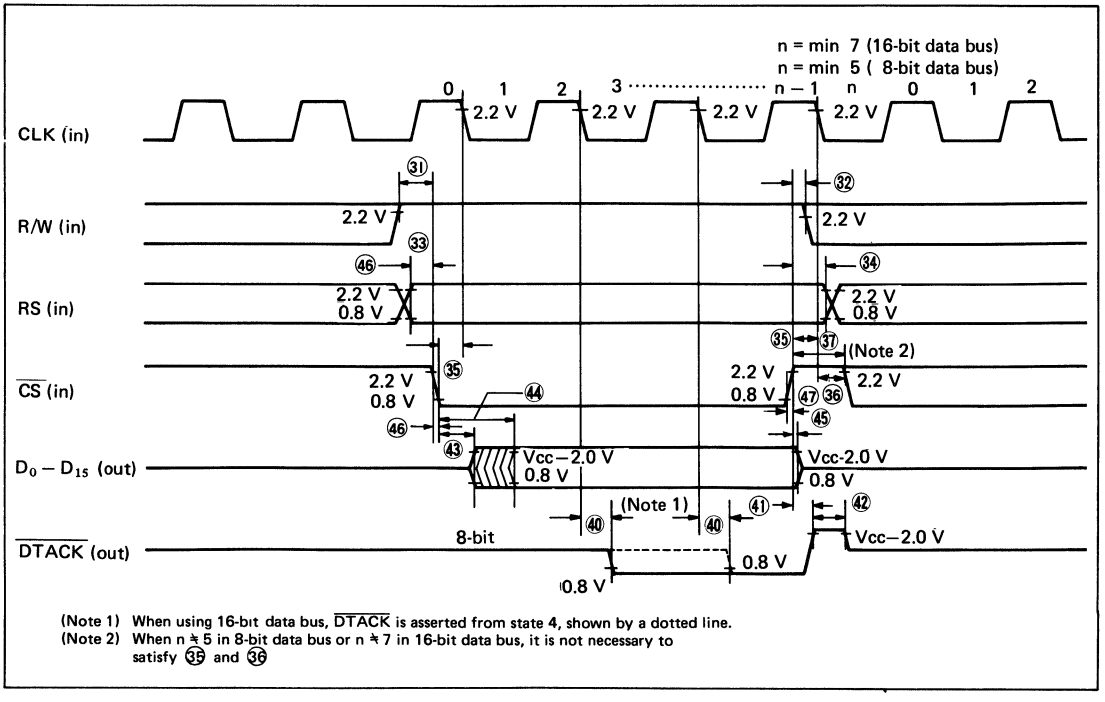


Figure 17 IRQ Output Timing



(Note 1) When using 16-bit data bus, DTACK is asserted from state 4, shown by a dotted line.
(Note 2) When n ≠ 5 in 8-bit data bus or n ≠ 7 in 16-bit data bus, it is not necessary to satisfy 35 and 36

Figure 18 MPU Read Cycle
HDC → MPU

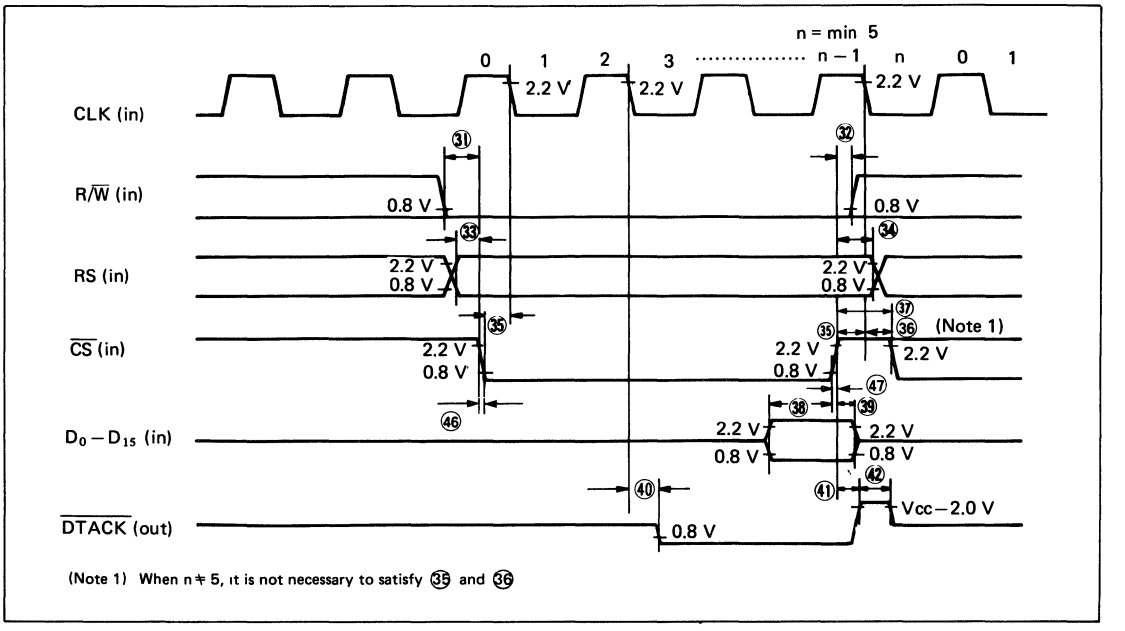
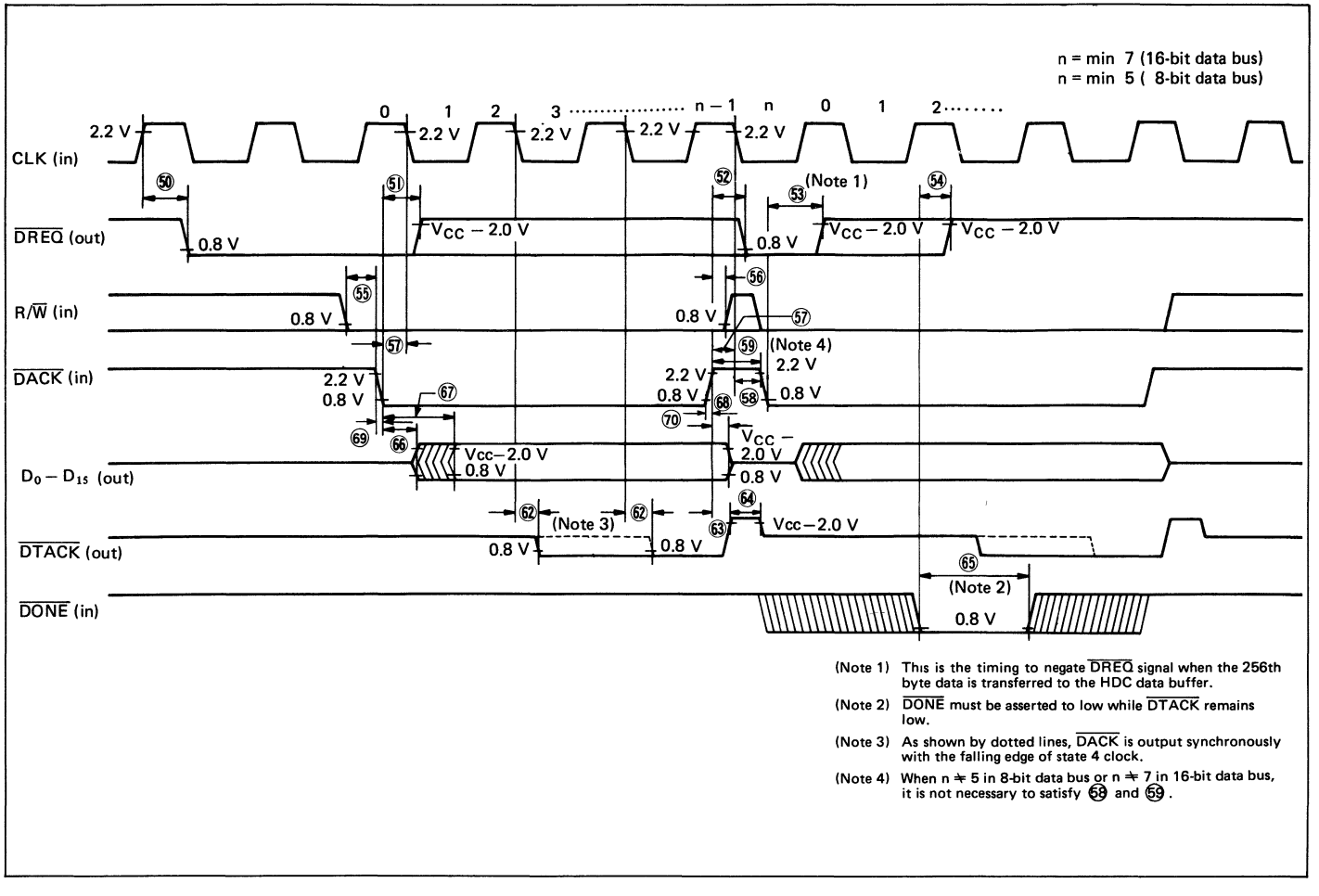


Figure 19 MPU Write Cycle
MPU → HDC
(8 or 16-bit data bus)



(Note 1) This is the timing to negate $\overline{\text{DREQ}}$ signal when the 256th byte data is transferred to the HDC data buffer.

(Note 2) $\overline{\text{DONE}}$ must be asserted to low while $\overline{\text{DTACK}}$ remains low.

(Note 3) As shown by dotted lines, $\overline{\text{DACK}}$ is output synchronously with the falling edge of state 4 clock.

(Note 4) When n ≠ 5 in 8-bit data bus or n ≠ 7 in 16-bit data bus, it is not necessary to satisfy ⑱ and ⑲.

Figure 20 DMA Read Cycle
HDC → Memory

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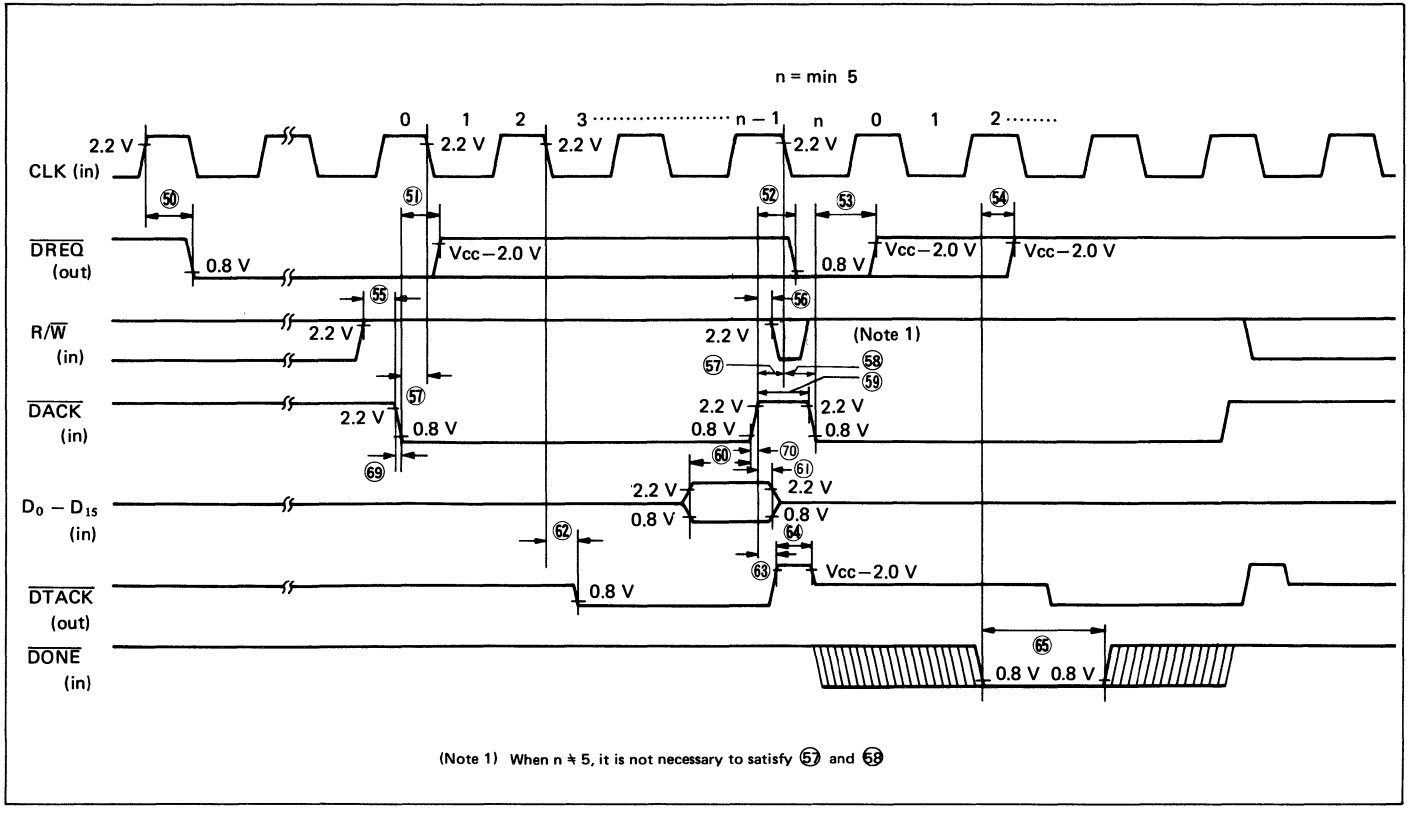


(Note 1) When n ≠ 5, it is not necessary to satisfy 57 and 58

Figure 21 DMA Write Cycle
Memory → HDC

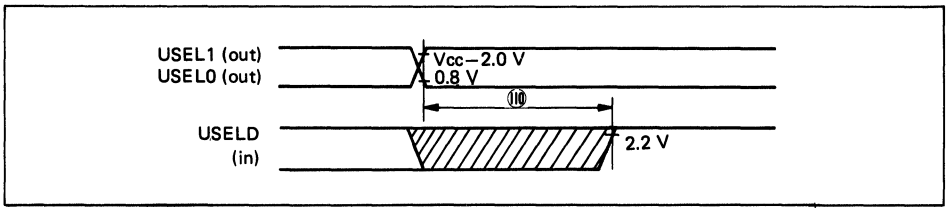
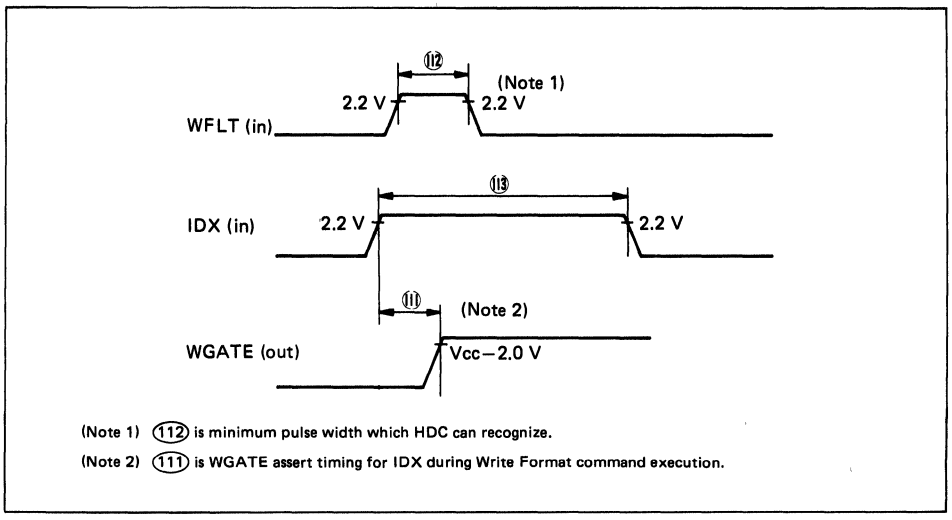


Figure 22 USEL, USELD Timing (ST506)



(Note 1) (112) is minimum pulse width which HDC can recognize.

(Note 2) (111) is WGATE assert timing for IDX during Write Format command execution.

Figure 23 WFLT, IDX, WGATE Timing (ST506)

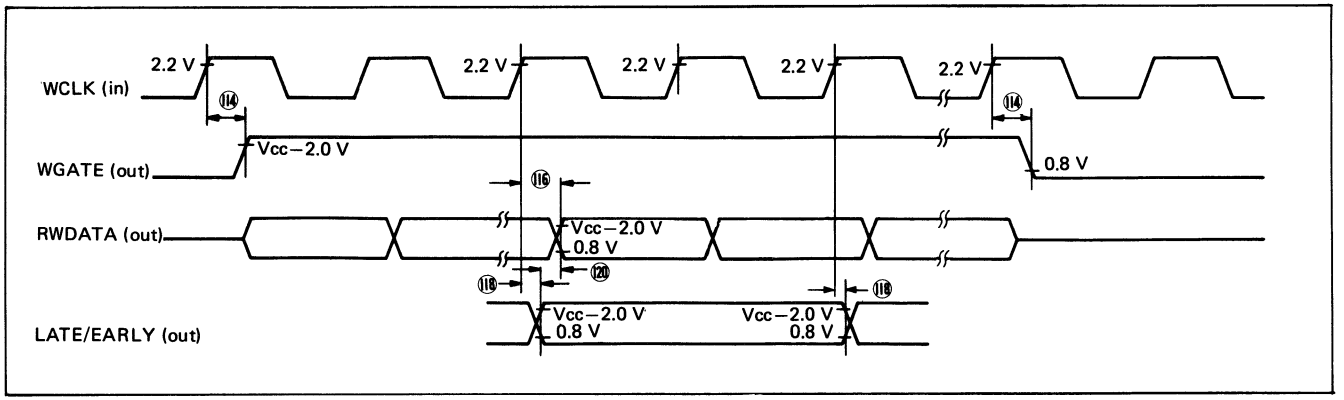


Figure 24 Write Operation (ST506)

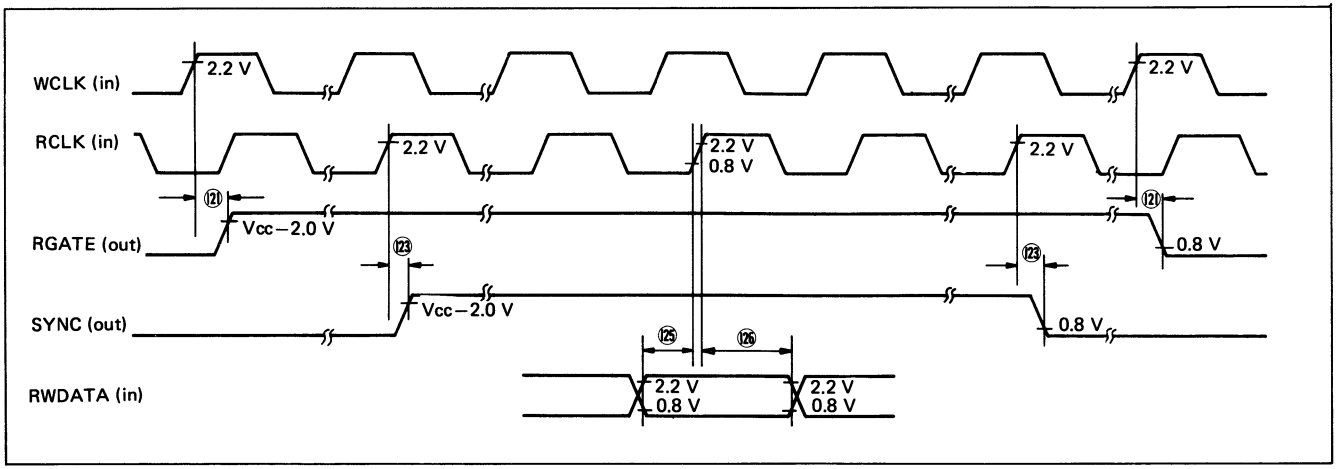


Figure 25 Read Operation (ST506)

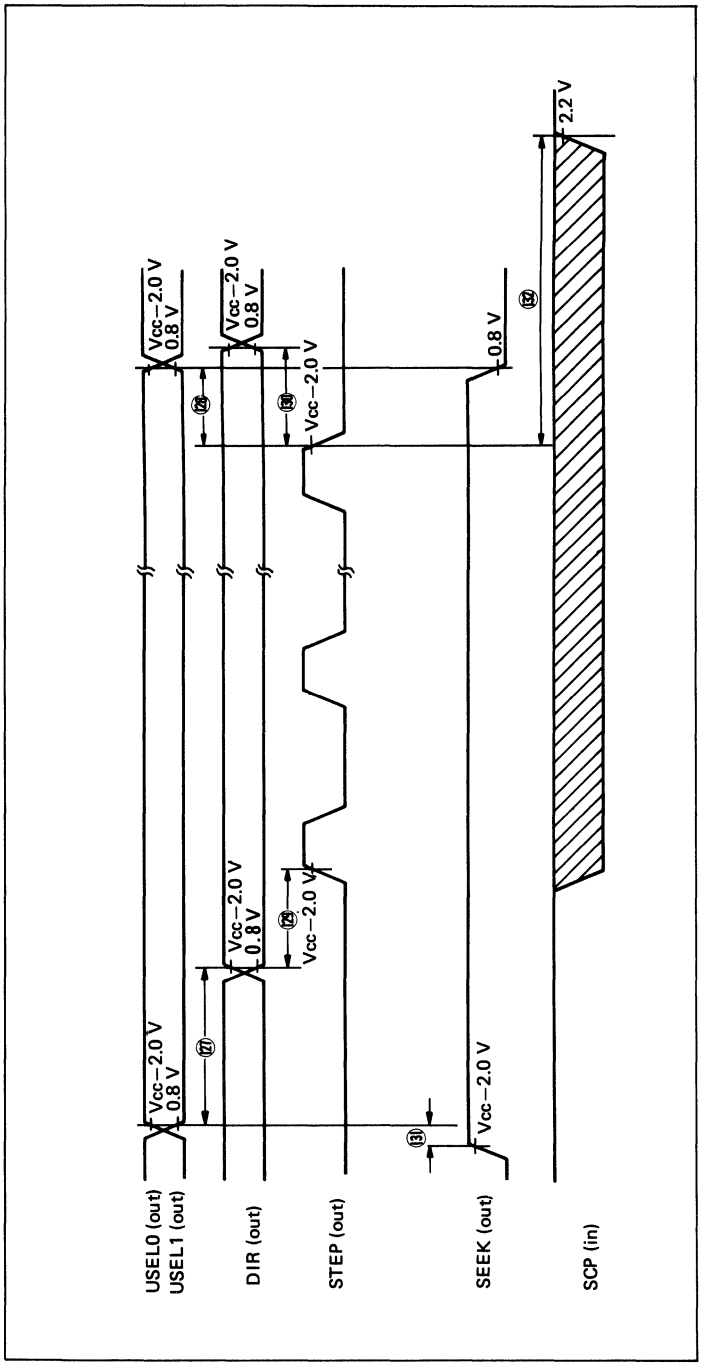


Figure 26 Head Positioning Operation (ST506)

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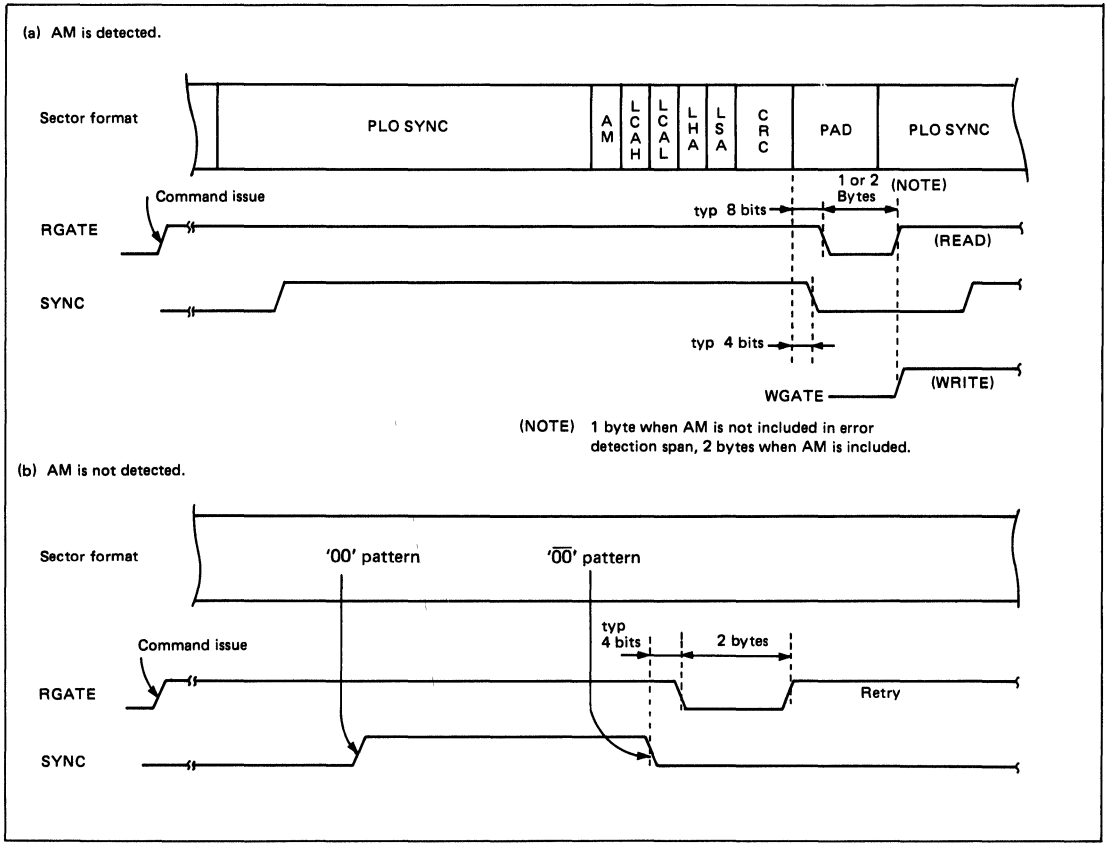

Figure 27 ID Search Timing Chart (ST506)

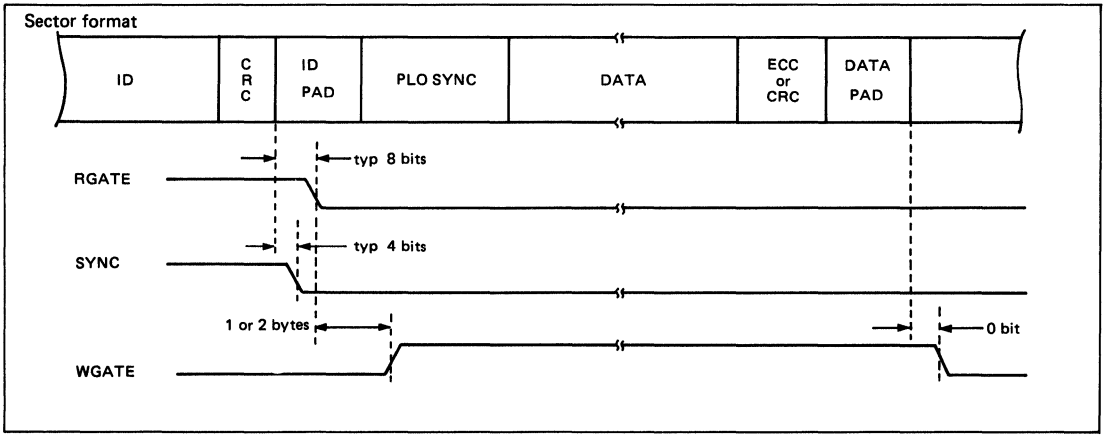

Figure 28 Write Data Timing (ST506)

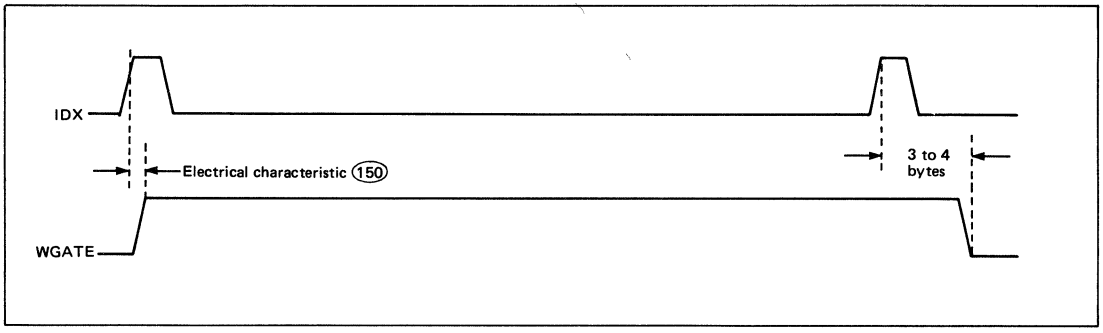

Figure 29 Write Format Timing (ST506)

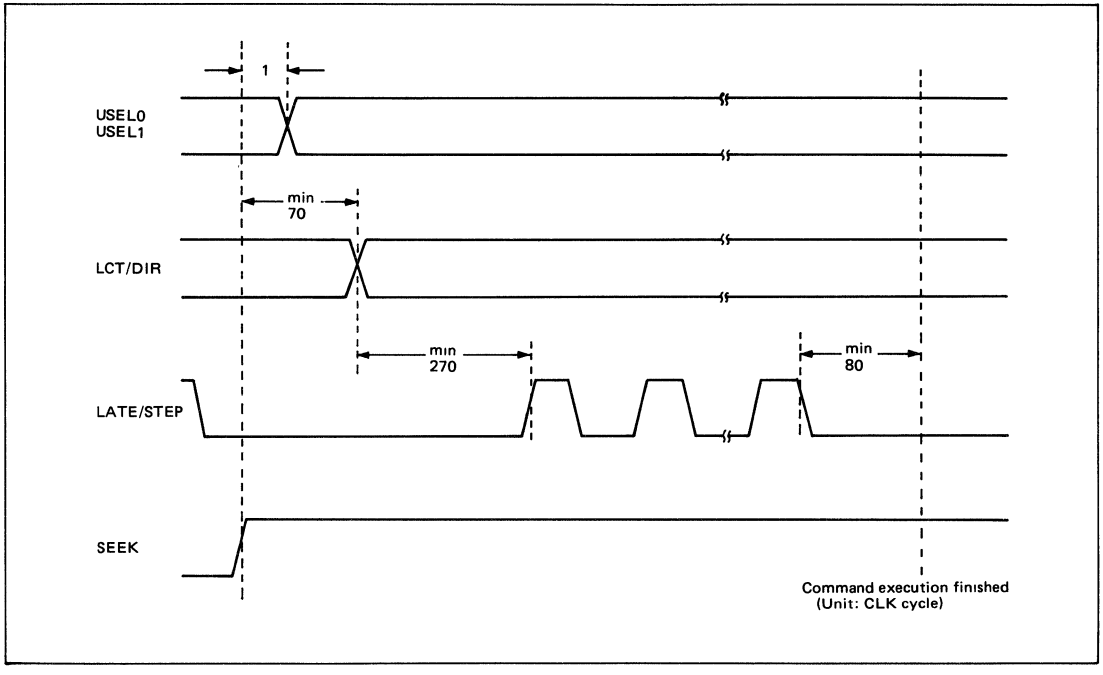

Figure 30 Seek, Recalibrate Command Execution Timing (ST506)

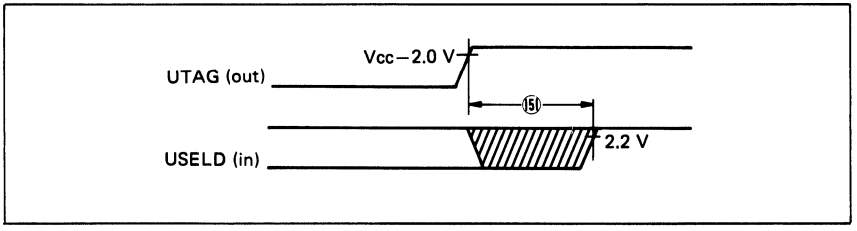

Figure 31 UTAG, USELD Timing (SMD)

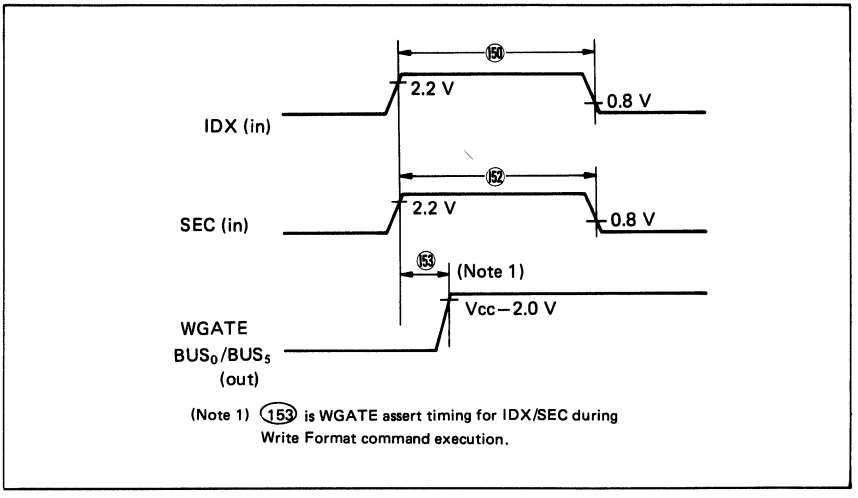

Figure 32 IDX/SEC, WGATE Timing (SMD)

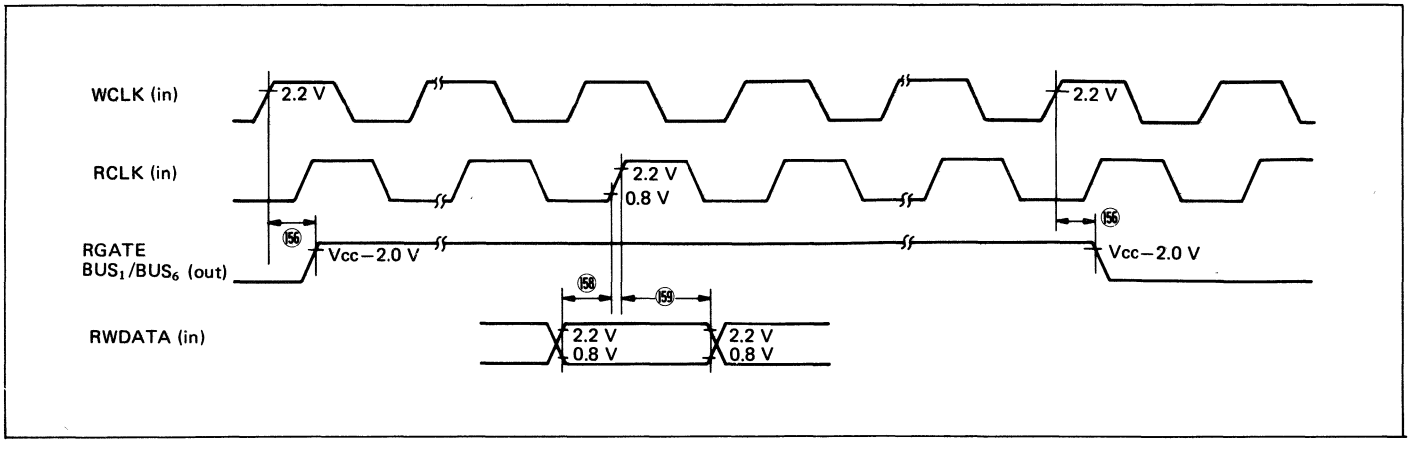

Figure 33 Read Operation (SMD)

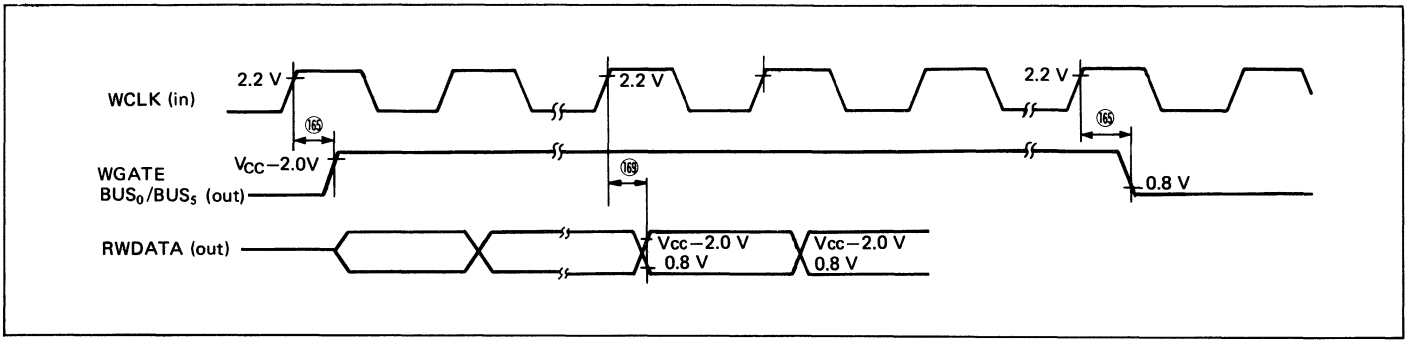

Figure 34 Write Operation (SMD)

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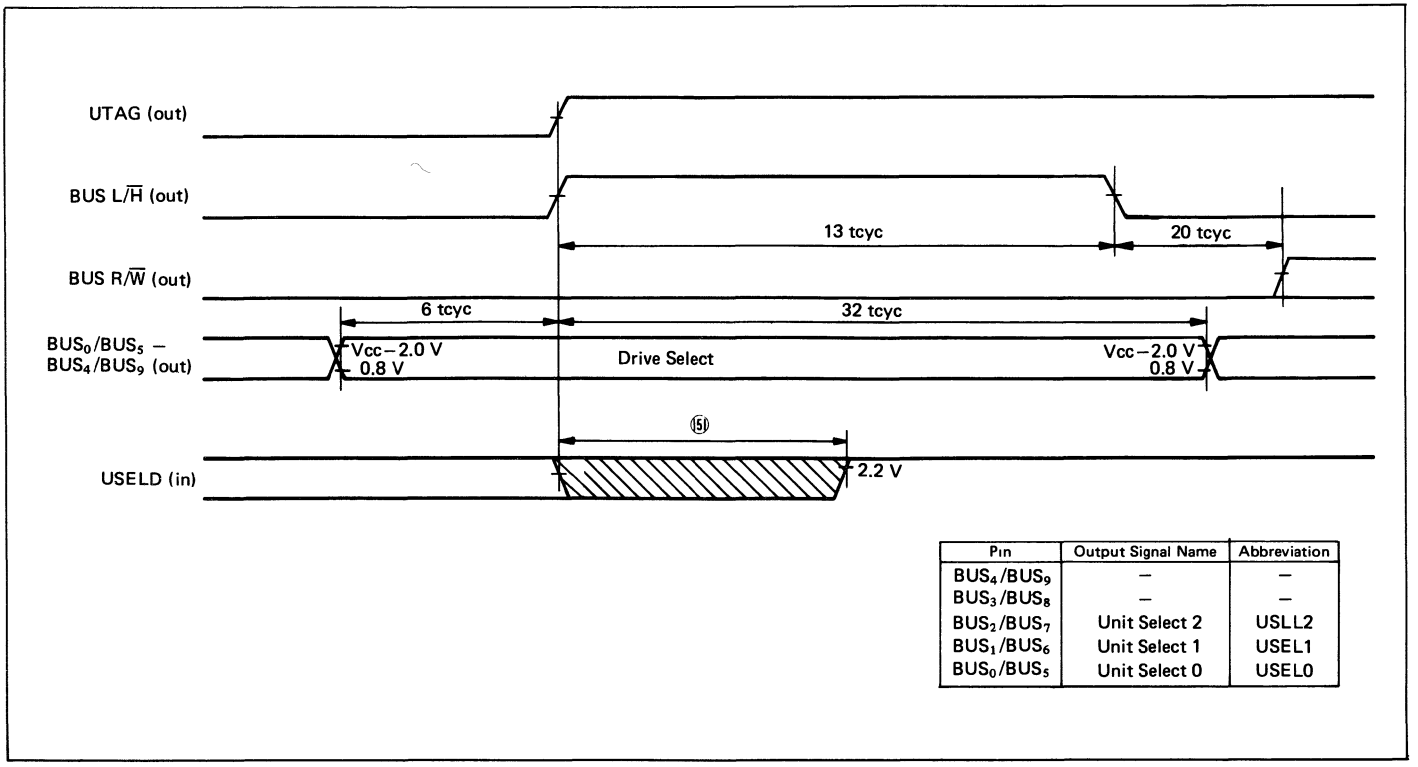
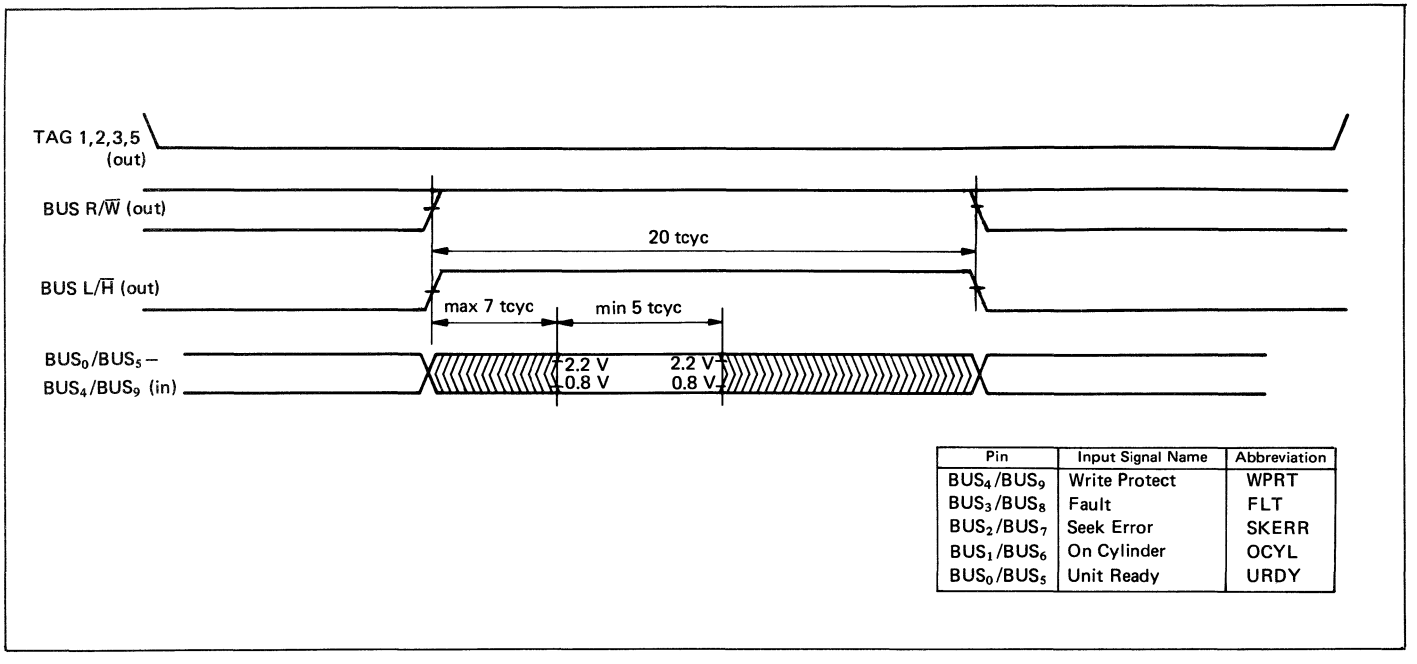


Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	Unit Select 2	USLL2
BUS_1/BUS_6	Unit Select 1	USEL1
BUS_0/BUS_5	Unit Select 0	USEL0

Figure 35 Drive Select Operation (SMD)



Pin	Input Signal Name	Abbreviation
BUS_4/BUS_9	Write Protect	WPRT
BUS_3/BUS_8	Fault	FLT
BUS_2/BUS_7	Seek Error	SKERR
BUS_1/BUS_6	On Cylinder	OCYL
BUS_0/BUS_5	Unit Ready	URDY

Figure 36 Drive Check Operation (SMD)

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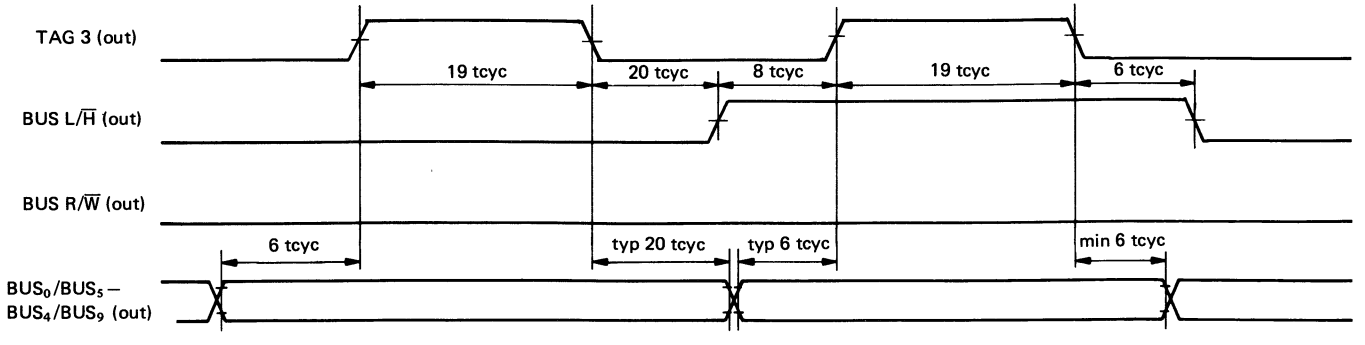


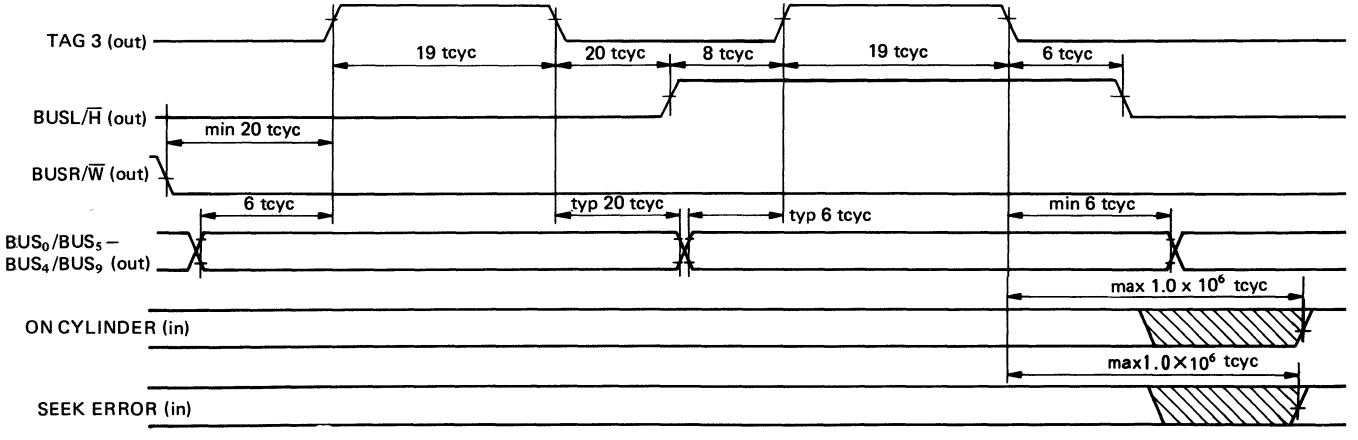
BUSL/H = low

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	(Reserve)	O	low
BUS_3/BUS_8	Strobe Late	STBL	low
BUS_2/BUS_7	Strobe Early	STBE	low
BUS_1/BUS_6	Return to Zero	RTZ	low
BUS_0/BUS_5	Reserve	O	low

BUSL/H = high

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Fault Clear	FCLR	high
BUS_3/BUS_8	Servo Offset Minus	SOFM	low
BUS_2/BUS_7	Servo Offset Plus	SOFP	low
BUS_1/BUS_6	Read Gate	RGATE	low
BUS_0/BUS_5	Write Gate	WGATE	low

Figure 37 Fault Clear Operation (SMD)



BUSL/$\overline{H}$ = low

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Reserve	O	low
BUS_3/BUS_8	Strobe Late	STBL	low
BUS_2/BUS_7	Strobe Early	STBE	low
BUS_1/BUS_6	Return to Zero	RTZ	high
BUS_0/BUS_5	Reserve	O	low

BUSL/$\overline{H}$ = high

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Fault Clear	FCLR	low
BUS_3/BUS_8	Servo Offset Minus	SOFM	low
BUS_2/BUS_7	Servo Offset Plus	SOFP	low
BUS_1/BUS_6	Read Gate	RGATE	low
BUS_0/BUS_5	Write Gate	WGATE	low

(Note) On Cylinder and Seek Error are checked by Polling command.

Figure 38 Recalibrate Command Execution Timing (SMD)

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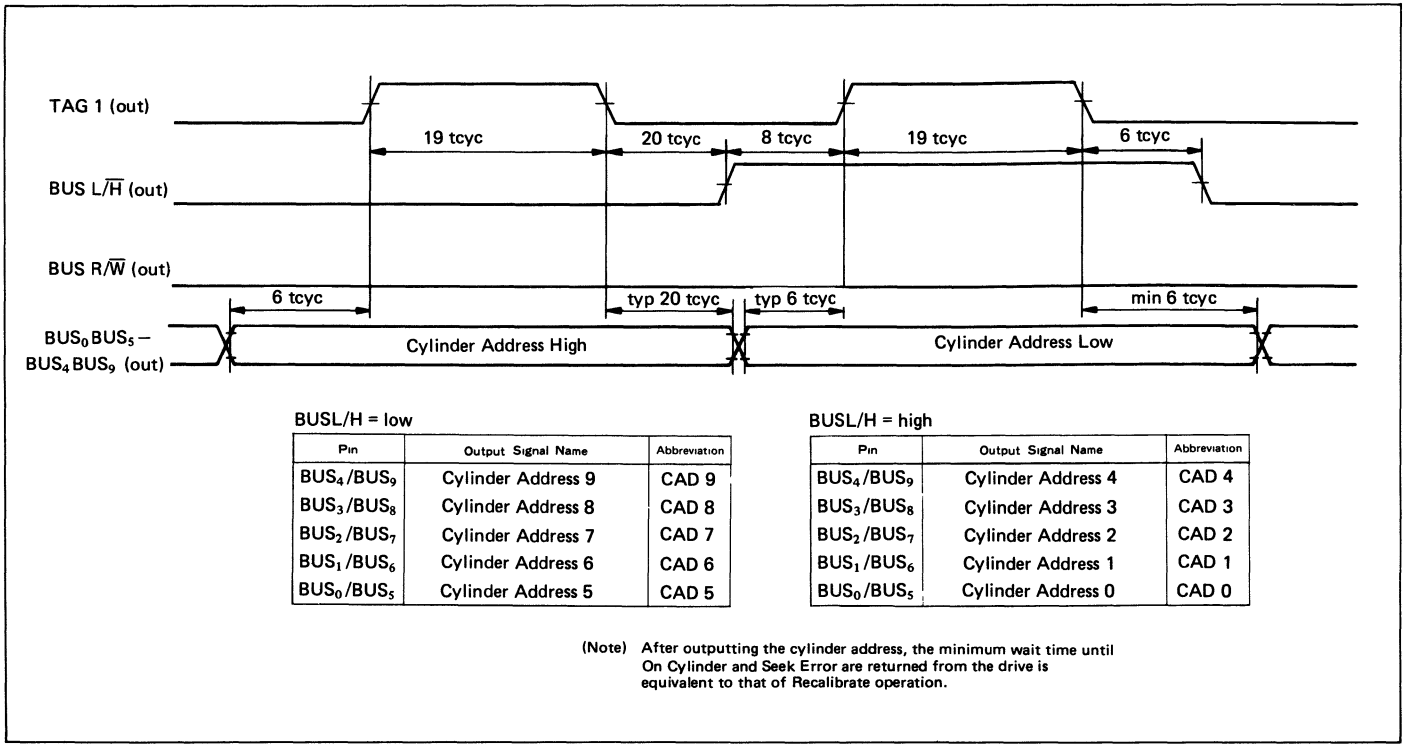


BUSL/H = low

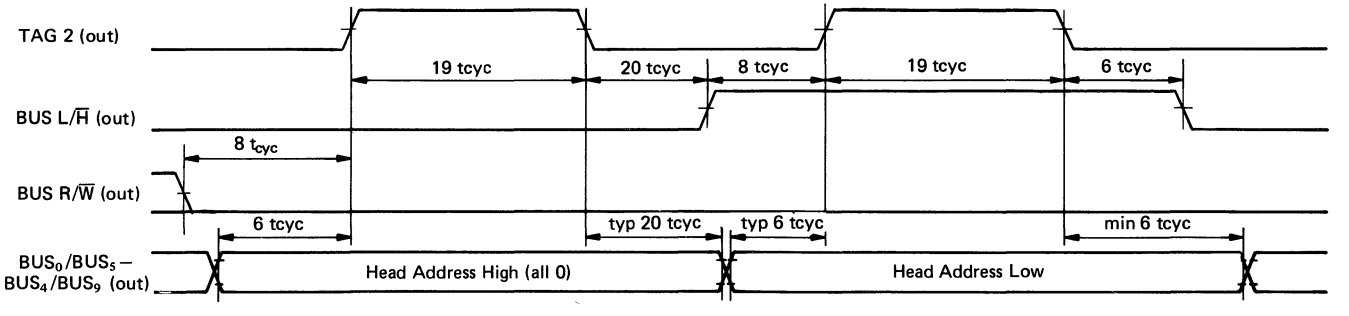
Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Cylinder Address 9	CAD 9
BUS_3/BUS_8	Cylinder Address 8	CAD 8
BUS_2/BUS_7	Cylinder Address 7	CAD 7
BUS_1/BUS_6	Cylinder Address 6	CAD 6
BUS_0/BUS_5	Cylinder Address 5	CAD 5

BUSL/H = high

Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Cylinder Address 4	CAD 4
BUS_3/BUS_8	Cylinder Address 3	CAD 3
BUS_2/BUS_7	Cylinder Address 2	CAD 2
BUS_1/BUS_6	Cylinder Address 1	CAD 1
BUS_0/BUS_5	Cylinder Address 0	CAD 0

(Note) After outputting the cylinder address, the minimum wait time until On Cylinder and Seek Error are returned from the drive is equivalent to that of Recalibrate operation.

Figure 39 Seek Command Execution Timing (SMD)



BUSL/$\overline{H}$ = low

Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Head Address 9	HAD 9
BUS_3/BUS_8	Head Address 8	HAD 8
BUS_2/BUS_7	Head Address 7	HAD 7
BUS_1/BUS_6	Head Address 6	HAD 6
BUS_0/BUS_5	Head Address 5	HAD 5

BUSL/$\overline{H}$ = high

Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Head Address 4	HAD 4
BUS_3/BUS_8	Head Address 3	HAD 3
BUS_2/BUS_7	Head Address 2	HAD 2
BUS_1/BUS_6	Head Address 1	HAD 1
BUS_0/BUS_5	Head Address 0	HAD 0

(Note) Head Address 5 – 9 are fixed at low level.

Figure 40 Head Selection Operation (SMD)

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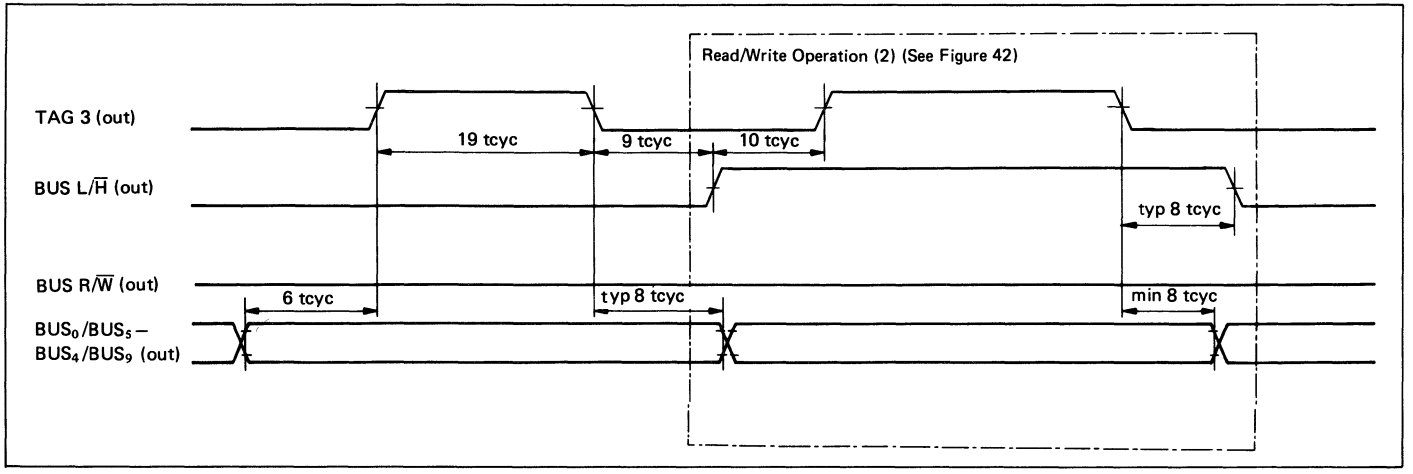


Figure 41 Read/Write Operation (1) (SMD)

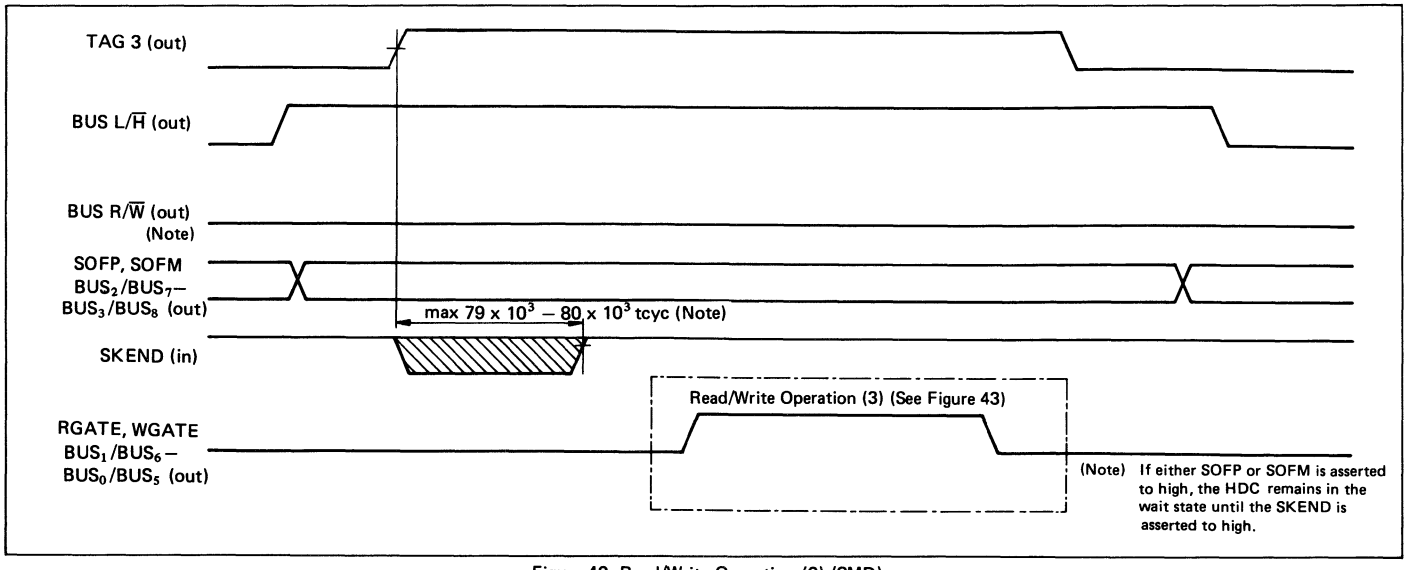
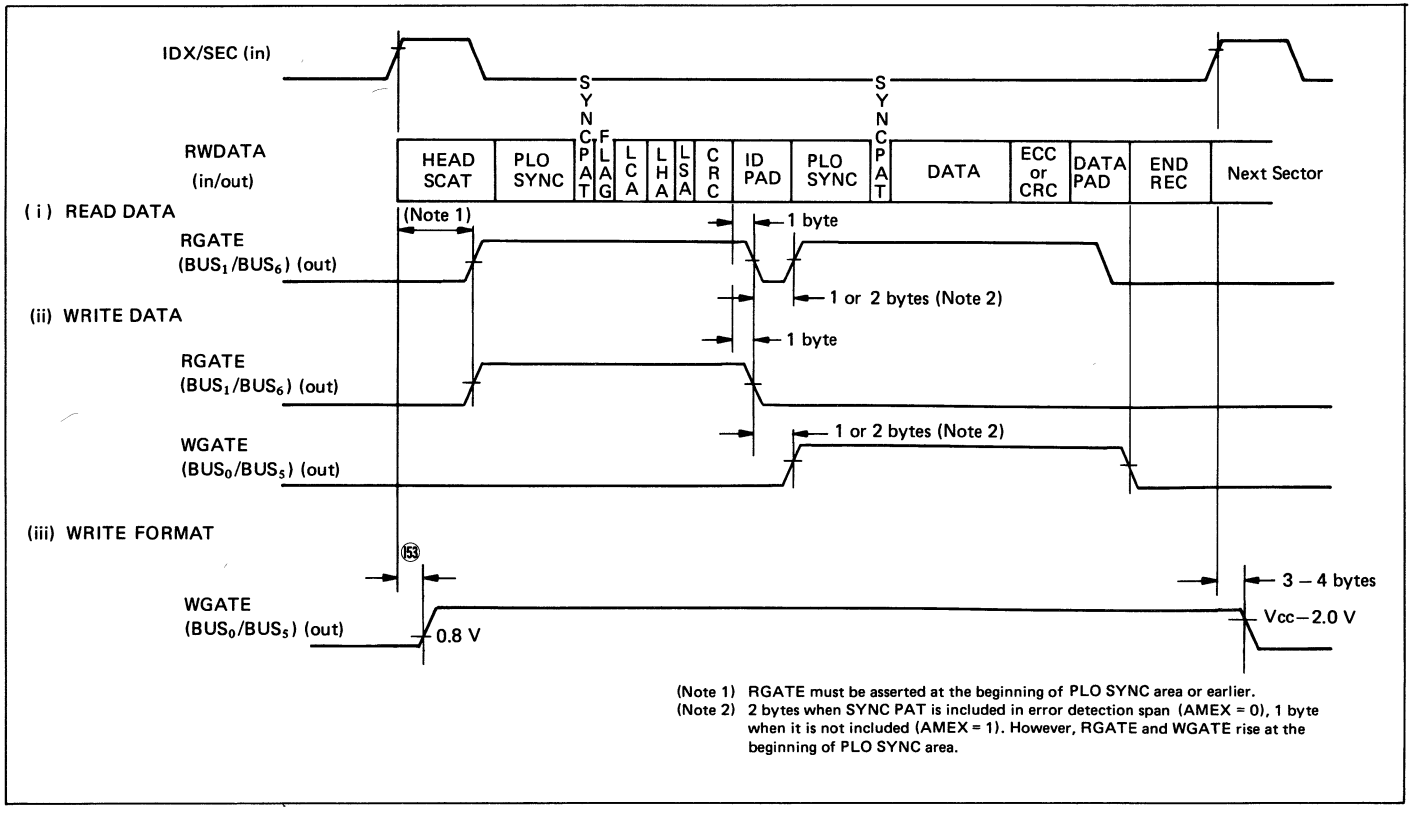


Figure 42 Read/Write Operation (2) (SMD)



(Note 1) RGATE must be asserted at the beginning of PLO SYNC area or earlier.
(Note 2) 2 bytes when SYNC PAT is included in error detection span (AMEX = 0), 1 byte when it is not included (AMEX = 1). However, RGATE and WGATE rise at the beginning of PLO SYNC area.

Figure 43 Read/Write Operation (3) (SMD)

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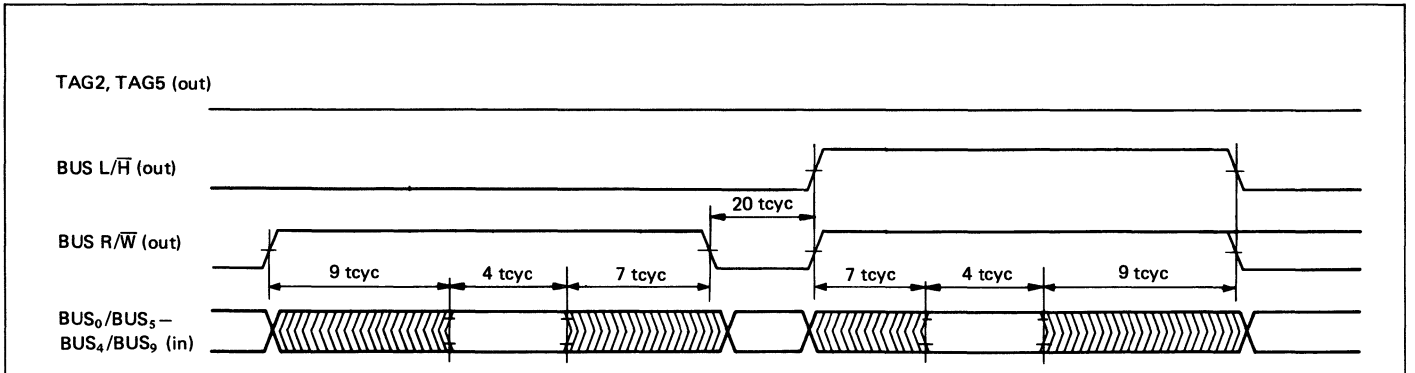


BUSL/H = low

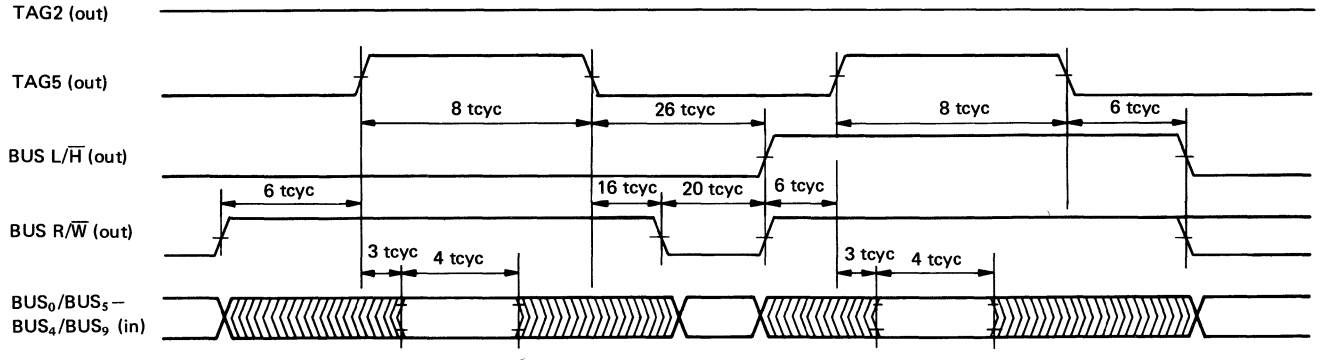
Pin	Input Signal Name	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	*	*
BUS_1/BUS_6	*	*
BUS_0/BUS_5	*	*

BUSL/H = high

Pin	Input Signal Name	Abbreviation
BUS_4/BUS_9	Write Protected	WPRT
BUS_3/BUS_8	Fault	FLT
BUS_2/BUS_7	Seek Error	SKERR
BUS_1/BUS_6	On Cylinder	OCYL
BUS_0/BUS_5	Unit Ready	URDY

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).
(Note 2) User Area

Figure 44 Sense Drive Operation (1) (SMD)



BUSL/H = low

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	* (Note 2)	*
BUS_0/BUS_5	SELECT ERROR	SELER

BUSL/H = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Write Error 3	WERR3
BUS_3/BUS_8	Write Error 2	WERR2
BUS_2/BUS_7	Write Error 1	WERR1
BUS_1/BUS_6	Status Error 2	SERR2
BUS_0/BUS_5	Status Error 1	SERR1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).
(Note 2) User Area

Figure 45 Check Drive Status (2) (SMD)

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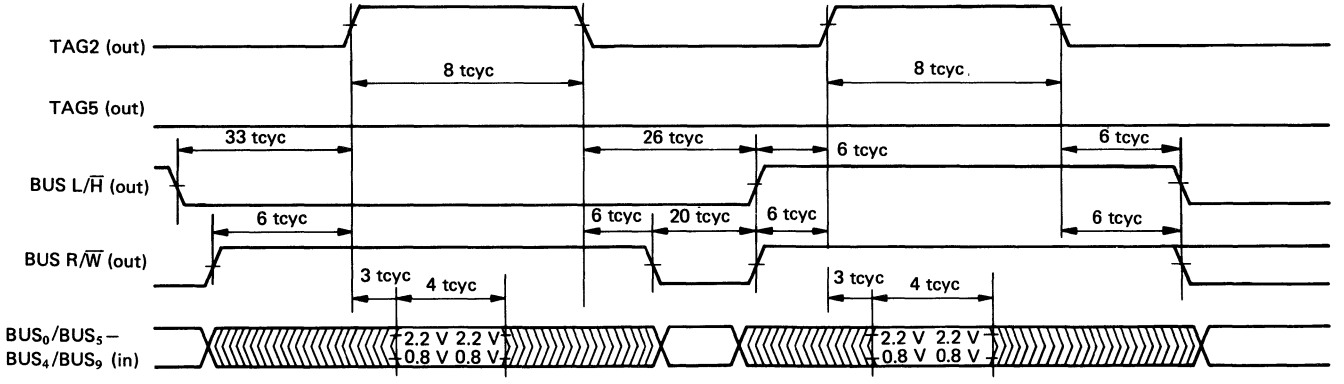


BUSL/$\overline{H}$ = low

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	* (Note 2)	*
BUS_0/BUS_5	Sector Address 32	SAD32

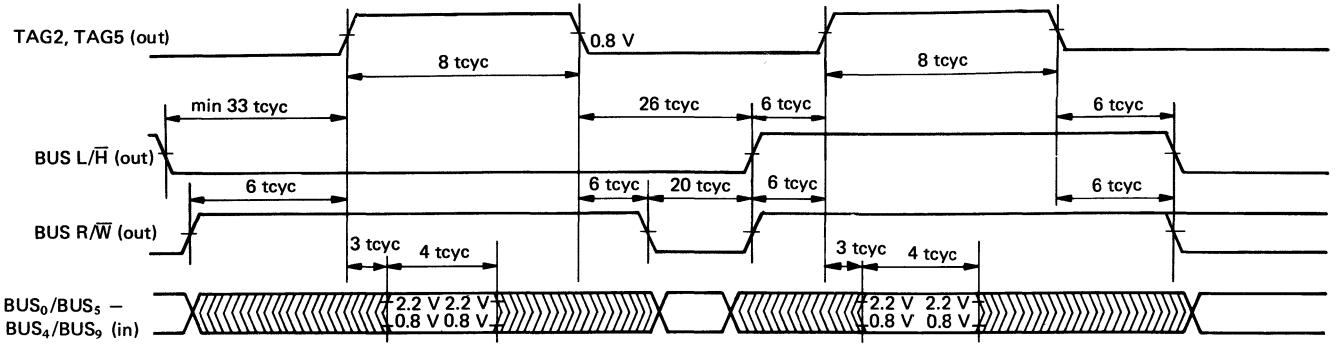
BUSL/$\overline{H}$ = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Sector Address 16	SAD16
BUS_3/BUS_8	Sector Address 8	SAD8
BUS_2/BUS_7	Sector Address 4	SAD4
BUS_1/BUS_6	Sector Address 2	SAD2
BUS_0/BUS_5	Sector Address 1	SAD1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).

(Note 2) User area

Figure 46 Check Drive Status (3) (SMD)



BUSL/H̄ = low

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	* (Note 2)	*
BUS_0/BUS_5	Device Type 32	DTP32

BUSL/H̄ = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Device Type 16	DTP16
BUS_3/BUS_8	Device Type 8	DTP8
BUS_2/BUS_7	Device Type 4	DTP4
BUS_1/BUS_6	Device Type 2	DTP2
BUS_0/BUS_5	Device Type 1	DTP1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).

(Note 2) User Area

Figure 47 Check Drive Status (4) (SMD)

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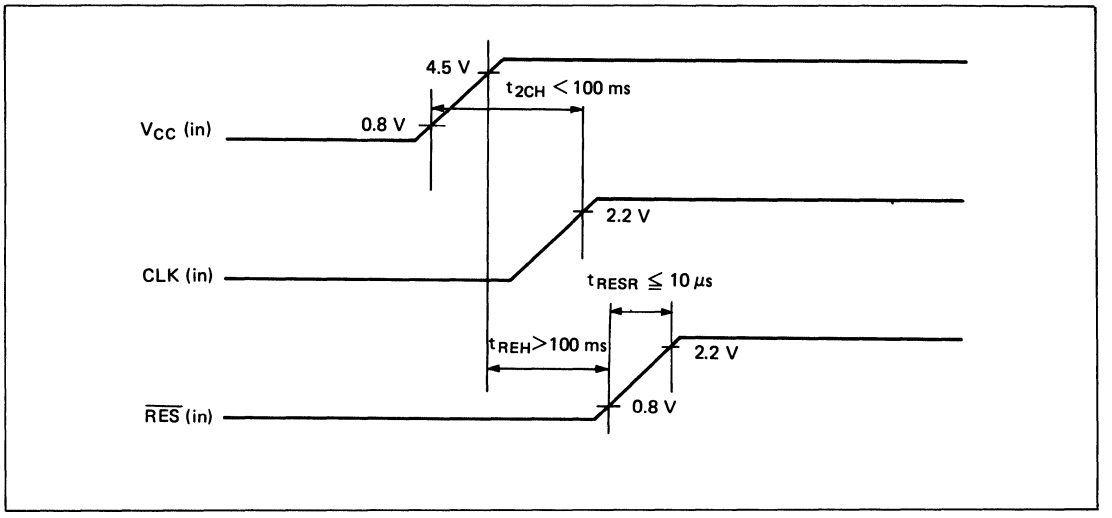

Figure 48 Timing Requirement during Power-On.