HD63310R
Smart Dual Port RAM (S-DPRAM)

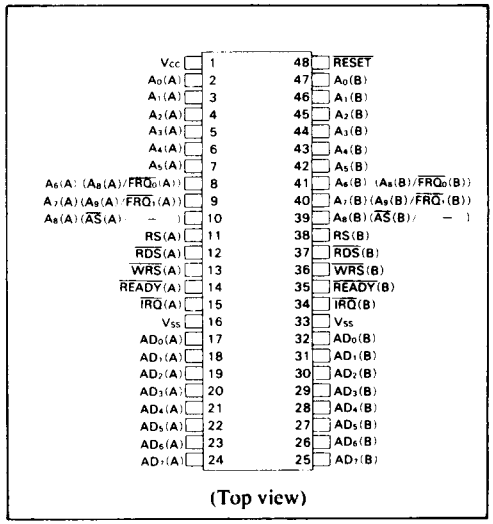
Description

Driven by the declining costs of VLSI CPUs, new multiprocessing and parallel-processing architectures are being explored to break the performance barrier of single CPU designs. A critical factor for multiprocessor performance is the choice of the communication mechanism between CPUs. A poorly designed communication scheme can destroy the potential for a multiprocessor design since message passing overhead can quickly offset the performance advantage of multiple CPUs.

An HD63310R S-DPRAM acts as a communication link between two CPUs. Thus, it replaces older, less flexible communication schemes such as parallel ports and FIFO ICs.

Programmable operating mode and bus interface tailor the S-DPRAM for a wide variety of multiprocessor system designs using industry standard MPUs.

Pin Arrangement

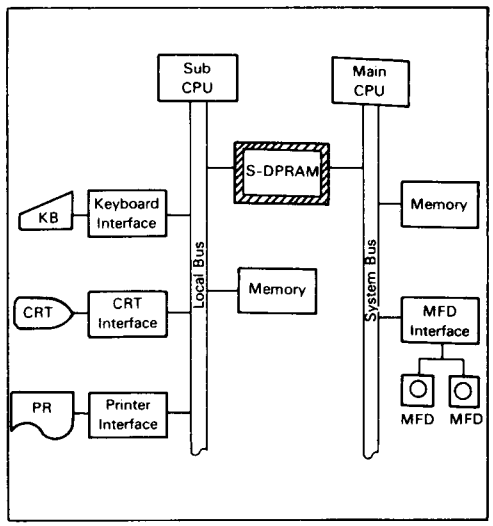


(Top view)

Features

- 1024-byte data buffer with dual ports
  —Configurable as a RAM (DPRAM mode) or two FIFOs (FIFO mode)
- Asynchronous bus operation on each port
- Programmable bus interface
  —Each bus configurable as a multiplexed or non-multiplexed address and data bus.
- Built-in programmable registers
  —8 semaphore registers for multiprocessing applications, 32 user-definable registers
- Programmable outputs
  —Interrupt outputs
  —FIFO status (full/empty, etc) outputs
- High speed operation and low power dissipation 2-μm CMOS circuit
- Single + 5V power supply

System Block Diagram



4

Pin Description

Symbol	Pin Number	Name	I/O
V_{CC}	1	Power supply	
V_{SS}	16, 33	Ground	
$\overline{RESET}$	48	Reset	I
A_0-A_5(A) A_0-A_5(B)	2-7 47-42	Address bus	I
AD_0-AD_7(A) AD_0-AD_7(B)	17-24 32-25	Address/data bus	I/O
$A_6/A_8/\overline{FRQ_0}$(A) $A_6/A_8/\overline{FRQ_0}$(B)	8 41	Multipurpose line (1): Address bit 6/8, FIFO data request 0	I/O
$A_7/A_9/\overline{FRQ_1}$(A) $A_7/A_9/\overline{FRQ_1}$(B)	9 40	Multipurpose line (2): Address bit 7/9, FIFO data request 1	I/O
$A_8/\overline{AS}$ (A) $A_8/\overline{AS}$ (B)	10 39	Multipurpose line (3): Address bit 8, Address strobe	I
RS (A/B)	11, 38	Register select	I
$\overline{RDS}$ (A/B)	12, 37	Read strobe	I
$\overline{WRS}$ (A/B)	13, 36	Write strobe	I
$\overline{READY}$ (A/B)	14, 35	Ready	O
$\overline{IRQ}$(A/B)	15, 34	Interrupt request	O

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} (Note 2)	−0.3 to +7.0	V
Input Voltage	Vin (Note 2)	−0.3 to V_{CC} +0.3	V
Allowable Output Current	|Io| (Note 3)	5	mA
Total Allowable Output Current	|Σ Io| (Note 4)	60	mA
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.
2. With respect to V_{SS} (system GND)
3. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.
4. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input Voltage	V_{IH} (Note)	2.2	–	V_{CC}	V
	V_{IL} (Note)	0	–	0.8	V
Operating Temperature	Topr	0	25	70	°C

Note: With respect to V_{SS} (system GND)

4

Electrical Charcteristics

DC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to +70°C, unless otherwise noted)

Item		Sym.	Min	Max	Unit	Test Condition
Input High Voltage		V_{IH}	2.2	V_{CC}	V	
Input Low Voltage		V_{IL}	V_{SS} −0.3	0.8	V	
Input Leakage Current	$A_0(A)-A_5(A)$, $A_0(B)-A_5(B)$, RS(A), RS(B), $\overline{RDS}$(A), $\overline{RDS}$(B), $A_8(A)/\overline{AS}(A)$, $A_8(B)/\overline{AS}(B)$, $\overline{WRS}$(A), $\overline{WRS}$(B), $\overline{RESET}$	Iin	−2.5	2.5	μA	Vin = 0 to V_{CC}
Three-State (Off State) Leakage Current	$AD_0(A)-AD_7(A)$, $AD_0(B)-AD_7(B)$, $A_6(A)/A_8(A)/\overline{FRQ_0}(A)$, $A_6(B)/A_8(B)/\overline{FRQ_0}(B)$, $A_7(A)/A_9(A)/\overline{FRQ_1}(A)$, $A_7(B)/A_9(B)/\overline{FRQ_1}(B)$	I_{TSI}	−10	10	μA	Vin = 0 to V_{CC}
Output Leakage Current	$\overline{IRQ}$(A), $\overline{IRQ}$(B)	I_{LOH}	−10	10	μA	V_{OH} = V_{CC}
Output High Voltage		V_{OH}	V_{CC} − 1.0	−	V	I_{OH} = −400 μA
			V_{CC} − 0.1	−	V	I_{OH} ≦ −10 μA
Output Low Voltage	$AD_0(A)-AD_7(A)$, $AD_0(B)-AD_7(B)$, $A_6(A)/A_8(A)/\overline{FRQ_0}(A)$, $A_6(B)/A_8(B)/\overline{FRQ_0}(B)$, $A_7(A)/A_9(A)/\overline{FRQ_1}(A)$, $A_7(B)/A_9(B)/\overline{FRQ_1}(B)$, $\overline{READY}$(A), $\overline{READY}$(B)	V_{OL}	−	0.5	V	I_{OL} = 2 mA
	$\overline{IRQ}$(A), $\overline{IRQ}$(B)		−	0.5	V	I_{OL} = 3.2 mA
Input Capacitance		Cin	−	20	pF	Vin = 0 V, Ta = 25°C, f = 1.0 MHz
Output Capacitance		Cout	−	20		
Current Dissipation	Operating Mode	I_{CC}	−	30	mA	V_{CC} = 5.25 V, V_{IH} = 2.2 V, V_{IL} = 0.8 V
	Standby Mode ($\overline{RDS}$, $\overline{WRS}$ = High)		−	1	mA	V_{CC} = 5.25 V, V_{IH} = V_{CC} − 0.2 V, V_{IL} = 0.2 V

Packaging Information

Part No.	Package
HD63310R	DP-48