HD61602/HD61603

(Segment Type LCD Driver)

HITACHI

Description

The HD61602 and the HD61603 are liquid crystal display driver LSIs with a TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for the liquid crystal display driver. Using the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Wide-range operating voltage
  - — Operates in a wide range of supply voltage: 2.2 V to 5.5 V
  - — Compatible with TTL interface at 4.5 V to 5.5 V
- Low current consumption
  - — Can run from a battery power supply (100 µA max. at 5 V)
  - — Standby input enables standby operation at lower current consumption (5 µA max. on 5 V)
- Internal power supply circuit for liquid crystal display driver (HD61602)
  - — Internal power supply circuit for liquid crystal display driver facilitates the connection to a microprocessor system

Ordering Information

Type No.	Package
HD61602R	80-pin plastic QFP (FP-80)
HD61602RH	80-pin plastic QFP (FP-80A)
HD61603R	80-pin plastic QFP (FP-80)

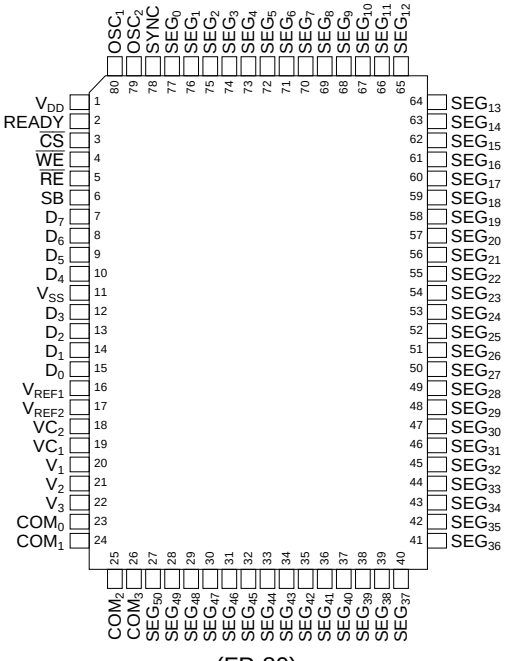
Versatile Segment Driving Capacity

Type No.	Driving Method		Display Segments	Example of Use	Frame Freq. (Hz) at f_{OSC} = 100 kHz	Package
HD61602	Static		51	8 segments × 6 digits + 3 marks	33	80-pin plastic QFP (FP-80, FP-80A, TFP-80)
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits + 4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin plastic QFP (FP-80)

Hitachi semiconductor

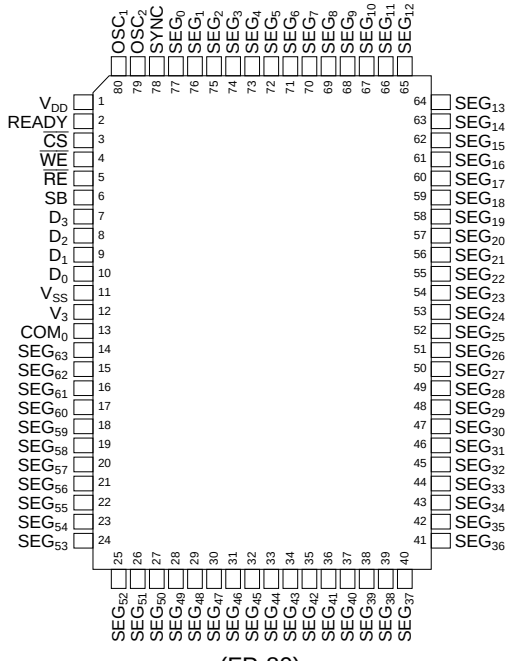
Pin Arrangement

HD61602R



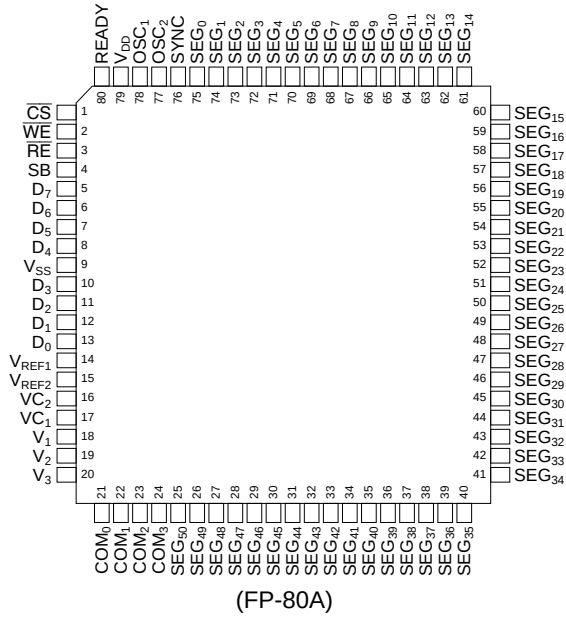
(FP-80)

HD61603R



(FP-80)

HD61602RH

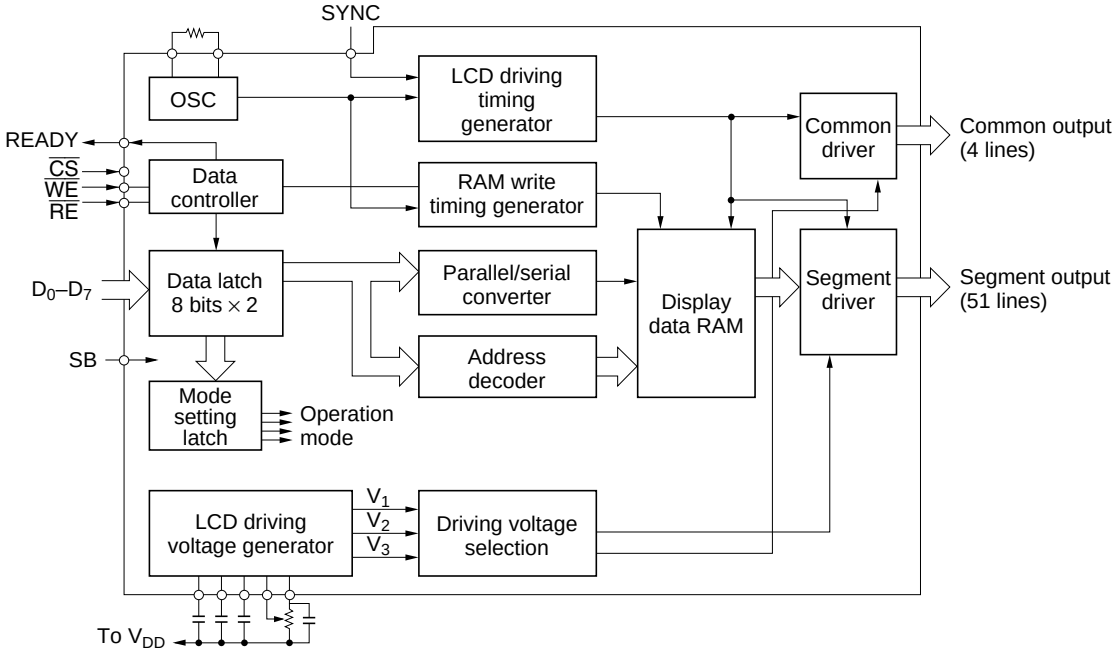


(FP-80A)

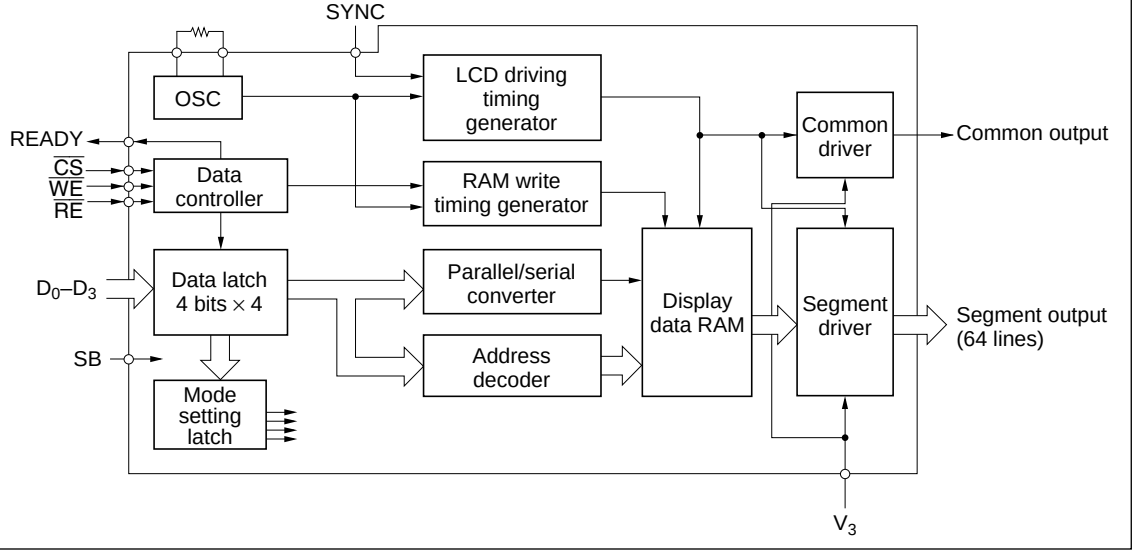
(Top view)

Block Diagram

HD61602



HD61603



Terminal Functions

HD61602 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0–D_7	8	Input	MCU	Data input terminal for 8-bit × 2-byte data.
V_{SS}	1	Power supply		Negative power supply.
V_{REF1}	1	Output	External R	Reference voltage output. Generates LCD driving voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2} \approx V_1$.
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.
V_1, V_2, V_3	3	Output (Input)	External C	LCD driving voltage outputs. An external C is connected to each terminal.
COM_0–COM_3	4	Output	LCD	LCD common (backplate) driving output.
SEG_0–SEG_{50}	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC1.

Note: Logic polarity is positive. 1 = high = active.

HD61603 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops the LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0–D_3	4	Input	MCU	Data input terminal from where 4-bit × 4 data are input.
V_{SS}	1	Power supply		Negative power supply.
V_3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V_3 is used as driving voltage.
COM_0	1	Output	LCD	LCD common (backplate) driving output.
SEG_0–SEG_{63}	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC_1.

Note: Logic polarity is positive. 1 = high = active.

Display RAM

HD61602 Display RAM

The HD61602 has an internal display RAM shown in figure 1. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to 1 segment of the LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

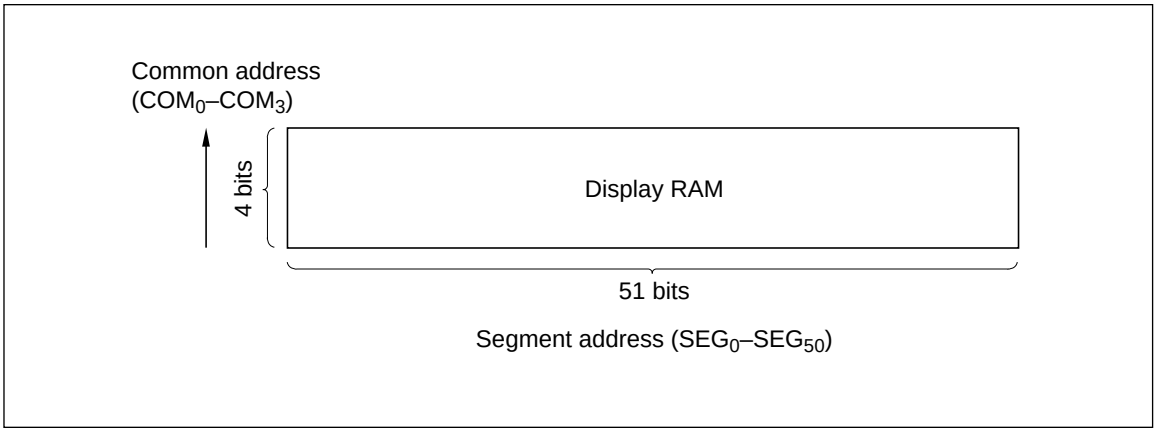


Figure 1 Display RAM

Reading Data from Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.

A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

1. Static drive

   In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 2).

2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 3).

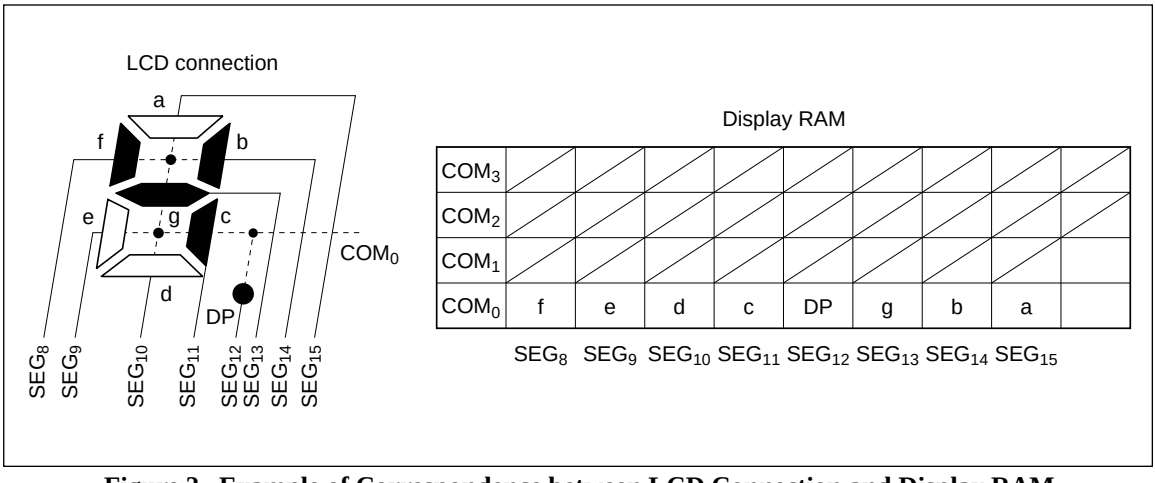


Figure 2 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61602)

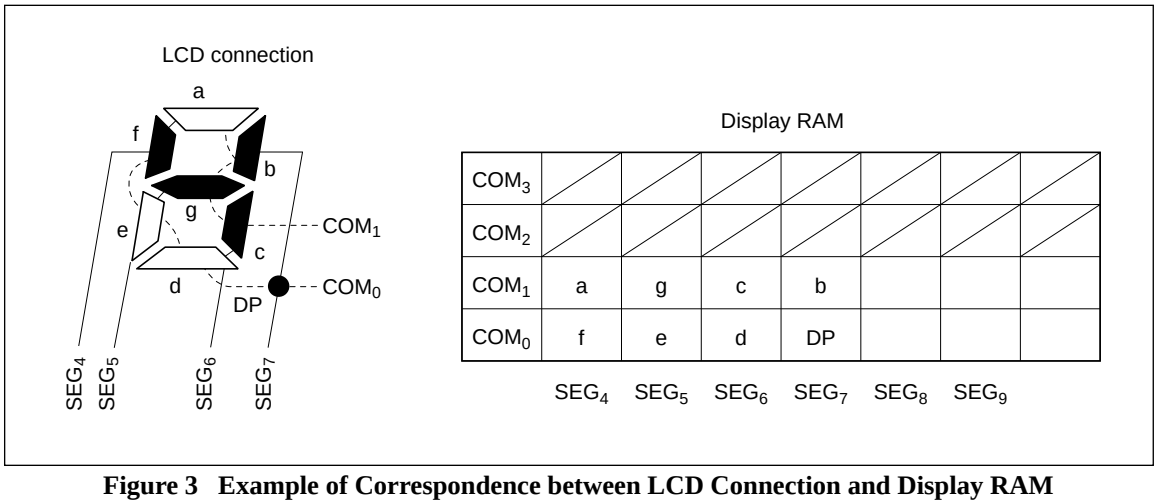


Figure 3 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61602)

3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed.

   "Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation to turn on/off the display of "Y" (figure 4).

4. 1/4 duty cycle drive

   In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed (figure 5).

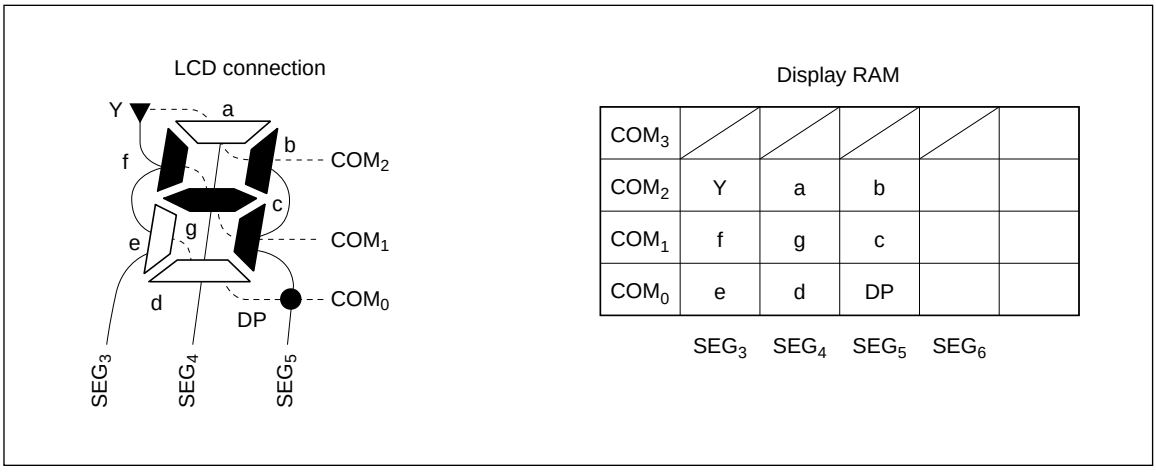


Figure 4 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61602)

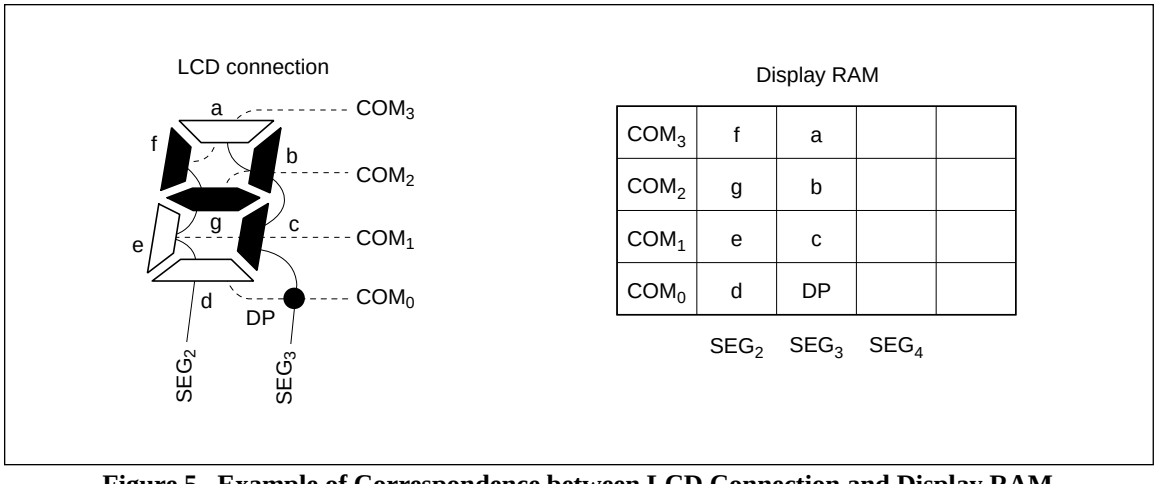


Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61602)

Writing Data into Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

3. 1/2 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.

4. 1/3 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.

5. 1/4 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in “Reading Data from Display RAM”.

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown figure 8 (allocation of digits). As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 6 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 7 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 for static, Ad12 for 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data.

Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

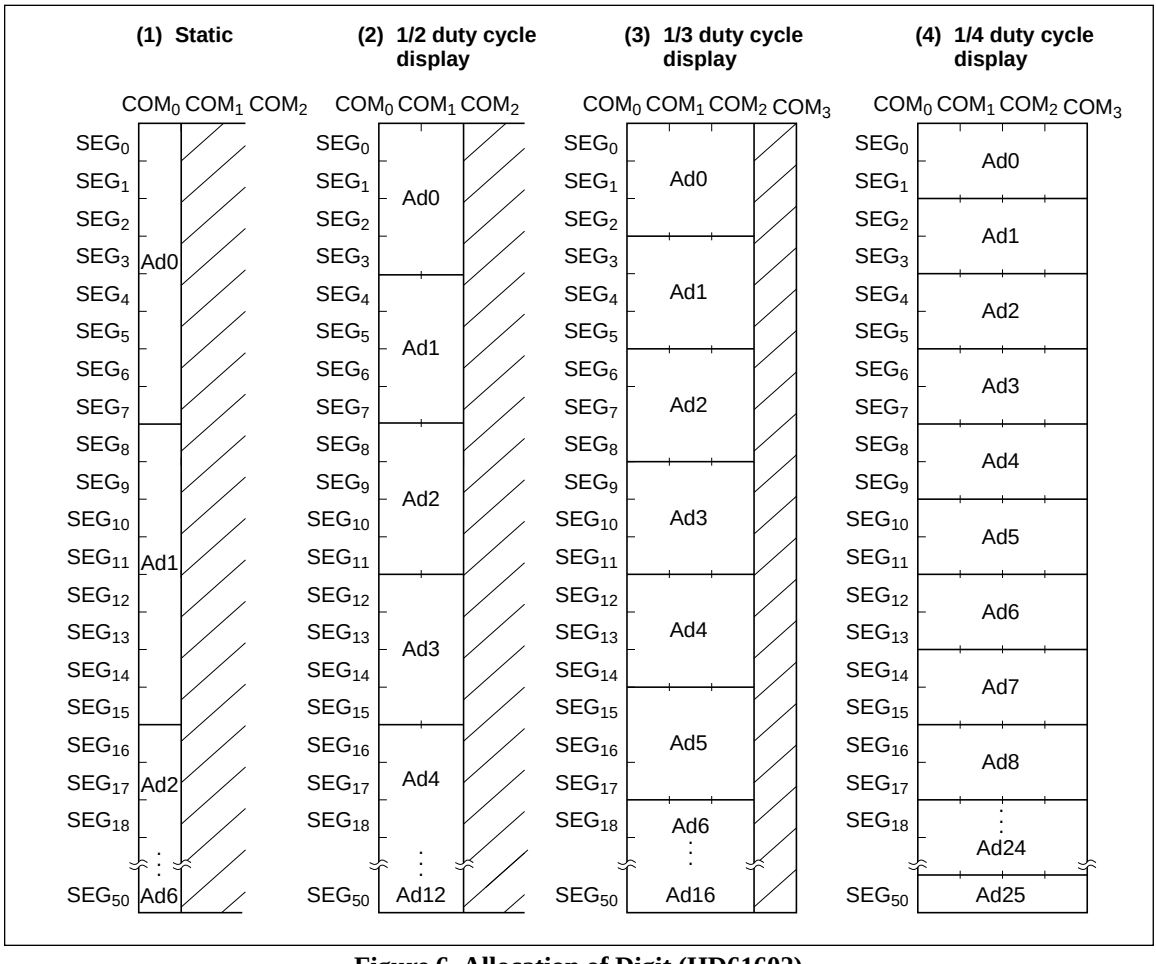


Figure 6 Allocation of Digit (HD61602)

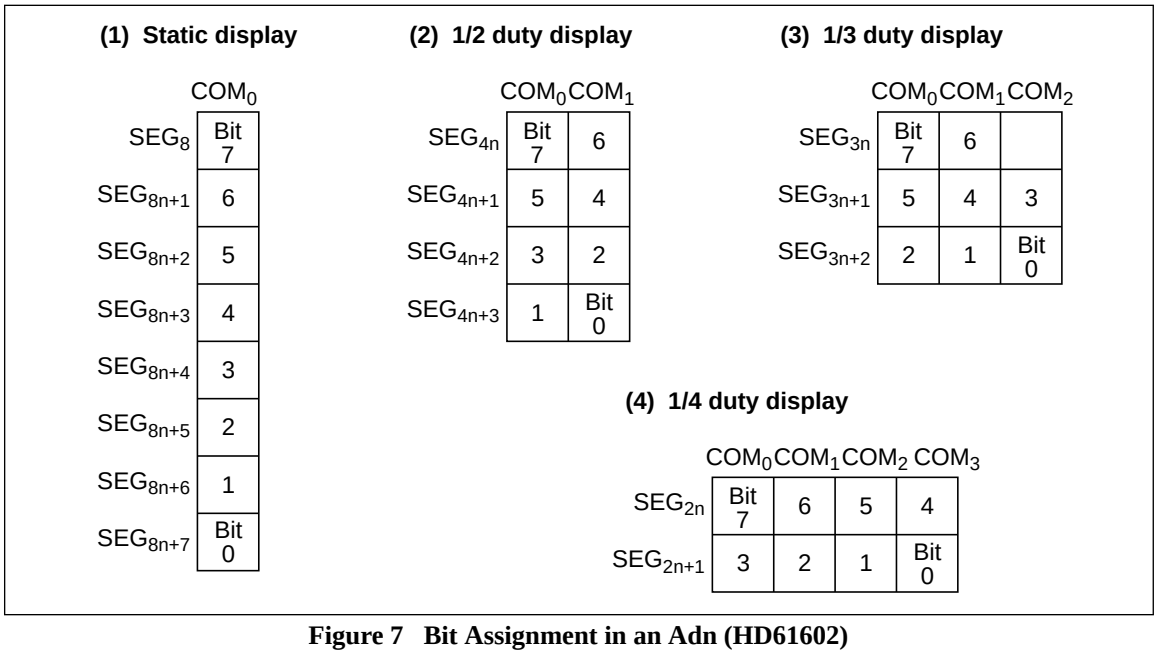


Figure 7 Bit Assignment in an Adn (HD61602)

HD61603 Display RAM

The HD61603 has an internal display RAM as shown in figure 8. Display data is stored in the RAM and output to the segment output terminal.

Reading Data from Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Figure 9 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

Writing Data into Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

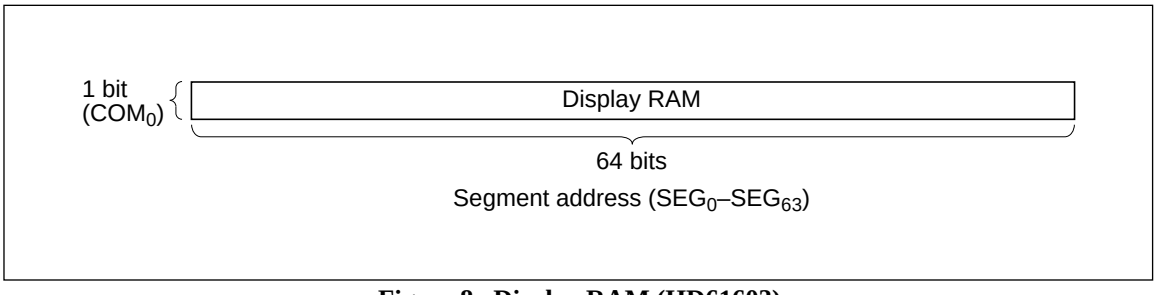


Figure 8 Display RAM (HD61603)

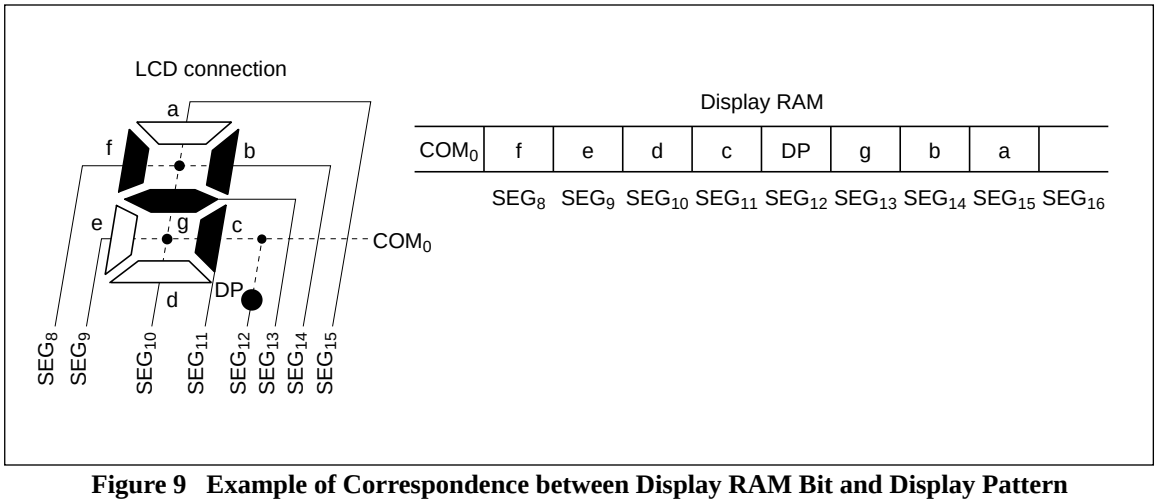


Figure 9 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 10. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 11 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

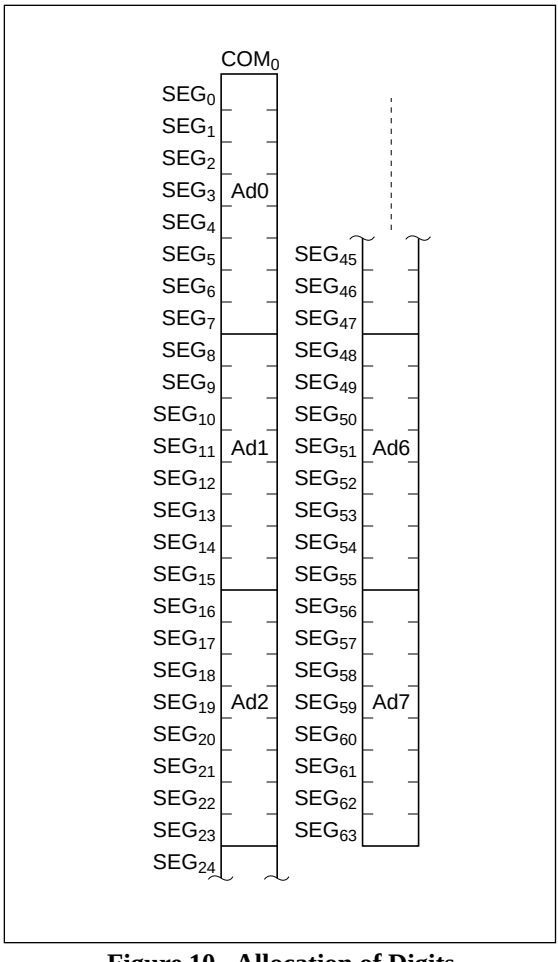


Figure 10 Allocation of Digits (HD61603)

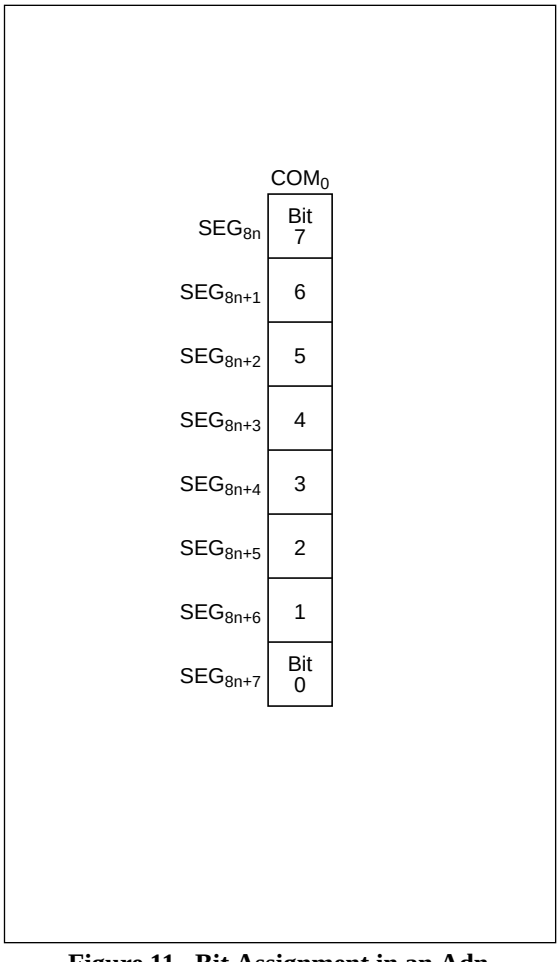


Figure 11 Bit Assignment in an Adn (HD61603)

Operating Modes

HD61602 Operating Modes

The HD61602 has the following operating modes:

1. LCD drive mode

   Determines the LCD driving method.

   a. Static drive mode
      LCD is driven statically.

   b. 1/2 duty cycle drive mode
      LCD is driven at 1/2 duty cycle and 1/2 bias.

   c. 1/3 duty cycle drive mode
      LCD is driven at 1/3 duty cycle and 1/3 bias.

   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/3 bias.

2. Data display mode

   Determines how to write display data into the data RAM.

   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.

   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.

   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.

   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.

3. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

   a. READY is mode always available (figure 12).

   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (figure 13).

4. LCD OFF mode

   In this mode, the HD61602 stops driving LCD and turns it off.

5. External driving voltage mode

   A mode for using external driving voltage (V_1, V_2, and V_3).

The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. Bit manipulation is independent of data display mode and can be used regardless of it.

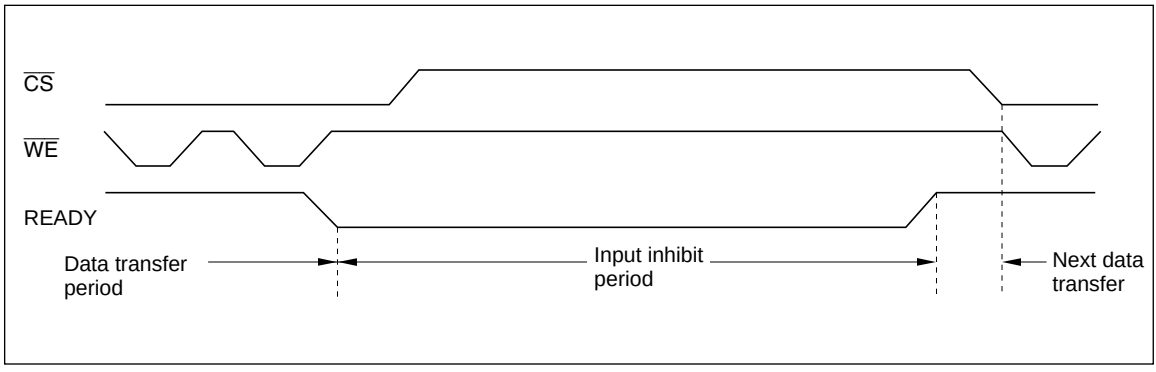


Figure 12 READY Output Timing (When It Is Always Available)

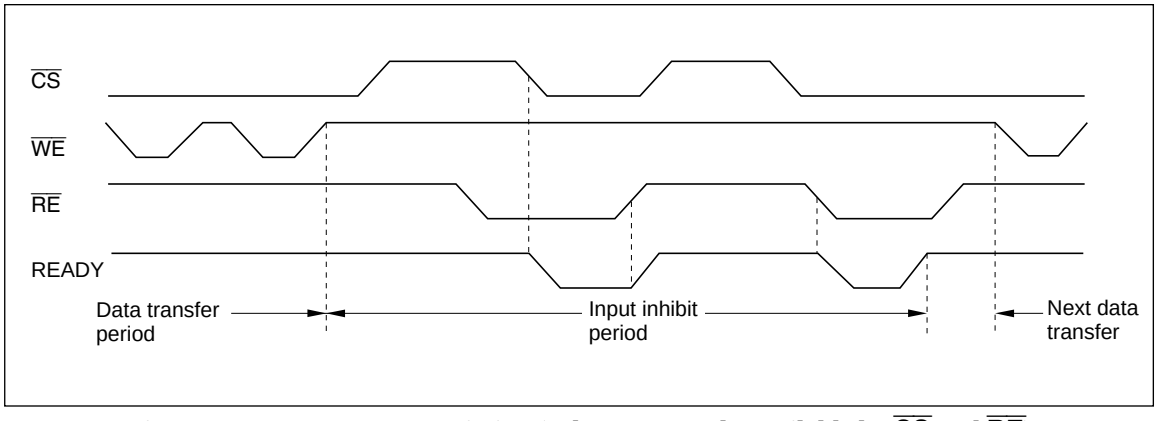


Figure 13 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

HD61603 Operating Modes

The HD61603 has the following modes:

1. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available (figure 14).

   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

2. LCD OFF mode

   In this mode, the HD61603 stops driving the LCD and turns it off.

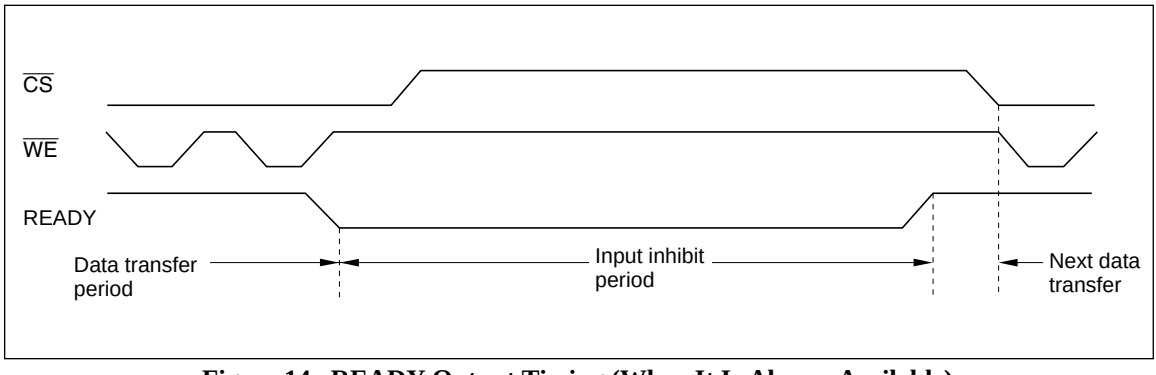


Figure 14 READY Output Timing (When It Is Always Available)

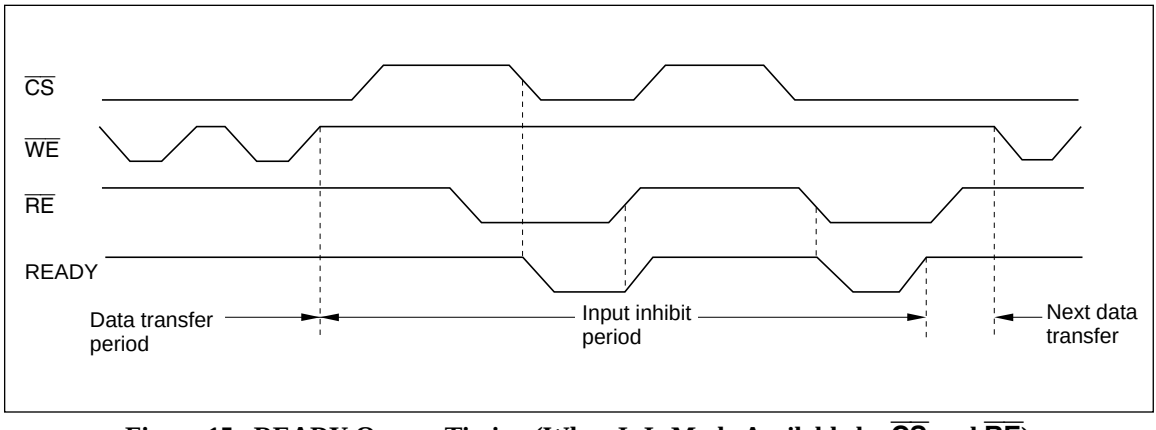


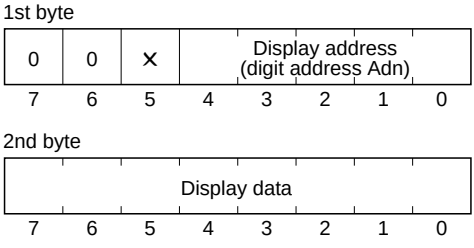
Figure 15 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

Input Data Formats

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (updates display on an 8-segment basis)



   a. Display address

      Digit address Adn in accordance with display mode

   b. Display data

      Pattern data that is written into the display RAM according to display mode and the address

2. Bit manipulation data (updates display on a segment basis)

   a. Display data

      Data that is written into 1 bit of the specified display RAM.

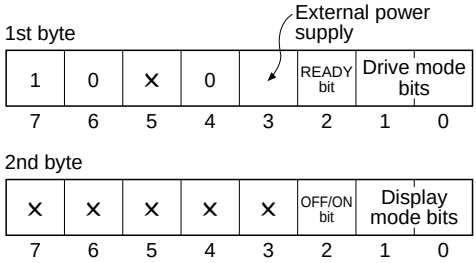
   b. COM address

      Common address of display RAM

   c. SEG address

      Segment address of display RAM

3. Mode setting data



   a. Display mode bits

      00: Static display mode

      01: 1/2 duty cycle display mode

      10: 1/3 duty cycle display mode

      11: 1/4 duty cycle display mode

   b. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered)

      0: LCD on

   c. Drive mode bits

      00: Static drive

      01: 1/2 duty cycle drive

      10: 1/3 duty cycle drive

      11: 1/4 duty cycle drive

   d. READY bit

      0: READY bus mode; READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered)

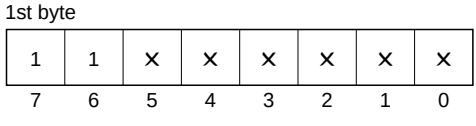
      1: READY port mode; READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

   e. External power supply bit

      0: Driving voltage is generated internally.

      1: Driving voltage is supplied externally. (Set to 1 when SYNC is entered.)

4. 1-byte instruction

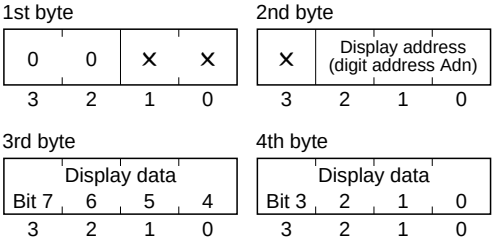


The first data (first byte) is ignored when bit 6 and bit 7 in the byte are 1.

HD61603 Input Data Formats

Input data is composed of 4 bits × 4. Input them as four 4-bit data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (updates display on an 8-segment basis)



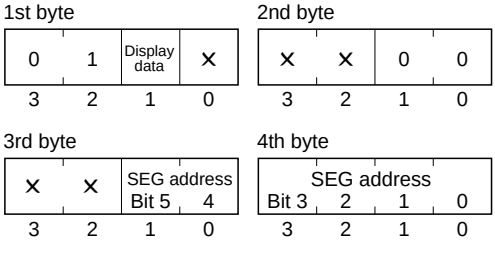
   a. Display address

      Digit address Adn shown in figure 10.

   b. Display data

      Pattern data that is written into the display RAM as shown in figure 11.

2. Bit manipulation data (updates display on a segment basis)



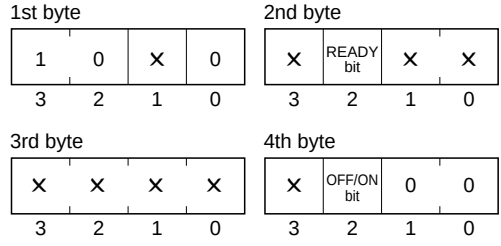
   a. Display data

      Data that is written into 1 bit of the specified display RAM.

   b. SEG address

      Segment address of display RAM (segment output)

3. Mode setting data



   a. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered.)

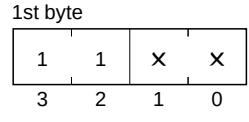
      0: LCD on

   b. READY bits

      0: READY bus mode; READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)

      1: READY port mode; READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

4. 1-byte instruction



The first data (4 bits) is ignored when bit 3 and 2 in the data are 1.

How to Input Data

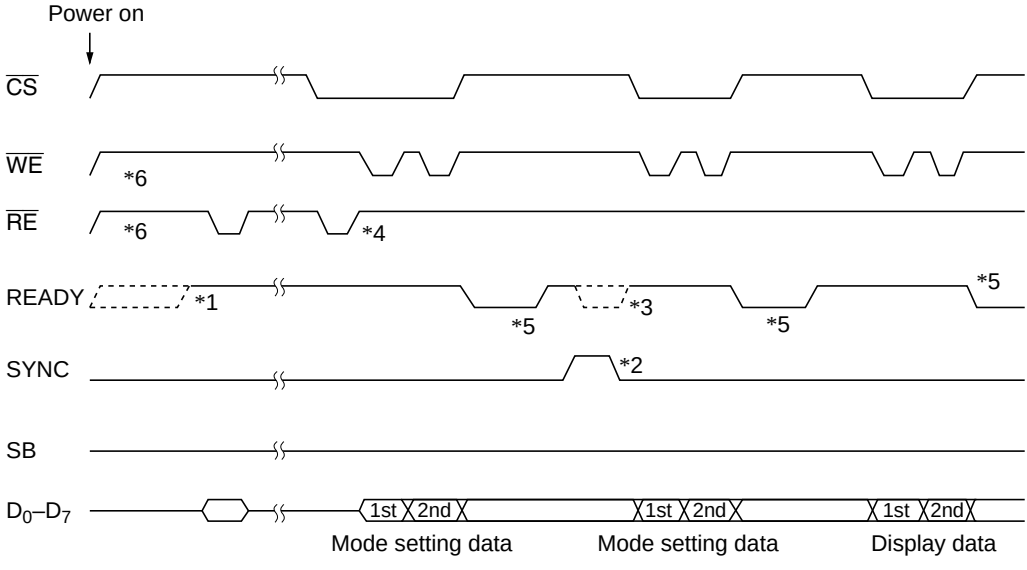
How to Input HD61602 Data

Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ inputs low (no display data changes).
2. Input 2 or more "1-byte instruction" data in which bit 7 and 6 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 16.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
2. High pulse should be applied to SYNC terminal when using two or more chips synchronously.
3. In the mode in which READY is always available, READY output is in definite while SYNC is high.
4. Reset the byte counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 16 Example of Data Transfer Sequence

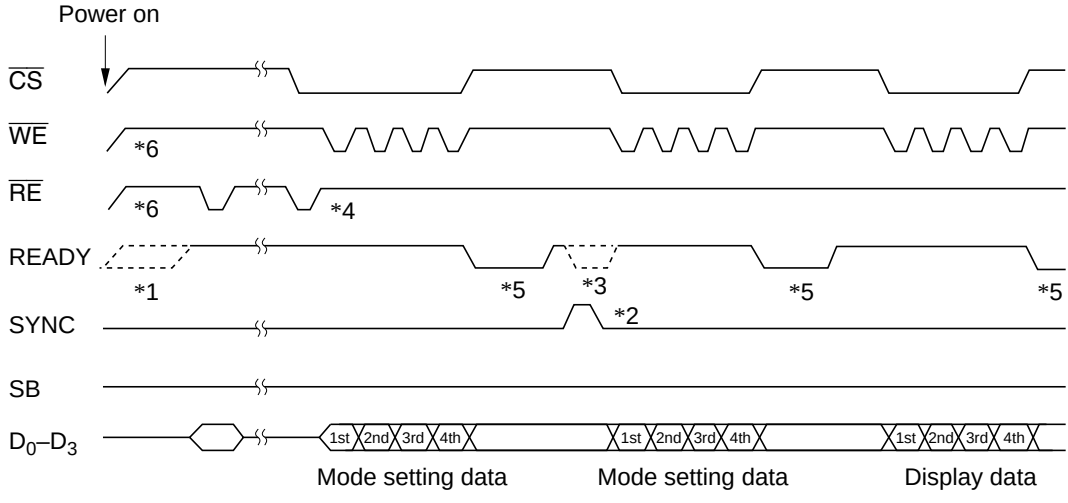
How to Input HD61603 Data

Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted, because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ low.
2. Input 4 or more "1-byte instruction" data (4-bit data) in which bit 3 and 2 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 17.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
2. High pulse should be applied to SYNC terminal when using two or more chips synchronously.
3. In the mode in which READY is always available, READY output is in definite while SYNC is high.
4. Reset the 4-bit data counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 17 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes:

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 18 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

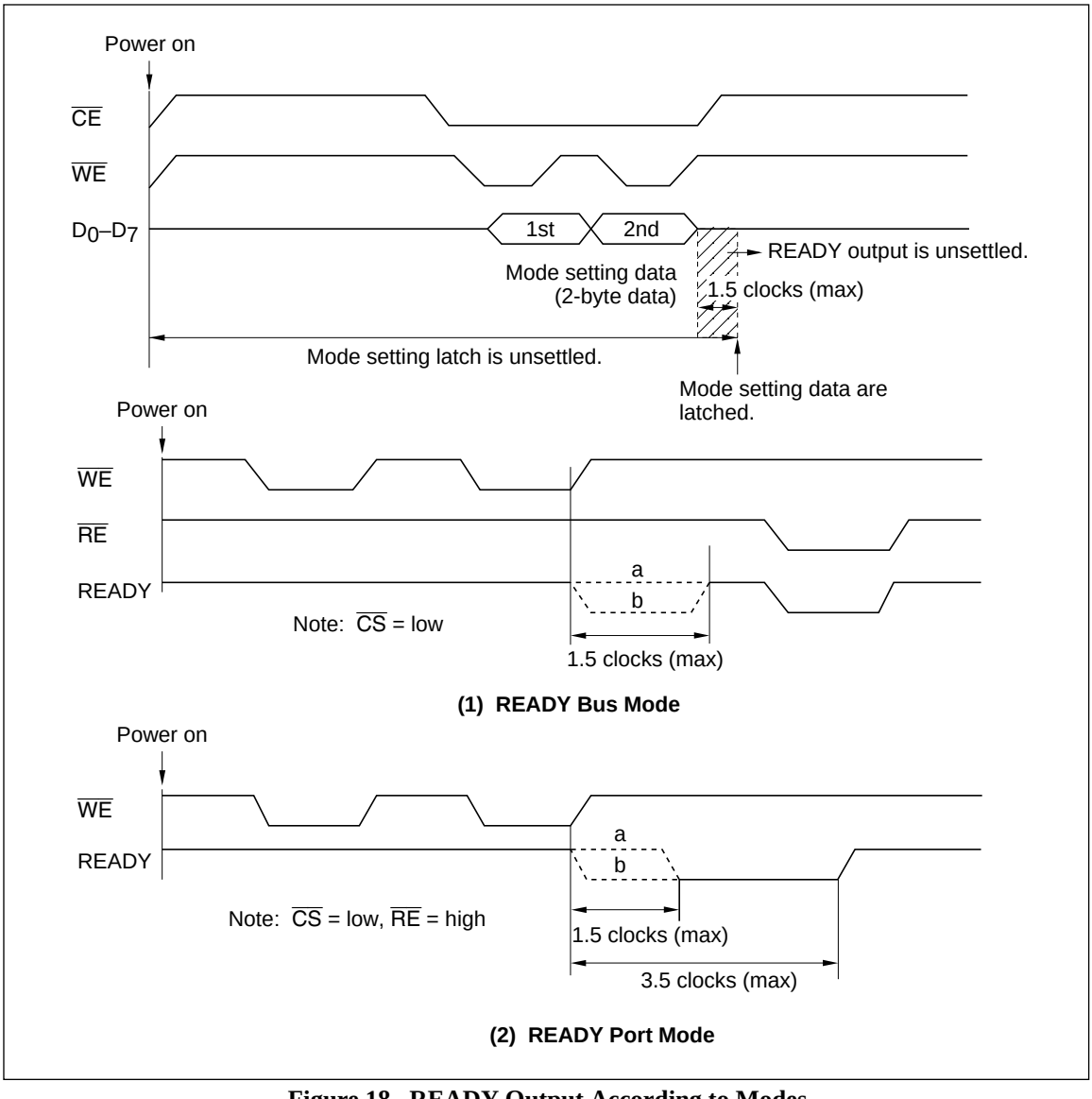


Figure 18 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See 3. Mode Setting Data in “Input Data Formats”.) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, a high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise by-pass capacitor ($\geq$ 1 µF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages (figure 19); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

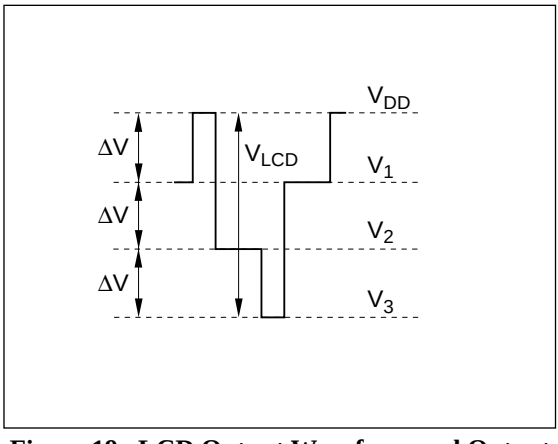


Figure 19 LCD Output Waveform and Output Levels

When Internal Drive Power Supply Is Used

When the internal drive power supply is used, attach C_1–C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 20.

Internal voltage is available by setting external voltage switching bits of mode setting data 0.

Figure 21 shows voltage characteristics between V_{DD} and V_{REF1}. Voltage is divided at R_1, and then input into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 21, and so V_{LCD} can be changed by regulating the voltage.

V_{REF2} is usually regulated by variable resistance, but when replacing R_1 with two nonvariable resistances take V_{REF1} between max and min into consideration as shown in figure 21.

Internal drive power supply is generated by using capacitance, and so large current cannot flow. When large liquid crystal display panel is used, examine the external drive power supply.

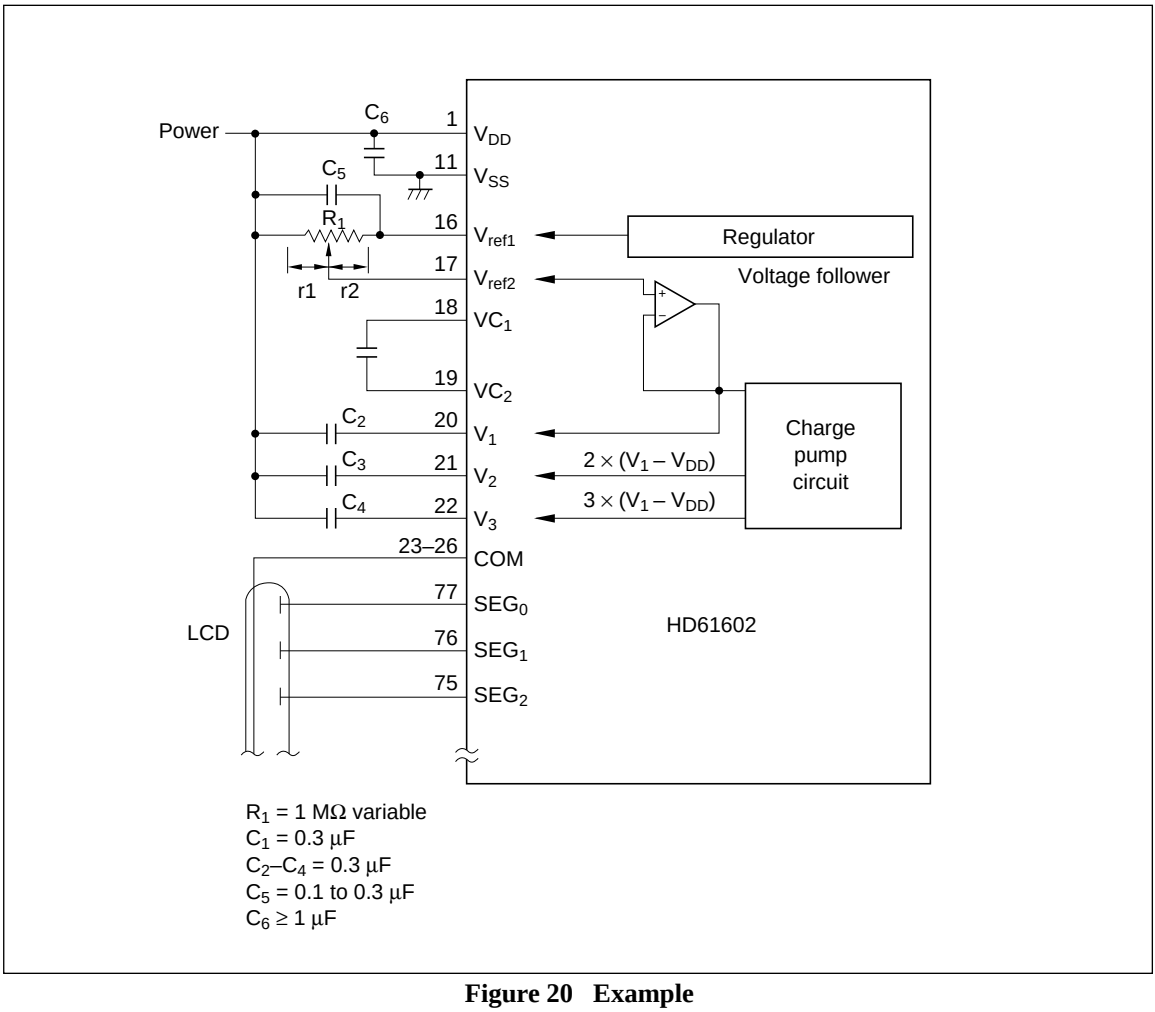


Figure 20 Example

When External Drive Power Supply Is Used

An external power supply can be used by setting external voltage switching bits of mode setting data to 1. When a large liquid crystal display panel is used, in multichip designs, which need accurate liquid crystal drive voltage, use the external power supply. See figure 22.

R_2–R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2, and V_3. C_2–C_4 are smoothing capacitors.

When regulating brightness, change the resistance value by setting R_5 variable resistance.

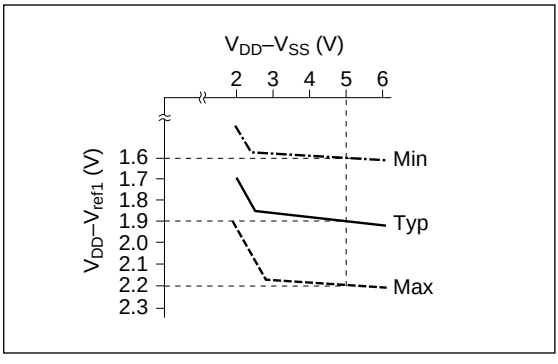
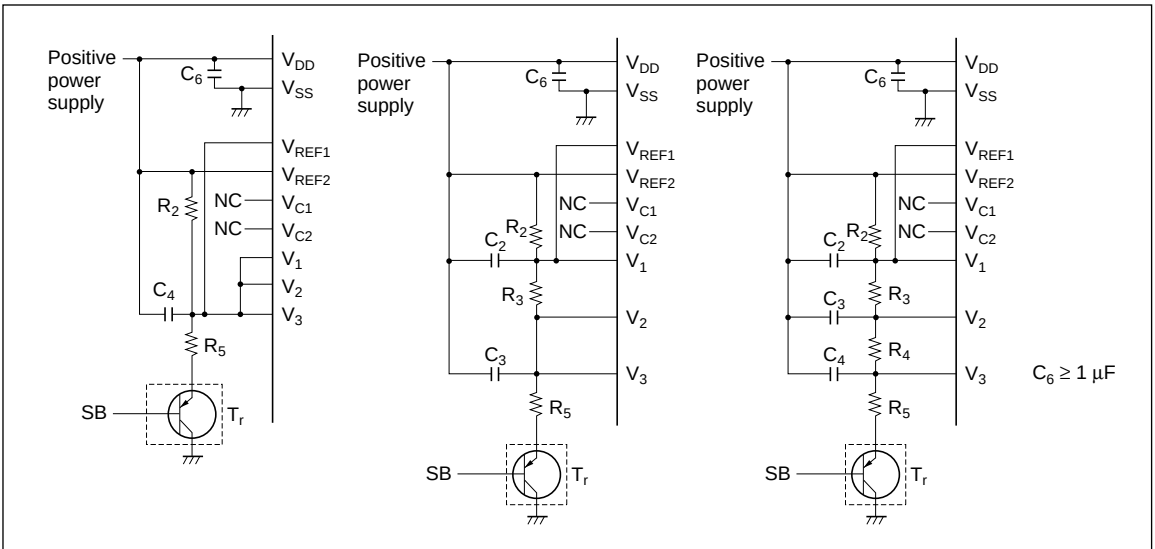


Figure 21 Voltage Characteristics between V_{DD} and V_{ref1}



Notes: 1. When standby mode is used, a transistor is required.
2. R_2–R_5 should be some kΩ–some tens of kΩ, and C_2–C_4 should be 0.1 µF–0.3 µF.

Figure 22 Example when External Drive Voltage Is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 23, apply LCD drive voltage from the external power supply.

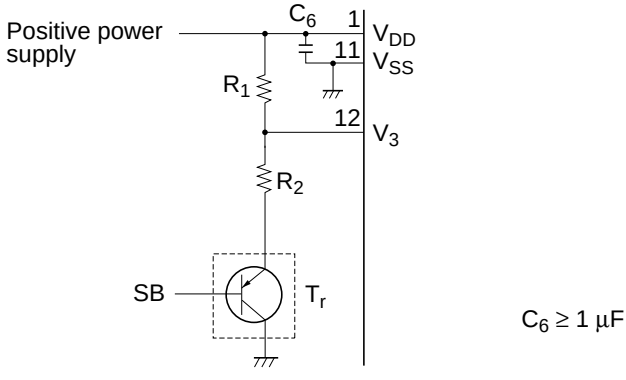
Oscillation Circuit

When Internal Oscillation Circuit Is Used

When the internal oscillation circuit is used, attach an external resister R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC_1 side shorter.)

When External Clock Is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC_1 can be used for the input pin. In this case, open pin OSC_2.



Note: When standby mode is used, a transistor is required.

Figure 23 Example of Drive Voltage Generator

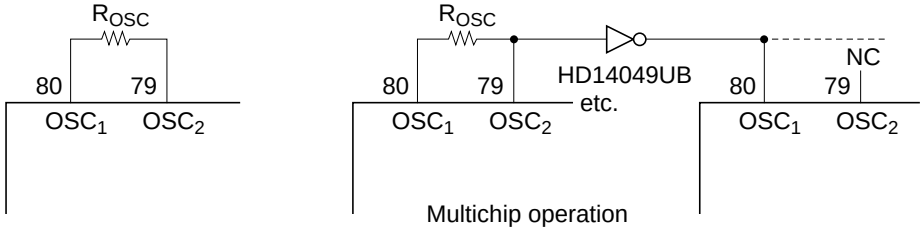


Figure 24 Example of Oscillation Circuit

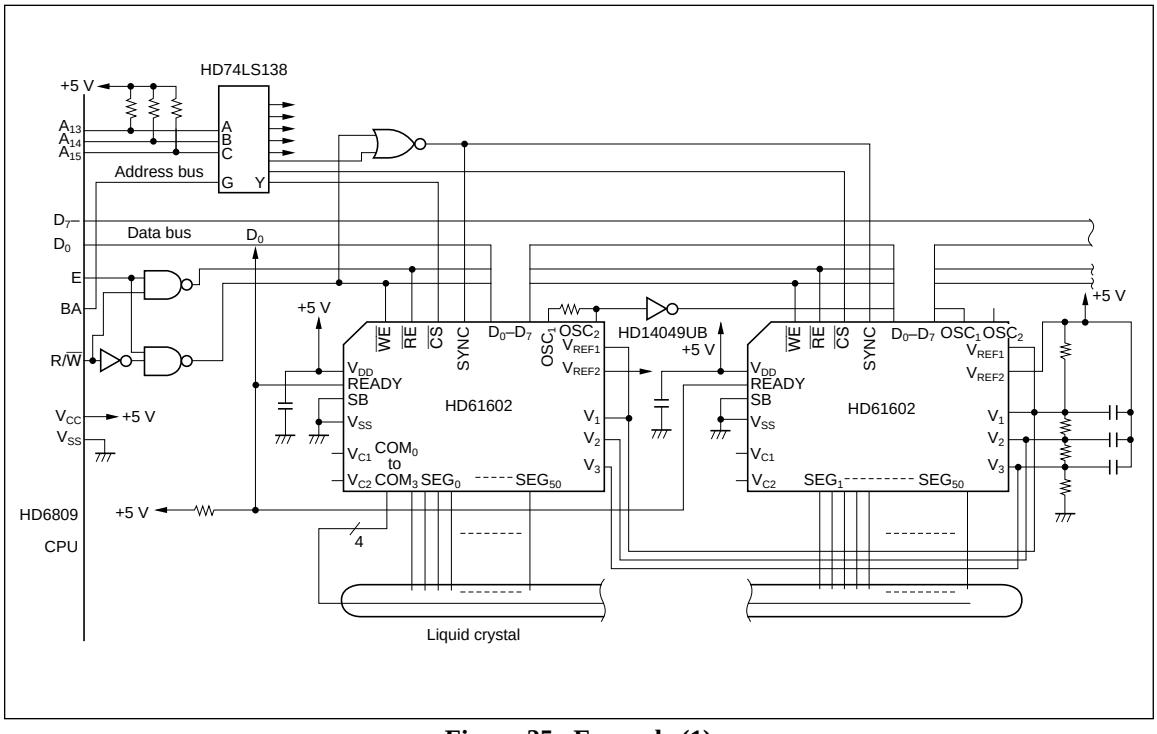


Figure 25 Example (1)

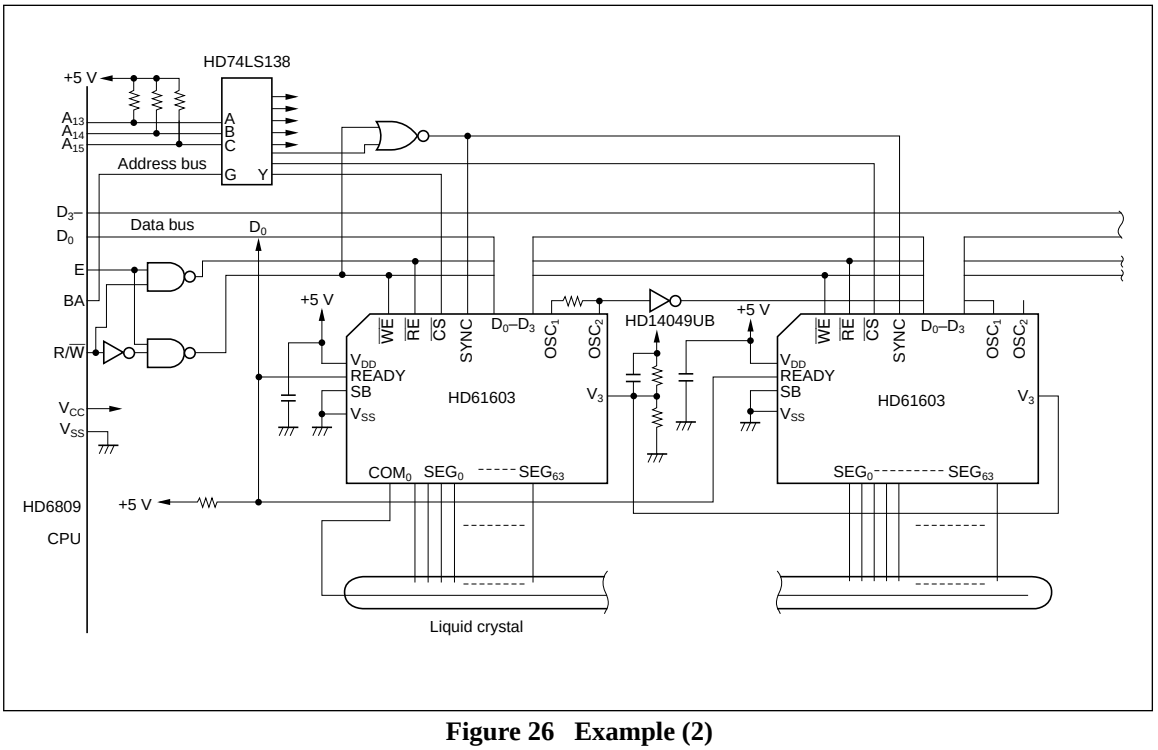


Figure 26 Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	–0.3 to +7.0	V
Terminal voltage*	V_T	–0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

		Limit			
Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	2.2	—	5.5	V
	V_1, V_2, V_3	0	—	V_{DD}	V
Terminal voltage*	V_T	0	—	V_{DD}	V
Operating temperature	T_{opr}	–20	—	75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics (1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC_1	V_{IH1}	0.8 V_{DD}	—	V_{DD}	V	
	Others	V_{IH2}	2.0	—	V_{DD}	V	
Input low voltage	OSC_1	V_{IL1}	0	—	0.2 V_{DD}	V	
	Others	V_{IL2}	0	—	0.8	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	V0 = V_{DD}
Output low voltage	READY	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
Input leakage current*1	Input terminal	I_{IL1}	–1.0	—	1.0	µA	V_{IN} = 0–V_{DD}
	V_1	I_{IL2}	–20	—	20	µA	V_{IN} = V_{DD}–V_3
	V_2, V_3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	—	—	0.3	V	±Id = 3 µA for each COM, V_3 = V_{DD}–3 V
	SEG_0–SEG_{50}	V_{d2}	—	—	0.6	V	±Id = 3 µA for each SEG, V_3 = V_{DD}–3 V
Power supply current		I_{DD}	—	—	100	µA	During display*2 R_{OSC} = 360 kΩ
		I_{DD}	—	—	5	µA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	—	—	0.4	V	V_{REF2} = V_{DD}–1 V, C_1–C_4 = 0.3 µF, RL = 3 MΩ

Notes: 1. V_1, V_2: apply only to HD61602.
2. Except the transfer operation of display data and bit data.

DC Characteristics (2) (V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
Input high voltage		V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
Input low voltage		V_{IL}	0	—	0.1 V_{DD}	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	V_{IN} = V_{DD}
Output low voltage	READY	V_{OL}	—	—	0.1 V_{DD}	V	I_{OL} = 0.04 mA
Input leakage current*1	Input terminal	I_{IL1}	–1.0	0	1.0	µA	V_{IN} = 0–V_{DD}
	V_1	I_{IL2}	–20	—	20	µA	V_{IN} = V_{DD}–V_3
	V_2, V_3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	—	—	0.3	V	±Id = 3 µA for each COM, V_3 = V_{DD}–3 V
	SEG_0–SEG_{50}	V_{d2}	—	—	0.6	V	±Id = 3 µA for each SEG, V_3 = V_{DD}–3 V
Power supply current		I_{SS}	—	—	50	µA	During display*2 R_{OSC} = 330 kΩ
		I_{SS}	—	—	5	µA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	—	—	0.4	V	V_{REF2} = V_{DD}–1 V, C_1–C_4 = 0.3 µF, RL = 3 MΩ, V_{DD} = 3–3.8 V

Notes: 1. V_1, V_2: apply only to HD61602.
2. Except the transfer operation of display data and bit data.

AC Characteristics (1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc} = 360 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing		t_S	400	—	—	ns	
		t_H	10	—	—	ns	
		t_{WH}	300	—	—	ns	
		t_{WL}	400	—	—	ns	
		t_{WR}	400	—	—	ns	
		t_{DL}	—	—	1.0	µs	Figure 31
		t_{EN}	400	—	—	ns	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

AC Characteristics (2) (V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc} = 330 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing (V_{DD} = 3.0–3.8 V)		t_S	1.5	—	—	µs	
		t_H	1.0	—	—	µs	
		t_{WH}	1.5	—	—	µs	
		t_{WL}	1.5	—	—	µs	
		t_{DL}	—	—	2.0	µs	Figure 32
		t_{WR}	1.5	—	—	µs	
		t_{EN}	2.0	—	—	µs	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

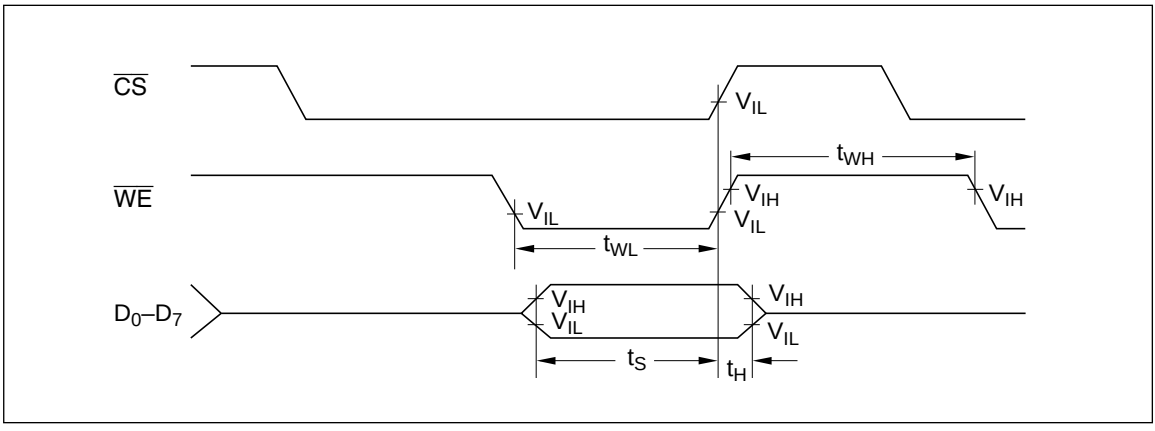


Figure 27 Write Timing ($\overline{RE}$ Is Fixed at High Level, and SYNC at Low Level)

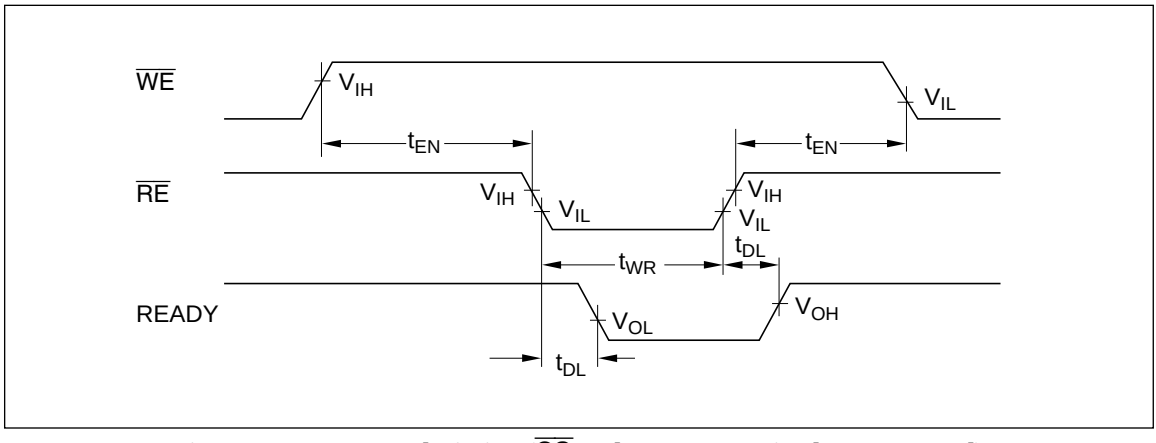


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC Are Fixed at Low Level)

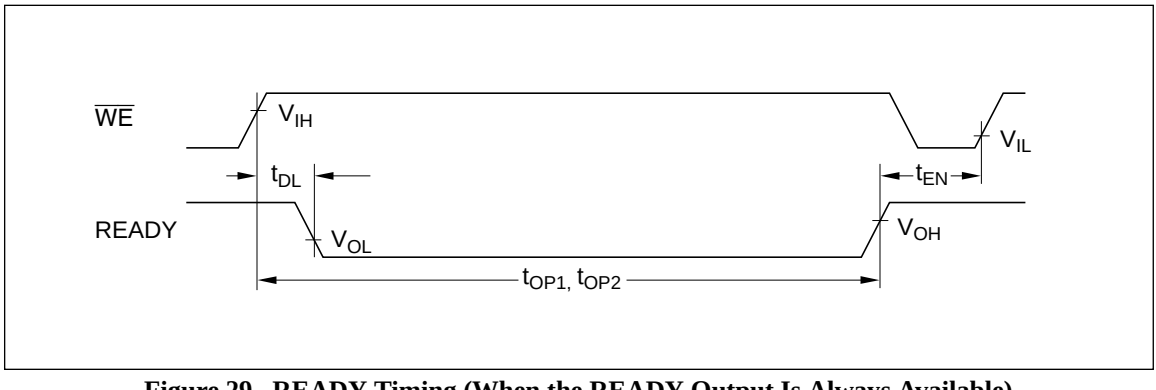


Figure 29 READY Timing (When the READY Output Is Always Available)

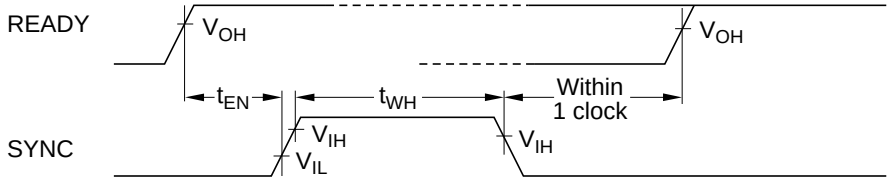


Figure 30 SYNC Timing

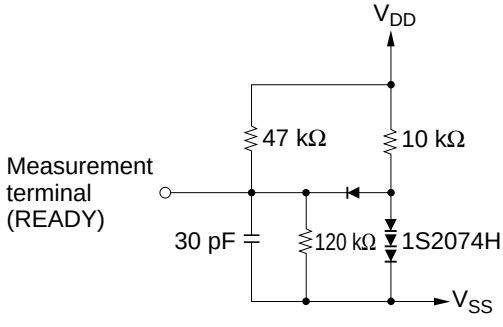


Figure 31 Bus Timing Load Circuit (LS-TTL Load)

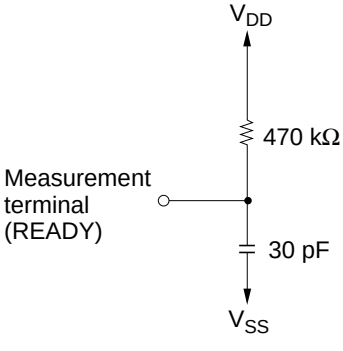


Figure 32 Bus Timing Load Circuit (CMOS Load)