HD61102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

HITACHI

Description

HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-controller in internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61102, which is produced by the CMOS process, can complete a portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61103A.

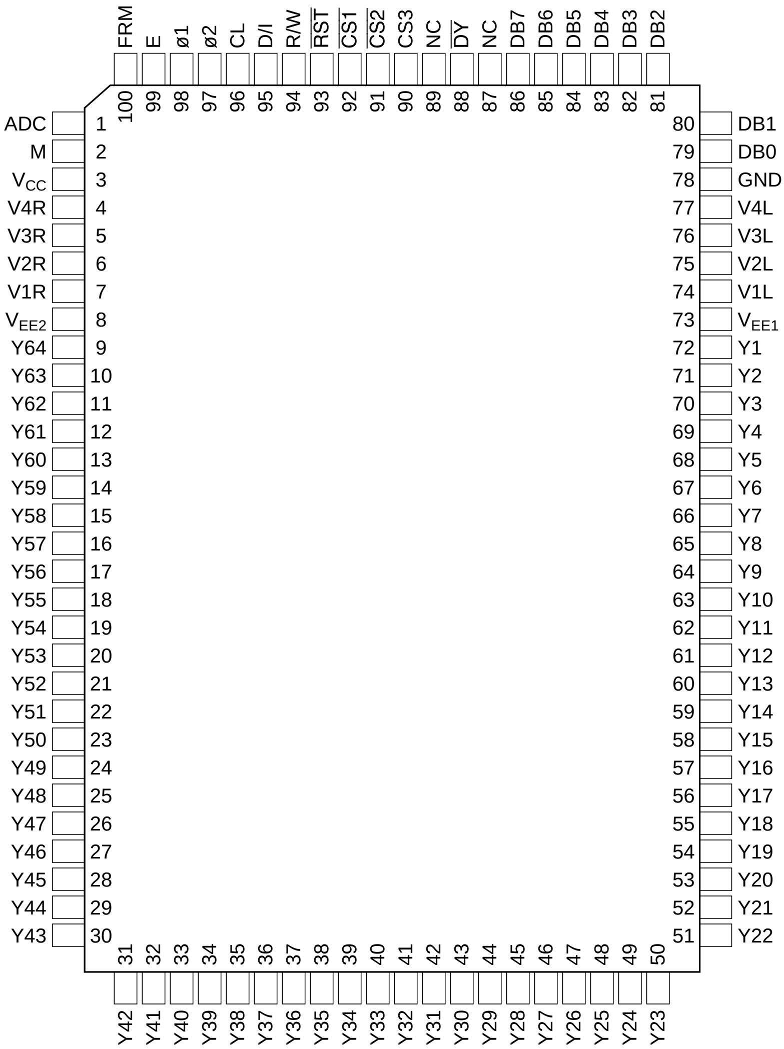
Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Internal display RAM address counter: Preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty:
  - Combination of frame control signal and data latch synchronization signal make it possible to select static or optional duty cycle
- Wide range of instruction function:
  - Display data read/write, display on/off, set address, set display start line, read status
- Lower power dissipation: during display 2 mW max
- Power supply
  - V_{CC}: +5 V ± 10%
  - V_{EE}: 0 V to –10 V
- Liquid crystal display driving level: 15.5 V max
- CMOS process

Ordering Information

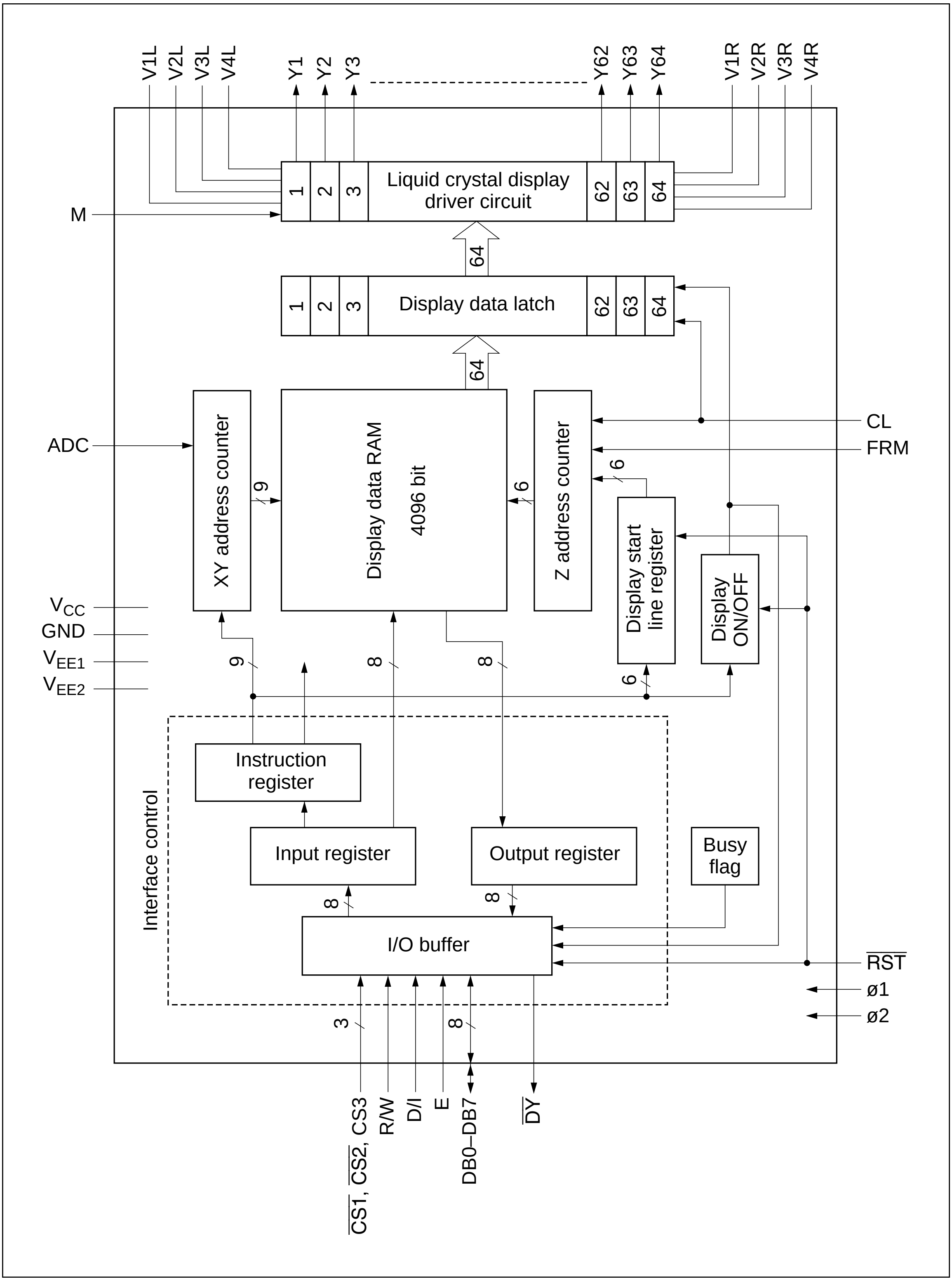
Type No.	Package
HD61102RH	100-pin plastic QFP (FP-100)

Pin Arrangement



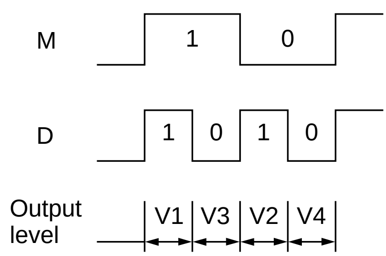
(Top view)

Block Diagram



Terminal Functions

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>V_{CC}
GND</td><td>2</td><td></td><td>Power supply</td><td>Power supply for internal logic.
Recommended voltage is:
GND = 0 V
V_{CC} = +5 V ± 10%</td></tr>
<tr><td>V_{EE1}
V_{EE2}</td><td>2</td><td></td><td>Power supply</td><td>Power supply for liquid crystal display drive circuit.
Recommended power supply voltage is V_{CC} –15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}.
V_{EE1} and V_{EE2} are not connected to each other in the LSI.</td></tr>
<tr><td>V1L, V1R
V2L, V2R
V3L, V3R
V4L, V4R</td><td>8</td><td></td><td>Power supply</td><td>Power supply for liquid crystal display drive.
Apply the voltage specified for the liquid crystals within the limit of V_{EE} through V_{CC}.
V1L (V1R), V2L (V2R): Selected level
V3L (V3R), V4L (V4R): Non-selected level
Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.</td></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
CS3</td><td>3</td><td>I</td><td>MPU</td><td>Chip selection
Data can be input or output when the terminals are in the following conditions:<table><tr><th>Terminal name</th><th>$\overline{CS1}$</th><th>$\overline{CS2}$</th><th>CS3</th></tr><tr><td>Condition</td><td>L</td><td>L</td><td>H</td></tr></table></td></tr>
<tr><td>E</td><td>1</td><td>I</td><td>MPU</td><td>Enable
At write (R/W = low): Data of DB0 to DB7 is latched at the fall of E.
At read (R/W = high): Data appears at DB0 to DB7 while E is high.</td></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>MPU</td><td>Read/write
R/W = High: Data appears at DB0 to DB7 and can be read by the MPU when E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
R/W = Low: DB0 to DB7 accepted at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.</td></tr>
<tr><td>D/I</td><td>1</td><td>I</td><td>MPU</td><td>Data/instruction
D/I = High: Indicates that the data of DB0 to DB7 is display data.
D/I = Low: Indicates that the data of DB0 to DB7 is display control data.</td></tr>
</table>

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1–$0, Y64–$63 ADC = Low: Y64–$0, Y1–$63
DB0–DB7	8	I/O	MPU	Data bus, three-state I/O common terminals.
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Synchronous signal to latch display data. The rising edge of the CL signal increments the display output address counter and latches the display data.
ø1, ø2	1	I	HD61103A	2-phase clock signal for internal operation. The ø1 and ø2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1–Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins output light on level when 1 is in the display RAM, and light off level when 0 is in it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	MPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level: 1. On/off register set to 0 (display off) 2. Display start line register set to line 0 (displays from line 0) After releasing reset, this condition can be changed only by instruction.
$\overline{DY}$	1	O	Open	Output terminal for test. Normally, don’t connect any lines to this terminal.
NC	2		Open	Unused terminals. Don’t connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

I/O Buffer: Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (most significant bit)
DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, that is namely, the internal state is maintained and no instruction executes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

Register: Both input register and output register are provided to interface to MPU whose the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

1. Input Register

   The input register is used to store data temporarily before writing it into display data RAM. The data from MPU is written into input register, then into display data RAM automatically by internal operation.

   When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of E signal.

2. Output Register

   The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. The read display data instruction outputs data stored in the output register while E is high. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

   Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 1 shows the MPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register).
1	0	Writes data into input register as internal operation (input register → display data RAM).
0	1	Busy check. Read of status data.
0	0	Instruction.

Busy Flag

Busy flag = 1 indicates that HD61102 is operating and no instructions except status read can be accepted (figure 2). The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing an instruction.

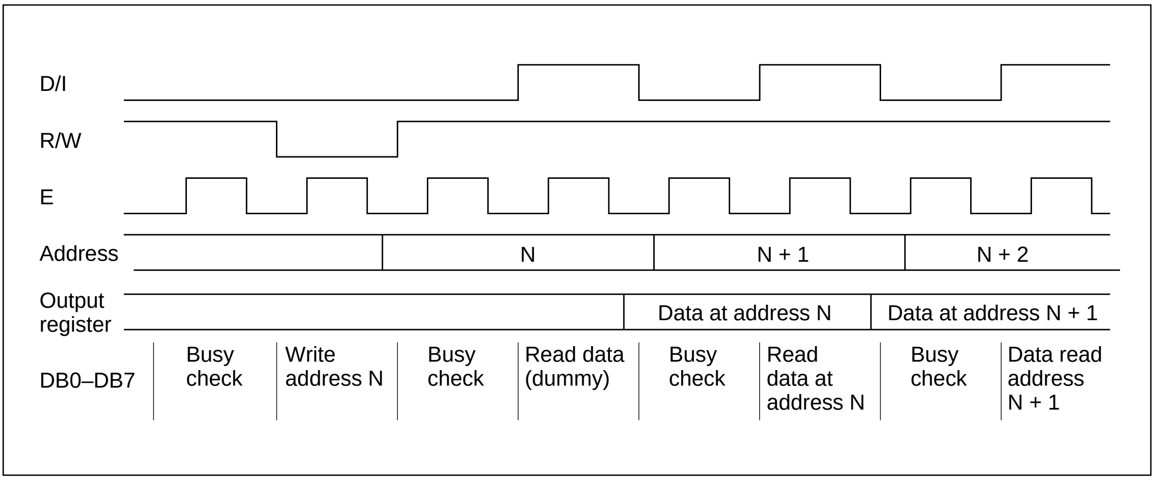


Figure 1 MPU Read Timing

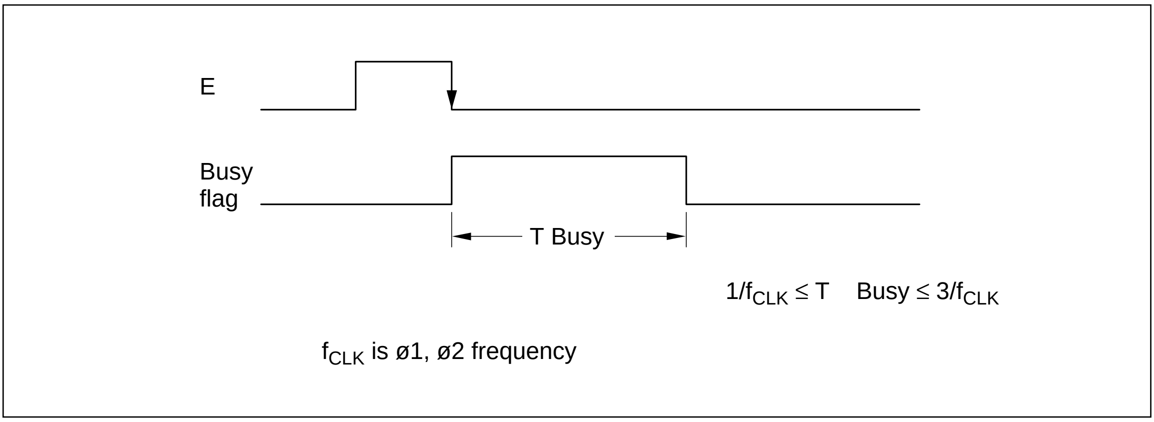


Figure 2 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by the display on/off instruction. $\overline{\mathrm{RST}}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by the status read instruction. The display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, C1 signal (display synchronous signal) should be input correctly.

Display Start Line Register

The register specifies a line in RAM that corresponds to the top line of the LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling the screen.

6-bit display start line information is written into this register by the display start line set instruction, with high level of FRM signal signalling the start of the display, the information in this register is transferred to the Z address counter, which controls the display address, and the Z address counter is preset.

X, Y Address Counter

A 9-bit counter that designates addresses of internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set by the respective instructions.

1. X Address Counter

   Ordinary register with no count functions. An address is set by instruction.

2. Y Address Counter

   An Address is set by instruction and it is increased by 1 automatically by display data R/W operations. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

As the ADC signal controls the Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, always connect ADC pin to V_{CC} or GND when using.

Figure 3 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

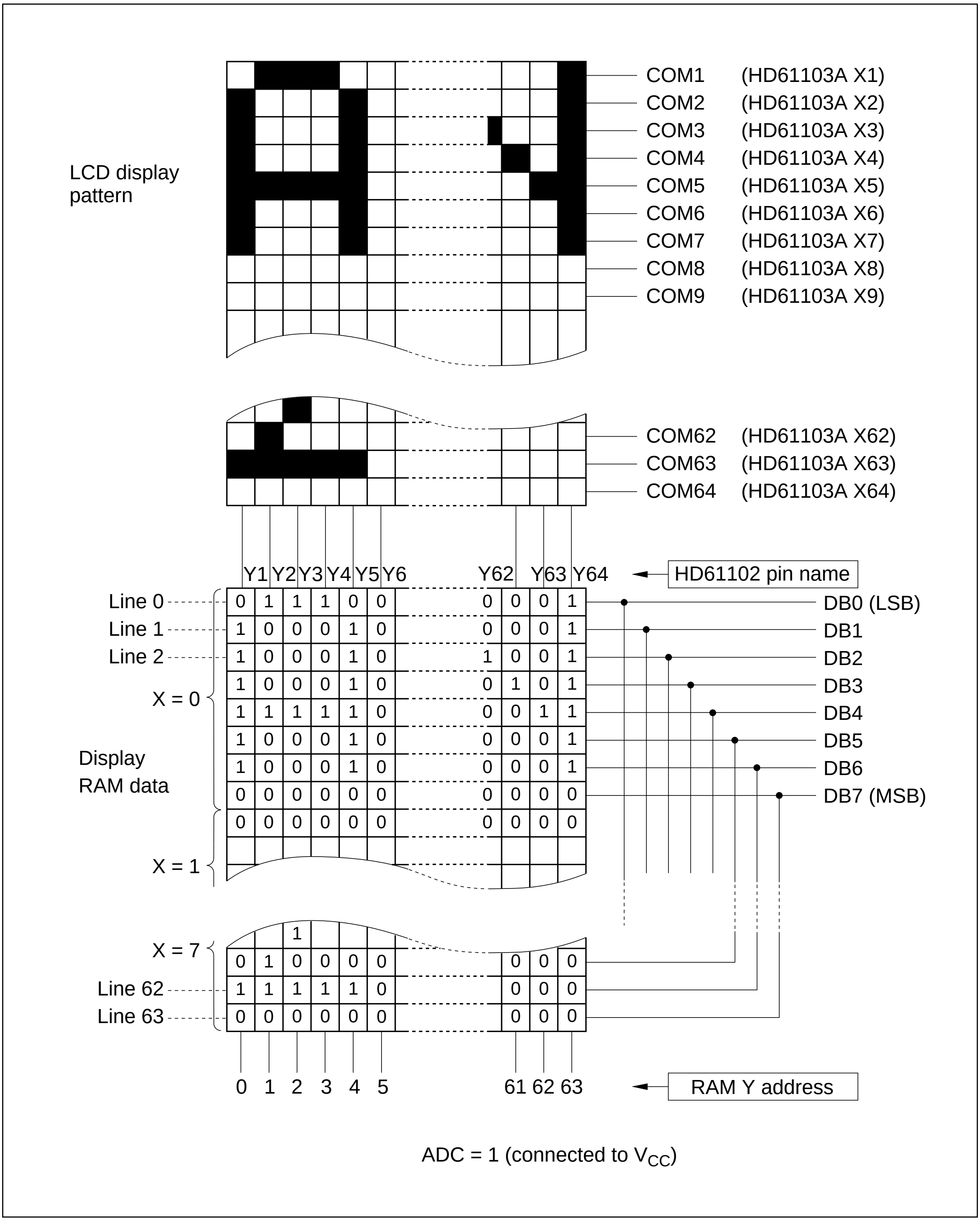


Figure 3 Relation between RAM Data and Display

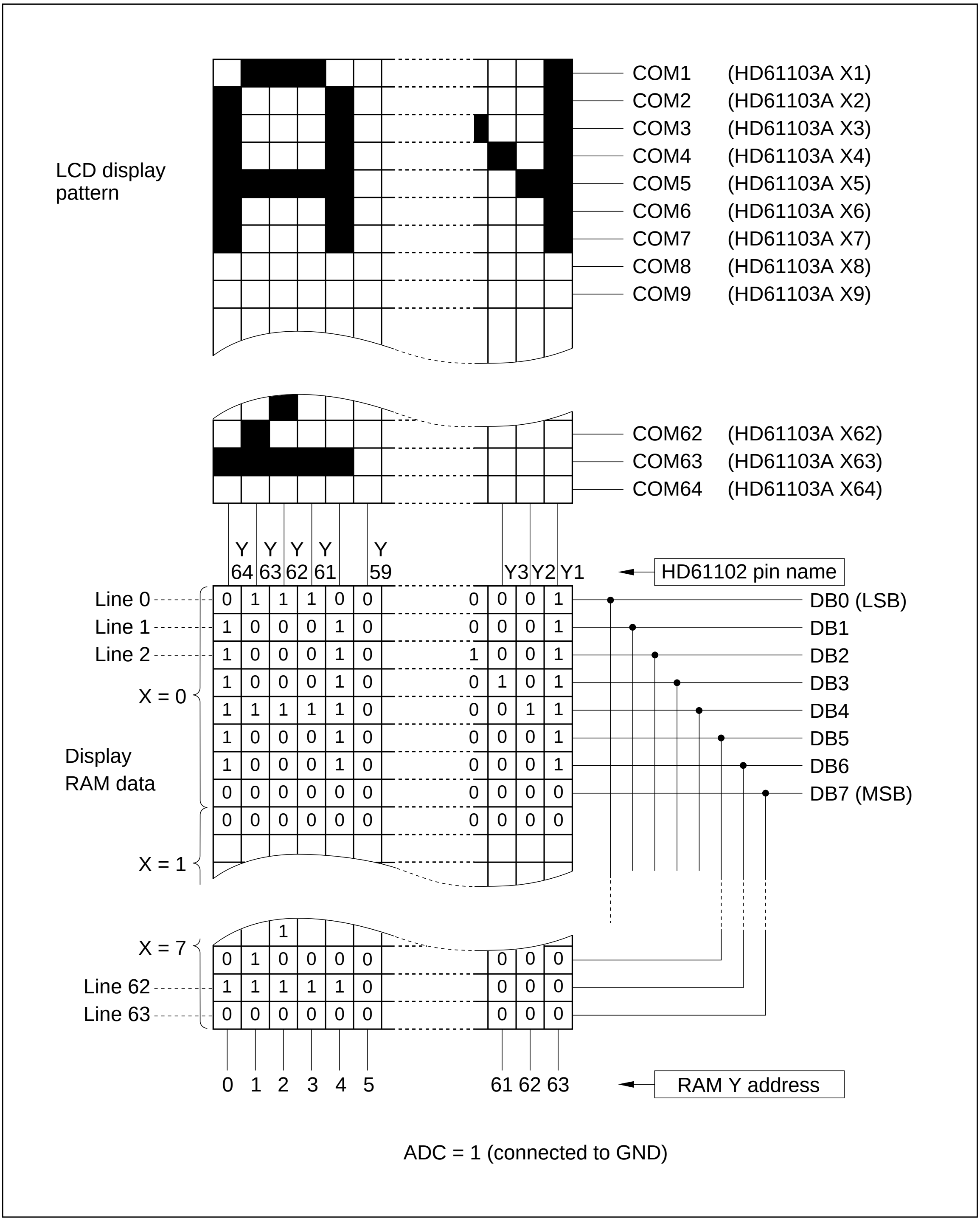


Figure 3 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At FRM high, the contents of the display start line register are preset in the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit.

Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{\text{RST}}$ terminal to low when turning power on.

1. Display off
2. Set display start line register line 0

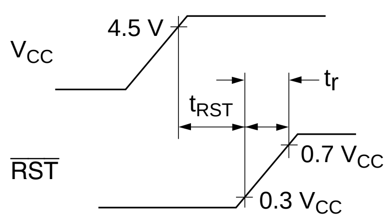
While $\overline{\text{RST}}$ is low level, no instruction except status read can be accepted. Therefore, carry out other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.

The conditions of the power supply at initial power up are as in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.

These explanations are detailed in the following pages. Generally, there are the following three kinds of instructions.

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction are used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than the status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is the proof that an instruction is not being executed.

Table 3 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.	
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.	
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM in the page (X address) register.	
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.	
Status read	1	0	Busy	0	ON/ OFF	RE- SET	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Executing internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note: 1. Busy time varies with the frequency (f_{CLK}) of ø1, and ø2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display On/Off

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen when D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display Start Line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen.

Figure 4 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Set Page (X Address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 5.

Set Y Address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7							DB0
Code	1	0	Busy	0	ON/OFF	RESET	0	0	0	0
			MSB							LSB

- Busy

  When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

- ON/OFF

  Shows the liquid crystal display conditions: on condition or off condition.

  When ON/OFF is 1, the display is in off condition.
  When ON/OFF is 0, the display is in on condition.

- RESET

  RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

  RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

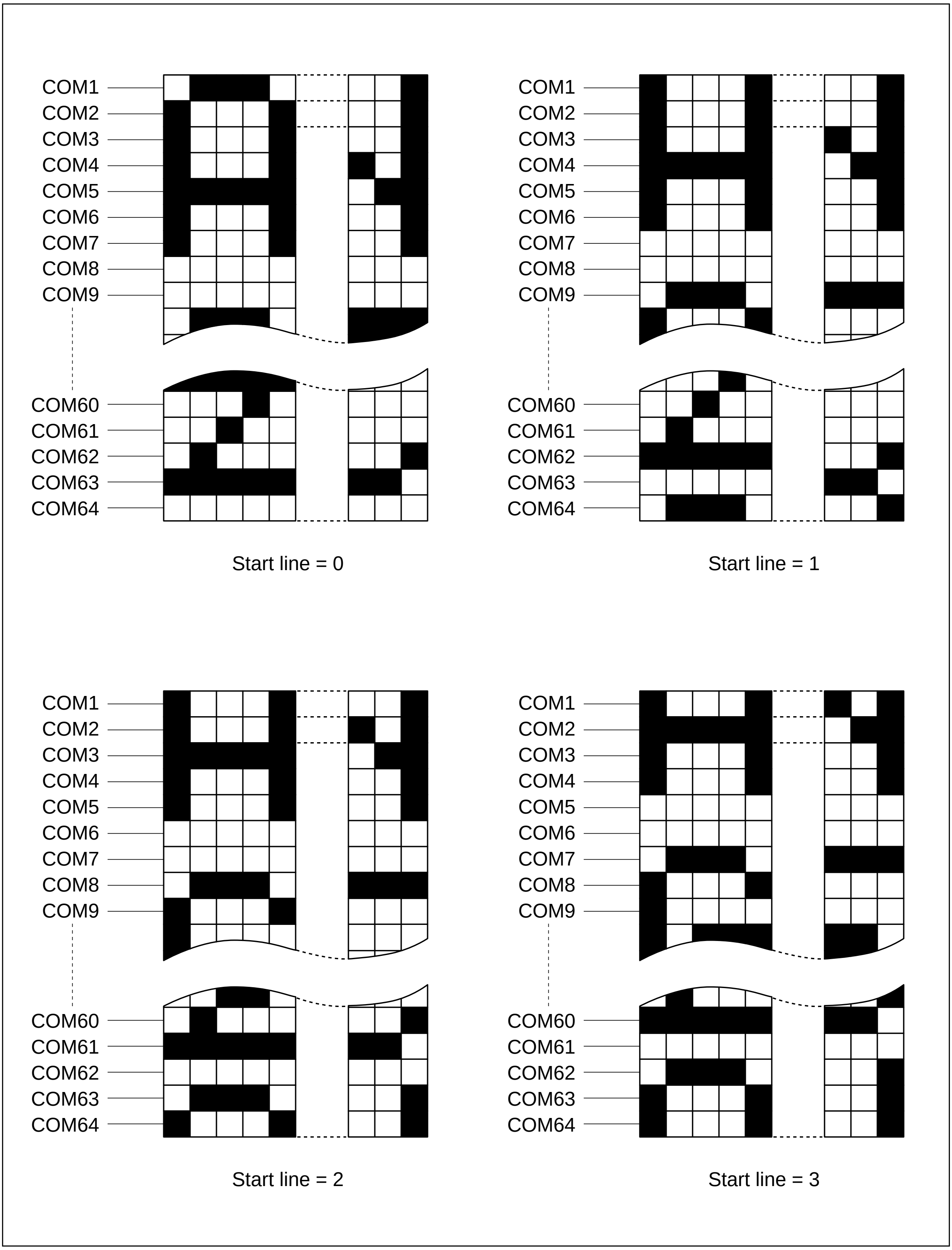


Figure 4 Relation between Start Line and Display

Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D
			MSB							LSB

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.

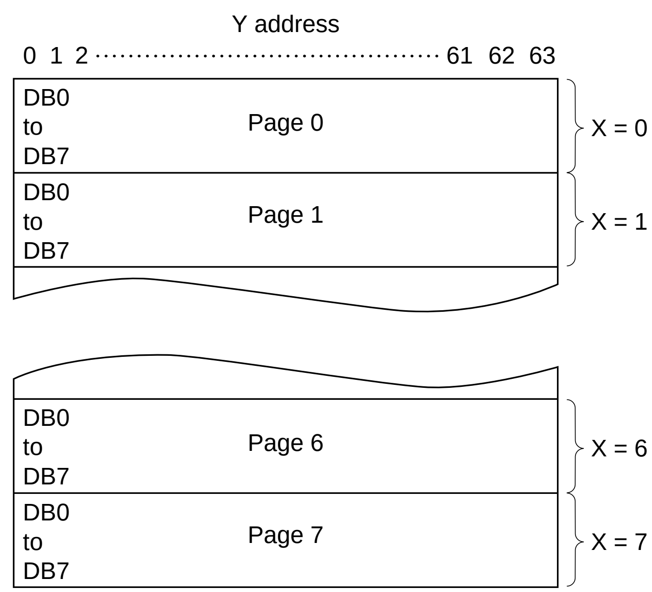
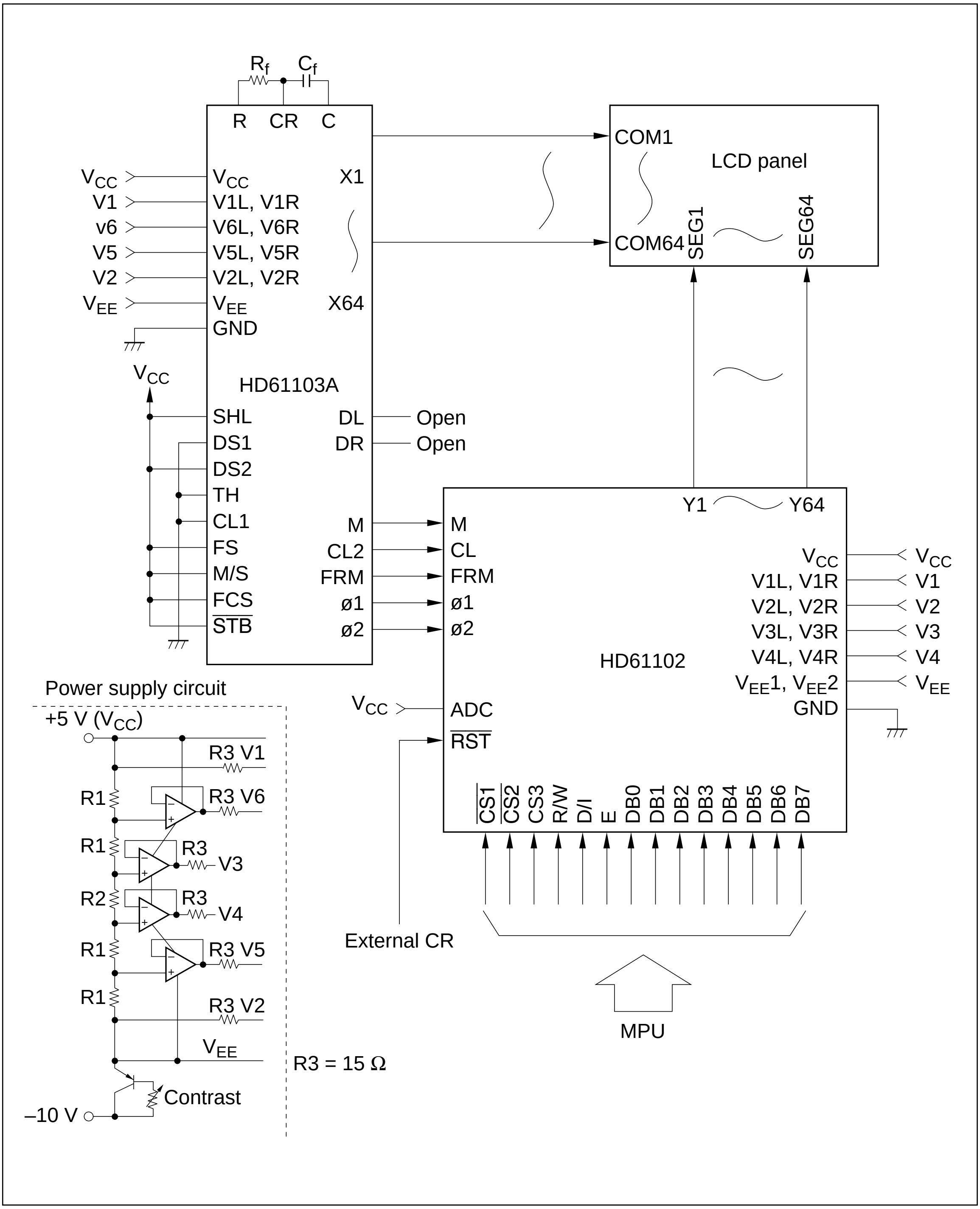
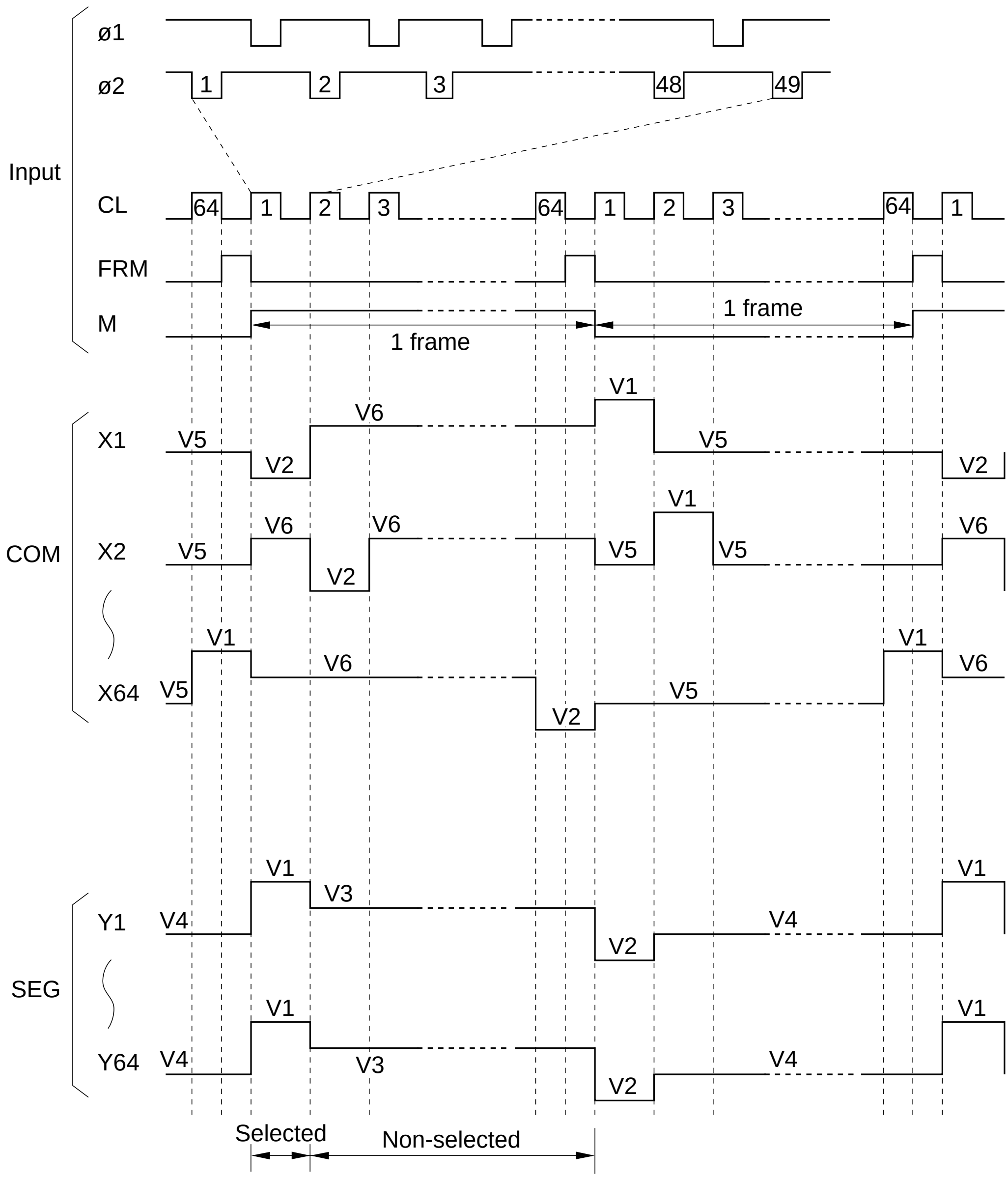


Figure 5 Address Configuration of Display Data RAM

Use of HD61102

Interface with HD61103A (1/64 Duty Cycle)





The waveforms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Figure 6 LCD Driver Timing Chart (1/64 Duty Cycle)

Interface with CPU

Example of Connection with HD6800

In this decoder (figure 7), addresses of HD61102 in the address area of HD6800 are:

Read/write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61102 by reading/writing the data at these addresses.

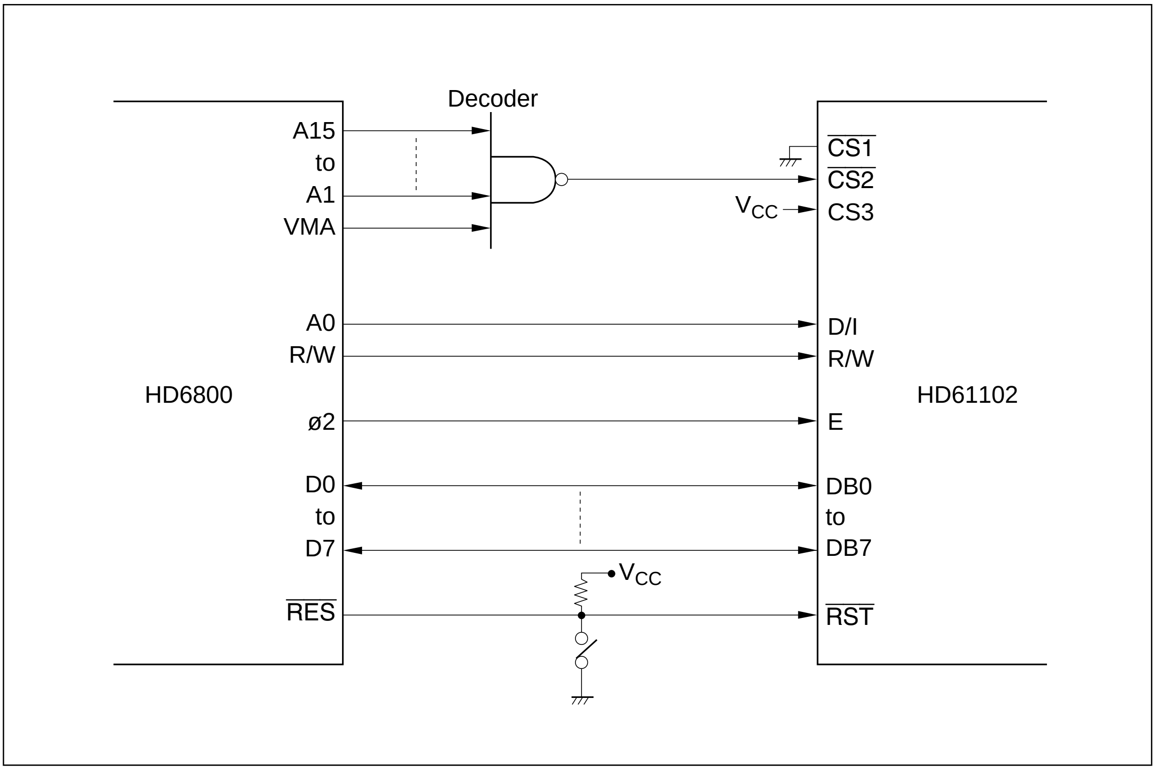


Figure 7 Example of Connection with HD6800 Series

Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus (figure 8).
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

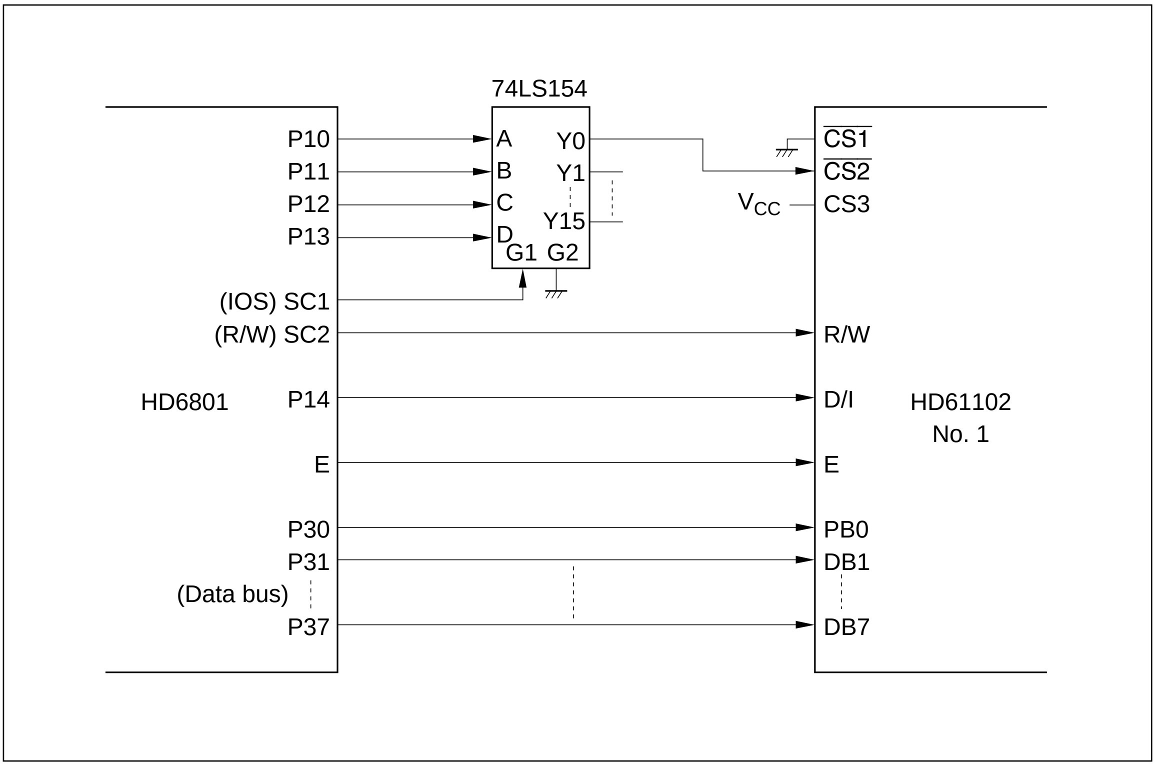


Figure 8 Example of Connection with HD6801

Example of Application

In this example (figure 9), two HD61103As output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

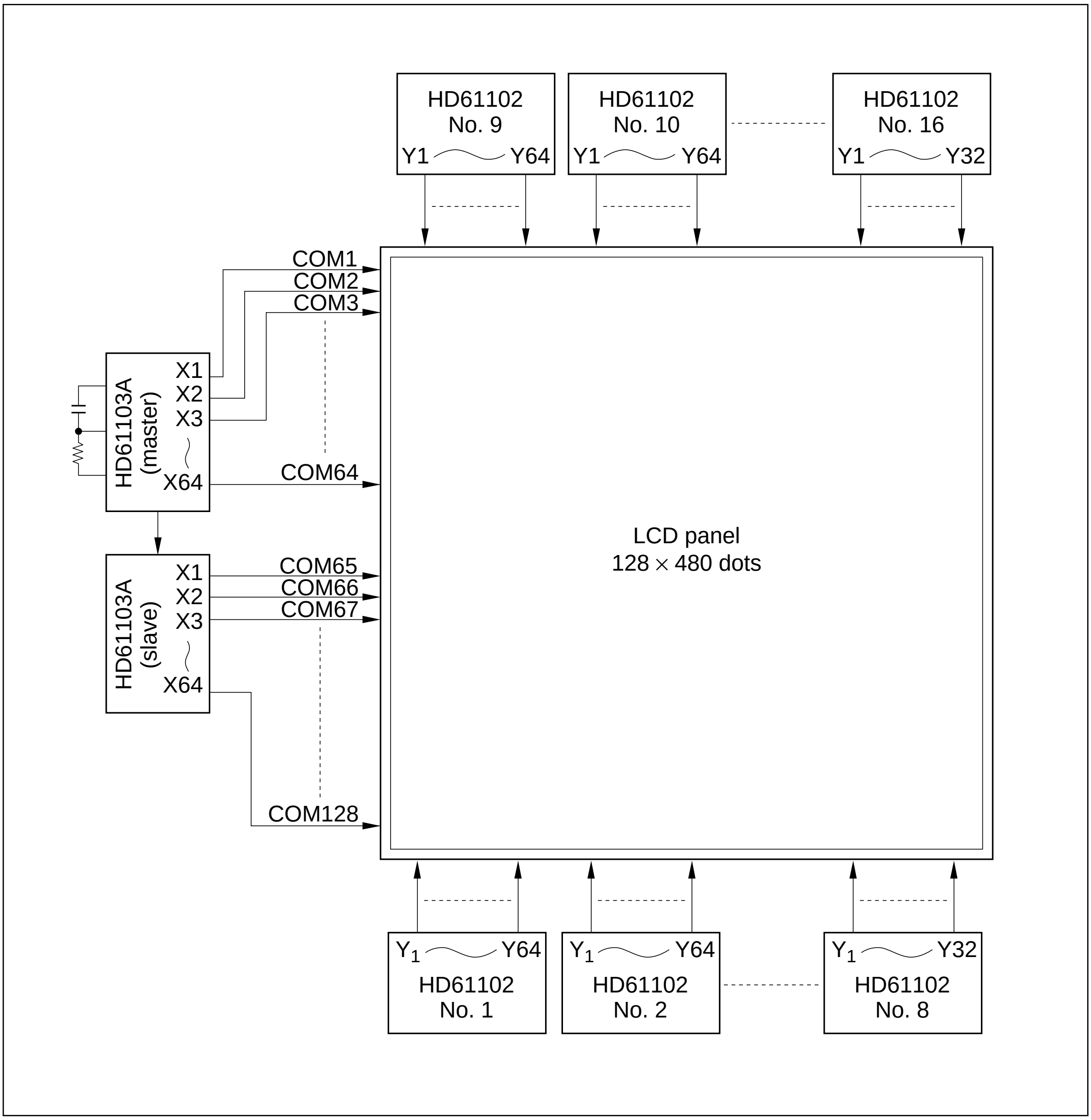


Figure 9 Application Example

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1}, V_{EE2}	V_{CC} – 16.5 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operating conditions. Use beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
   Maintain
   $V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC, and DB0–DB7.

Electrical Characteristics (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition	Notes
Input high voltage	V_{IHC}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	$0.3 \times V_{CC}$	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND – V_{CC}	4
High impedance off input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND – V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} – V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	V_{CC} – V_{EE} = 15 V $\pm I_{LOAD}$ = 0.1 mA	7
Dissipation current	$I_{CC}(1)$	—	—	100	µA	During display	8
	$I_{CC}(2)$	—	—	500	µA	During access Access cycle = 1 MHz	8

Notes: 1. Applies to M, FRM, CL, $\overline{RST}$, ø1, ADC, and ø2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to input terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Applies to Y1–Y64.
7. Specified when liquid crystal display is in 1/64 duty.

Operation frequency: f_{CLK} = 250 kHz (ø1 and ø2 frequency)
Frame frequency: f_M = 70 Hz (FRM frequency)

Specified in the state of

Output terminal: Not loaded
Input level: $V_{IH} = V_{CC}$ (V)
V_{IL} = GND (V)

Measured at V_{CC} terminal

Interface AC Characteristics

MPU Interface (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
E cycle time	t_{CYC}	1000	—	—	ns	Fig. 10, Fig. 11
E high level width	P_{WEH}	450	—	—	ns	
E low level width	P_{WEL}	450	—	—	ns	
E rise time	t_r	—	—	25	ns	
E fall time	t_f	—	—	25	ns	
Address setup time	t_{AS}	140	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data setup time	t_{DSW}	200	—	—	ns	Fig. 10
Data delay time	t_{DDR}	—	—	320	ns	Fig. 11, Fig. 12
Data hold time (write)	t_{DHW}	10	—	—	ns	Fig. 10
Data hold time (read)	t_{DHR}	20	—	—	ns	Fig. 11

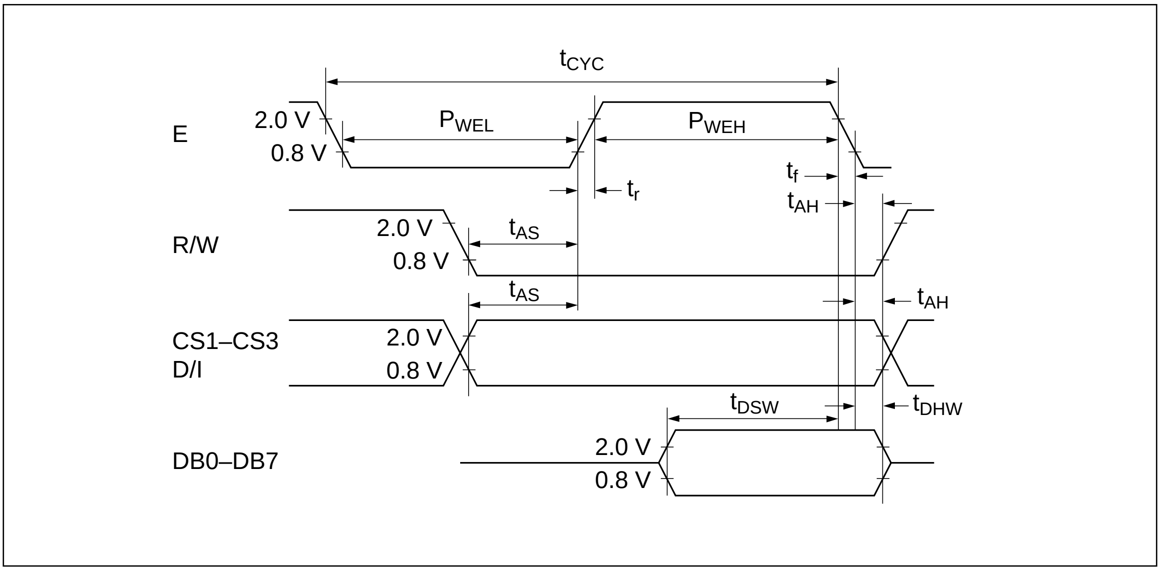


Figure 10 CPU Write Timing

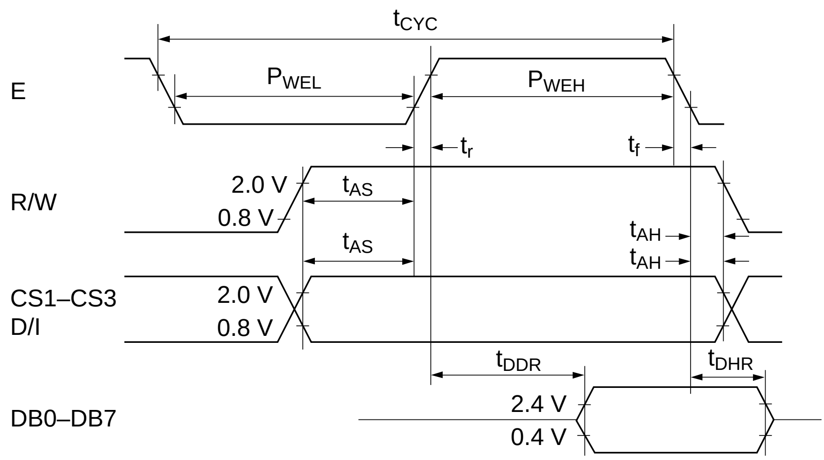


Figure 11 CPU Read Timing

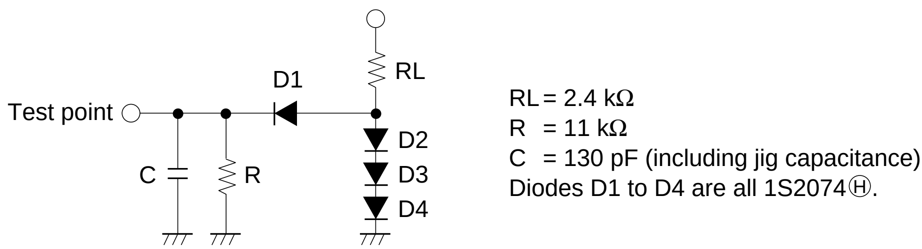


Figure 12 DB0–DB7: Load Circuit

Clock Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition
ø1, ø2 cycle time	t_{cyc}	2.5	—	20	µs	Fig. 13
ø1 low level width	$t_{WLø1}$	625	—	—	ns	
ø2 low level width	$t_{WLø2}$	625	—	—	ns	
ø1 high level width	$t_{WHø1}$	1875	—	—	ns	
ø2 high level width	$t_{WHø2}$	1875	—	—	ns	
ø1—ø2 phase difference	t_{D12}	625	—	—	ns	
ø2—ø1 phase difference	t_{D21}	625	—	—	ns	
ø1, ø2 rise time	t_r	—	—	150	ns	
ø1, ø2 fall time	t_f	—	—	150	ns	

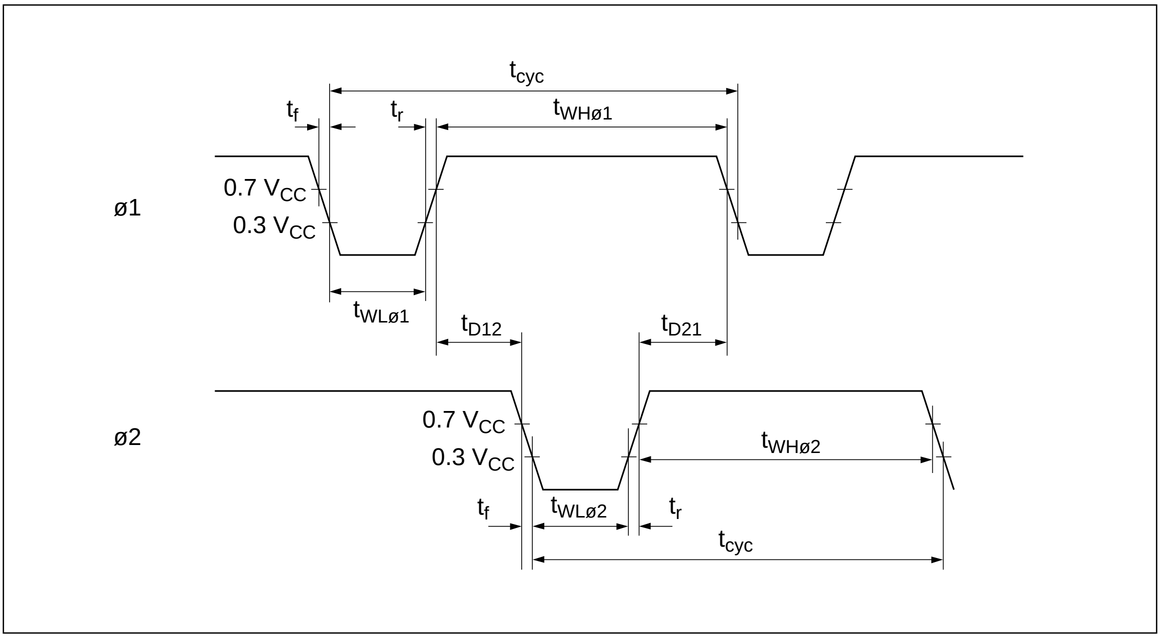


Figure 13 External Clock Waveform

Display Control Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

		Limit				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 14
M delay time	t_{DM}	–2	—	+2	µs	
CL low level width	t_{WLCL}	35	—	—	µs	
CL high level width	t_{WHCL}	35	—	—	µs	

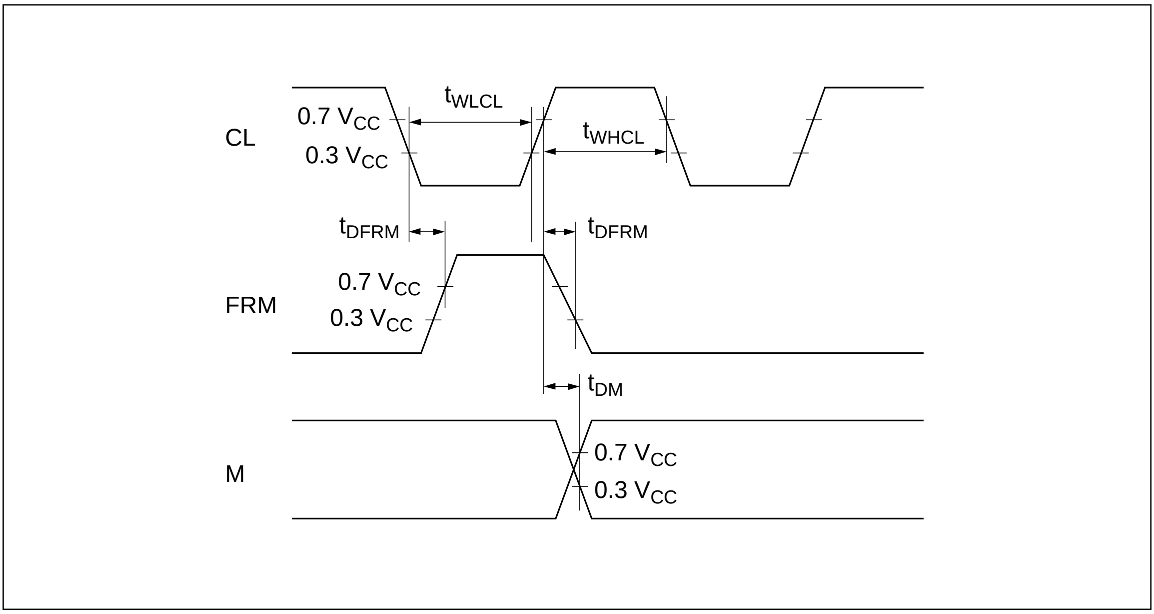


Figure 14 Display Control Signal Waveform