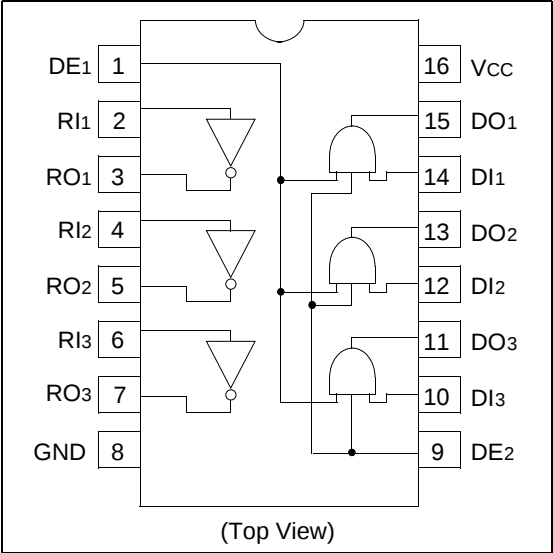


HD29468

Triple Line Drivers / Receivers

The HD29468 features line drivers and receivers for unbalanced transmissions, which meet the specs of IBM 360 and 370. This device has three drivers and receivers in one package. Input of driver and output of receiver are compatible with low power schottky TTL circuit and operates from a single 5 V power supply. The driver has two types of enable inputs. Sprius noise can be prevented by grounding either input when power supply is throw or cut off. The outputs are protected from short circuit and the wired logic is available due to emitter follower from for party line data bus applications. The device operates at high speed. Low to high level and high to low level propagation delay times defference are 10 ns max.

Pin Arrangement



Function Table

Driver

Input			Output
DI	DE1	DE2	DO
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Receiver

Input	Output
RI	RO
L	H
H	L

H : High level
L : Low level
X : Immaterial

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage	VCC	+7	V
Driver Input Voltage	VID	−0.5 to +7	V
Driver Output Voltage	VOD	−0.5 to +7	V
Receiver Input Voltage	VIR	−0.5 to +7	V
Power Dissipation (Ta = 25 °C)	^{*1} DP	1000	mW
	FP	785	
Operating Temperature	Ta	0 to +75	°C
Storage Temperature	Tstg	−65 to +150	°C

Notes: 1. The above data were taken by the ΔVBE method,mounting on a glass epoxy board (40 × 40 × 1.6 mm) of 10 % wiring density.

2. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.75	5.00	5.25	V
Operating Temperature	Ta	0	—	75	°C

Electrical Characteristics

Driver (VCC = 5.0 V ±5 %, Ta = 0 to +75°C)

Item	Symbol	Conditions	Min	Max	Unit
High Level Input Voltage	VIH		2.0	—	V
Low Level Input Voltage	VIL		—	0.8	V
Input Clamp Voltage	VIK	VCC = 4.75 V, IIN = −18 mA	—	−1.5	V
High Level Output Voltage	VOH	VCC = 4.75 V, VIH = 2.0 V IOH = −59.3 mA (Ta = 25 °C)	3.11	—	V
		VCC = 5.25 V, VIH = 2.0 V IOH = −78.1 mA	—	4.1	
Low Level Output Voltage	VOL	VCC = 5.25 V, VIL = 0.8 V IOL = −0.24 mA, VIH = 4.5 V	—	0.15	V
High Level Input Current	DI	IIH VCC = 5.25 V, VIH = 2.7 V	—	20	μA
	DE		—	60	
Low Level Input Current	DI	IIL VCC = 5.25 V, VIL = 0.4 V	—	−400	μA
	DE		—	−1200	
High Level Output Current	IOH	VCC=4.75 V, VIL = 0 V, VOH = 5.0 V	—	100	μA
		VCC = 4.75 V, VIH = 4.5 V, VOH = 5.0 V	—	100	
Short Circuit Output Current	IOS	VCC = 5.25 V, VIH = 4.5 V	—	−30	mA

Receiver (Ta = 0 to +75 °C)

Item	Symbol	Conditions	Min	Max	Unit
High Level Output Threshold Voltage	VOTH	VCC = 4.75 V, VIL = 1.15 V IOH = −400 μA	2.7	—	V
Low Level Output Threshold Voltage	VOTL	VCC = 5.25 V, VIH = 1.55 V IOL = 8 mA	—	0.5	V
High Level Output Voltage	VOH	VCC = 4.75 V, VIN : Open IOH = −400 μA	2.7	—	V
Low Level Output Voltage	VOL	VCC = 4.75 V IOL = 8 mA	—	0.5	V
		VIH = 1.55 V IOL = 4 mA	—	0.4	
Input Resistance	RIN	VCC = 0 V	7.4	20	kΩ
High Level Input Current	IIH	VCC = 4.75 V, VIH = 3.11 V	—	0.42	mA
Low Level Input Current	IIL	VCC = 5.25 V, VIL = 0.15 V	0.04	−0.24	mA
Short Circuit Output Current	IOS	VCC = 5.25 V, VIL = 0 V	−20	−100	mA

Driver / Receiver (Ta = 0 to +75 °C)

Item	Symbol	Conditions	Min	Max	Unit
Supply Voltage	ICCH	VCC = 5.25 V, VIH = 4.5 V	—	37	mA
	ICCL	VCC = 5.25 V, VIL = 0 V	—	55	

Switching Characteristics

Driver (VCC = 5.0 V, Ta = 25 °C)

Item	Symbol	Conditions	Min	Max	Unit
Rise Propagation Delay Time	tPLH	RL = 47.5 Ω	6.5	18.5	ns
Fall Propagation Delay Time	tPHL		6.5	18.5	ns
Propagation Delay Time Difference ^{*1}	ΔtPD		—	10	ns

Note: 1. ΔtPD= |tPLH – tPHL|

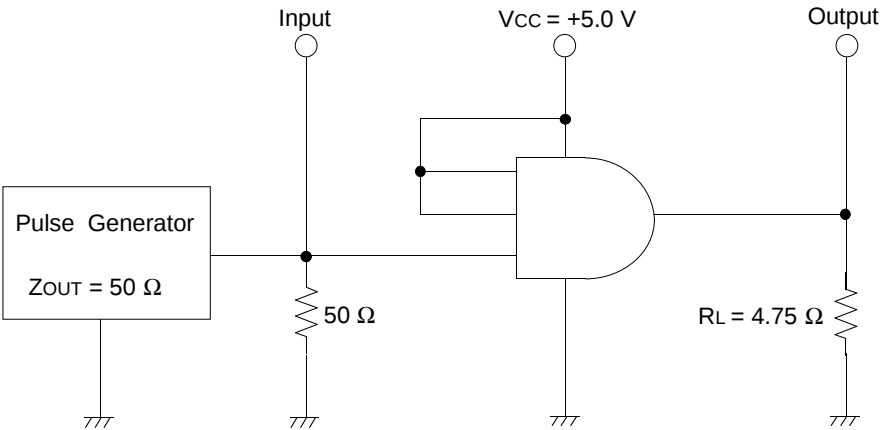
Receiver (VCC = 5.0 V, Ta = 25 °C)

Item	Symbol	Conditions	Min	Max	Unit
Rise Propagation Delay Time	tPLH	RL = 2 kΩ, CL = 15pF	7.5	19.5	ns
Fall Propagation Delay Time	tPHL		7.5	19.5	ns
Propagation Delay Time Difference ^{*1}	ΔtPD		—	10	ns

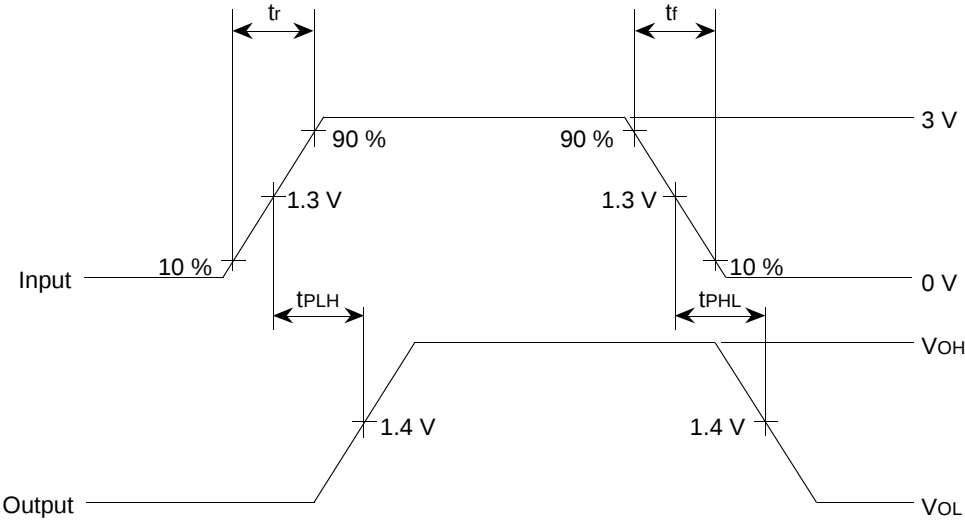
Note: 1. ΔtPD= |tPLH – tPHL|

Driver

Test Circuit



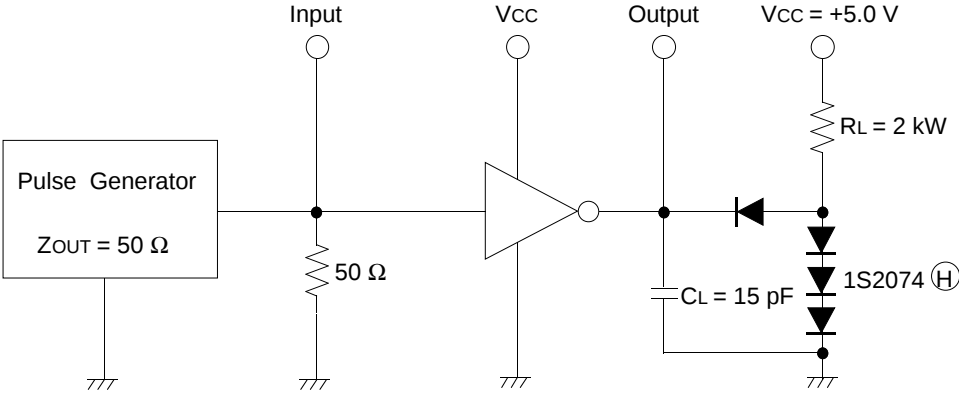
Waveforms



Notes: 1. $t_r = 15 \text{ ns}$, $t_f = 6 \text{ ns}$
2. Input waveforms : PRR = 1 MHz, duty cycle 50 %

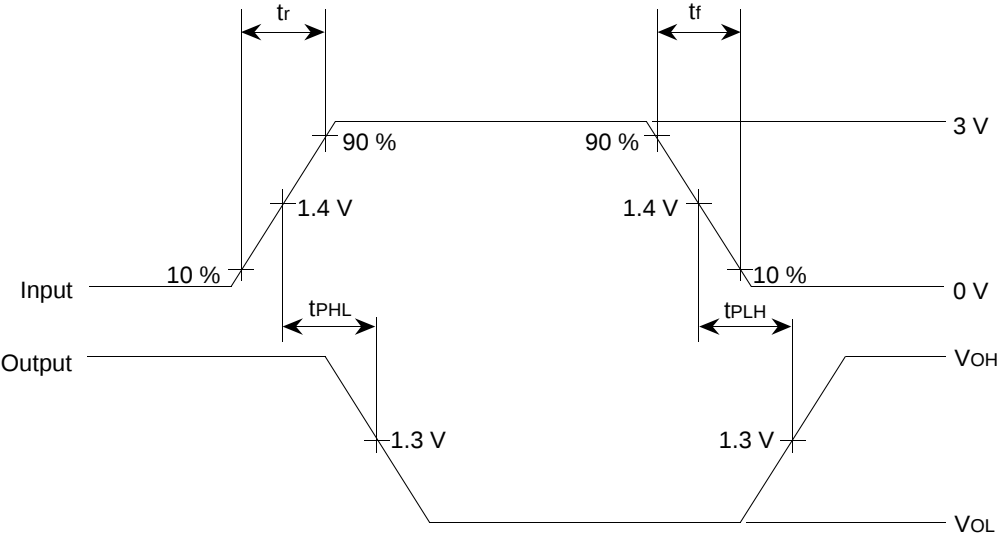
Driver

Test Circuit



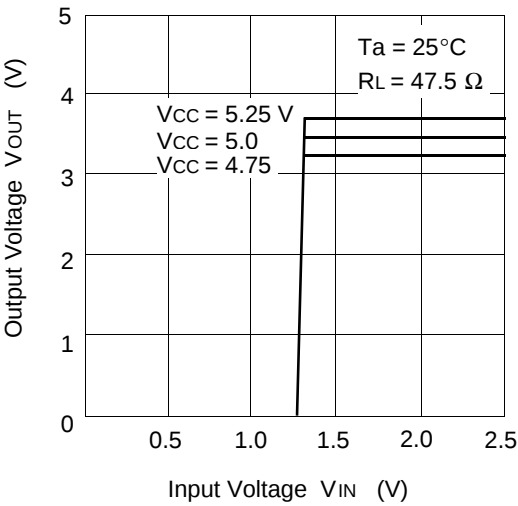
Note: 1. CL includes probe and jig capacitance.

Waveforms

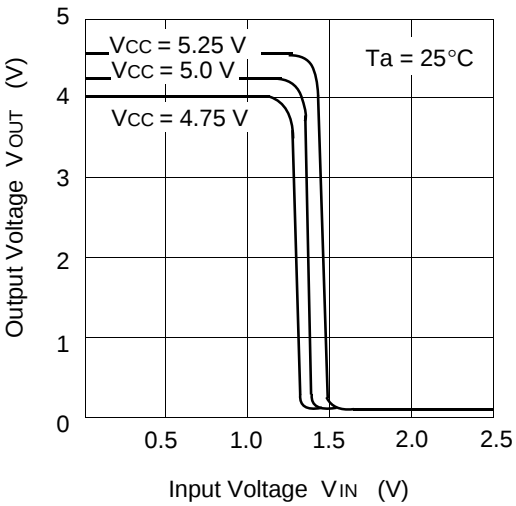


- Notes: 1. $t_r = t_f = 10 \text{ ns}$
2. Input waveforms : PRR = 1 MHz, duty cycle 50 %

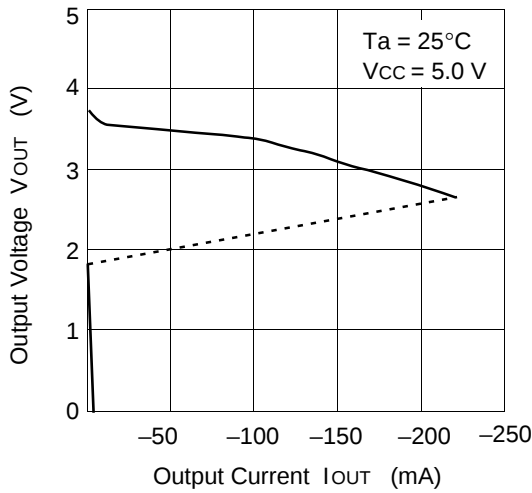
Driver VIN – VOUT



Receiver VIN – VOUT



Driver IOUT – VOUT



Receiver IOUT – VOUT

