

HCD65R660S / HCU65R660S

650V N-Channel Super Junction MOSFET

FEATURES

- ❑ Originative New Design
- ❑ Superior Avalanche Rugged Technology
- ❑ Robust Gate Oxide Technology
- ❑ Very Low Intrinsic Capacitances
- ❑ Excellent Switching Characteristics
- ❑ Unrivalled Gate Charge : 14 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 0.6 Ω (Typ.) @ $V_{GS}=10V$
- ❑ 100% Avalanche Tested

$$BV_{DSS} = 650 \text{ V}$$

$$R_{DS(on) \text{ typ}} = 0.6 \Omega$$

$$I_D = 6.2 \text{ A}$$

D-PAK

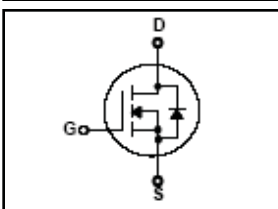


I-PAK



HCD65R660S HCU65R660S

1.Gate 2. Drain 3. Source



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	650	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	6.2	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	3.5	A
I_{DM}	Drain Current – Pulsed (Note 1)	18	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	120	mJ
I_{AR}	Avalanche Current (Note 1)	2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	1	mJ
dv/dt	Peak Diode Recovery dv/dt	15	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)*	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	63	W
	- Derate above 25°C	0.5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient*	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.8	--	4.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.0 A	--	0.6	0.66	Ω
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	650	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	--	--	10	μA
		V _{DS} = 520 V, T _J = 125 °C	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	--	--	±100	nA
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	550	--	pF
C _{oss}	Output Capacitance		--	250	--	pF
C _{rss}	Reverse Transfer Capacitance		--	8	--	pF
R _g	Gate Resistance	V _{GS} = 0 V, V _{DS} = 0 V, f = 1MHz	--	4	--	Ω
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 325 V, I _D = 6.2 A, R _G = 25 Ω	--	20	--	ns
t _r	Turn-On Rise Time		--	20	--	ns
t _{d(off)}	Turn-Off Delay Time		--	50	--	ns
t _f	Turn-Off Fall Time		--	20	--	ns
Q _g	Total Gate Charge	V _{DS} = 520 V, I _D = 6.2 A, V _{GS} = 10 V	--	14	--	nC
Q _{gs}	Gate-Source Charge		--	3.5	--	nC
Q _{gd}	Gate-Drain Charge		--	4.5	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I _S	Continuous Source-Drain Diode Forward Current		--	--	6.2	A
I _{SM}	Pulsed Source-Drain Diode Forward Current		--	--	18	
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 6.2 A, V _{GS} = 0 V	--	--	1.3	V
t _{rr}	Reverse Recovery Time	I _S = 3 A, V _{GS} = 0 V di _F /dt = 100 A/μs	--	250	--	ns
Q _{rr}	Reverse Recovery Charge		--	2	--	uC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=2\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

Typical Characteristics

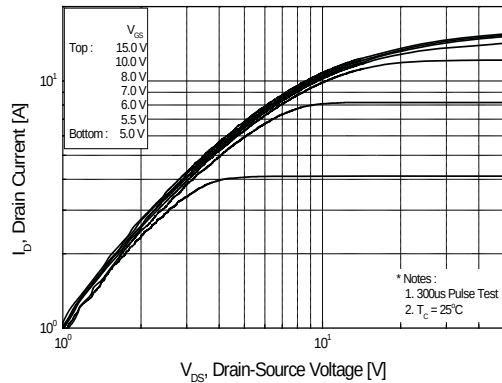


Figure 1. On Region Characteristics

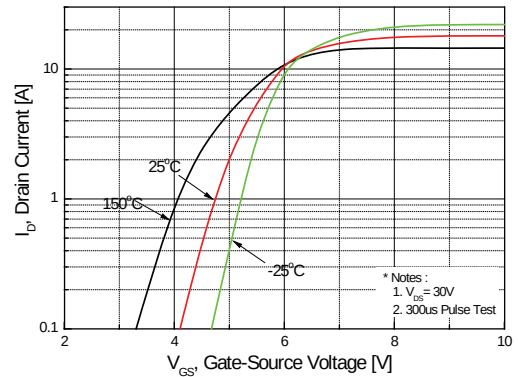


Figure 2. Transfer Characteristics

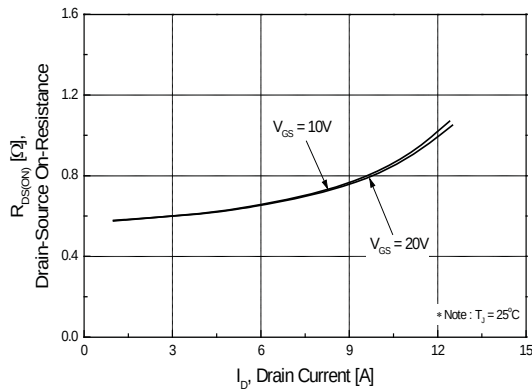


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

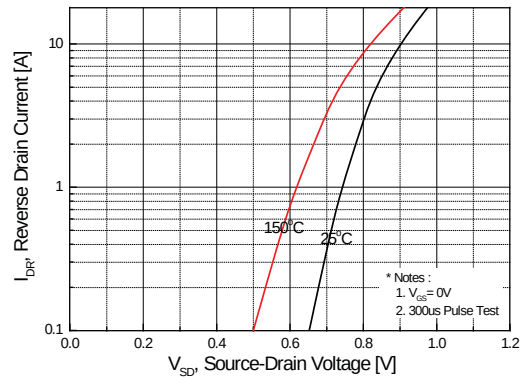


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

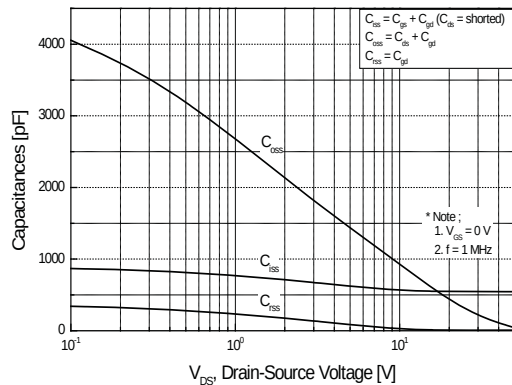


Figure 5. Capacitance Characteristics

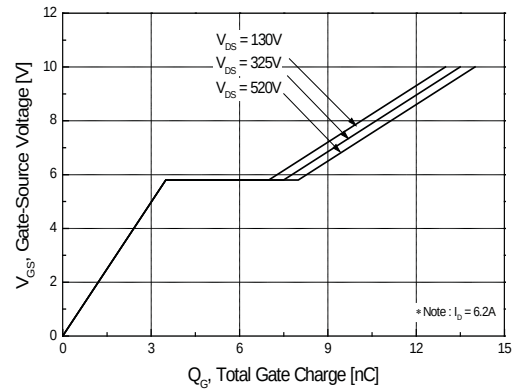


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

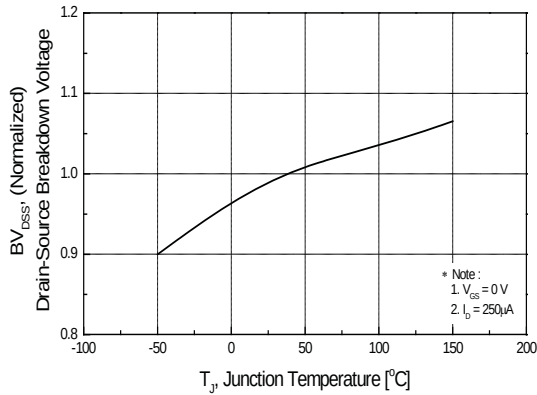


Figure 7. Breakdown Voltage Variation vs Temperature

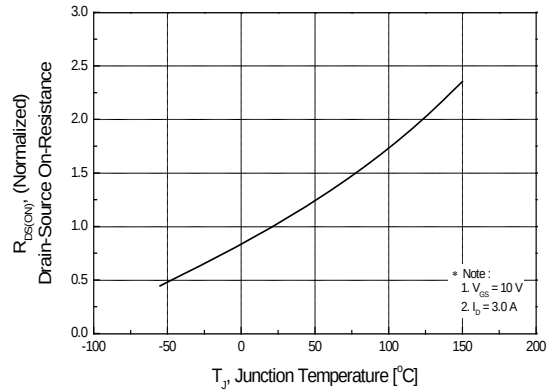


Figure 8. On-Resistance Variation vs Temperature

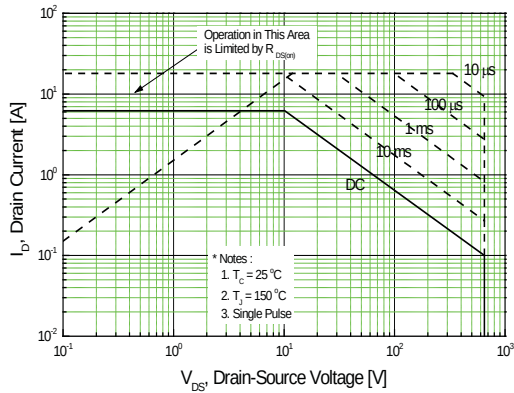


Figure 9. Maximum Safe Operating Area

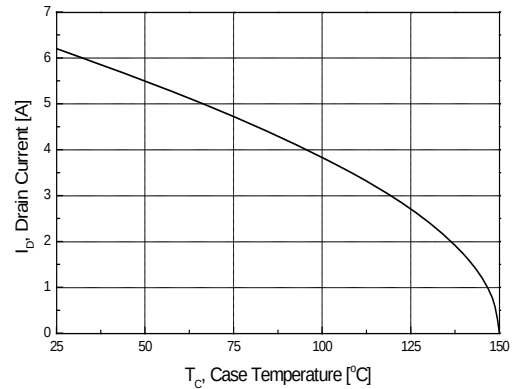


Figure 10. Maximum Drain Current vs Case Temperature

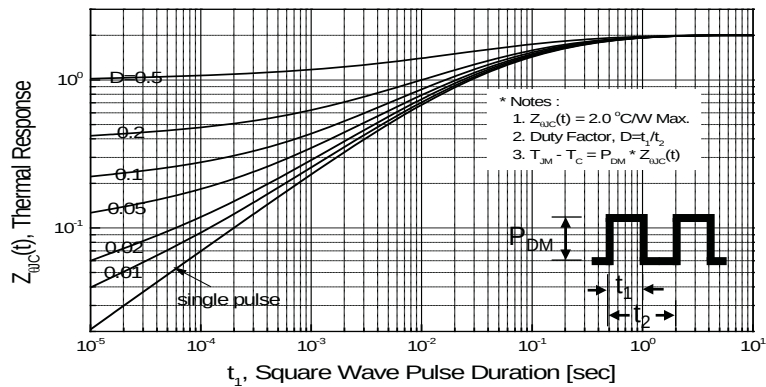


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

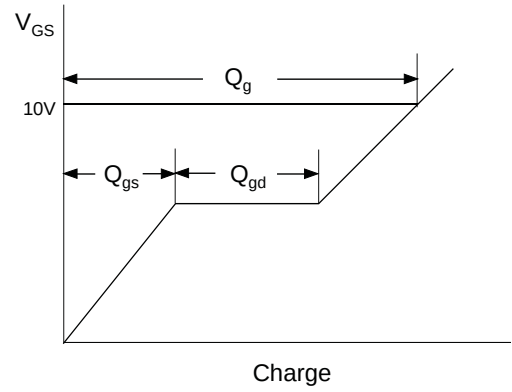
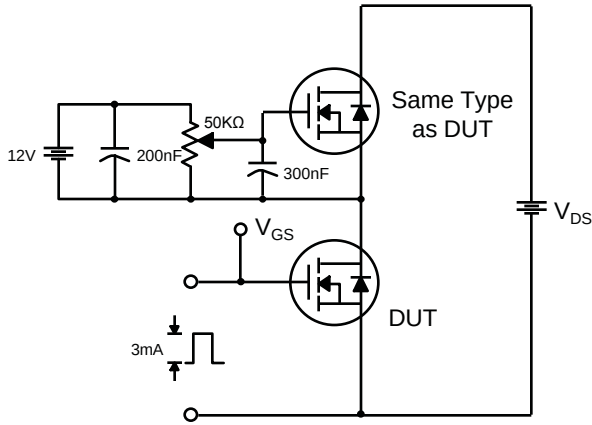


Fig 13. Resistive Switching Test Circuit & Waveforms

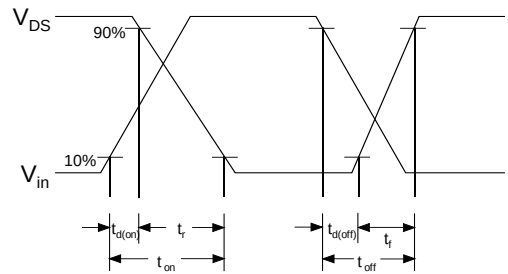
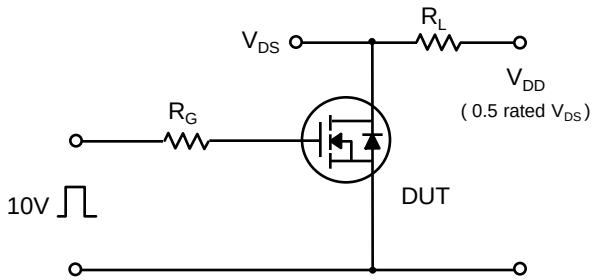


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

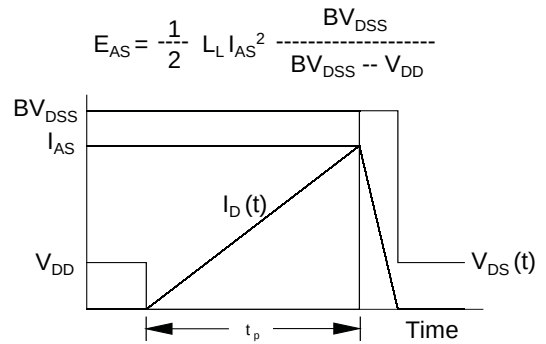
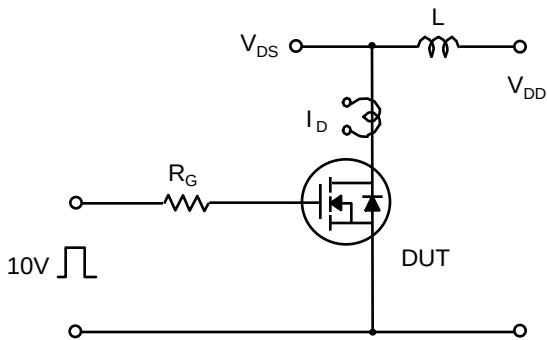
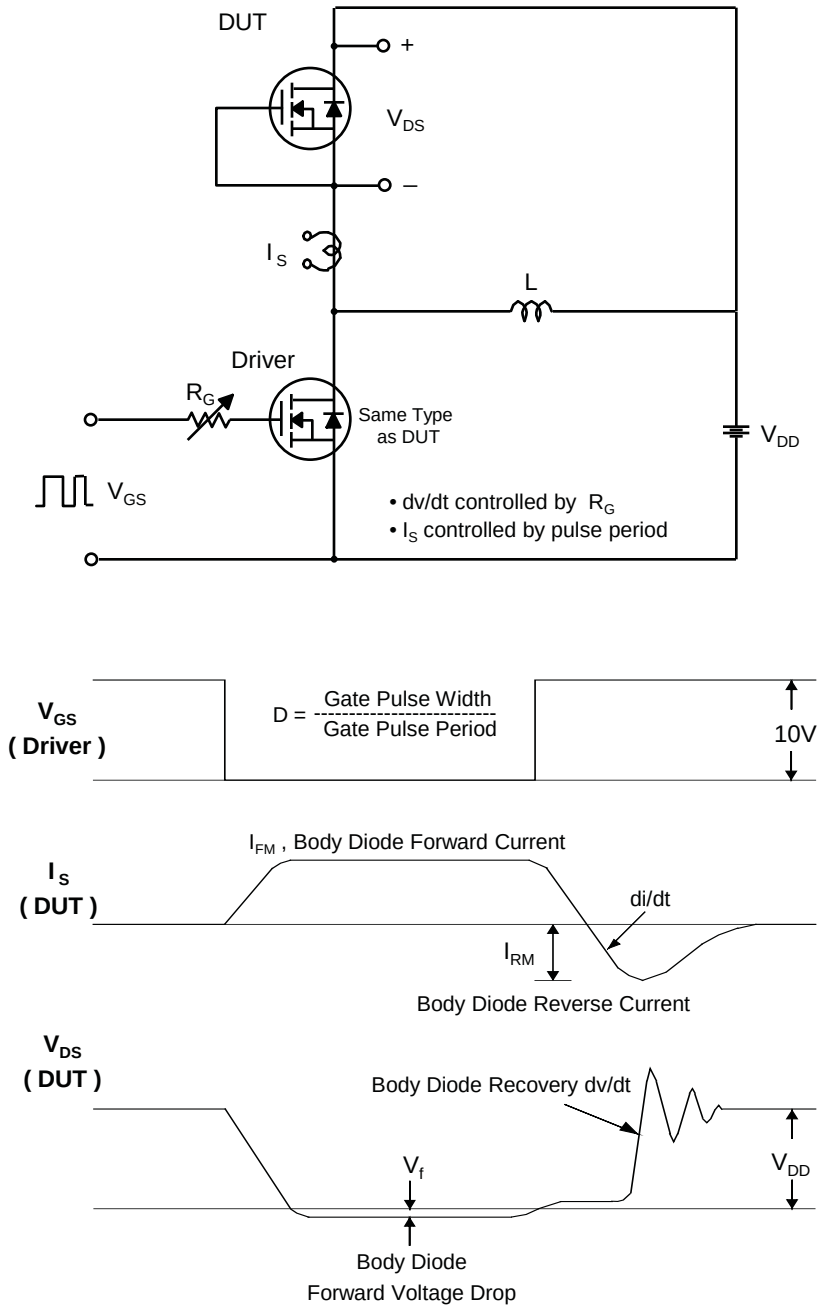


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

TO-252A
(D-PAK)