High Integrated and Low Power Smart Card Interface

Description

The HCM8035 is the cost efficient successor of the established integrated contact smart card reader IC HCM8025.It offers a high level of security for the card by performing current limitation, short-circuit detection, ESD protection as well as supply supervision.The current consumption during the standby mode of the contact reader is very low as it operates in the 3V supply domain.The HCM8035 is there the ideal component for a power efficient contact reader.

Applications

- Pay TV
- Electronic payment
- Identification
- IC card readers for banking

Features

- 5V,3V,1.8V smart card supply
- DC-to-DC converter for generation separately powered from 2.7V--5.5V supply
- Very low power consumption in Deep Shutdown Mode
- SW compatible to NXP8035
- Automatic activation and deactivation sequences initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, falling VREG VDD(INTF),VDDP
- Enhanced card-side (ESD) protection of (> 8 kV)
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7 and C8)
- External clock input up to 26 MHz
- Card clock generation up to 20 MHz using pins CLKDIV1 and CLKDIV2 with synchronous frequency changes of fXTAL, fXTAL/2, fXTAL/4 or fXTAL/8
- Supply supervisor for killing spikes during power on and off
- Multiplexed status signal using pin OFFN
- Chip Select digital input for parallel operation of several HCM8035 ICs

Ordering information

Package	QFN32L（5x5x0.75-0.5）
XXYY	Date code
XXXXXX	Wafer batch number

Top view

Typical Application

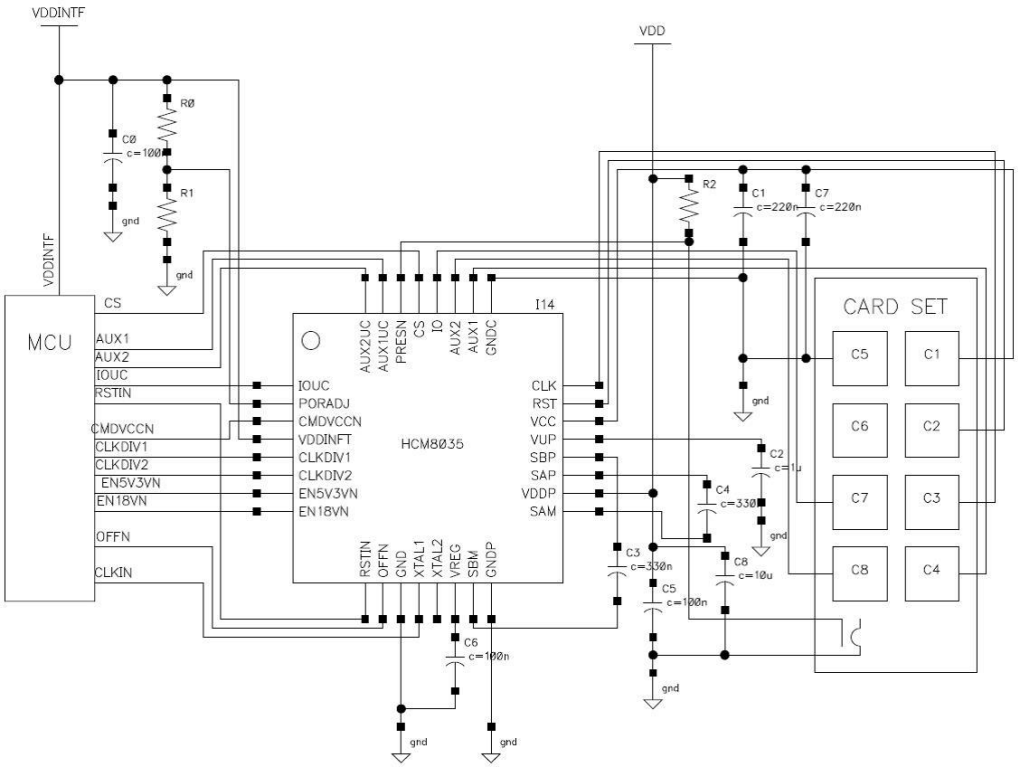


Fig 1

Pin Configurations and Functions

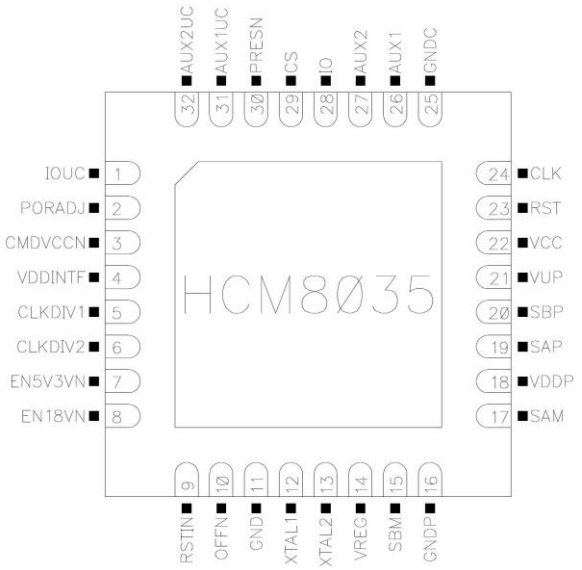


Fig 2

Table 1

NO.	NAME	TYP	DESCRIPTION
1	I/OUC	I/O	host data I/O line (internal 10 k pull-up resistor to VDD(INTF))
2	PORADJ	I	Input for VDD(INTF) supervisor. PORADJ threshold can be changed with an external R bridge
3	CMDVCCN	I	start activation sequence input from the host (active LOW)
4	VDDINTF	P	interface supply voltage
5	CLKDIV1	I	control with CLKDIV2 for choosing CLK frequency
6	CLKDIV2	I	control with CLKDIV1 for choosing CLK frequency
7	EN_5V/3VN	I	control signal for selecting V_{CC} = 5 V (HIGH) or V_{CC} = 3 V (LOW) if EN_1.8 VN = High
8	EN_1.8VN	I	control signal for selecting V_{CC} = 1.8 V (low)
9	RSTIN	I	card reset input from the host (active HIGH)
10	OFFN	O	NMOS interrupt to the host (active LOW) with 10 kΩ internal pull-up resistor to $V_{DD(INTF)}$
11	GND	P	ground
12	XTAL1	I	crystal connection 1
13	XTAL2	O	crystal connection 2
14	VREG	P	Internal supply voltage
15	SAM	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330nF or 100 nF with ESR < 100 mΩ at Freq=100kHz
16	GNDP	P	DC-to-DC converter power supply ground
17	SBM	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330nF or 100nF with ESR < 100 mΩ at Freq=100kHz
18	VDDP	P	Power supply voltage
19	SBP	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330nF or 100nF with ESR < 100 mΩ at Freq=100kHz
20	SAP	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330nF or 100nF with ESR < 100 mΩ at Freq=100kHz
21	VUP	I/O	DC-to-DC converter output decoupling capacitor connected between VUP and GNDP; C = 1 µF with ESR < 100 mΩ at Freq=100kHz
22	VCC	P	supply for the card (C1), decouple to GND with 2 × 220nF capacitors with ESR < 100 mΩ
23	RST	O	card reset (C2)
24	CLK	O	clock to the card (C3)
25	GNDC	P	card signal ground
26	AUX1	I/O	auxiliary data line to and from the card (C4), internal 10 kΩ pull-up resistor to VCC
27	AUX2	I/O	auxiliary data line to and from the card (C8), internal 10 kΩ pull-up resistor to VCC

28	I/O	I/O	data line to and from the card (C7), internal 10 kΩ pull-up resistor to V_{CC}
29	CS	I	Chip Select input from the host (active High)
30	PRESN	I	Card presence contact input (active LOW); if PRESN is true, then the card is considered as present. A debouncing feature of 4.05 ms typical is built in
31	AUX1UC	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to VDD(INTF)
32	AUX2UC	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to VDD(INTF)

Absolute Maximum Ratings

All card contacts are protected against a short-circuit with any other card contact.

Stress beyond the limiting values can damage the device permanently. The values are stress ratings only and functional operation of the device under these conditions is not implied.

Table 2

Symbol	Parameter	Conditions	Min	Max	Unit
VDDP	Power supply voltage		-0.3	6	V
VDDINTF	Interface supply voltage		-0.3	6	V
VIH	HIGH-level input voltage	CS, PRESN, CMDVCCN, CLKDIV2, CLKDIV1, EN1.8VN, EN5V3VN, RSTIN, OFFN, PORADJ, XTAL1, IOUC, AUX1UC, AUX2UC, VDDP, VDDINTF	-0.3	6	V
		IO, RST, AUX1, AUX2 and CLK	-0.3	5.75	V
Tamb	Ambient temperature		-25	+85	℃
Tstg	Storage temperature		-55	+150	℃
Tj	Junction temperature			+125	℃
Ptot	Total power dissipation			0.45	W
VESD	Electrostatic discharge voltage	HBM on card pins I/O, RST, V_{CC}, AUX1, CLK, AUX2, PRESN	-10	+10	kV
		HBM on all other pins	-2	+2	kV
		MM on all pins	-200	+200	V
		FCDM on all pins	-500	+500	V

Electrical Characteristics

Table 3 Test condition: T=25°C, VDDP=3.3V,VDDP(INTF)=3.3V,unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
VDDP	Power supply voltage		2.7	3.3	5.5	V
VDDINTF	Interface supply voltage		1.6	3.3	5.5	V
IDDP	Power supply current	Deep shutdown mode; f_{XTAL} = stopped	-	0.1	3	μA
		Shutdown mode; f_{XTAL} = stopped	-	300	500	μA
		Active mode; CLK = $f_{XTAL}/2$; V_{CC} = +5 V; no load	-	-	5	mA
		Active mode; CLK = $f_{XTAL}/2$; V_{CC} = +5 V; I_{CC} = 65 mA	-	-	220	mA
		Active mode; CLK = $f_{XTAL}/2$; V_{CC} = +3 V; I_{CC} = 65 mA	-	-	160	mA
		Active mode; CLK = $f_{XTAL}/2$; V_{CC} = +1.8 V; I_{CC} = 35 mA	-	-	120	mA
IDDINTF	Interface supply current	Deep shutdown mode, f_{XTAL} = stopped; present card	-	-	1	μA
		Shutdown mode; f_{XTAL} = stopped; present card	-	-	1	μA
Vth(VREG)	Threshold voltage on pin VREG	Internal voltage regulator falling	1.38	1.45	1.52	V
Vhys(VREG)	Hysteresis voltage on pin VREG		90	100	110	mV
Vth(VDDP)	Threshold voltage on pin VDDP	Pin VDDP falling	2.15	2.25	2.35	V
Vhys(VDDP)	Hysteresis voltage on pin VDDP		90	100	110	mV
tw	Pulse width		3.0	6.5	8.9	ms
Vth(L)(PORADJ)	Threshold voltage on pin PORADJ	External resistors on PORADJ	0.81	0.85	0.89	V
Vhys(PORADJ)	Hysteresis voltage on pin PORADJ		30	60	90	mV
IL	Leakage current	Pin PORADJ	-1	-	+1	μA
VREG						

V_o	Output voltage		1.62	1.80	1.98	V
tr	Rise time	Exit of deep shutdown mode	-	-	200	μs
VUP (DC-DC converter)						
VOH	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	5.10	5.60	7.00	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	3.50	3.95	5.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.60	7.00	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	5.10	5.80	7.00	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.80	7.00	V
SAP (DC-to-DC converter)						
VOH	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	-	-	6.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
DC-to-DC converter capacitors						
CSAPSAM	DC/DC converter capacitors	Connected between SAP and SAM (330 nF) , VDDP=3.3v	231	-	429	nF
		Connected between SAP and SAM (100 nF) ， VDDP=5v	70	-	130	nF
CSBPSBM	DC/DC converter capacitors	Connected between SBP and SBM (330 nF) , VDDP=3.3v	231	-	429	nF
		Connected between SBP and SBM (100 nF) ， VDDP=5v	70	-	130	nF
CVUP	DC/DC converter capacitors	Connected to VUP(1uF)	700	-	1300	nF
Card supply voltage (Vcc)						
Cdec	Decoupling capacitance	Connected on V_{CC} (220 nF + 220 nF 10 %)	396	-	484	nF

V_o	Output voltage	Inactive mode ； no load	-0.1	-	+0.1	V
		Inactive mode ； Io = 1 mA	-0.1	-	+0.3	V
Io	Output current	Active mode at grounded pin Vcc	-	-	-1	mA
VCC	Supply voltage	Active mode; 5 V card; ICC < 65 mA DC	4.75	5.0	5.25	V
		Active mode; 3 V card; ICC < 65 mA DC	2.85	3.05	3.15	V
		Active mode; 1.8 V card; ICC < 35 mA DC	1.71	1.83	1.89	V
		Active mode; current pulses of 40 nA/s， ICC < 200 mA, t < 400 ns; 5 V card	4.65	5.0	5.25	V
		Active mode; current pulses of 40 nA/s， ICC < 200 mA, t < 400 ns; 3 V card	2.76	-	3.20	V
		Active mode; current pulses of 5 nA/s，ICC < 200 mA, t < 400 ns; 1.8 V card	1.66	-	1.94	V
Vripple(p-p)	Peak to peak ripple voltage	20 kHz to 200 MHz	-	-	350	mV
ICC	Supply current	VCC = 0 V to 5 V, 3 V	-	-	65	mA
		VCC = 0 V to 1.8 V	-	-	35	mA
SR	Slew rate	5 V card	0.055	0.18	0.8	V/ μ s
		3 V card	0.040	0.18	0.8	V/ μ s
		1.8 V card	0.025	0.18	0.8	V/ μ s
Crystal oscillator (XTAL1 and XTAL2)						
Cext	External capacitance	Connected on pins XTAL1/XTAL2	-	-	33	pF
fxtal	Crystal frequency		2	-	27	MHz
fxtal(XTAL1)	Crystal frequency on pin XTAL1	With 56 pF serial capacitor	0	-	27	MHz
Data lines（I/O, I/OUC, AUX1, AUX2, AUXIUC, AUX2UC）						
td	Delay time	Falling edge on pins I/O (I/OUC)	-	-	200	ns
tw(pu)	Pull-up pulse width		200		400	ns
fmax	Maximum frequency	Frequency on data lines	-	-	1	MHz
C_i	Input capacitance	On data lines	-	-	10	pF
Data lines on the card (I/O, AUX1, AUX2); (integrated 10K Ω pull-up resistor to V_{CC})						
V_o	Output voltage	Inactive mode ;no load	0	-	0.1	V

		Inactive mode;Io=1mA	0	-	0.3	V
Io	Output current	Inactive mode， at grounded pin IO	-	-	-1	mA
VOL	LOW-level output voltage	I_{OL} = 1 mA	0	-	0.3	V
		I_{OL} ⩾ 15 mA	V_{CC} - 0.4	-	VCC	V
VOH	HIGH-level output voltage	No load	0.9 V_{CC}	-	V_{CC} + 0.1	V
		I_{OH} < -40 μA 5 V or 3 V	0.75 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < -20 μA 1.8 V	0.75 V_{CC}		V_{CC} + 0.1	V
		I_{OH} ⩾ -15 mA	0	-	0.4	V
VIL	LOW-level input voltage		-0.3	-	+0.8	V
VIH	HIGH-level input voltage	VCC = +5 V	0.6 V_{CC}	-	V_{CC} + 0.3	V
		VCC = +3 V or 1.8 V	0.7 V_{CC}	-	V_{CC} + 0.3	V
Vhys	Hysteresis voltage	on I/O	30	75	120	mV
IIL	LOW-level input current	on I/O; VIL = 0	-	-	600	μA
ILH	HIGH-level leakage current	on I/O; V_{IH} = V_{CC}	-	-	10	μA
tr(i)	Input rise time	From V_{IL} max to V_{IH} min	-	-	1.2	μs
tf(i)	Input fall time	From V_{IL} max to V_{IH} min	-	-	1.2	μs
tr(o)	Output rise time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	μs
tf(o)	Output fall time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	μs
Rpu	Pull-up resistance	connected to VCC	8	10	12	kΩ
Ipu	Input current	V_{OH} = 0.9 V_{CC}, C = 80 pF	-8	-6	-4	mA
Data lines to the system（I/OUC, AUX1UC, AUX2UC)；（internal pull-up resistor to $V_{DD(INTF)}$)						
VOL	LOW-level output voltage	I_{OL} = 1 mA	0	-	0.3	V
VOH	HIGH-level output voltage	No load	0.9 VDD(INTF)	-	$V_{DD(INTF)}$ + 0.1	V
		IOH ⩽ 40 μA; VDD(INTF) >2 V	0.75 VDD(INTF)	-	VDD(INTF)+ 0.1	V
		IOH ⩽ 20 μA; VDD(INTF) <2 V	0.75 VDD(INTF)	-	VDD(INTF)+ 0.1	V
VIL	LOW-level input voltage		0.3	-	0.3 VDD(INTF)	V
VIH	HIGH-level input voltage		0.7 VDD(INTF)		VDD(INTF) + 0.3	V
Vhys	Hysteresis voltage	Pin IOUC	0.05 VDD(INTF)	-	0.25 VDD(INTF)	V
ILH	HIGH-level leakage current	VIH = VDD(INTF)			10	μA

IIL	LOW-level input current	V_{IL} = 0			600	μA
Rpu	Pull-up resistance	Pull up to VDD(INTF)	8	10	12	kΩ
tr(i)	Input rise time	From V_{IL} max to V_{IH} min	-	-	1.2	μs
tf(i)	Input fall time	From V_{IL} max to V_{IH} min	-	-	1.2	μs
tr(o)	Output rise time	C_L ≤ 30 pF; 10 % to 90 % from 0 to $V_{DD(INTF)}$	-	-	0.1	μs
tf(o)	Output fall time	C_L ≤ 30 pF; 10 % to 90 % from 0 to $V_{DD(INTF)}$	-	-	0.1	μs
Ipu	Pull up current	V_{OH} = 0.9 V_{DD}, C = 30 pF	-1	-	-	mA
Internal oscillator						
fosc(int)	Internal oscillator frequency	Inactive state: osc(int)_low		180		kHz
		Active state osc(int)_high		2		MHz
Reset output to the card (RST)						
V_o	Output voltage	Inactive mode，no load	0	-	0.1	V
		Active mode ，Io= 1 mA	0	-	0.3	V
Io	Output current	Active mode and at grounded pin RST	-	-	-1	mA
Td	Delay time	RST enabled，RSTIN between RST	-	-	200	ns
VOL	LOW-level output voltage	I_{OL}= 200 μA, VCC = +5 V	0	-	0.3	V
		I_{OL}= 200 μA, VCC = +3 V or 1.8 V	0	-	0.2	V
		I_{OL} = 20 mA (current limited)	V_{CC} - 0.4	-	VCC	V
VOH	HIGH-level output voltage	I_{OH} = -200 μA	0.9 V_{CC}	-	VCC	V
		I_{OH} = -20 mA (current limited)	0	-	0.4	V
Tr	Rise time	C_L = 100 pF V_{CC} = +5 V and +3 V	-	-	0.1	μs
		C_L = 100 pF V_{CC} = +18 V	-	-	0.2	μs
t_f	Fall time	C_L = 100 pF V_{CC} = +5 V and +3 V	-	-	0.1	μs
		C_L = 100 pF V_{CC} = +18 V	-	-	0.2	μs
Clock output to the card (CLK)						
V_o	Output voltage	Inactive mode，no load	0	-	0.1	V
		Active mode，I_o = 1 mA	0	-	0.3	V
Io	Output current	Active mode and at grounded pin CLK	-	-	-1	mA
VOL	LOW-level output	I_{OL} = 200 μA	0	-	0.3	V

	voltage	I_{OL} = 70 mA (current limited)	V_{CC}-0.4	-	VCC	V
VOH	HIGH-level output voltage	I_{OH} = -200 μA	0.9 V_{CC}	-	VCC	V
		I_{OH} = -70 mA (current limited)	0	-	0.4	V
Tr	Rise time	CL = 30 pF [2]	-	-	16	ns
t_f	Fall time	CL = 30 pF [2]	-	-	16	ns
fCLK	Frequency on pin CLK	operational	0	-	20	MHz
	Duty cycle	CL = 30 pF [2]	45	-	55	%
SR	Slew rate	Rise and fall; C_L = 30 pF; VCC = +5 V	0.2	-	-	V/ns
		Rise and fall; C_L = 30 pF; VCC = +3 V	0.12	-	-	V/ns
		Rise and fall; C_L = 30 pF; VCC = +1.8 V	0.072	-	-	V/ns

Control inputs（CS, CMDVCCN, CLKDIV1, CLKDIV2, RSTIN, EN5V3VN, EN18VN)						
VIL	LOW-level input voltage		-0.3	-	+0.3 VDD(INTF)	V
VIH	HIGH-level input voltage		0.7 VDD(INTF)	-	$V_{DD(INTF)}$ + 0.3	V
Vhys	Hysteresis voltage	On control input	0.05 VDD(INTF)	-	0.25 VDD(INTF)	V
ILL	LOW-level leakage current	V_{IL} = 0	-	-	1	μA
ILH	HIGH-level leakage current	VIH = VDD(INTF)	-	-	1	μA
Card presence input(PRESN); pin PRESN integrated pull down resistor to GND						
VIL	LOW-level input voltage		0.3	-	+0.3 VDD(INTF)	V
VIH	HIGH-level input voltage		0.7 VDD(INTF)	-	VDD(INTF) + 0.3	V
Vhys	Hysteresis voltage		0.05 VDD(INTF)	-	0.10 VDD(INTF)	V
ILL	LOW-level leakage current	V_{IL} = 0	-	-	1	μA
ILH	HIGH-level leakage current	VIH = VDD(INTF)	-	-	5	μA
OFFN output (pin OFFN is a NMOS drain with a pull up resistor to $V_{DD(INTF)}$)						
VOL	LOW-level output voltage	I_{OL} = 2 mA	0	-	0.3	V

VOH	HIGH-level output voltage	I_{OH} = -15 μA	0.75 VDD(INTF)	-			V
Rpu	Pull-up resistance		8	10	12		kΩ
Protections and limitation							
Tsd	Shutdown temperature	At die	-	150	-		℃
IOlim	Output current limited	on pin I/O	-15	-	+15		mA
		on pin CLK	-70	-	+70		mA
		on pin RST	-20	-	+20		mA
		on pin VCC = 5 V or 1.8 V	90	125	160		mA
		on pin VCC = 3 V	90	160	260		mA
Isd	Shutdown current	on pin VCC = 5 V or 1.8 V	80	115	150		mA
		on pin VCC = 3 V	80	150	250		mA

Functional Block Diagram

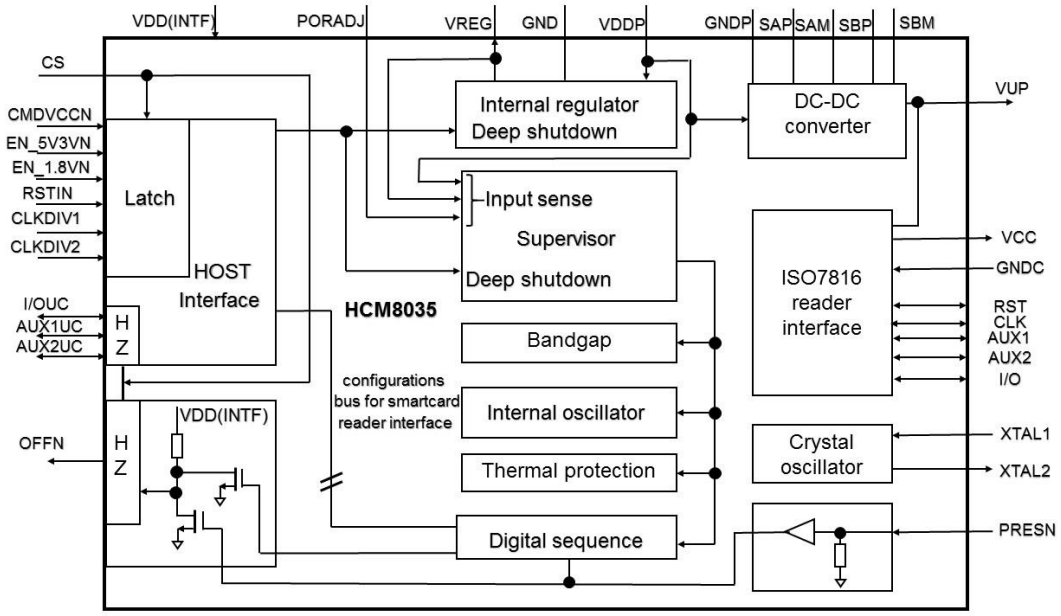


Fig 3

Functional Descriptions

Remark: The ISO 7816 terminology convention has been adhered to throughout this document, and it is assumed that the reader is familiar with this convention.

Power supply

Power supply voltage V_{DDP} is from 2.7 V to 5.5 V.

All interface signals with the system controller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during powering up or powering down.

Internal regulator V_{REG} is 1.8 V.

After powering the device, OFFN remains low until CMDVCCN is set high and PRESN is low.

During power off, OFFN falls low when V_{DDP} is below the threshold voltage falling.

While the card is not activated, CMDVCCN is kept at high level. To save power consumption, the

frequency of the internal oscillator ($f_{osc(int)}$) used for the activation sequences is put in low frequency mode.

This device includes a DC-to-DC converter to generate the 5 V, 3 V or 1.8 V card supply.

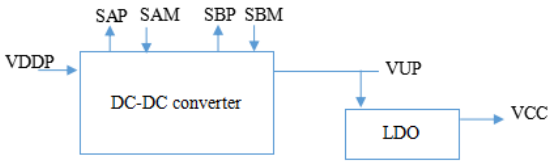


Fig 4

voltage(V_{CC}). The DC-to-DC converter is separately supplied by V_{DDP} and G_{NDP}. The DC-to-DC converter operates as a voltage tripler, doubler or follower according to the respective values of V_{CC} and V_{DDP}.

Special care has to me made in the selection of the capacitors of the DC/DC converter specially with respect to capacitor value versus voltage and ESR.

The operating mode is as follows:

Table 5

Pin VCC voltage	Pin VDDP voltage	DC-DC converter state
5V	>3.5V	X 1
5V	<3.5V	X 2
3V	>3.5V	X 0
3V	<3.5V	X 1
1.8V	>3.5V	X 0
1.8V	<3.5V	X 0

Voltage supervisor

The voltage supervisor is used as a power-on reset, and also as supply drop detection during a card session. The threshold of the voltage supervisor is set internally in the IC for VDDP and VREG. The threshold can be adjusted externally for VDD(INTF) using the PORADJ pin. As long as VREG is less than $V_{th(VREG)} + V_{hys(VREG)}$, the IC remains inactive whatever the levels on the command lines are. The inactivity lasts for the duration of t_w after VREG has reached a level higher than $V_{th(VREG)} + V_{hys(VREG)}$. The outputs of the VDDP, VREG and VDD(INTF) supervisors are combined and sent to a digital controller in

order to reset the TDA8035. The reset pulse of approximately 5.7 ms (t_w = 2048 * 1/($f_{osc(int)\_Low}$) is used internally for maintaining the IC in an inactive mode during the supply voltage power-on. A deactivation sequence is performed when:

- VREG falls below $V_{th(VREG)}$
- VDD(INTF) falls below Vth(PORADJ)
- VDDP falls below $V_{th(VDDP)}$

Clock circuitry

To generate the card clock CLK, the TDA8035 can either use an external clock provided on XTAL1 pin or a crystal oscillator connected on both XTAL1 and XTAL2 pins. The TDA8035 automatically detects when an external clock is provided on XTAL1. Consequently, there is no need for an extra pin to configure the clock source(external clock or crystal).

The automatic clock source detection is performed on each activation command (CMDVCCN pin falling edge). During a time window defined by the internal oscillator, the presence of an external clock on XTAL1 pin is checked. If a clock is detected, the crystal oscillator is kept stopped, else, the crystal oscillator is started. It is mandatory when an external clock is used, that the clock is applied on XTAL1 before CMDVCCN falling edge signal.

The frequency is chosen as f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$ via the pins CLKDIV1 and CLKDIV2. Both selection inputs are not changed simultaneously. A minimum of 10 ns is required between changes on CLKDIV1 and CLKDIV2.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45 % of the smallest period. This ensures that the first and last clock pulse around the change has the correct width. When changing the frequency dynamically, the change is effective for only 10 periods of XTAL1 after the command.

The duty cycle on pin CLK is between 45 % and 55 %:

- When an external clock is used on XTAL1 pin and f_{XTAL} is used, the duty cycle is between 48 % and 52 %. The subsequent rise and fall times ($t_{r(i)}$ and $t_{f(i)}$) conform to values listed in Table 4. It has to connect a 56 pF serial capacitor (see Figure 1).
- CLK frequency is f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$:

Table 6

CLKDIV1	CLKDIV2	CLK
1	0	fXTAL
1	1	fXTAL/2
0	1	fXTAL/4
0	0	fXTAL/8

It is guaranteed between 45 % and 55 % of the period by the frequency dividers.

I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

To enter the idle state, both lines (I/O and I/OUC) are pulled HIGH via a 10 k resistor (I/O to VCC and I/OUC to VDD(INTF)).

I/O is referenced to V_{CC}, and I/OUC to $V_{DD(INTF)}$ which allows operation with VCC VDD(INTF).

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes the slave.After a time delay $t_{d(edge)}$, the logic 0 present on the master side is transmitted to the slave side.

When the master side returns to logic 1, the slave side transmits the logic 1 during the time delay t_{pu} and both sides return to their idle states.

The active pull-up feature ensures fast Low to High transitions. It is able to deliver more than 1 mA to an output voltage of 0.9 V_{CC} on an 80 pF load. At the end of the active pull-up pulse, the output voltage depends on the internal pull-up resistor and on the load current.

The current to and from the cards I/O lines is internally limited to 15 mA.

The maximum frequency on these lines is 1.5 MHz.

CS control

The CS (Chip Select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is low, the signals CMDVCCN, RSTIN, CLKDIV1, CLKDIV2, EN_5V/3VN and EN_1.8VN are latched.

I/OUC, AUX1UC and AUX2UC are set to high impedance pull-up mode and data is no longer passed to

or from the smart card. The OFFN output is a 3-state output.

Shutdown mode and Deep Shutdown mode

After power-on reset, the circuit enters the Shutdown mode if CMDVCCN input pin is set to a logic high.

A minimum number of circuits are active while waiting for the microcontroller to start a session.

1.All card contacts are inactive (approximately 200 **Ω** to GND).

2.I/OUC, AUX1UC and AUX2UC are high impedance (10 kW pull-up resistor connected to VDD(INTF)).

3.Voltage generators are stopped.

4.Voltage supervisor is active.

5.The internal oscillator runs at its low frequency.

A Deep Shutdown mode can be entered by forcing CMDVCCN input pin to a logic-High state and EN_5V/3VN, EN _1.8VN input pins to a logic-Low state. Deep Shutdown mode can only be entered when the smart card reader is inactive. In Deep Shutdown mode, all circuits are disabled. The OFFN pin follows the status of PRESN pin. To exit Deep Shutdown mode, change the state of one or more of the three control pins.

Activation sequence

The following sequence then occurs with crystal oscillator (see Figure 5):
T = 64 * T_{oscint} (freq high)

1.CMDVCCN is pulled low (t0)

2.Crystal oscillator start-up time (t0).

3.The internal oscillator changes to its high frequency and DC-to-DC starts t1 = t0 + 768 Tosc (freq low).

4.V_{CC} rises from 0 to selected V_{CC} value (5 V, 3 V, 1.8 V) with a controlled slope ($t_2 = t_1 + 3T/2$)

5.I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 10T$), until now, they were pulled LOW

6.CLK is applied to the C3 contact ($t_4 = t_3 + \times$) with 200 ns < × < 10 × $1/f_{Xtal}$

7.RST is enabled ($t_5 = t_1 + 13T$).

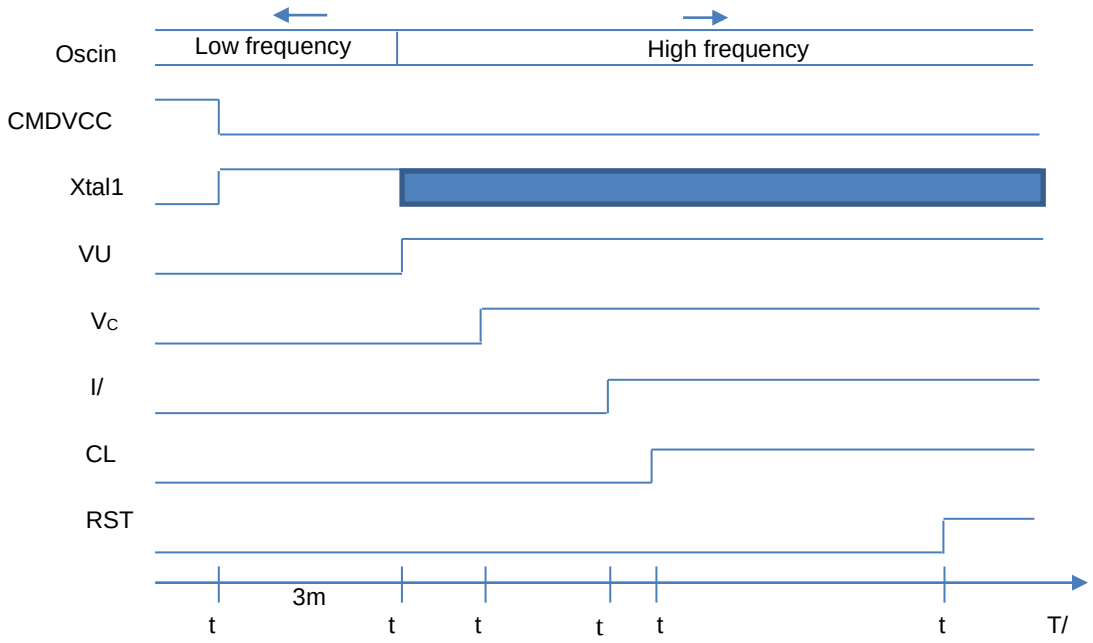


Fig 5

Deactivation sequence

When a session is completed, the microcontroller sets the CMDVCCN line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Figure 6):

1.RST goes LOW ($t_{11} = t_{10} + 3T/64$)

2.CLK is stopped LOW ($t_{12} = t_{11} + T/2$)

3.I/O, AUX1 and AUX2 are pulled LOW ($t_{13} = t_{11} + T$)

4.V_{CC} falls to zero ($t_{14} = t_{11} + 3T/2$). The deactivation sequence is completed when V_{CC} reaches its inactive state.

5.VUP falls to zero ($t_{15} = t_{11} + 7T/2$).

6.V_{CC} < 0.4 V ($t_{de} = t_{11} + 3T/2 +$ V_{CC} fall time).

7.All card contacts become low-impedance to GND. I/OUC, AUX1UC and AUX2UC remain pulled up to $V_{DD(INTF)}$ via a 10 kΩ resistor.

8.The internal oscillator reverts to its lower frequency.

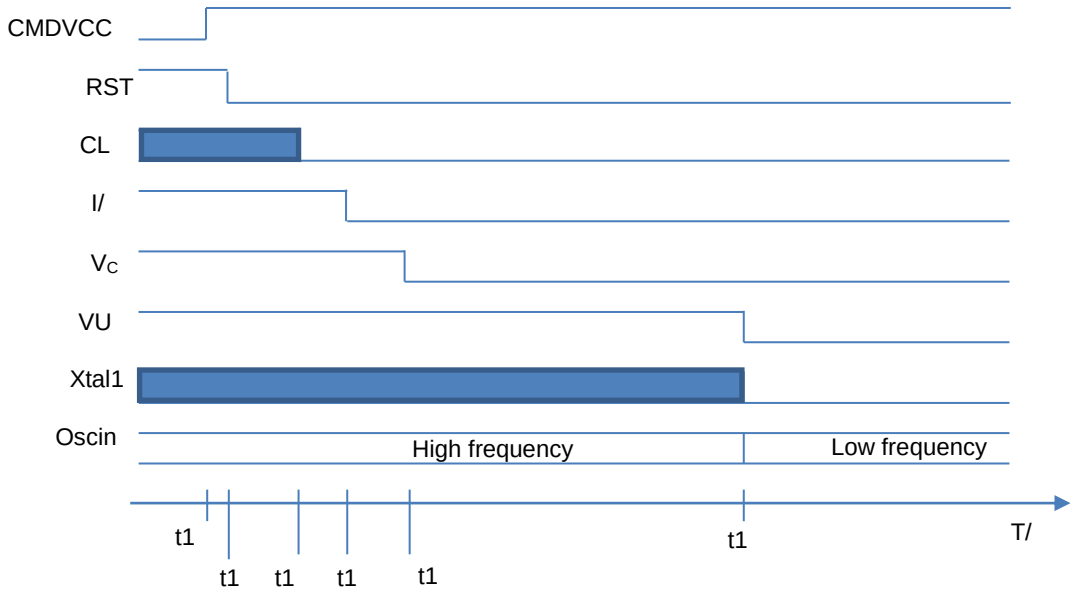


Fig 6

V_{CC} regulator

V_{CC} buffer is able to deliver up to 65 mA continuously at V_{CC} = 5 V and V_{CC} = 3 V, and 35 mA at V_{CC} = 1.8 V.

V_{CC} buffer has an internal overload detection at approximately 125 mA.

This detection is internally filtered, allowing the card to draw spurious current pulses of up to 200 mA for some milliseconds, without causing a deactivation. The average current value must remain below the maximum.

Fault detection

The circuit monitors the following fault conditions:
- short-circuit or high current on V_{CC}
- Card removal during transaction
- V_{DDP} or $V_{DD(INTF)}$ or V_{reg} dropping
- overheating.

There are two different cases (see Figure 7):

1. CMDVCCN High (outside a card session): OFFN is Low when the card is not in the reader, and High when the card is in the reader. The supply supervisor detects a supply voltage drop on V_{DDP} and generates an internal power-on reset pulse, but it does not act upon OFFN. The card is not powered-up, so no short-circuit or overheating is detected.

2. CMDVCCN Low (within a card session): OFFN falls Low in any of the previously mentioned cases. As soon as the fault is detected, an emergency deactivation is automatically performed. When the system controller sets CMDVCCN back to High, it senses OFFN again. After a complete deactivation sequence, the system controller sets CMDVCCN back to High and it senses OFFN again. This is to distinguish between a hardware problem or a card extraction. OFFN reverts to High when the card is still present.

A bounce can occur on the PRESN signal during card insertion or withdrawal. The bounce depends on the type of card presence switch within the connector (normally closed or normally open), and on the mechanical characteristics of the switch. To prevent this bounce, a debounce function of approximately 4.05 ms (tdeb = 1280 * 1/(fosc(int)_Low) is integrated in the device.

When the card is inserted, OFFN goes High only at the end of the debounce time (see Figure 8)
When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRESN. OFFN goes Low.

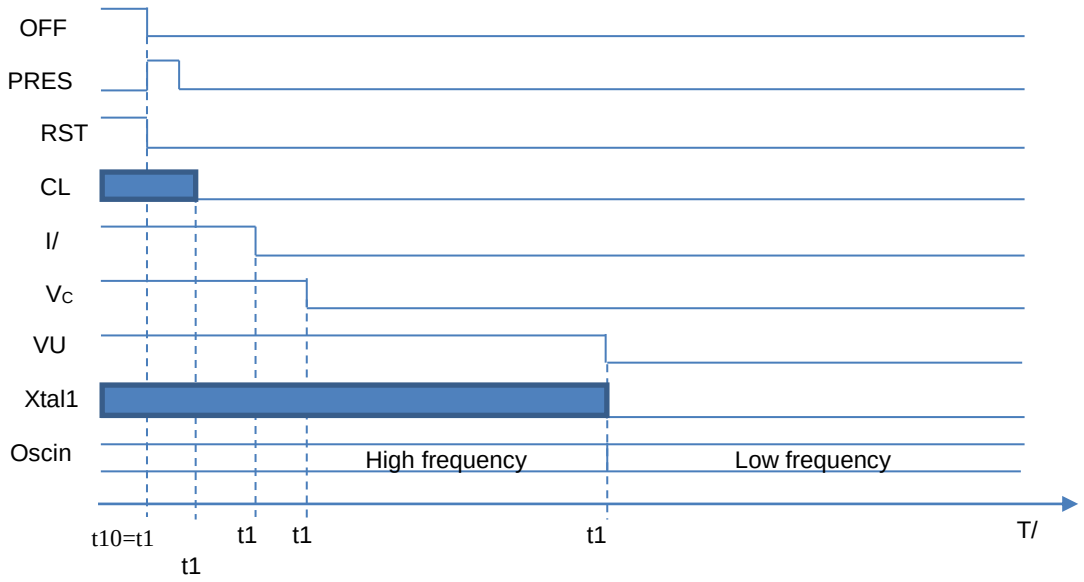


Fig 7

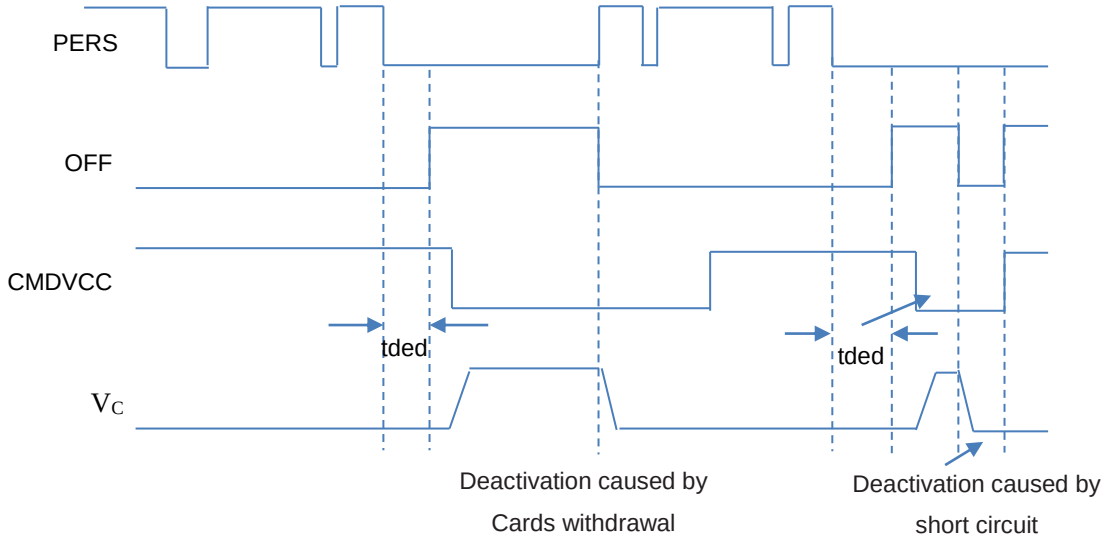


Fig 8

Application information

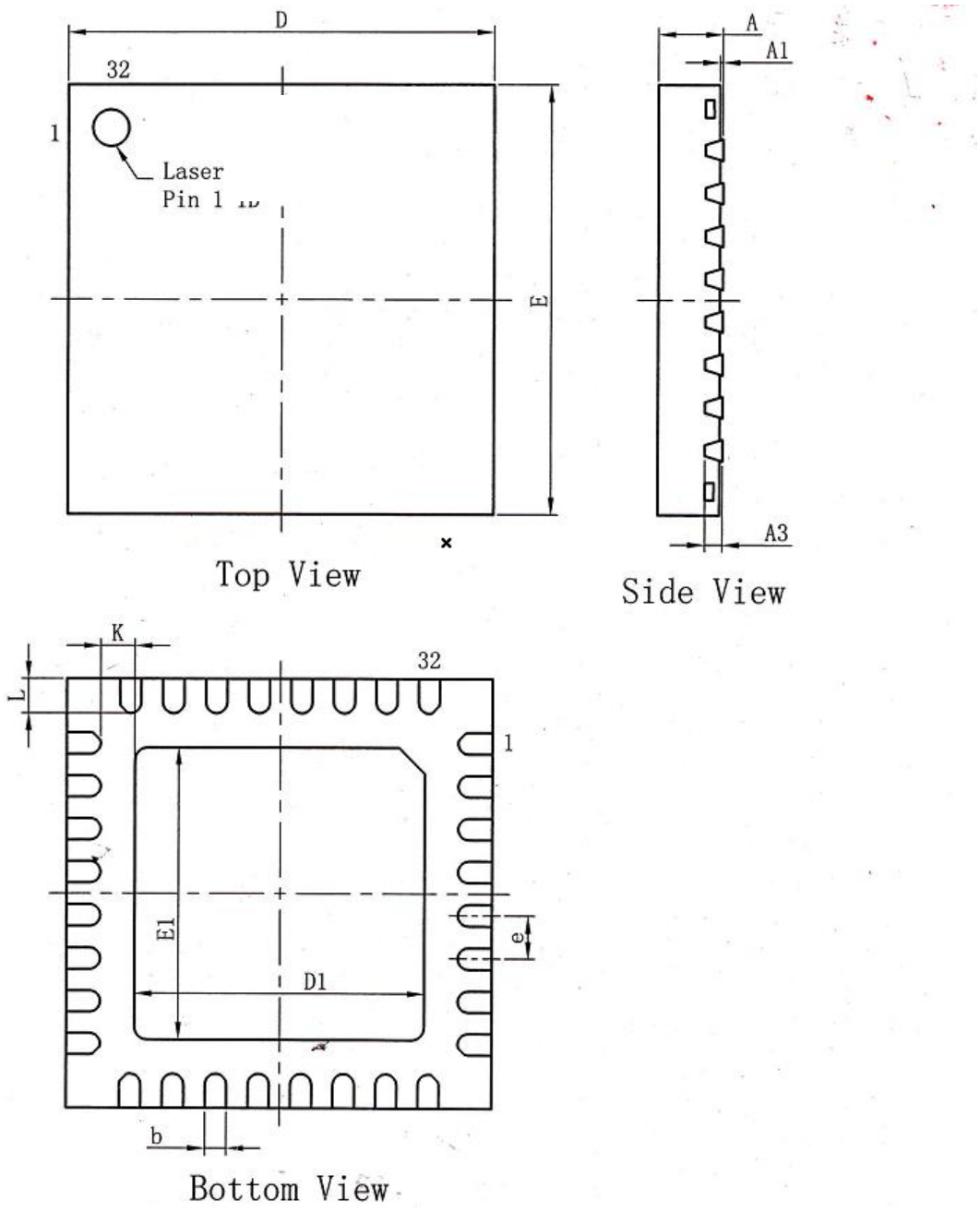
1. Place close to the protected pin with good (low resistive) and straight connection to the main ground.
2. Place close to the supply pin with good (low resistive) and straight connection to GNDP.
3. Place close to HCM8035´s VCC pin with good connection to GNDC.
4. Place close to card connector´s C1 (VCC) pin with good connection to GNDC.
5. Optional bridge. If not used, R1 must be 0 **Ω** and R2 absent (direct connection to $V_{DD(INTF)}$).
6. GNDP and GNDC are connected to the main ground with a straight and low resistive connection.
7. The card connector represented here has a normally closed presence switch.
8. DC/DC converter capacitance value:

   If VDDP=3.3v, C3=C4= 330nF & C5=1uF.

   If VDDP=5.0v, C3=C4= 100nF & C5=1uF.

Package Outline

QFN 32（5x5x0.75_0.5）



Dimensions

	A	A1	A3	b	D	E	D1	E1	e	K	L	Unit
max	0.80	0.05	-	0.30	5.10	5.10	3.50	3.50	-	0.20	0.32	mm
typ	0.75	0.02	0.20	0.25	5.00	5.00	3.40	3.40	0.50	-	0.40	
min	0.70	0.00	-	0.20	4.90	4.90	3.30	3.30	-	-	0.48	