RCL Semiconductors Ltd.

Tri–State Octal D-Type Flip-Flops (Edge Triggered) HC374

GENERAL DESCRIPTION

HC374 is fabricated in the high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

These 8-bit flip-flops with 3-state outputs are specifically designed for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

HC374 has octal positive edge triggered D-type flip-flops. On the positive transition of the clock (CK) input, data at the inputs D, meeting the setup and hold time requirement, are transferred to the Q outputs.

An output-enable input ($\overline{OE}$) places the eight outputs in either a normal logic state (H or L logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

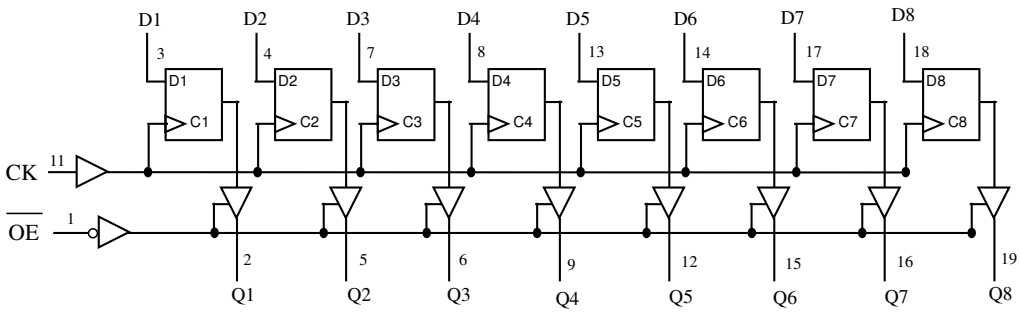
$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

$\overline{OE}$ should be tied to VDD through a pull-up resistor to ensure the high-impedance state during power up or power down,; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FEATURES

- Wide operating supply voltage range: 2-6V
- Output Drive at V_{DD} = 5V : ±6mA
- Typical propagation delay: 14ns
- Low input current: < 1μA
- Low quiescent supply current: 80μA maximum
- Octal D-type flip-flops in a single package
- Full Parallel access for Loading

LOGIC DIAGRAM



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FUNCTIONAL DESCRIPTION

Truth Table

Inputs			Outputs
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level.
Z = high impedance state
Q_0= The level of the output before steady state input conditions were established

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (V_{DD})	- 0.5 ~ + 7.0	V
DC input or output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{DD} +0.5	V
DC Current Drain per pin, any output (I_{out})	±35	mA
DC Current Drain per pin, V_{DD} or GND (Icc)	±70	mA
Storage Temperature(T_{STG})	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Normal	Max.	Unit
DC Supply Voltage (V_{DD})		2.0	5.0	6.0	V
V_{IH} High-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V	1.5 3.15 4.2			V
V_{IL} Low-level Input Voltage	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			0.5 1.35 1.8	V
V_I Input Voltage		0		V_{DD}	V
V_O Output Voltage		0		V_{DD}	V
Operating Temperature (TA)	74HC374	-40		+85	°C
	54HC374	-55		+125	°C
Input Rise/Fall Times (tr, tf)	V_{DD}=2.0V V_{DD}=4.5V V_{DD}=6.0V			1000 500 400	ns

Note: 2. All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

(unless otherwise specified)

Parameter	Test Conditions		VDD	TA =25 °C			54HC374		74HC374		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	V_I=V_{IH} or V_{IL}	I_{OH}= -20μA	2.0V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6.0V	5.9	5.999		5.9		5.9		
		I_{OH}= -6mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH}= -7.8mA	6.0V	5.48	5.8		5.2		5.34		
V_{OL}	V_I=V_{IH} or V_{IL}	I_{OL} = 20μA	2.0V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6.0V		0.001	0.1		0.1		0.1	
		I_{OL} = 6mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8mA	6.0V		0.15	0.26		0.4		0.33	
I_I	V_I=V_{DD} or 0		6.0V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O =V_{DD} or 0		6.0V		±0.01	±0.5		±10		±5	μA
Icc	V_I=V_{DD} or 0	I_O =0	6.0V			8		160		80	μA
Ci			2~6V		3	10		10		10	pF

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING TEMPERATURE RANGE (unless otherwise noted)

Parameter		VDD	TA =25 °C		54HC374		74HC374		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
fclock	Clock frequency	2.0V		6		4		5	MHz
		4.5V		30		20		24	
		6.0V		35		24		28	
t_w	Pulse duration, CK high or low	2.0V	80		120		100		ns
		4.5V	16		24		20		
		6.0V	14		20		17		
t_{su}	Setup time, data before CK↑	2.0V	100		150		125		ns
		4.5V	20		30		25		
		6.0V	17		25		21		
t_h	Hold time, data after CK↑	2.0V	10		13		12		ns
		4.5V	5		5		5		
		6.0V	5		5		5		

AC ELECTRICAL CHARACTERISTICS （CL = 50pF)

Parameter	From (Input)	To (Output)	VDD	TA =25 °C			54HC374		74HC374		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
f_{max}			2.0V	6	12		4		5		MHz
			4.5V	30	60		20		24		
			6.0V	35	70		24		28		
t_{pd}	CK	Any Q	2.0V		63	180		270		225	ns
			4.5V		17	36		54		45	
			6.0V		15	31		46		38	
t_{en}	$\overline{OE}$	Any Q	2.0V		60	150		225		190	ns
			4.5V		16	30		45		38	
			6.0V		14	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2.0V		36	150		225		190	ns
			4.5V		17	30		45		38	
			6.0V		16	26		38		32	
t_t		Any Q	2.0V		28	60		90		75	ns
			4.5V		8	12		18		15	
			6.0V		6	10		15		13	

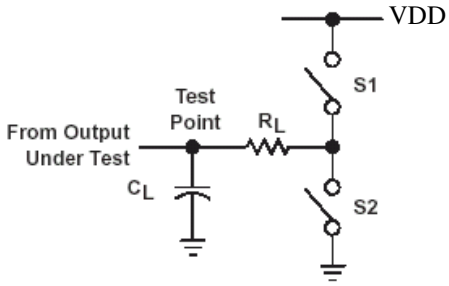
AC ELECTRICAL CHARACTERISTICS (CL = 150pF)

Parameter	From (Input)	To (Output)	VDD	TA =25 °C			54HC374		74HC374		Unit
				Min.	Typ.	Max	Min.	Max.	Min.	Max.	
f_{max}			2.0V	6	12				5		MHz
			4.5V	30	60				24		
			6.0V	35	70				28		
t_{pd}	CK	Any Q	2.0V		80	230		345		290	ns
			4.5V		22	46		69		58	
			6.0V		19	39		58		49	
t_{en}	$\overline{OE}$	Any Q	2.0V		70	200		300		250	ns
			4.5V		25	40		60		50	
			6.0V		22	34		51		43	
t_t			2.0V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6.0V		13	36		53		45	

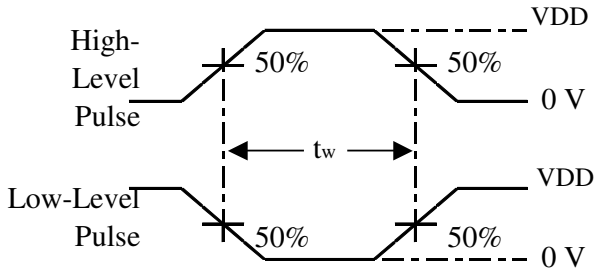
Parameter	Test Conditions	Typ.	Unit
C_{PD} Power Disspation Capitance	TA =25 °C , No Load	100	pF

Note 3: C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD}\cdot VDD^2\cdot f + Icc \cdot VDD$, and the no load dynamic current consumption, $Is = C_{PD}\cdot VDD\cdot f_i + Icc$

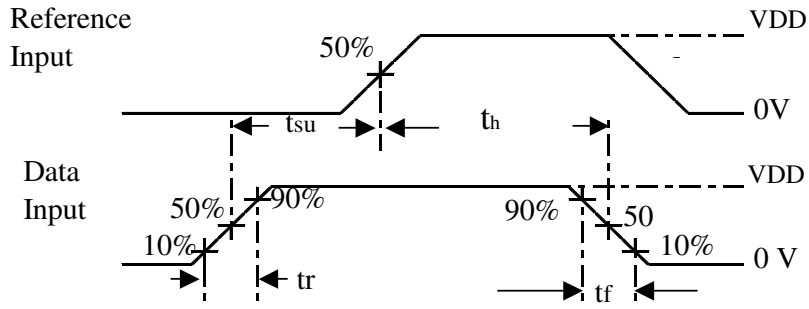
AC TEST CIRCUIT AND AC SWITCHING WAVEFORM



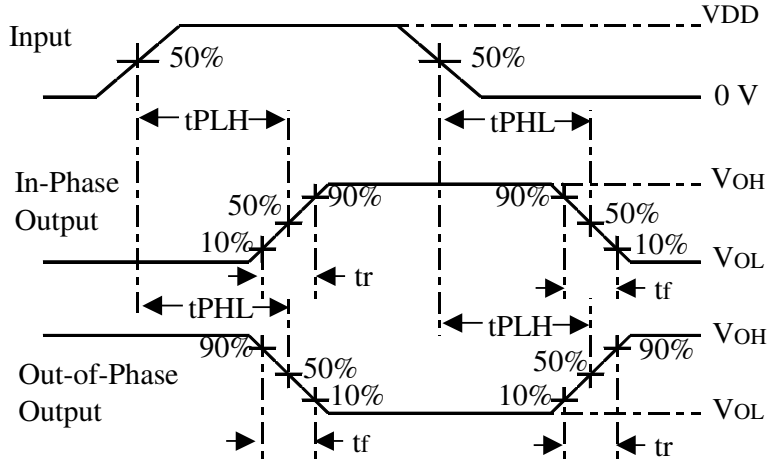
PARAMETER		R_L	C_L	S1	S2
ten	t_{PZH}	1kΩ	50pF or 150pF	Open	Closed
	t_{PZL}			Closed	Open
tdis	t_{PHZ}	1kΩ	50pF	Open	Closed
	t_{PLZ}			Closed	Open
tpd or t_t		---	50pF or 150pF	Open	Open



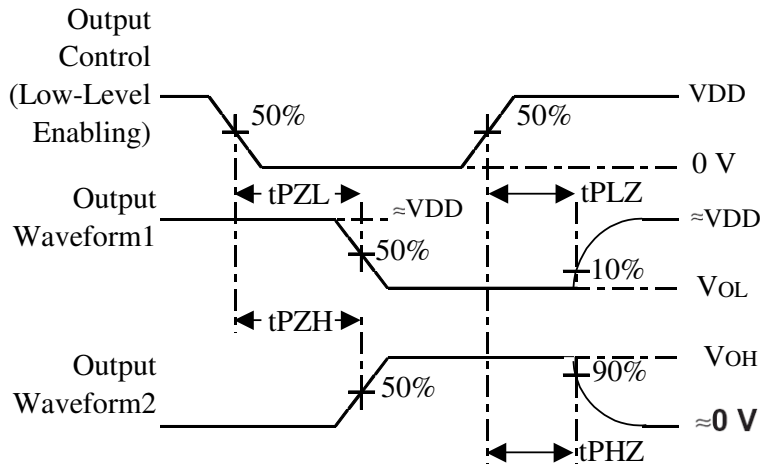
Voltage Waveforms
Pulse Durations



Voltage Waveforms
Setup and Hold and Input rise and Fall times



Voltage Waveforms
Propagation Delay and Output Transition Times



Voltage Waveforms
Enable and disable times for 3-state outputs

NOTES 4: 1) C_L includes probe and test-fixture capacitance.

2) Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3) Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:

PRR δ 1 MHz, Z_O = 50Ω ., tr = 6 ns, tf = 6 ns.

4) For clock inputs, fmax is measured when the input duty cycle is 50%.

5) The outputs are measured one at a time with one input transition per measurement.

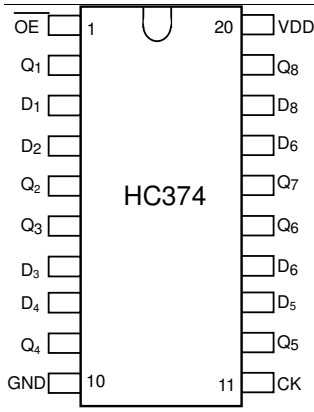
6) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

7) t_{PZL} and t_{PZH} are the same as t_{en}.

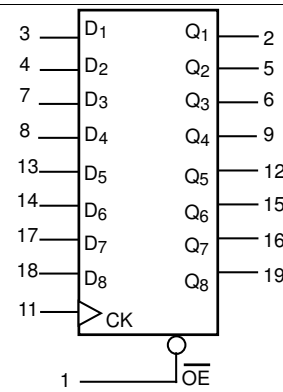
8) t_{PLH} and t_{PHL} are the same as t_{pd}.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
3, 4, 7, 8, 13, 14, 17, 18	D1– D8	Data Inputs
2, 5, 6, 9, 12, 15, 18, 19	Q1 – Q8	Outputs
10	GND	Ground (0V)
11	CK	Clock input (active at rising edge)
1	$\overline{OE}$	Output Enable
20	VDD	Positive power supply

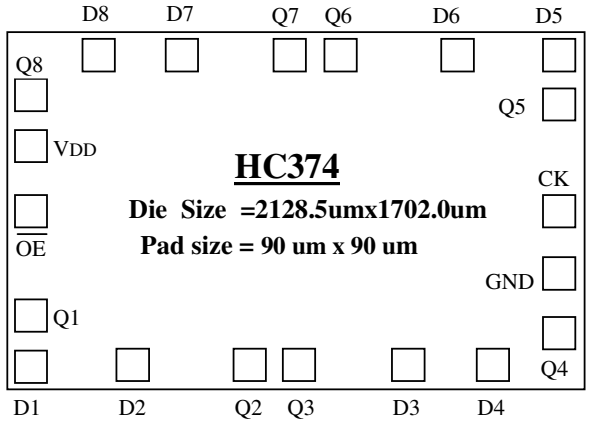


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

Q1	(-779.8, -337.8)	Q5	(689.5, 247.7)
D1	(-779.8, -977.7)	D5	(689.5, 387.7)
D2	(-496.0, -977.7)	D6	(405.7, 387.7)
Q2	(-171.0, -977.7)	Q6	(80.7, 387.7)
Q3	(- 31.0, -977.7)	Q7	(-59.3, 387.7)
D3	(273.5, -977.7)	D7	(-363.8, 387.7)
D4	(502.3, -977.7)	D8	(-592.6, 387.7)
Q4	(689.5, -385.7)	Q8	(-779.8, 274.1)
GND	(689.5, -224.1)	VDD	(-779.8, 134.1)
CK	(689.5, -45.1)	$\overline{OE}$	(-779.8, -44.9)

Note: Substrate should be connected to VDD or left it open.

PAD IDENTIFICATION