XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F420 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

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Product Features

- 84 MHz Cortex-M4 32-bit CPU platform
- 128 K bytes FLASH memory, with erase and write protection function
- 24 K bytes RAM memory
- 6-channel DMAC
- Up to 52 general-purpose I/O pins
- Clock, crystal oscillator
  - External high-speed crystal oscillator 8 MHz~32 MHz
  - Internal high-speed clock 22 MHz~24 MHz
  - Internal low-speed clock 38.4 KHz and 32.768 KHz configurable
  - PLL clock up to 84 MHz
  - Hardware supports clock real-time calibration and mutual monitoring
- Timer/Counter
  - 3 composite timers
  - 9 basic timers: BTIM0~8
  - 3 general purpose timers: GTIM0~2
  - 1 high-performance 3-channel complementary output 16-bit timer / counter
  - 1 high-performance 1-channel complementary output 16-bit timer / counter
  - 1 independent IWDT, built-in dedicated 10 KHz oscillator provides IWDT counting
  - 1 window WWDT
  - 1 CTRIM clock calibration, can be used as a basic timer
- Communication interface
  - 4-channel USART standard communication interface
  - 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
- Hardware CRC-16/32 module
- Globally unique 6-byte ID number
- Integrates two high-speed and high-precision SARADCs with 12-bit 1 Msps sampling, up to 16 channels, and internal integrated temperature sensor
- 2-way voltage comparator with integrated 64-level voltage programmable reference input
- Integrated low voltage detector LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40~105 ℃, 2.0~5.5 V
- Package type: LQFP64/48, QFN48/32

Support Model

HC32F420FAUB-QFN32TR	HC32F420JAUB-QFN48TR
HC32F420JATB-LQ48	HC32F420KATB-LQFP64

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1 Overview

The HC32F420 series is a 32-bit microcontroller with a high-performance ARM® Cortex®-M4 core. The operating voltage range is 2.0 ~ 5.5 V and the operating temperature range is -40 ~ 105 °C. It has rich peripheral configurations and a variety of Working mode to apply to different application scenarios.

This product provides a variety of packaging forms, and the peripheral configurations are different in each packaging form.

Typical Application

- Internet of things application, smart home
- Smart meters, smart transportation, medical equipment, handheld devices
- Motor application, frequency conversion control
- Alarm systems, printers, scanners and other industrial applications

2 Product lineup

2.1 Product name

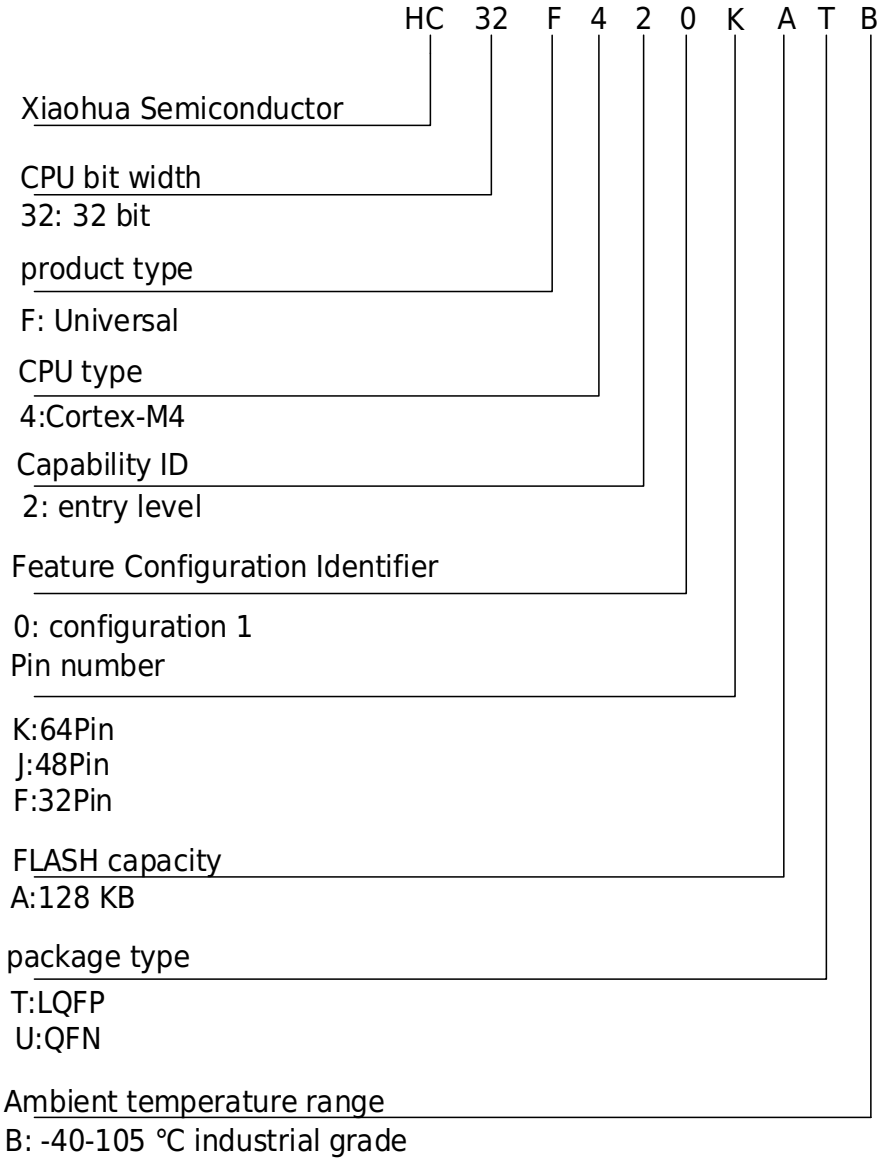


Figure 2-1 Product name

2.2 Product Features

Table 2-1 Product Features

Function		Product Model			
		HC32F420FAUB	HC32F420JAUB	HC32F420JATB	HC32F420KATB
Pin number		32	48	48	64
Number of GPIOs		27	38	38	52
Encapsulation		QFN	QFN	LQFP	LQFP
Temperature range		-40 ~ 105 ℃			
Supply voltage range		2.0 ~ 5.5 V			
Memory	Flash	128 KB			
	SRAM	24 KB			
DMAC		6			
Port interrupt		27	38	38	52
Communcation Interfaces	USART	4			
	SPI	2			
	I2C	2			
Timers	Composite timer	CTIM0/1/2			
	Advanced timer	ATIM0/3			
	IWDT	1			
	WWDT	1			
Analog	12bit ADC	2 10 channels	2 10 channels	2 10 channels	2 16 channels
	VC	2			
	OTS	✓			
Timer	RCH	22 ~ 24 MHz			
	RCL	32.768/38.4 KHz			
	XTH	8 ~ 32 MHz			
	PLL	15 ~ 84 MHz			
Unique Identifier (UID)		✓			
Low Voltage Detector (LVD)		✓			
Debug interface		SWD			

3 Functional module

3.1 Functional block diagram

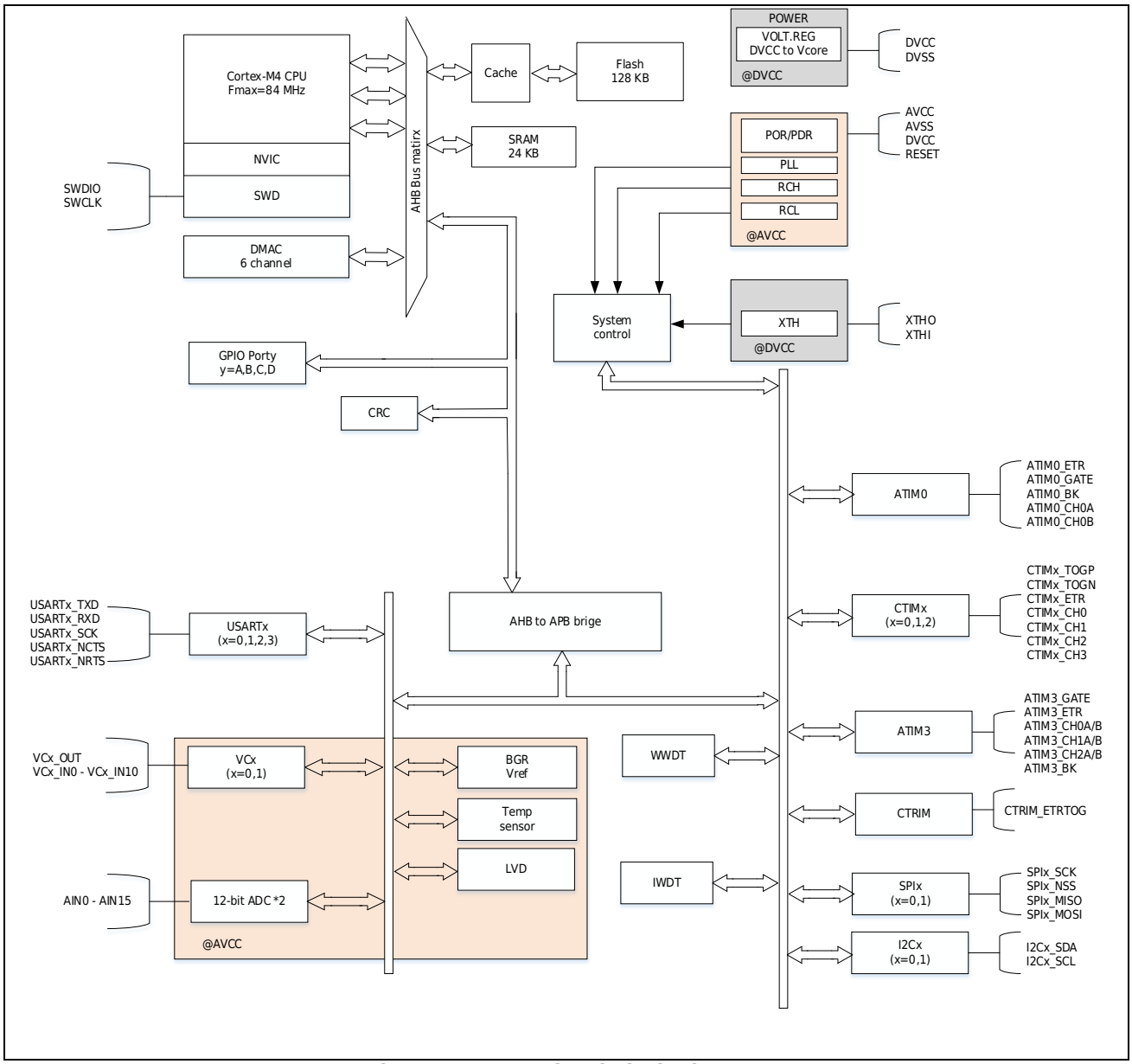


Figure 3-1 Functional Block Diagram

3.2 32 -bit CORTEX M4 core

The ARM® Cortex®-M4 processor includes a 32-bit RISC processor.

Table 3-1 Kernel description

Classification	Note
Architecture	Armv7E-M Harvard
MPU	Not present
ISA Support	Thumb/Thumb-2
Pipeline	3-stage + branch speculation
DSP Extensions	Single cycle 16/32-bit MAC Single cycle dual 16-bit MAC 8/16-bit SIMD arithmetic Hardware Divide (2-12 Cycles)
Interrupts	Non-maskable Interrupt (NMI+ 1 to 64 physical interrupts)
Interrupt Priority Levels	8 priority levels
Wake-up Interrupt Controller	Up to 64 Wake-up Interrupts
Sleep Modes	Integrated WFI and WFE Instructions and Sleep On Exit capability. Sleep & Deep Sleep Signals.
Bit Manipulation	Integrated Instructions & Bit Banding
Trace	Not support
Debug	Serial Wire Debug ports. Up to 8 Breakpoints and 4 Watchpoints.

3.3 128 K Byte FLASH controller

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming Support ISP, IAP, ICP functions.

3.4 24 K Byte RAM controller

Support byte (8-bit), half-word (16-bit), word (32-bit) three kinds of read and write operations, zero waiting period.

In Deep Sleep mode, RAM data is preserved.

3.5 Clock system

Support frequency division and switching of different clock sources.

Peripheral clocks can be enabled or disabled individually.

3.6 Operating mode

- Active Mode: CPU running, peripheral function modules running.
- Sleep Mode: The CPU stops running, and the peripheral function modules run.
- Deep sleep mode: The CPU stops running, the high-speed clock stops, and the low-power function modules run.

3.7 General IO port

Up to 52 GPIO ports can be provided, some of which are multiplexed with analog ports.

- Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes.
- Support position, clear, and clear operations.
- Support push-pull output, open-drain output.
- Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function.
- Output drive capability is configurable.

3.8 Interrupt controller

The ARM® Cortex®-M4 processor has a built-in nested vectored interrupt controller (NVIC). This product supports up to 64 interrupt request (IRQ) inputs; there are eight interrupt priorities, which can handle complex logic and enable real-time control and interrupt handling.

3.9 Reset controller

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset, and the program counter PC will point to the starting address.

Table 3-2 Interrupt sources

Serial number	Interrupt source
1	Power-on power-down reset POR PDR
2	External Reset Pin reset
3	IWDT reset
4	WWDT reset
5	Cortex-M4 LOCKUP hardware reset
6	Cortex-M4 SYSRESETREQ software reset
7	LVD reset

3.10 DMA controller

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.
- Composed of 6 channels, capable of performing 6 independent DMA transfers.
- You can set the transfer destination address, transfer source address, transfer data size, transfer request source and transfer mode, and can control the start of transfer operation and the forced termination of transfer for each channel.

- Support multiple hardware trigger sources to trigger DMA transfer.
- Comply with system bus (AHB) and support 32-bit address space (4 GB).

3.11 Timer/counter

Table 3-3 Timer Features

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Advanced timer	ATIM0	16/32	1/2/4/8/16 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	ATIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Composite timer	CTIM0/1/2	16	1~32768	Up count	4	4	No

The composite timer CTIM of each unit can be configured as a general-purpose timer that supports 4- way comparison and capture functions, or as 3 basic timers.

The advanced timer includes two timers ATIM0 and ATIM3, whose characteristics are as follows:

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

ATIM0 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reload function, or as a 32-bit timer/counter without reload function. ATIM0 has 2-way capture compare function, which can generate 2-way PWM independent output or 1 group of PWM complementary output. With dead zone control function.

ATIM3 is a multi-channel general-purpose timer with all the functions of ATIM0. It can generate 3 groups of PWM complementary outputs or 6 channels of PWM independent output, and a maximum of 6 channels of input capture. With dead zone control function.

3.12 Clock Calibrator CTRIM

The clock calibration timer can calibrate the RCH/RCL clock frequency, and when the RCH real-time calibration is enabled, and there is an accurate reference clock in the system, the full working range of the RCH can be calibrated to an accuracy of 0.5 %.

The Clock Calibration Timer can also be used as a general-purpose timer or an automatic wake-up timer.

3.13 Watchdog

IWDT is a configurable 12-bit timer that provides reset when MCU is abnormal; built-in 10 KHz low-speed clock input as counter clock. In debug mode, you can choose to pause or continue to run; IWDT can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

3.14 Universal synchronous asynchronous transceiver USART

This product is equipped with 4-way universal synchronous asynchronous transceiver module (USART). Universal synchronous asynchronous transceiver module (USART) can flexibly perform full-duplex data exchange with external devices; this USART supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, smart card interface (ISO/ IEC7816-3), Infrared protocol (IrDA and 38 K modulation), LIN protocol. Support hardware flow control operation (CTS/ RTS operation), multi-processor operation. The timer inside the module cooperates to support UART receiving and sending timeout function, synchronization interval measurement and automatic baud rate automatic detection.

3.15 Synchronous Serial Interface SPI

This product is equipped with 2-way synchronous serial interface, which can be used for synchronous serial communication between MCU and external devices. This module supports full-duplex, single-line half-duplex and simplex communication.

- Can be configured as master or slave, support multi-machine mode
- The maximum communication rate of host mode is 24 Mbps
- The maximum communication rate of the slave mode is 12 Mbps

3.16 I2C bus

This product is equipped with 2-way I2C and adopts serial synchronous clock, which can realize data transmission between devices at different rates.

- Support standard (100 Kbps)/ fast (400 Kbps)/ high speed (1 Mbps) three working rates
- Support 7-bit addressing function

3.17 Unique identification number UID

Each chip has a unique 6-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID addresses are: 0x0100 14E0 - 0x0100 14E5.

3.18 CRC16/32 hardware cyclic redundancy check code

- CRC16 algorithm reference model CRC-16/X25, polynomial is 0x1021.
- CRC32 algorithm reference model CRC-32, polynomial is 0x04C1 1DB7.

3.19 12 Bit SARADC

This product is equipped with 2 channels of 12- bit successive approximation high-precision analog-to-digital converters, and the sampling rate of a single ADC reaches 1 Msps.

- 18 input channels, including 16 external pin inputs, 1 internal temperature sensor voltage, 1 AVCC/3
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5 V reference voltage, built-in 2.5 V reference voltage
- 3 conversion modes: single conversion, sequential scan continuous conversion, continuous conversion accumulation
- Built-in voltage follower to measure signals with high output impedance
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion

3.20 Voltage comparator VC

This product is equipped with 2-way VC, which is used to compare the magnitude of two input analog voltages, and output high/low level according to the comparison result.

- 11 configurable positive external input channels
- 11 configurable negative external input channels
- 4 internal negative input channels
  - 1 internal temperature sensor voltage
  - Reference voltage configured by 1 ADC module
  - 1- way 64-step resistor divider
  - 1 core voltage

3.21 Low Voltage Detector LVD

Detect chip power supply voltage or chip pin voltage.

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07
- 16- step threshold voltage
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results, reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

3.22 Embedded debugging system

The core of this MCU is ARM® Cortex®-M4, which includes hardware for advanced debugging functions.

- Support SWD debugging interface
- Support Keil/IAR and other debugging and development software

3.23 In-line programming mode

This product supports in-circuit programming (ISP).

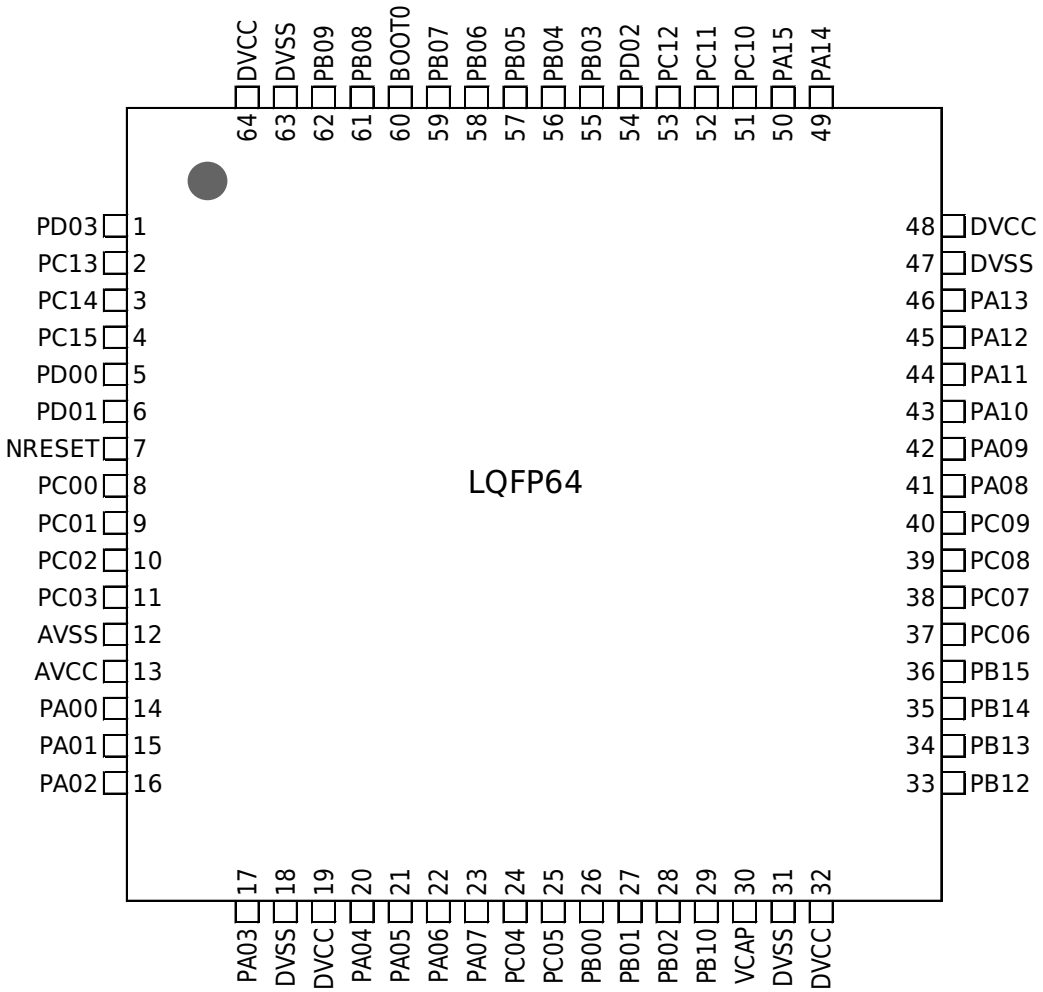
- Use UART interface
- Multiplexing of UART interface and SWD interface

3.24 High security

The built-in FLASH of this product supports 4 levels of read protection, and the current protection level can be read through the FLASH_LOCKSTATE register. When programming the chip with a programmer, the read protection level of FLASH can be configured.

4 Pin Configuration and Functions (Pinouts)

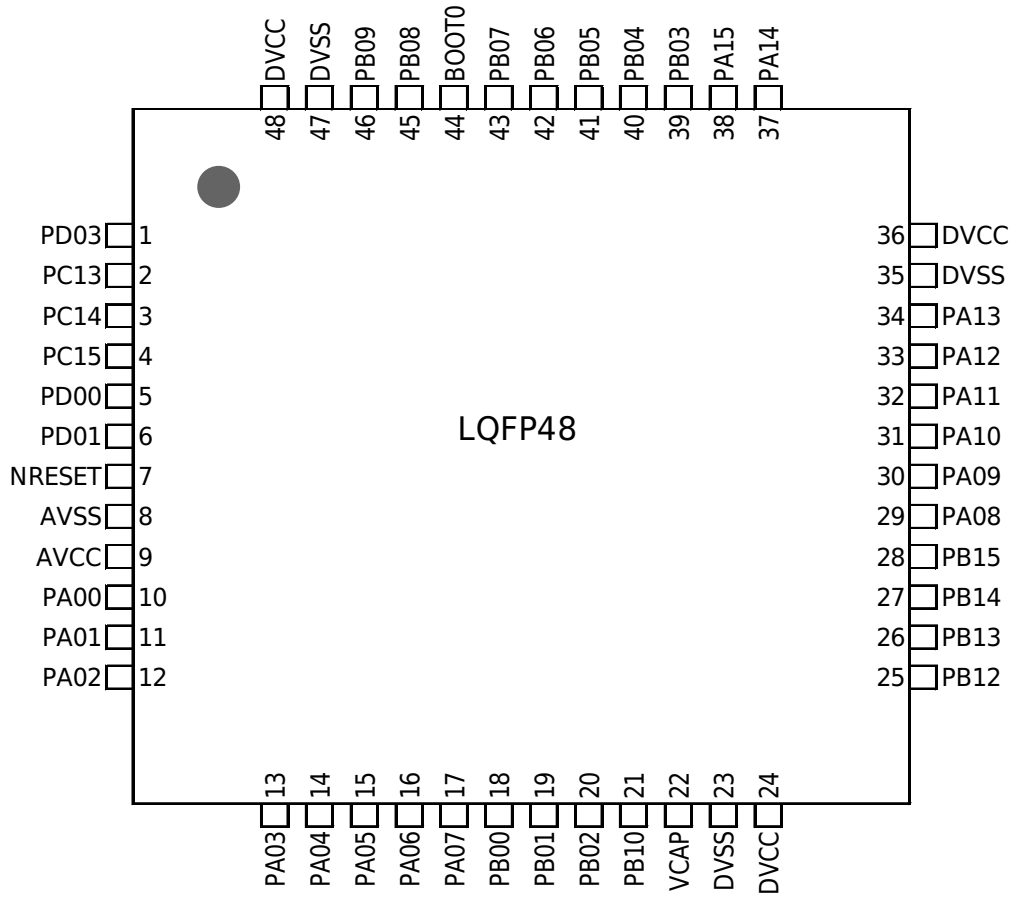
4.1 Pin Configuration Diagram



Note:

– *The BOOT0 pin is used to control FLASH programming, see [4.3 Module signal description] for details.*

Figure 4-1 LQFP64 pin configuration diagram

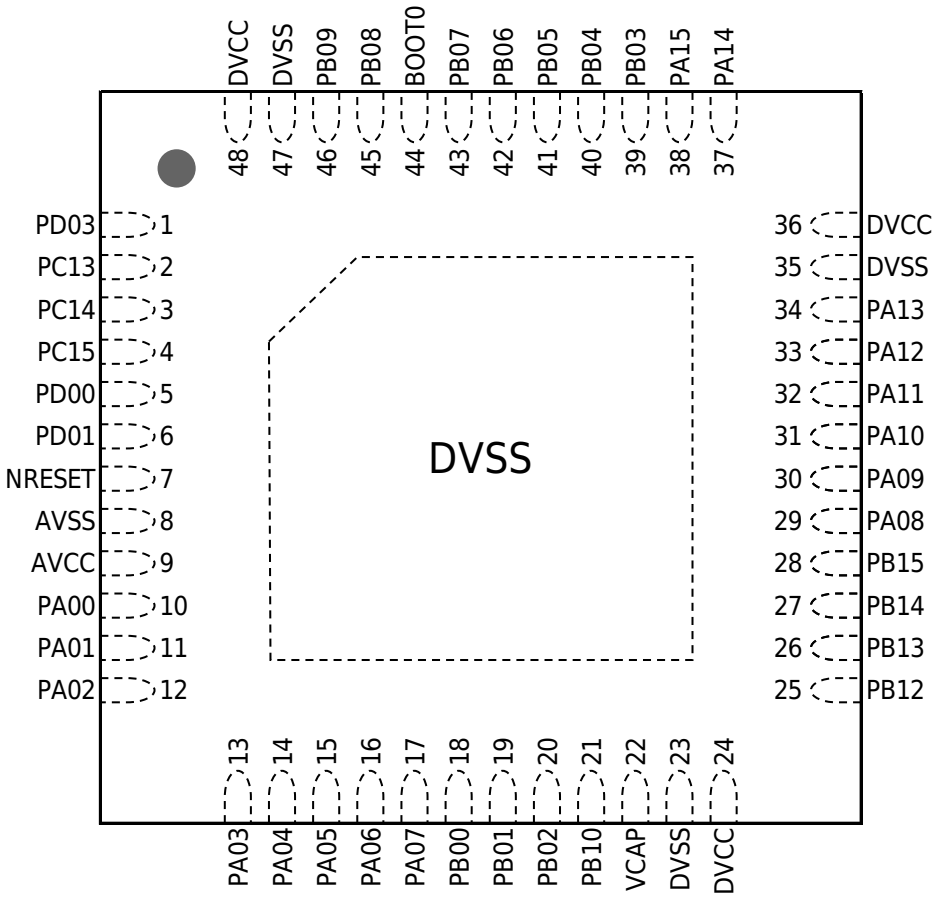


Note:

– *For details of the IO not drawn out of this package, see [4.2 Pin Function Table].*

– *The BOOT0 pin is used to control FLASH programming, see [4.3 Module signal description] for details.*

Figure 4-2 LQFP48 Pin Configuration Diagram

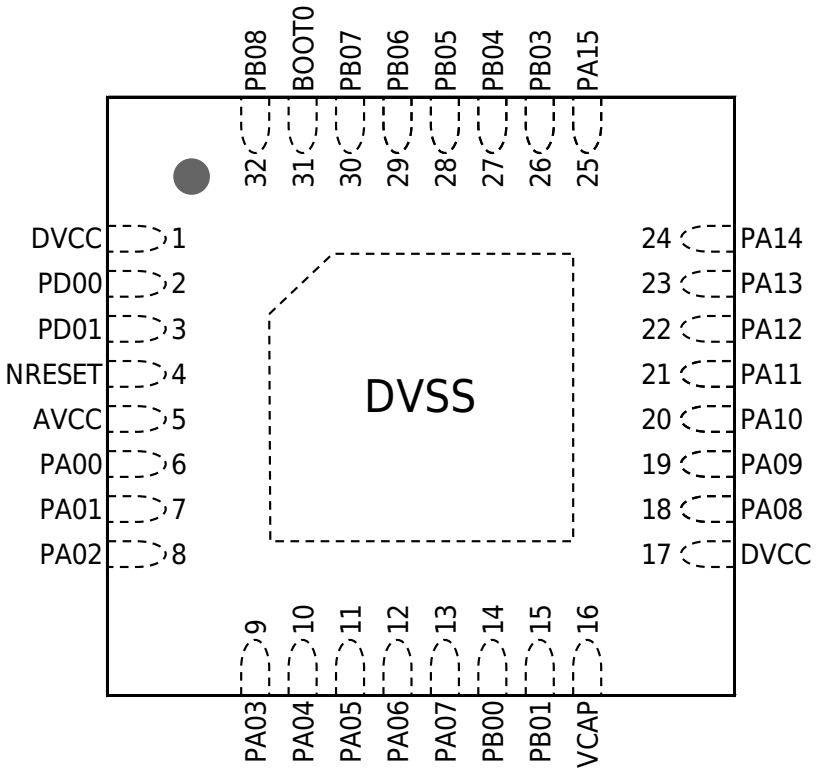


Note:

– *For details about the IO not exported by this package, see [4.2 Pin Function Table].*

– *The BOOT0 pin is used to control FLASH programming, see [4.3 Module signal description] for details.*

Figure 4-3 QFN48 pin configuration diagram



Note:

- *For details about the IO not exported by this package, see [4.2 Pin Function Table].*
- *The BOOT0 pin is used to control FLASH programming, see [4.3 Module signal description] for details.*

Figure 4-4 QFN32 pin configuration diagram

4.2 Pin Function Table

Table 4-1 Pin Function Description

LQFP64	LQFP48/QFN48	QFN32	Pin Name	Analog	Digital Function					
					GPIO	AF1	AF2	AF3	AF4	AF5
1	1	-	PD03		PD03	ATIM0_BK	CTIM0_CH0	CTIM1_TOGP	ATIM3_BK	USART2_TXD
2	2	-	PC13	LVDIN0	PC13	SPI0_SCK	CTIM2_CH0	I2C1_SCL	ATIM3_CH0A	USART3_NCTS
3	3	-	PC14		PC14	SPI0_MISO	CTIM2_CH1	I2C1_SDA	ATIM3_CH1A	USART3_NRTS
4	4	-	PC15		PC15	SPI0_MOSI	CTIM2_ETR		ATIM3_CH2A	USART3_SCK
5	5	2	PD00	XTHI	PD00	SPI0_CS	CTIM0_CH2	I2C0_SCL	ATIM3_CH0B	I2C1_SCL
6	6	3	PD01	XTHO	PD01	LVD_OUT	CTIM0_CH3	I2C0_SDA	ATIM3_CH2B	I2C1_SDA
7	7	4	NRESET							
8	-	-	PC00	AIN10	PC00	ATIM0_BK	CTIM1_TOGP	CTRIM_ETRTOG	SPI0_MISO	
9	-	-	PC01	AIN11	PC01	ATIM0_CH0A	CTIM1_TOGN		SPI0_MOSI	
10	-	-	PC02	AIN12	PC02	ATIM0_CH0B		SPI0_CS	SPI1_MISO	USART0_NCTS
11	-	-	PC03	AIN13	PC03	ATIM0_GATE		SPI0_SCK	SPI1_MOSI	USART0_NRTS
12	8	-	AVSS							
13	9	5	AVCC							
14	10	6	PA00	AIN0/VCIN0	PA00	ATIM0_ETR	CTIM0_CH0	CTIM0_ETR	VC0_OUT	USART1_NCTS
15	11	7	PA01	AIN1/VCIN1	PA01	MCO	CTIM0_CH1	SPI1_CS	USART2_NCTS	USART1_NRTS
16	12	8	PA02	AIN2/VCIN2	PA02	CTIM1_TOGN	CTIM0_CH2	VC1_OUT	USART3_NRTS	USART1_TXD
17	13	9	PA03	AIN3/VCIN3	PA03	LVD_OUT	CTIM0_CH3	SPI1_SCK	USART3_TXD	USART1_RXD
18	-	-	DVSS							
19	-	-	DVCC							
20	14	10	PA04	AIN4/VCIN4	PA04	ATIM3_CH0A	PCLK0_OUT	SPI0_CS	USART3_RXD	USART1_SCK

LQFP64	LQFP48/QFN48	QFN32	Pin Name	Analog	Digital Function					
					GPIO	AF1	AF2	AF3	AF4	AF5
21	15	11	PA05	AIN5/VCIN5	PA05	ATIM3_CH1A	CTIM0_CH0	CTIM0_ETR	USART3_NCTS	SPI0_SCK
22	16	12	PA06	AIN6	PA06	ATIM3_CH2A	USART2_RXD	CTIM1_CH0	ATIM3_BK	SPI0_MISO
23	17	13	PA07	AIN7	PA07	ATIM3_CH0B	USART3_TXD	CTIM1_CH1	USART2_NRTS	SPI0_MOSI
24	-	-	PC04	AIN14	PC04	ATIM3_CH1B		I2C0_SCL		USART0_SCK
25	-	-	PC05	AIN15	PC05	ATIM3_CH2B	CTIM0_TOGP	I2C0_SDA	ATIM0_ETR	
26	18	14	PB00	AIN8/VCIN6	PB00	ATIM3_CH1B	CTIM2_ETR	CTIM1_CH2	ATIM0_CH0A	USART3_SCK
27	19	15	PB01	AIN9/ExRef/VCIN7	PB01	ATIM3_CH2B	CTIM2_TOGP	CTIM1_CH3	ATIM0_CH0B	PCLK1_OUT
28	20	-	PB02		PB02	CTIM0_CH3	CTIM2_TOGN	ATIM3_GATE	ATIM0_GATE	USART2_RXD
29	21	-	PB10		PB10	CTIM0_CH2			I2C1_SCL	USART2_TXD
30	22	16	VCAP							
31	23	-	DVSS							
32	24	17	DVCC							
33	25	-	PB12	VCIN8	PB12	I2C0_SCL	ATIM3_BK	CTRIM_ETRTOG	SPI1_CS	USART2_SCK
34	26	-	PB13		PB13	I2C0_SDA	ATIM3_CH0B		SPI1_SCK	USART2_NCTS
35	27	-	PB14		PB14		ATIM3_CH1B	CTIM1_TOGP	SPI1_MISO	USART2_NRTS
36	28	-	PB15		PB15	MCO	ATIM3_CH2B	CTIM1_TOGN	SPI1_MOSI	
37	-	-	PC06		PC06	ATIM3_ETR	CTIM2_CH0	CTIM1_CH0		USART2_NCTS
38	-	-	PC07		PC07		CTIM2_CH1	CTIM1_CH1	SPI1_SCK	USART2_NRTS
39	-	-	PC08		PC08	I2C1_SCL	CTIM2_CH2	CTIM1_CH2		USART2_SCK
40	-	-	PC09		PC09	I2C1_SDA	CTIM2_CH3	CTIM1_CH3		
41	29	18	PA08		PA08	CTIM0_TOGP	ATIM3_CH0A	CTRIM_ETRTOG	USART3_RXD	USART0_SCK
42	30	19	PA09		PA09	CTIM0_TOGN	ATIM3_CH1A	ATIM0_BK	CTIM1_CH2	USART0_TXD
43	31	20	PA10		PA10	I2C1_SCL	ATIM3_CH2A	ATIM0_CH0A	CTIM1_CH3	USART0_RXD

LQFP64	LQFP48/QFN48	QFN32	Pin Name	Analog	Digital Function					
					GPIO	AF1	AF2	AF3	AF4	AF5
44	32	21	PA11		PA11	VC0_OUT	ATIM3_GATE	ATIM0_CH0B	USART1_NCTS	USART0_NCTS
45	33	22	PA12		PA12	VC1_OUT	ATIM3_ETR	ATIM0_GATE	USART1_NRTS	USART0_NRTS
46	34	23	SWDIO/PA13		PA13	ATIM3_BK	CTIM2_CH2	ATIM0_ETR	USART1_RXD	I2C0_SCL
47	35	-	DVSS							
48	36	-	DVCC							
49	37	24	SWCLK/PA14		PA14	CTIM0_CH1	CTIM2_CH3	USART2_SCK	USART1_TXD	I2C0_SDA
50	38	25	PA15		PA15	SPI0_CS	CTIM1_CH0	CTIM1_ETR	USART1_SCK	USART0_TXD
51	-	-	PC10		PC10		USART3_TXD		ATIM3_CH0A	ATIM0_CH0A
52	-	-	PC11		PC11	CTIM0_TOGN	USART3_RXD		ATIM3_CH1A	ATIM0_CH0B
53	-	-	PC12		PC12		USART3_NCTS	CTIM2_ETR	ATIM3_CH2A	ATIM0_GATE
54	-	-	PD02		PD02		USART3_NRTS	CTIM1_ETR	ATIM3_CH0B	ATIM0_ETR
55	39	26	PB03		PB03	CTIM0_CH1	USART0_RXD	I2C1_SDA	ATIM3_CH1B	SPI0_SCK
56	40	27	PB04	VCIN9	PB04	CTIM1_CH0	CTIM2_TOGP	PCLK0_OUT	ATIM3_CH2B	SPI0_MISO
57	41	28	PB05	VCIN10	PB05	CTIM1_CH1	CTIM2_TOGN	USART3_SCK	USART2_TXD	SPI0_MOSI
58	42	29	PB06		PB06	USART0_TXD	CTIM2_CH0	SPI1_MISO	I2C0_SCL	USART2_RXD
59	43	30	PB07	LVDIN1	PB07	USART0_RXD	CTIM2_CH1	SPI1_MOSI	I2C0_SDA	PCLK1_OUT
60	44	31	BOOT0/PB11		PB11					
61	45	32	PB08	LVDIN2	PB08	CTRIM_ETRTOG	CTIM2_CH2		I2C0_SCL	ATIM0_BK
62	46	-	PB09		PB09	SPI1_CS	CTIM2_CH3	I2C0_SDA	I2C1_SDA	
63	47	-	DVSS							
64	48	1	DVCC							

Note:

– *The IO port is reset to the analog input state, and the sleep mode and deep sleep mode maintain the previous port state.*

4.3 Module signal description

Table 4-2 Module Signal Description

Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	VCAP	LDO core power supply output (Only for internal circuit use, an external decoupling capacitor is required, see [6.1.3 Power sipply scheme] for capacitance value)
ISP	BOOT0	On power-up, external RESET pin, and LVD reset: BOOT0 enters the online programming mode at a high level, and online programming can be performed through the host computer; BOOT0 is the working mode for low level.
XTH	XTHI	XTH input
	XTHO	XTH Output
ADC	AIN0~AIN15	ADC input channel 0-15
	ExRef	ADC external reference voltage
VC	VCIN0~VCIN10	VC input 0-10
	VC0_OUT	VC0 comparison output
	VC1_OUT	VC1 comparison output
LVD	LVDIN0	Voltage detection input 0
	LVDIN1	Voltage detection input 1
	LVDIN2	Voltage detection input 2
	LVD_OUT	Voltage detection output
USART x=0,1,2,3	USARTx_TXD	USART data transmitter
	USARTx_RXD	USART data receiver
	USARTx_SCK	USART working clock
	USARTx_NCTS	USART hardware flow control CTS input
	USARTx_NRTS	USART hardware flow control RTS output
SPI x=0,1	SPIx_MISO	SPI module host input and slave output data signal
	SPIx_MOSI	SPI module master output slave input data signal
	SPIx_SCK	SPI module clock signal
	SPIx_NSS	SPI slave select signal
I2C x=0,1	I2Cx_SDA	I2C module data signal
	I2Cx_SCL	I2C module clock signal
Composite timer CTIMx x=0,1,2 y=0,1,2,3	CTIMx_CHy	Timer capture input compare output
	CTIMx_TOGP	Timer 's TOGP pin output
	CTIMx_TOGN	Timer 's TOGN pin output
	CTIMx_ETR	External input signal of Timer
Advanced timer	ATIM0_CHyA	Timer capture input compare output A

Modules	Pin name	Description
ATIM0 y=0	ATIM0_CHyB	Timer's capture input compare output B
	ATIM0_ETR	External input signal of Timer
	ATIM0_GATE	Timer gate signal
	ATIM0_BK	Timer brake control signal
Advanced timer ATIM3 y=0,1,2	ATIM3_CHyA	Timer capture input compare output A
	ATIM3_CHyB	Timer's capture input compare output B
	ATIM3_ETR	External input signal of Timer
	ATIM3_GATE	Timer gate signal
	ATIM3_BK	Timer brake control signal
Clock calibrator CTRIM	CTRIM_ETRTOG	CTRIM 's external clock input, reverse output

5 Typical application circuit diagram

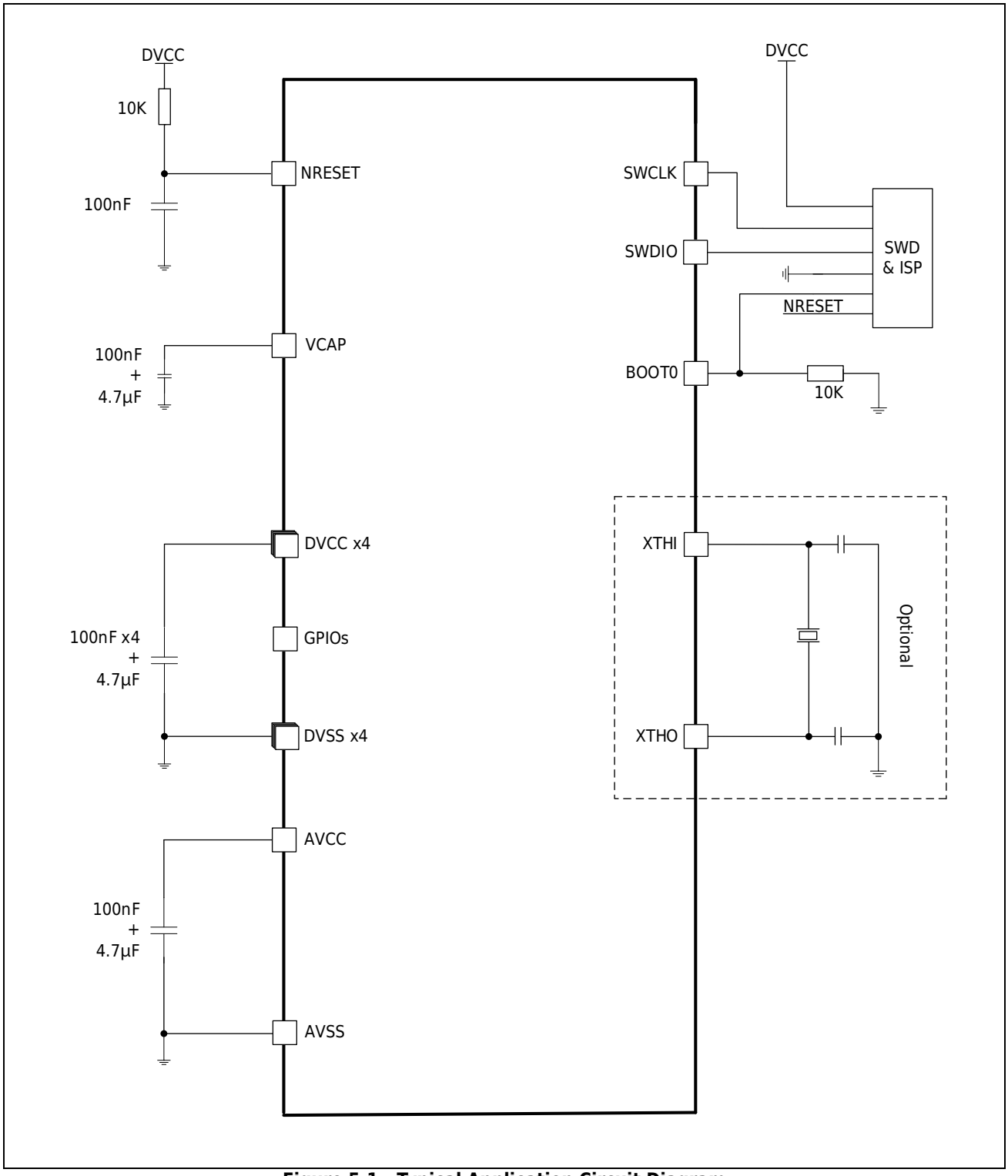


Figure 5-1 Typical Application Circuit Diagram

Note:

– *Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.*

6 Electrical characteristics

6.1 Test Conditions

All voltages are referenced to VSS unless otherwise noted.

6.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed under the worst-case environmental temperature, power supply voltage, and clock frequency conditions on the production line by conducting tests on 100 % of the products at ambient temperatures T_A=25 °C and T_A=T_{Amax} (T_{Amax} matching the selected temperature range).

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3 Σ).

6.1.2 Typical value

Unless otherwise specified, typical data is based on T_A=25 °C and VCC=3.3 V (2.0 V ≤ VCC ≤ 5.5 V voltage range). These data are only used for design guidance and not tested.

6.1.3 Power supply scheme

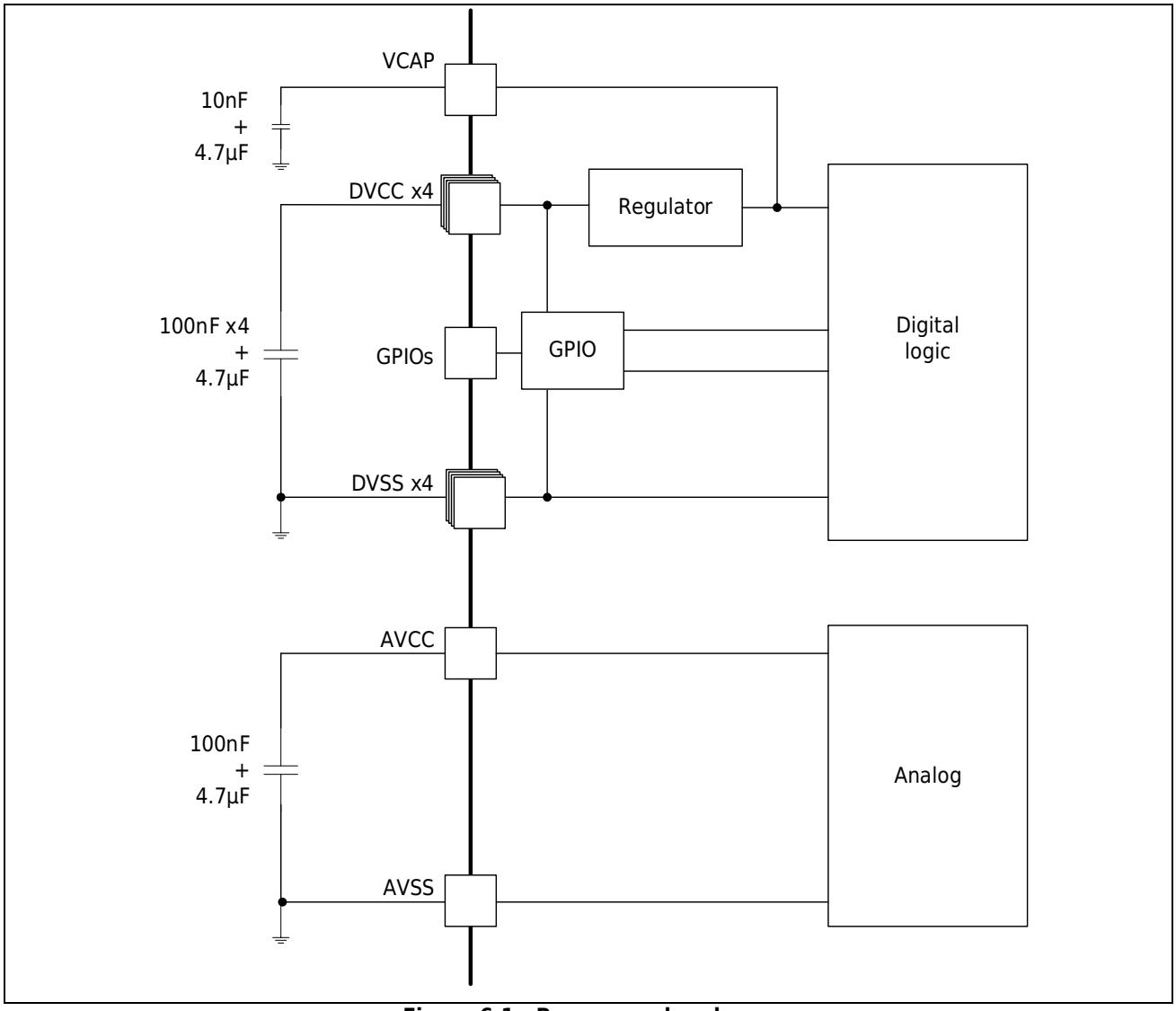


Figure 6-1 Power supply scheme

Note:

– *Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.*

6.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 6-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS - 0.3	VCC + 0.3	V
$\lvert \Delta VCC_x \rvert$	Voltage difference between different power supply pins		50	mV
$\lvert VSS_x - VSS \rvert$	Voltage difference between different ground pins		50	mV
V_{ESDHBM}	ESD electrostatic discharge voltage (human body model)	Refer to [6.3.12 Absolute Maximum (Electrical Sensitivity)] electrical parameters		V

Table 6-2 Voltage Characteristics

Symbol	Description	Maximum Value	Unit
I_{VCC}	The total current (supply current) through the DVCC/AVCC power cord (1)	100	mA
I_{VSS}	The total current through the VSS ground wire (outflow current) (1)	100	mA
I_{IO}	Output sink current on any I/O and control pin	20	mA
	Output current on any I/O and control pin	-20	mA
$I_{INJ(PIN)}$(2)(3)	Injection current of NRESET pin	+/-5	mA
	The injection current of the XTHI pin of XTH	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
$\sum I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 6-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

6.3 Operating conditions

6.3.1 General working conditions

Table 6-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency		0	84	MHz
f_{PCLK0}	Internal APB0 clock frequency		0	84	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	84	MHz
DVCC	Standard operating voltage		2.0	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	2.0	5.5	V
P_D	Power dissipation T_A=105 ℃	LQFP64		308 (reference value)	mW
	Power dissipation T_A=105 ℃	LQFP48		267 (reference value)	mW
	Power dissipation T_A=105 ℃	QFN48		667 (reference value)	mW
	Power dissipation T_A=105 ℃	QFN32		377 (reference value)	mW
T_A	Ambient temperature		-40	105	℃
T_J	Junction temperature range		-40	125	℃

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300 mV difference between DVCC and AVCC during power-up and normal operation.
3. In the case of lower power dissipation, T_A can be extended to this range as long as T_J does not exceed the maximum value of T_J.

6.3.2 Working conditions at power-up and power-down

Table 6-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{Vcc}	VCC rising rate		1	∞	μs/V
t_{Vcc}	VCC falling rate		10	∞	μs/V

6.3.3 Embedded reset and LVD module features

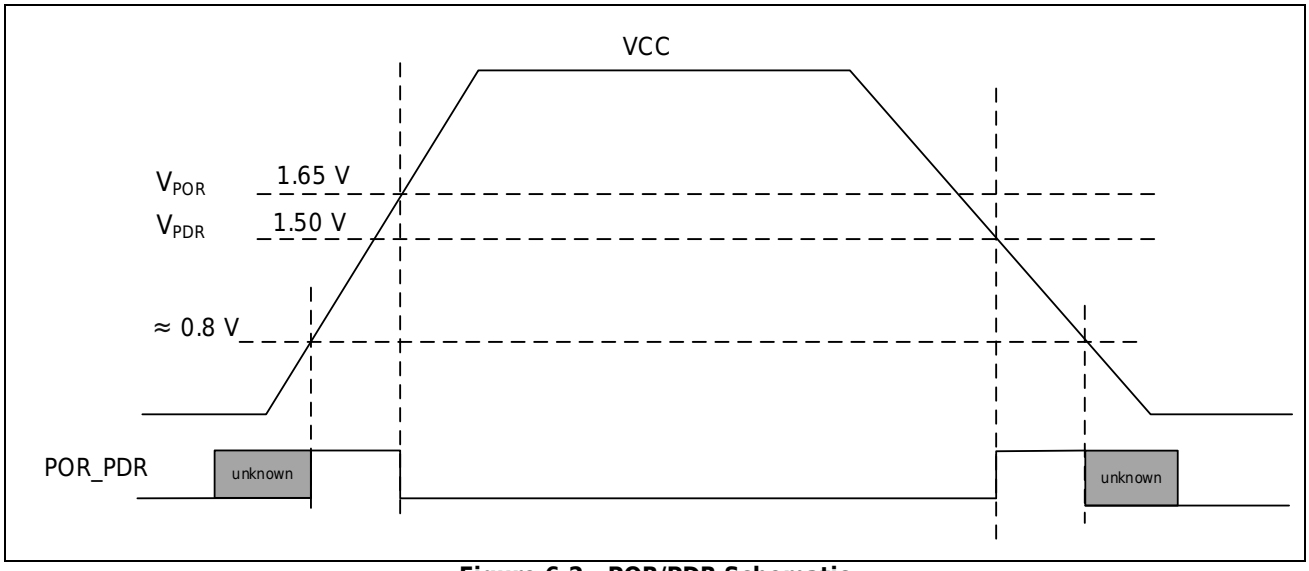


Figure 6-2 POR/PDR Schematic

1. Guaranteed by design, not tested in production.

Table 6-6 POR/PDR

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{POR}	POR release voltage (power-on process)			1.65		V
V_{PDR}	PDR detection voltage (power-down process)			1.50		V

Table 6-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ex}	External input voltage range		0		VCC	V
V_{level}	Detection threshold	LVD_CR.VTDS = 0b0000 LVD_CR.VTDS = 0b0001 LVD_CR.VTDS = 0b0010 LVD_CR.VTDS = 0b0011 LVD_CR.VTDS = 0b0100 LVD_CR.VTDS = 0b0101 LVD_CR.VTDS = 0b0110 LVD_CR.VTDS = 0b0111 LVD_CR.VTDS = 0b1000 LVD_CR.VTDS = 0b1001 LVD_CR.VTDS = 0b1010 LVD_CR.VTDS = 0b1011 LVD_CR.VTDS = 0b1100 LVD_CR.VTDS = 0b1101 LVD_CR.VTDS = 0b1110 LVD_CR.VTDS = 0b1111	1.70 1.80 1.89 1.98 2.08 2.17 2.27 2.36 2.46 2.55 2.65 2.74 2.84 2.93 3.02 3.12	1.80 1.90 2.00 2.10 2.20 2.30 2.40 2.50 2.60 2.70 2.80 2.90 3.00 3.10 3.20 3.30	1.90 2.00 2.11 2.22 2.32 2.43 2.53 2.64 2.74 2.85 2.95 3.06 3.17 3.27 3.38 3.48	V
$T_{response}$	Response time			80		μs
T_{setup}	Establishment time			400		μs
V_{hyste}	Hysteresis voltage			40		mV
T_{filter}	Filter time	LVD_CR.FltTime = 0b000 LVD_CR.FltTime = 0b001 LVD_CR.FltTime = 0b010 LVD_CR.FltTime = 0b011 LVD_CR.FltTime = 0b100 LVD_CR.FltTime = 0b101 LVD_CR.FltTime = 0b110 LVD_CR.FltTime = 0b111		7 20 47 100 420 1700 6820 27300		μs

1. The data is based on the assessment results and is not tested in production.

6.3.4 Built-in reference voltage

Table 6-8 Built-in Reference Voltages

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5 v Reference Voltage	Normal temperature 25 °C VCC=3.3 V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5 v Reference Voltage	-40 ~ 105 °C VCC=2.8 V~5.5 V	2.463	2.5	2.538	V(1)
V_{REF15}	Internal 1.5 v Reference Voltage	Normal temperature 25 °C VCC=3.3 V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5 v Reference Voltage	-40 ~ 105 °C VCC=2.0 V~5.5 V	1.477	1.5	1.523	V(1)
T_{Coeff}	Internal 2.5 v 1.5 v temperature coefficient	-40 ~ 105 °C			120	ppm/°C
$T_{stable(BGR)}$	BGR stable time	Normal temperature 25 °C VCC=3.3 V		20		μs

1. The data is based on the assessment results and is not tested in production.

6.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in digital input mode and connected to a static level - VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- When the access time of the flash memory is adjusted to different f_{HCLK}, different Flash Waits are set (see the FLASH_WAIT register in the reference manual for details).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$,$f_{PCLK1} = f_{HCLK}$.

Table 6-9 Operating Current Characteristics

Symbol	Parameter	Conditions			Typical value(1)	Max(2)	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	VCAP=1.2 V VCC=3.3 V T_A=25 °C	RCH clock source	4 M	870	-	µA
				6 M	1800	-	
				12 M	3270	-	
				22.12 M	5760	-	
				24 M	6230	-	
			PLL RCH4M to xxM clock source	16 M	5510	-	
				24 M	7960	-	
				32 M	10150	-	
				64 M	19260	-	
				84 M	24870	-	
	All peripherals clock OFF, Run while(1) in RAM	VCAP=1.2 V VCC=3.3 V T_A=25 °C	RCH clock source	4 M	870	-	µA
				6 M	1140	-	
				12 M	1970	-	
				22.12 M	3330	-	
				24 M	3590	-	
			PLL RCH4M to xxM clock source	16 M	3760	-	
				24 M	5330	-	
				32 M	6650	-	
				64 M	12400	-	
				84 M	16000	-	
I_{DD} (Run CoreMark)	All peripherals clock OFF, Flash Cache on, Run while(1) in Flash	VCAP=1.2 V VCC=3.3 V T_A=25 °C	RCH clock source	4 M Flash Wait=0	953	-	µA
				6 M Flash Wait=0	1262	-	
				12 M Flash Wait=0	2189	-	
				22.12 M	3749	-	

Symbol	Parameter	Conditions			Typical value(1)	Max(2)	Unit
				Flash Wait=0			
				24 M Flash Wait=1	4025	-	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	3365	-	
				24 M Flash Wait=1	4733	-	
				32 M Flash Wait=1	5867	-	
				64 M Flash Wait=2	10790	-	
				84 M Flash Wait=3	13858	-	
	All peripherals clock OFF,Flash Cache off, Run while(1) in Flash	VCAP=1.2 V VCC=3.3 V T_A=25 °C	RCH clock source	4 M Flash Wait=0	1308	-	µA
				6 M Flash Wait=0	1793	-	
				12 M Flash Wait=0	3214	-	
				22.12 M Flash Wait=0	5527	-	
				24 M Flash Wait=1	5124	-	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	4671	-	
				24 M Flash Wait=1	5840	-	
				32 M Flash Wait=1	7252	-	
				64 M Flash Wait=2	11380	-	
				84 M Flash Wait=3	12704	-	
I_{DD} (Run mode)	All peripherals clock ON,Flash Cache on, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	1310	1492	µA
				6 M Flash Wait=0	1803	2009	
				12 M Flash Wait=0	3278	3559	
				22.12 M Flash Wait=0	5770	6180	
				24 M Flash Wait=1	6246	6663	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	4842	5172	
				24 M Flash Wait=1	6973	7398	
				32 M Flash Wait=1	8836	9350	
				64 M Flash Wait=2	16708	17553	
				84 M Flash Wait=3	21643	22680	
	All peripherals clock ON,,Flash Cache off, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	1294	1477	µA
				6 M Flash Wait=0	1780	1986	
				12 M Flash Wait=0	3231	3515	

Symbol	Parameter	Conditions			Typical value(1)	Max(2)	Unit
				22.12 M Flash Wait=0	5685	6097	
				24 M Flash Wait=1	5100	5460	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	4781	5112	
				24 M Flash Wait=1	5826	6202	
				32 M Flash Wait=1	7305	7752	
				64 M Flash Wait=2	12654	13317	
				84 M Flash Wait=3	15680	16453	
	All peripherals clock OFF,Flash Cache on, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105°C	RCH clock source	4 M Flash Wait=0	875	1036	μA
				6 M Flash Wait=0	1150	1325	
				12 M Flash Wait=0	1980	2200	
				22.12 M Flash Wait=0	3345	3645	
				24 M Flash Wait=1	3620	3920	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	3100	3350	
				24 M Flash Wait=1	4346	4660	
				32 M Flash Wait=1	5345	5708	
				64 M Flash Wait=2	9830	10410	
				84 M Flash Wait=3	12695	13402	
	All peripherals clock OFF,,Flash Cache off, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	860	1121	μA
				6 M Flash Wait=0	1126	1305	
				12 M Flash Wait=0	1931	2150	
				22.12 M Flash Wait=0	3262	3560	
				24 M Flash Wait=1	2515	2763	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	3035	3286	
				24 M Flash Wait=1	3241	3500	
				32 M Flash Wait=1	3865	4160	
				64 M Flash Wait=2	5880	6270	
				84 M Flash Wait=3	6870	7293	
I_{DD} (Sleep mode)	All peripherals clock ON,Flash Cache on, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	868	1149	μA
				6 M Flash Wait=0	1140	1310	
				12 M Flash	1957	2165	

Symbol	Parameter	Conditions			Typical value(1)	Max(2)	Unit
				Wait=0			
				22.12 M Flash Wait=0	3319	3593	
				24 M Flash Wait=1	3585	3860	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	3072	3309	
				24 M Flash Wait=1	4313	4598	
				32 M Flash Wait=1	5290	5617	
				64 M Flash Wait=2	9669	10180	
				84 M Flash Wait=3	12460	13067	
	All peripherals clock ON,Flash Cache off, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	859	1160	µA
				6 M Flash Wait=0	1158	1330	
				12 M Flash Wait=0	1994	2204	
				22.12 M Flash Wait=0	3385	3665	
				24 M Flash Wait=1	3657	3936	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	3121	3361	
				24 M Flash Wait=1	4386	4675	
				32 M Flash Wait=1	5387	5724	
				64 M Flash Wait=2	9862	10379	
				84 M Flash Wait=3	12706	13332	
	All peripherals clock OFF, Flash Cache on, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCH clock source	4 M Flash Wait=0	444	582	µA
				6 M Flash Wait=0	505	646	
				12 M Flash Wait=0	689	837	
				22.12 M Flash Wait=0	967	1132	
				24 M Flash Wait=1	1034	1200	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	1375	1535	
				24 M Flash Wait=1	1765	1940	
				32 M Flash Wait=1	1900	2080	
				64 M Flash Wait=2	2940	3170	
				84 M Flash Wait=3	3669	3929	
	All peripherals clock OFF, Flash Cache off, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-	RCH clock source	4 M Flash Wait=0	456	596	µA
				6 M Flash Wait=0	523	666	

Symbol	Parameter	Conditions			Typical value(1)	Max(2)	Unit
		40 °C~105 °C		12 M Flash Wait=0	725	877	
				22.12 M Flash Wait=0	1036	1205	
				24 M Flash Wait=1	1109	1277	
			PLL RCH12M to xxM clock source	16 M Flash Wait=0	1425	1588	
				24 M Flash Wait=1	1840	2020	
				32 M Flash Wait=1	1995	2185	
				64 M Flash Wait=2	3140	3375	
				84 M Flash Wait=3	3926	4198	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCL32K clock source	Flash Cache ON	13.4	126	µA
				Flash Cache OFF	12.2	127	
	All peripherals clock OFF, Run while(1) in Flash			Flash Cache ON	9.7	122	
				Flash Cache OFF	8.5	123	
I_{DD} (LP Sleep)	All peripherals clock ON, Run while(1) in Flash	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	RCL32K clock source	Flash Cache ON	10	123	µA
				Flash Cache OFF	10.1	123.4	
	All peripherals clock OFF, Run while(1) in Flash			Flash Cache ON	6.4	119	
				Flash Cache OFF	6.5	120.1	
I_{DD} (DeepSleep)	All peripherals clock OFF	VCAP=1.2 V VCC=2.0 V~5.5 V T_A=-40 °C~105 °C	NO CLK	-	3.8	118	µA
	All peripherals clock OFF		RCL32K	-	5.1	119	
	All peripherals clock OFF		RCL38K	-	5.1	119	
	Other peripherals clock OFF		RCL32K	WDT	5.2	119	
	Other peripherals clock OFF		RCL32K	LVD	3.8	117	
	Other peripherals clock OFF		RCL32K	WDT+LVD	5.3	119	

1. Typical values are at 25 °C & VCC = 3.3 V unless otherwise specified.
2. Unless otherwise specified, the maximum value is the maximum value within the range of VCC = 2.0 V~5.5 V & Temperature = -40 °C~105 °C.
3. The data is based on the assessment results and is not tested in production.

6.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used at wake-up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Table 6-10 Wake-up time from low-power modes

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
T_{wu}	Sleep mode wake-up time			1.8		μs
	Deep sleep wake-up time	RCH = 24 MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.
2. The data is based on the assessment results and is not tested in production.

6.3.7 External timer characteristic

6.3.7.1 External input high-speed clock

Table 6-11 External input high-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTH_ext}	User external clock frequency (1)			8	32	MHz
V_{XTHH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTHL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTH)}$	Rise time (1)				10	ns
$T_{f(XTH)}$	Falling time (1)				10	ns
$T_{w(XTH)}$	Enter high or low time (1)		15			ns
$C_{in(XTH)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		40		60	%
IL	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

6.3.7.2 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8-32 MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

External XTH crystal oscillator(1) (2)

Table 6-12 High Speed External Clock XTH

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency		8		32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32 M			40	Ohm
		24 M			60	
		16 M			80	
		8 M			120	
CLX(3)	Load capacitance	Both pins have load capacitors	4	12	20	pF
Gm	transconductance	SYSCTRL_XTHCR[3:0] = 0b1111		12.42		mS
		SYSCTRL_XTHCR[3:0] = 0b1110		7.813		
		SYSCTRL_XTHCR[3:0] = 0b1101		2.778		
		SYSCTRL_XTHCR[3:0] = 0b1100		1.395		
		SYSCTRL_XTHCR[3:0] = 0b1011		7.107		
		SYSCTRL_XTHCR[3:0] = 0b1010		4.490		
		SYSCTRL_XTHCR[3:0] = 0b1001		1.597		
		SYSCTRL_XTHCR[3:0] = 0b1000		0.803		
		SYSCTRL_XTHCR[3:0] = 0b0111		4.982		
		SYSCTRL_XTHCR[3:0] = 0b0110		3.150		
		SYSCTRL_XTHCR[3:0] = 0b0101		1.121		
		SYSCTRL_XTHCR[3:0] = 0b0100		0.564		
		SYSCTRL_XTHCR[3:0] = 0b0011		3.854		
		SYSCTRL_XTHCR[3:0] = 0b0010		2.433		
		SYSCTRL_XTHCR[3:0] = 0b0001		0.868		
		SYSCTRL_XTHCR[3:0] = 0b0000		0.436		
Duty	Duty ratio		40	50	60	%
Idd(4)	Current	SYSCTRL_XTHCR[3:0] = 0b1110		800	2500	μA
		SYSCTRL_XTHCR[3:0] = 0b1010		650	1500	μA
		SYSCTRL_XTHCR[3:0] = 0b0110		450	1000	μA

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		SYSCTRL_XTHCR[3:0] = 0b0010		350	800	μA
T_{start}(5)	Start time	32 M, CL=16 pF@ SYSCTRL_XTHCR[3:0] = 0b1110		1	2	ms
		24 M,CL=16 pF@ SYSCTRL_XTHCR[3:0] = 0b1110		1.5	2.5	ms
		16 MHz,CL=16 pF@ SYSCTRL_XTHCR[3:0] = 0b1010		2	3	ms
		8 MHz,CL=16 pF@ SYSCTRL_XTHCR[3:0] = 0b0110		6	20	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{LX} refers to the load capacitors C_{L1} and C_{L2} of the two pins of XTAL. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, it should be based on parameters such as the frequency of the crystal oscillator and ESR, and the capacitive reactance of the PCB and MCU pins should be taken into consideration.
4. Current varies with frequency and drive configuration.
5. T_{start} is the start-up time, which is the period of time from when the software enables XTH until a stable frequency output is obtained. This value is measured on a standard crystal resonator under the setting of XTH_CR.Startup=10. It may vary greatly depending on the crystal manufacturer and model.

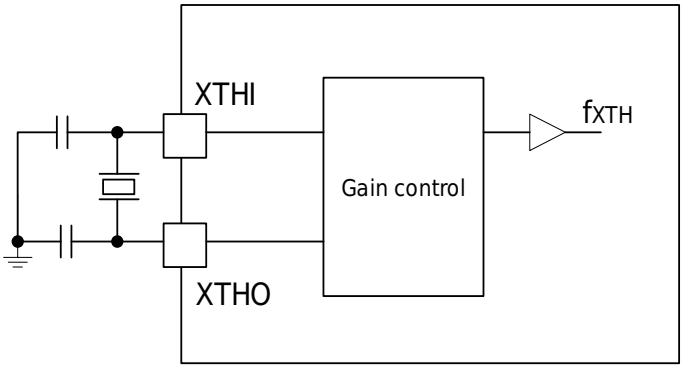


Figure 6-3 Schematic diagram of external clock

6.3.8 Internal timer characteristics

6.3.8.1 Internal RCH oscillator

Table 6-13 Internal RCH Oscillator

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Dev	RCH oscillator accuracy	User-trimmed with clock_trim for given VCC and T_A conditions		0.25		%
		VCC =2 V ~ 5.5 V T_A = -40 °C ~ 105 °C	-3.5		+3.5	%
F_{CLK}	Oscillation frequency			24		MHz
I_{CLK}	Power consumption	RCH = 24 MHz		200		μA
DC_{CLK}	Duty Cycle (1)		45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

6.3.8.2 Internal RCL oscillator

Table 6-14 Internal RCL Oscillator

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Dev	RCL oscillator accuracy	User-trimmed with clock_trim for given VCC and T_A conditions		0.5		%
		VCC = 2 V ~ 5.5 V T_A = -40 °C ~ 105 °C	-5		5	%
F_{CLK}	Oscillation frequency			32.768		KHz
T_{CLK}	Start time			150		μs
DC_{CLK}	Duty Cycle (1)		35	50	65	%

1. Resulted from comprehensive evaluation, not tested in production.

6.3.9 PLL Characteristic

Table 6-15 PLL Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{in}(1)	Input clock		4	8	32	MHz
Duty_in(1)	Input clock duty cycle		40		60	%
F_{out}	Output frequency		15	-	84	MHz
Duty_out(1)	Output duty cycle		45%	-	55%	
T_{lock}(1)	Lock time	Input frequency 4 MHz	-	40		μs

1. Resulted from comprehensive evaluation, not tested in production.
2. F_{out} does not include the two intervals of "greater than 25 MHz and less than 30 MHz" and " greater than 50 MHz and less than 60 MHz".

6.3.10 Memory Characteristics

Table 6-16 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EC_{FLASH}	Erase times	Regulator voltage=1.5 V, T_A = 25 ℃	20K			cycles
RET_{FLASH}	Data retention period	T_A = 105 ℃	10			Years
		Room temperature	100			Years
T_{w_prog}	Programming time		6		7.5	μs
T_{p_erase}	Page erase time		4		5	ms
T_{m_erase}	Whole chip erase time		30		40	ms

6.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

Table 6-17 EFT Characteristics

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4A
EFT to Power (IEC61000-4-4)	Class:2A

Software recommendations

The software process must include the control of program run-away, such as:

- Corrupted program counter;
- Unexpected reset;
- Critical data is corrupted (control registers, etc.);

When performing ESD testing, a voltage exceeding the application requirements can be directly applied to the chip. When an unexpected action is detected, the software part needs to be strengthened to prevent unrecoverable errors.

6.3.12 Absolute Maximum (Electrical Sensitivity)

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 6-18 Absolute maximum values

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ESDHBM}	ESD @ Human Body Mode			4		KV
V_{ESDCDM}	ESD @ Charge Device Mode			1		KV
$I_{latchup}$	Latch up current@105 ℃			100		mA
	Latch up current@25 ℃			300		mA

6.3.13 I/O port characteristics

6.3.13.1 Output characteristics——ports

Table 6-19 Port output characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 5 mA, VCC = 3.3 V(1)	VCC-0.25		V
		Sourcing10 mA, VCC = 3.3 V(2)	VCC-0.6		V
V_{OL}	Low level output voltage Sink Current	Sinking 6 mA, VCC = 3.3 V(1)		VSS+0.25	V
		Sinking 15 mA, VCC = 3.3 V(2)		VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing10 mA, VCC = 3.3 V(1)	VCC-0.25		V
		Sourcing 20 mA, VCC = 3.3V(2)	VCC-0.6		V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 10 mA, VCC = 3.3 V(1)		VSS+0.25	V
		Sinking 20 mA, VCC = 3.3 V(2)		VSS+0.6	V

1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

6.3.13.2 Input Characteristics - Ports PA, PB, PC, PD

Table 6-20 Port input characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=2.0 v	0.7VCC			V
		VCC=3.3 v	0.7VCC			V
		VCC=5.5 v	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=2.0 v			0.3VCC	V
		VCC=3.3 v			0.3VCC	V
		VCC=5.5 v			0.3VCC	V
V_{hys}(1)	Input voltage hysteresis (VIH - VIL)	VCC=2.0 v		0.3		V
		VCC=3.3 v		0.4		V
		VCC=5.5 v		0.6		V
R_{pullup}	Pullup resistor	Pullup enabled VCC=3.3 V		80		kΩ
$R_{pulldown}$	Pulldown resistor	Pulldown enabled VCC=3.3 V		40		kΩ
C_{input}	Input capacitance			5		pF

1. Resulted from comprehensive evaluation, not tested in production.

6.3.13.3 Port external input sampling requirements——Timer Gate/Timer Clock

Table 6-21 Port External Input Sampling Requirements

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$t_{(int)}$	External interrupt timing	External trigger signal for the interrupt flag(1)		30		ns
$t_{(cap)}$	Timer capture timing	Timer capture pulse width		0.5		μs
$t_{(clk)}$	Timer clock frequency applied to pin	Timer external clock input f_{HCLK} = 4 MHz			PCLK/2	MHz

1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.
2. Resulted from comprehensive evaluation, not tested in production.

6.3.13.4 Port leakage characteristics - PA, PB, PC, PD

Table 6-22 Port Leakage Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (1)(2)		±50		nA

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

6.3.14 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 6-23 Advanced Timer (ATIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=84 MHz	11.9		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=84 MHz	0	42	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}

1. Guaranteed by design, not tested in production.

Table 6-24 Composite Timer (CTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=84 MHz	11.9		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=84 MHz	0	42	MHz
Res_{Tim}	Timer resolution			16	Bit
		free counting		32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}

1. Guaranteed by design, not tested in production.

Table 6-25 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10 kHz	0.4	209715	ms

1. Guaranteed by design, not tested in production.

6.3.15 Communication Interface

6.3.15.1 I2C features

I2C interface characteristics are as follows:

Table 6-26 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100 K)		Fast mode (400 K)		High speed mode (1 M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7		1.25		0.5		μs
t_{SCLH}	SCL clock high time	4.0		0.6		0.26		μs
$t_{SU.SDA}$	SDA establishment time	250		100		50		μs
$t_{HD.SDA}$	SDA hold time	0		0		0		μs
$t_{HD.STA}$	Start condition hold time	2.5		0.625		0.25		μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5		0.6		0.25		μs
$t_{SU.STO}$	Stop condition establishment time	0.25		0.25		0.25		μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		μs

1. Guaranteed by design, not tested in production.

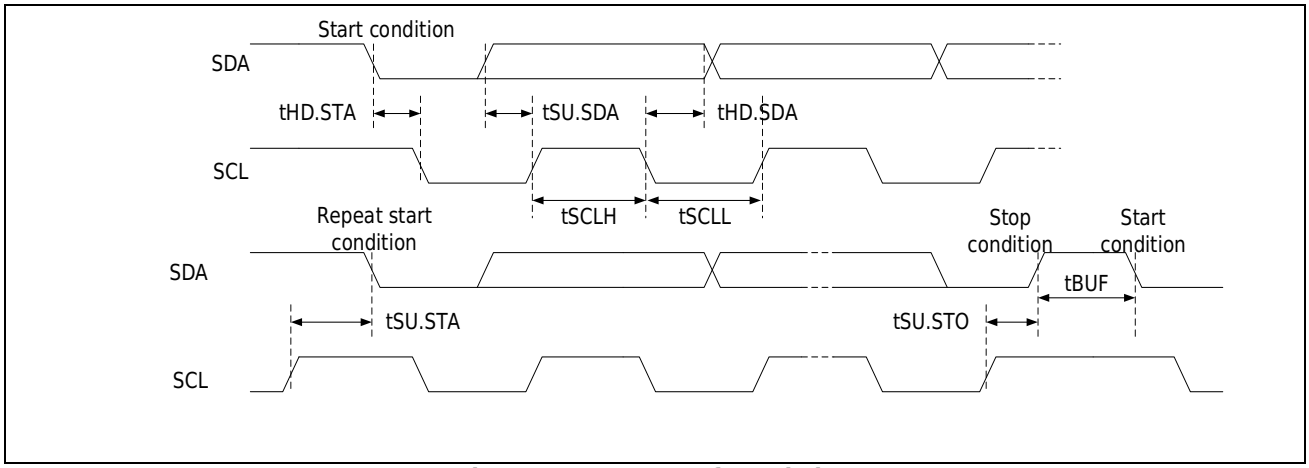


Figure 6-4 I2C Interface Timing

6.3.15.2 SPI features

Table 6-27 SPI Interface Features(1)(2)

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period (3)	Host sending mode f_{PCLK} = 60MHz	33.3	-	ns
		Host receiving mode (Disable host delay sampling) f_{PCLK} = 60MHz	133	-	ns
		Host receiving mode (Enable host delay sampling) f_{PCLK} = 60MHz	66.6		ns
		Slave sending mode (Disable host delay sampling) f_{PCLK} = 60MHz	133		ns
		Slave sending mode (Enable host delay sampling) f_{PCLK} = 60MHz	66.6		ns
		Slave receiving mode f_{PCLK} = 60MHz	66.6		ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output		-	2	ns
$t_{h(MO)}$	Hold time of host data output		0	-	ns
$t_{v(SO)}$	Effective time of slave data output		-	21+1.5xT_{PCLK}	ns
$t_{h(SO)}$	Hold time of slave data output		15+0.5xT_{PCLK}	-	ns
$t_{su(MI)}$	Setup time of host data input		22	-	ns
$t_{h(MI)}$	Hold time of host data input		2	-	ns
$t_{su(SI)}$	Setup time of slave data input		0	-	ns
$t_{h(SI)}$	Hold time of slave data input		1+1.5xT_{PCLK}	-	ns

1. Guaranteed by design, not tested in production.
2. The data is given based on the condition that VCC=3.0V.
3. The maximum frequency division coefficient in the master mode is PCLK/2, and that in the slave mode is PCLK/4.

The waveform and timing parameters of the SPI interface signal are as follows:

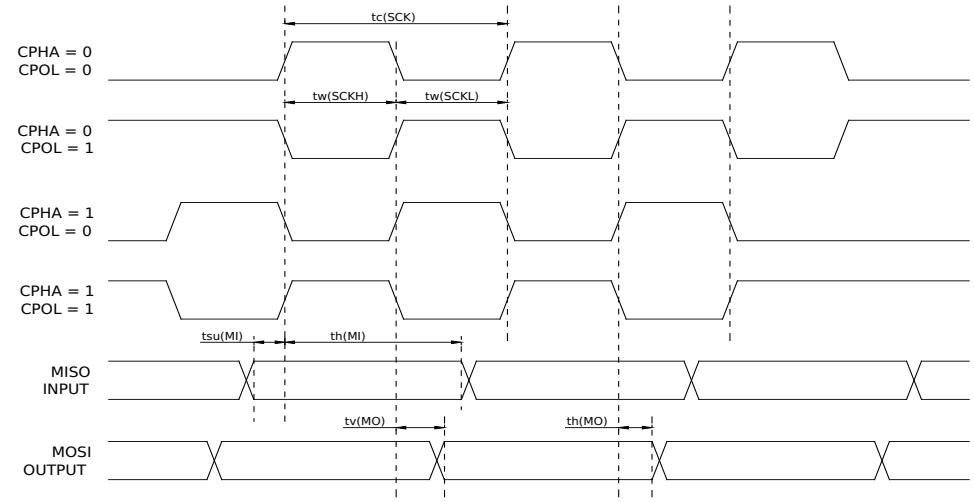


Figure 6-5 SPI Timing Diagram (Host Mode)

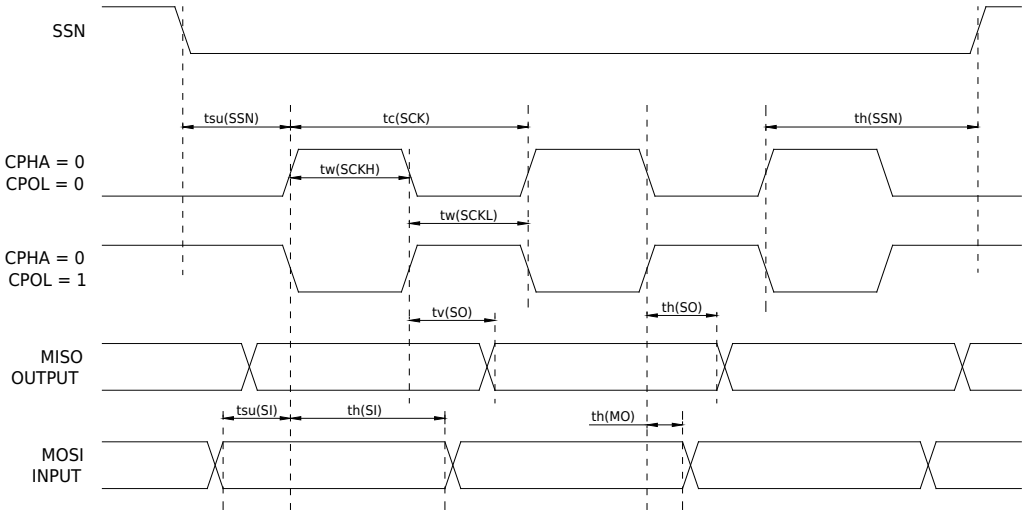


Figure 6-6 SPI timing diagram (slave mode CPHA=0)

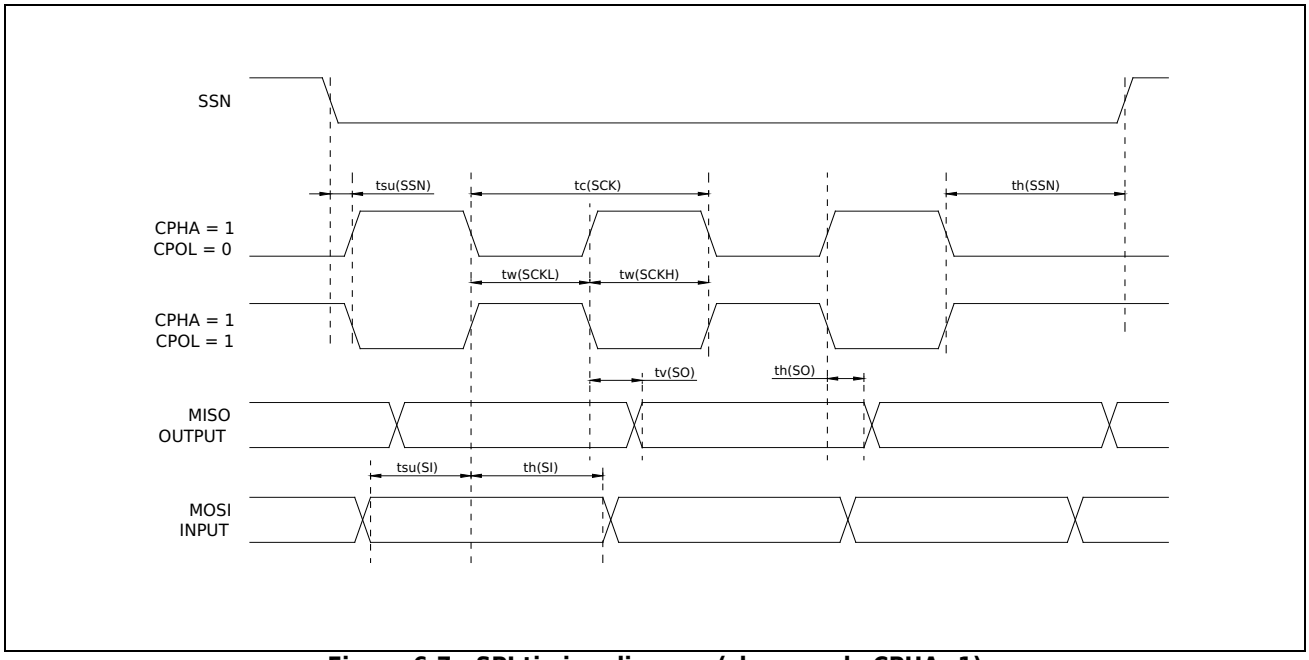


Figure 6-7 SPI timing diagram (slave mode CPHA=1)

6.3.16 NRESET pin characteristics

The NRESET pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 6-28 RESET pin characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(NRESET)}$ (1)	Input low level voltage		-0.3		0.8	V
$V_{IH(NRESET)}$	Input high level voltage		0.8*VCC		VCC+0.5	
$V_{hys(NRESET)}$	Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$		80		kOhm
$V_{F(NRESET)}$ (1)	Input filter pulse				2	μs
$V_{NF(NRESET)}$ (1)	Input unfiltered pulse		10			μs

1. Guaranteed by design, not tested in production.

6.3.17 12Bit ADC characteristics

Table 6-29 12Bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	2.0		AVCC	V
I_{ADC1}	Active current including reference generator and buffer	200 kSPS		1.3		mA
I_{ADC2}	Active current without reference generator and buffer	1 MSPS		0.7		mA
C_{ADC}	ADC input capacitance			4.0	5.0	pF
R_{ADC}(1)	ADC sampling switch impedance			1.8		KOhm
R_{AIN}(1)	ADC external input resistor(2)				100	KOhm
F_{ADCCLK}	ADC clock Frequency				24 M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			30		μs
$T_{ADCCONV}$	Conversion time		18	24	25	cycles
ENOB(1)	Effective Bits	1 MSPS@VCC>=2.7 v 500 KSPS@VCC>=2.4 v 200 KSPS@VCC>=2.0 v REF=EXREF	9.7	10.8		Bit
		1 MSPS@VCC>=2.7 v 500 KSPS@VCC>=2.4 v 200 KSPS@VCC>=2.0 v REF=VCC	9.7	10.7		Bit
		200 KSPS@VCC>=2.0 v REF=internal 1.5 V		10.0		Bit
		200 KSPS@VCC>=2.8 v REF=internal 2.5 V		10.3		Bit
SNR(1)	Signal to Noise Ratio	1 MSPS@VCC>=2.7 v 500 KSPS@VCC>=2.4 v 200 KSPS@VCC>=2.0 v REF=EXREF	61.5	68.5		dB
		1 MSPS@VCC>=2.7 v 500 KSPS@VCC>=2.4 v 200 KSPS@VCC>=2.0 v REF=VCC	60.8	68.1		dB
		200 KSPS@VCC>=2.0 v REF=internal 1.5 V		63.5		dB
		200 KSPS@VCC>=2.8 v REF=internal 2.5 V		65.3		dB
DNL(1)	Differential non-linearity	200 KSps; VREF=EXREF/AVCC	-1		2.5	LSB
INL(1)	Integral non-linearity	200 KSps; VREF=EXREF/AVCC		±3		LSB
E_o	Offset error			±5		LSB
E_g	Gain error			±5		LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:

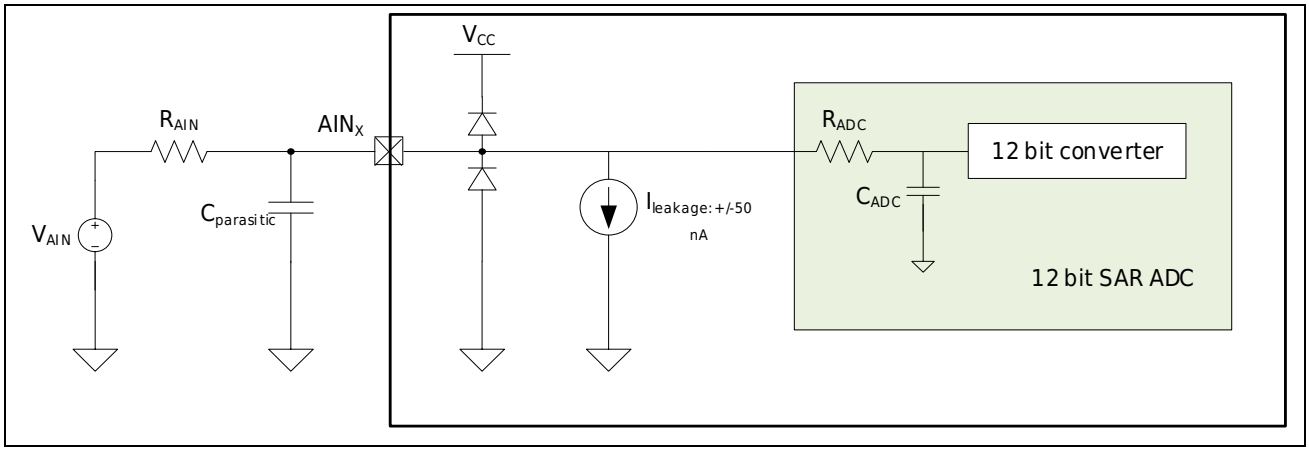


Figure 6-8 ADC typical application

Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN}=\frac{M}{F_{ADCCLK}*C_{ADC}*(N+1)*\ln(2)}-R_{ADC}\ (N=12)$$

Among them F_{ADCCLK} is the ADC clock frequency, the register ADC_CR0<3:1> can set the relationship between it and the PCLK frequency, as shown in the following table:

Table 6-30 Relationship between ADC clock frequency F_{ADCCLK} and PCLK frequency division ratio

ADC_CR0<3:1>	Ratio=F_{PCLK}/F_{ADCCLK}
0b000	1
0b001	4
0b010	6
0b011	8
0b100	10
0b101	12
0b110	14
0b111	16

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

Table 6-31 Relationship between sampling time t_{sa} and ADC clock frequency F_{ADCCLK}

ADC_CR0<13:12>	M
0b00	3
0b01	6
0b10	9
0b11	10

Table 6-32 The relationship between ADC maximum clock frequency F_{ADCCLK} and external resistance R_{AIN} (M=9, under the condition of sampling error 0.5LSB)

R_{AIN}(Kohm)	F_{ADCCLK}(MHz)
10	21.1
30	7.8
50	4.8
80	3.0
100	2.4
120	2.0
150	1.6

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{parasitic}$;
- In addition to considering R_{AIN} value, if the internal resistance of signal source V_{AIN}, it also needs to be considered.

6.3.18 Temperature sensor characteristics

When the measurement channel of the ADC selects the output voltage of the temperature sensor, the current ambient temperature can be calculated based on the output result of the ADC and the calibration value stored in the Flash memory.

Table 6-33 Temperature sensor parameters

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Temp Range	The operating ambient temperature range of the temperature sensor	-	-40	-	105	°C
ΔTerror	Temperature error	-	-	±5	-	°C

6.3.19 VC Characteristics

Table 6-34 VC Characteristics

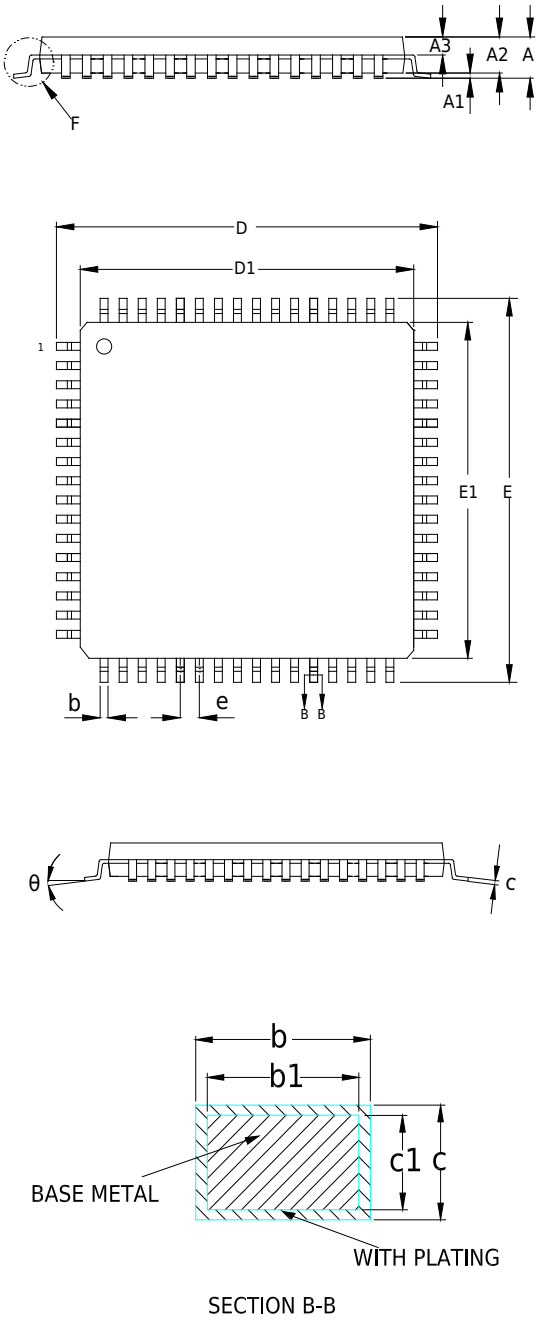
Symbol	Parameter	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
V_{in}	Input voltage range			0		5.5	V
V_{incom}	Input common mode range			0.3		VCC-0.3	V
V_{offset}	Input offset	Room temperature 25 °C 3.3 V		-15		+15	mV
I_{comp}	Comparator's current	VC_CR0.BIAS = 0b00 VC_CR0.BIAS = 0b01 VC_CR0.BIAS = 0b10 VC_CR0.BIAS = 0b11			0.3 1.2 10 20		μA
$T_{response}$	Comparator's response time when one input cross another	VC_CR0.BIAS = 0b00 VC_CR0.BIAS = 0b01 VC_CR0.BIAS = 0b10 VC_CR0.BIAS = 0b11			20 5 1 0.2		μs
T_{setup}	Comparator's setup time when ENABLE. Input signals unchanged.	VC_CR0.BIAS = 0b00 VC_CR0.BIAS = 0b01 VC_CR0.BIAS = 0b10 VC_CR0.BIAS = 0b11			20 5 1 0.2		μs
T_{warmup}	From main bandgap enable to Temp sensor voltage, ADC internal 1.5 V,2.5 V reference stable				20		μs
T_{filter}	Digital filter time(1)	Filter clock =150 KHz	VC_CR1.FltTime = 0b000 VC_CR1.FltTime = 0b001 VC_CR1.FltTime = 0b010 VC_CR1.FltTime = 0b011 VC_CR1.FltTime = 0b100 VC_CR1.FltTime = 0b101 VC_CR1.FltTime = 0b110 VC_CR1.FltTime = 0b111		7 20 47 100 420 1700 6820 27300		μs

1. When the filter clock is PCLK, the filter time is detailed in the reference manual.

7 Package information

7.1 Package size

LQFP64 package

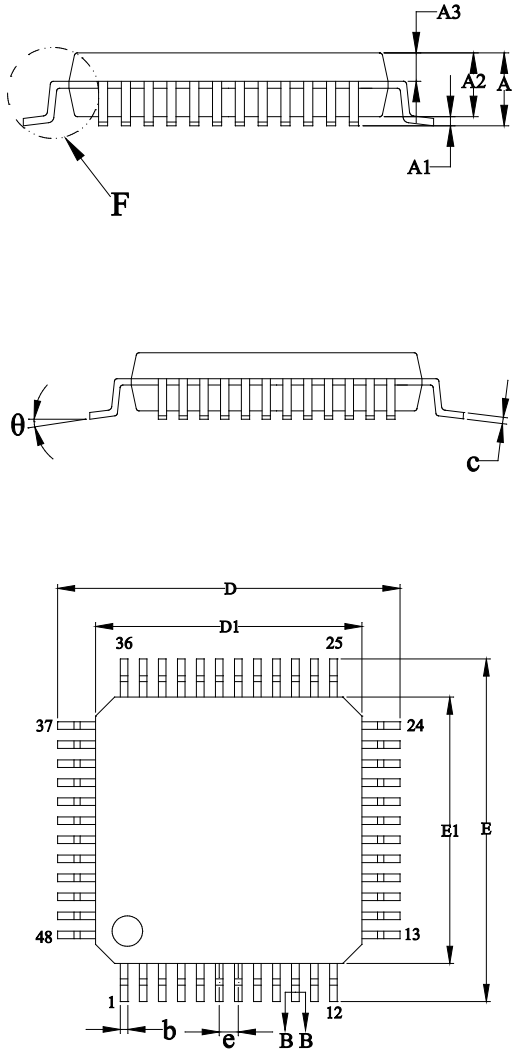


Symbol	10x10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	--	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.127	0.16
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0°	--	7°

Note:

– *Dimensions "D1" and "E1" do not include mold flash.*

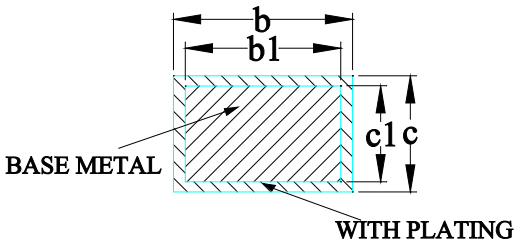
LQFP48 package



Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	--	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.127	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

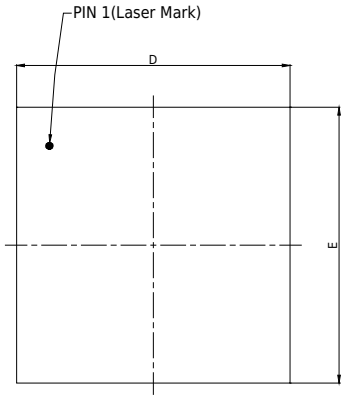
Note:

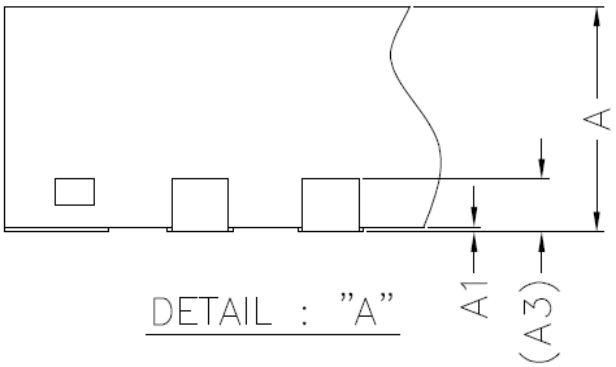
– *Dimensions "D1" and "E1" do not include mold flash.*

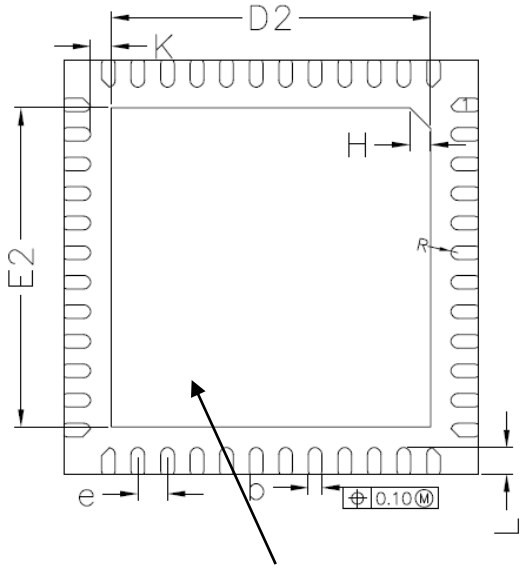


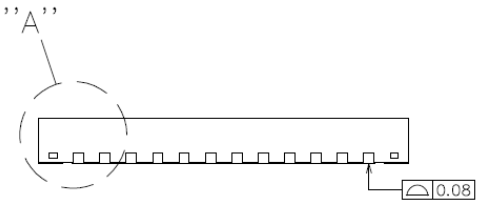
SECTION B-B

QFN48 package







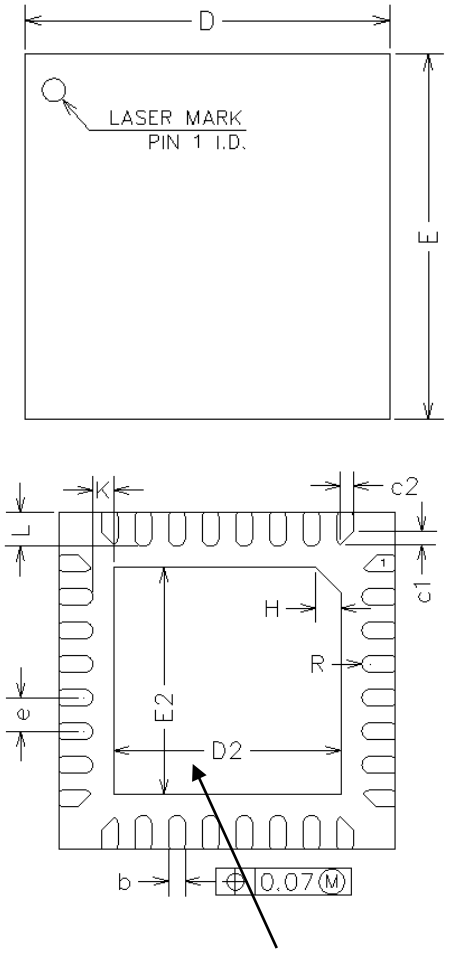


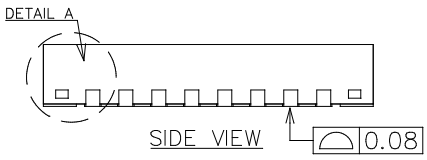
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
c	0.18	0.20	0.23
D	6.90	7.00	7.10
D2	5.20	5.35	5.50
e		0.50BSC	
E	6.90	7.00	7.10
E2	5.20	5.35	5.50
L	0.3	0.4	0.5
h	0.30	0.35	0.40
L/F die pad size(mil)		224 x 224	

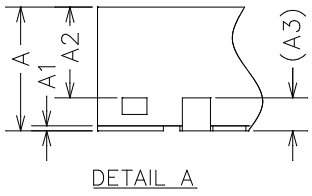
Note:

- *Exposed Pad Area needs to be connected to DVSS.*

QFN32 packaging







Symbol	4x4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
c1	-	0.10	-
c2	-	0.10	-
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.40BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.25	0.30	0.35
H		0.55REF	
K	0.20	-	-
L/F die pad size(mil)		122 x 122	

Note:

– *Exposed Pad Area must be connected to DVSS.*

7.2 Schematic diagram of pad

LQFP64 packaging (10 mm x 10 mm)

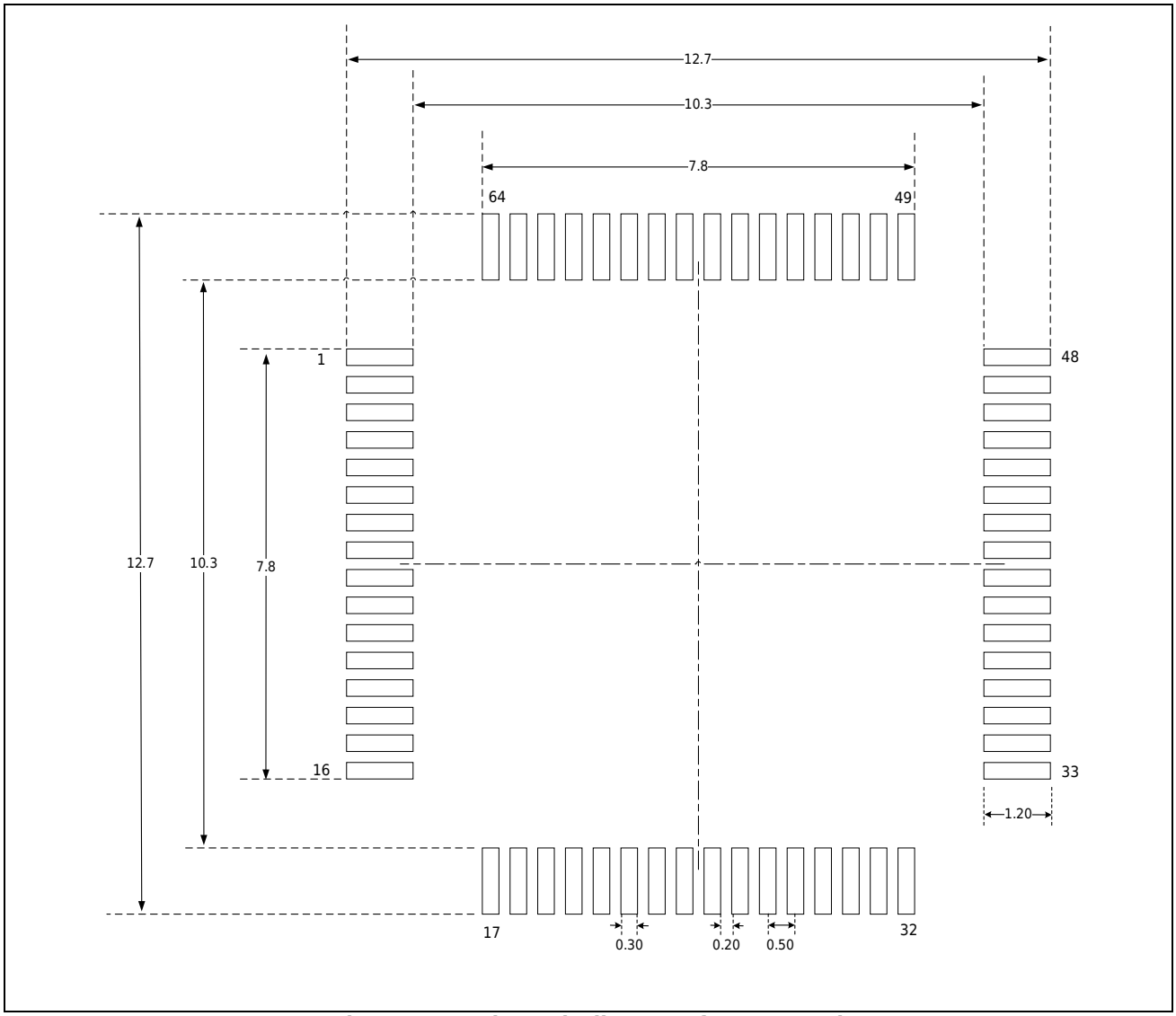


Figure 7-1 Schematic diagram of LQFP64 pad

Note:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

LQFP48 package (7 mm x 7 mm)

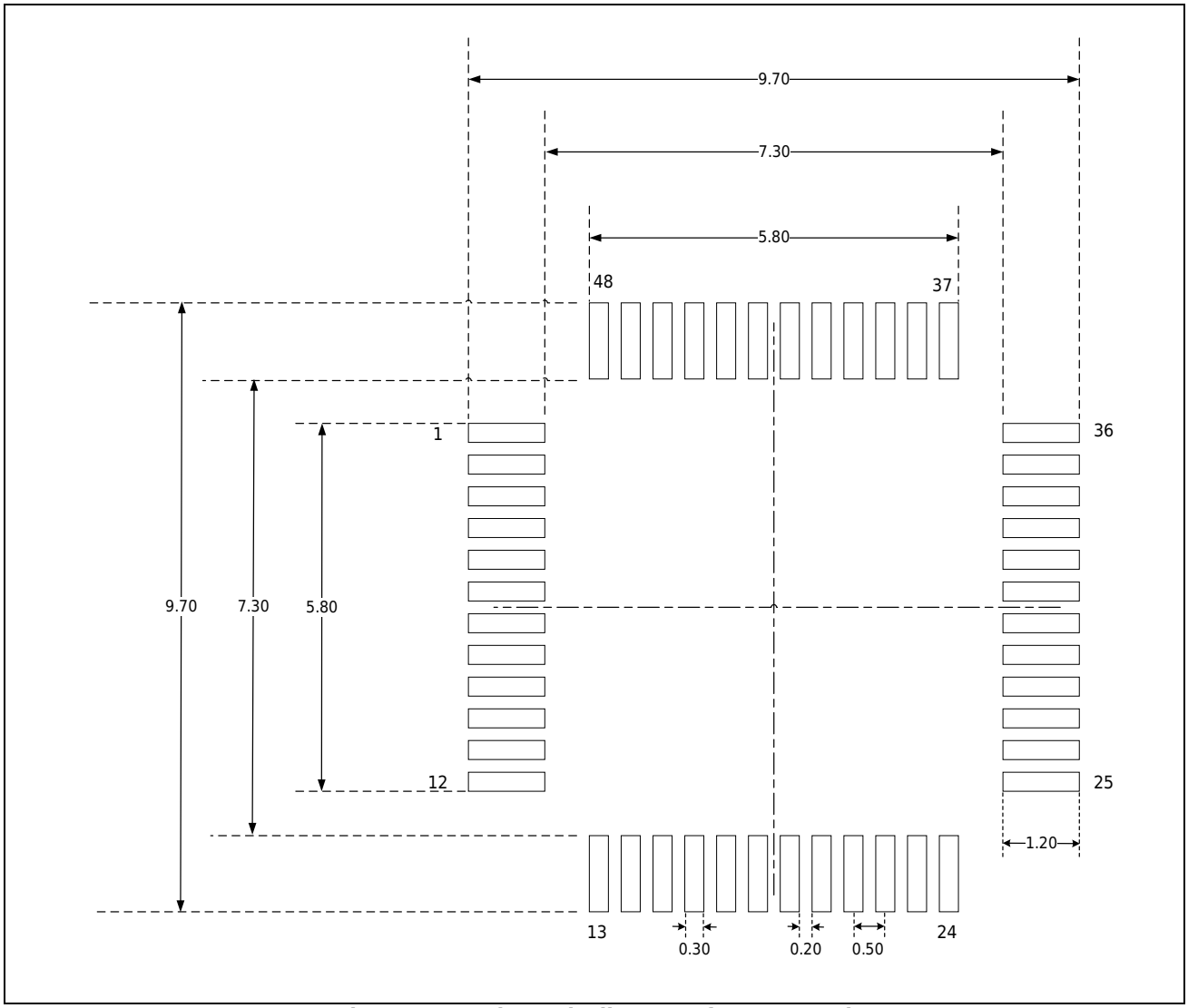


Figure 7-2 Schematic diagram of LQFP48 pad

Note:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

QFN48 package (7 mm x 7 mm)

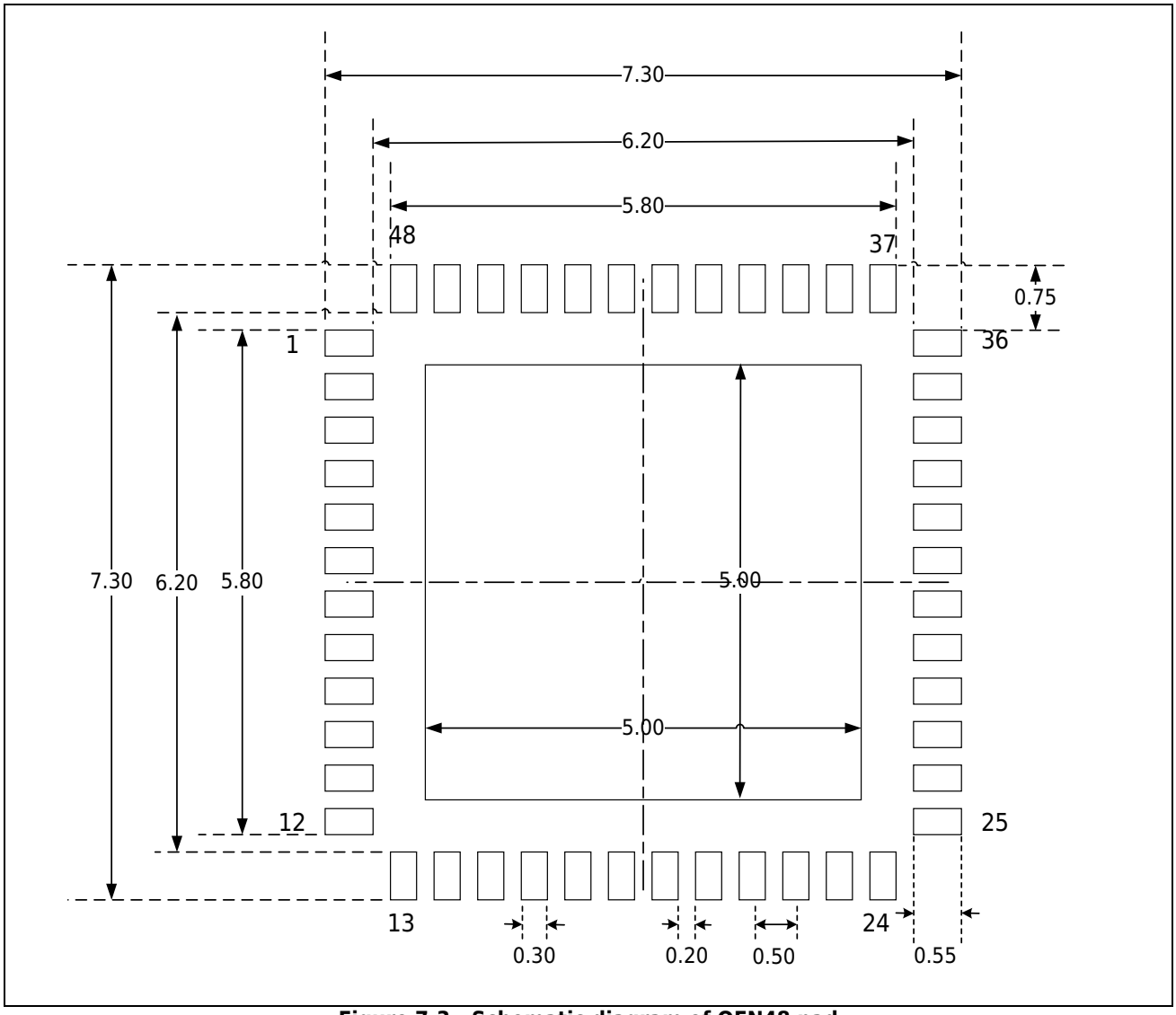


Figure 7-3 Schematic diagram of QFN48 pad

Note:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

QFN32 package (4 mm x 4 mm)

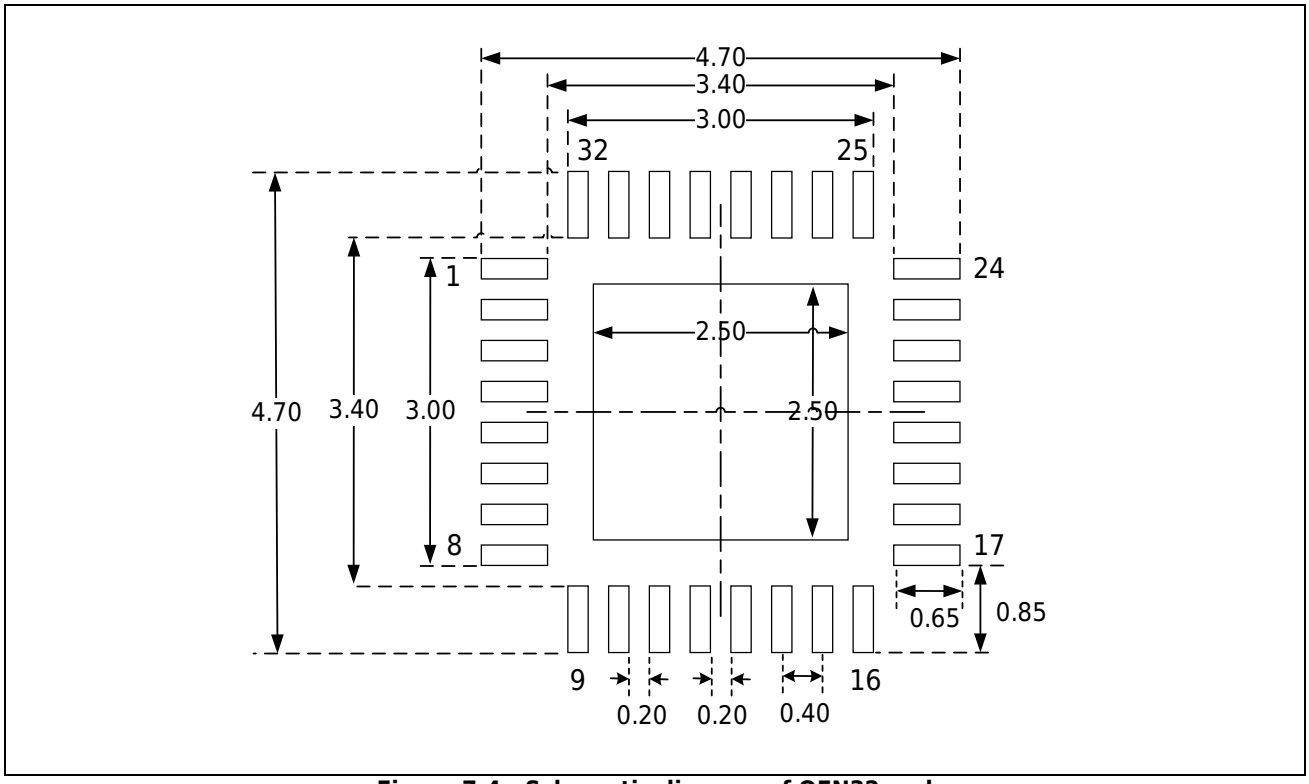


Figure 7-4 Schematic diagram of QFN32 pad

Note:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

7.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

LQFP64 package (10 mm x 10 mm)

LQFP48 package (7 mm x 7 mm)

QFN48 package (7 mm x 7 mm)

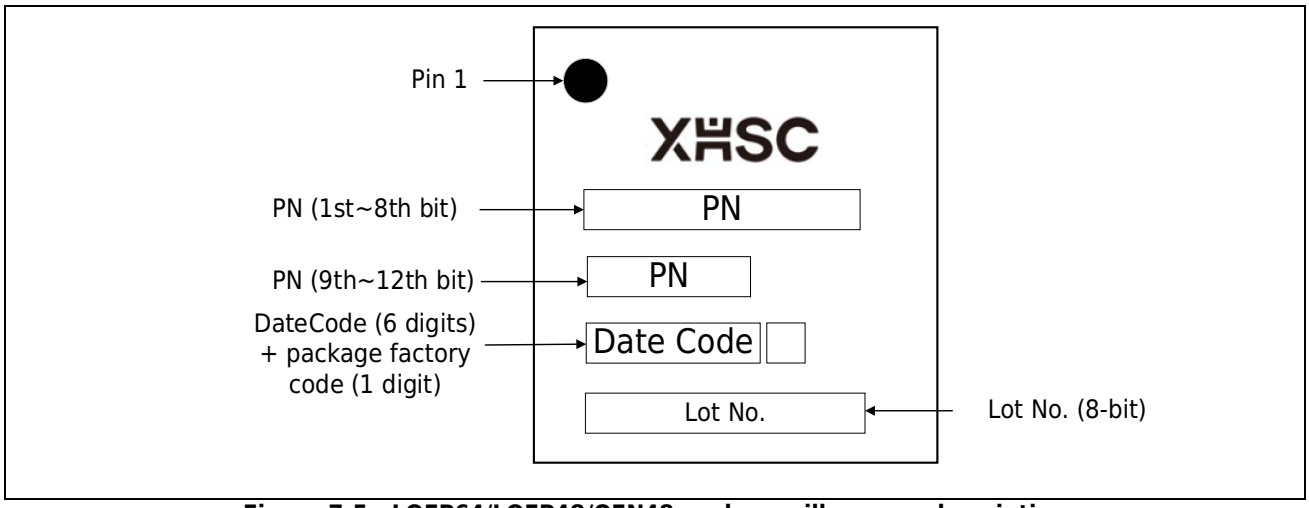


Figure 7-5 LQFP64/LQFP48/QFN48 package silk screen description

QFN32 package (4 mm x 4 mm)

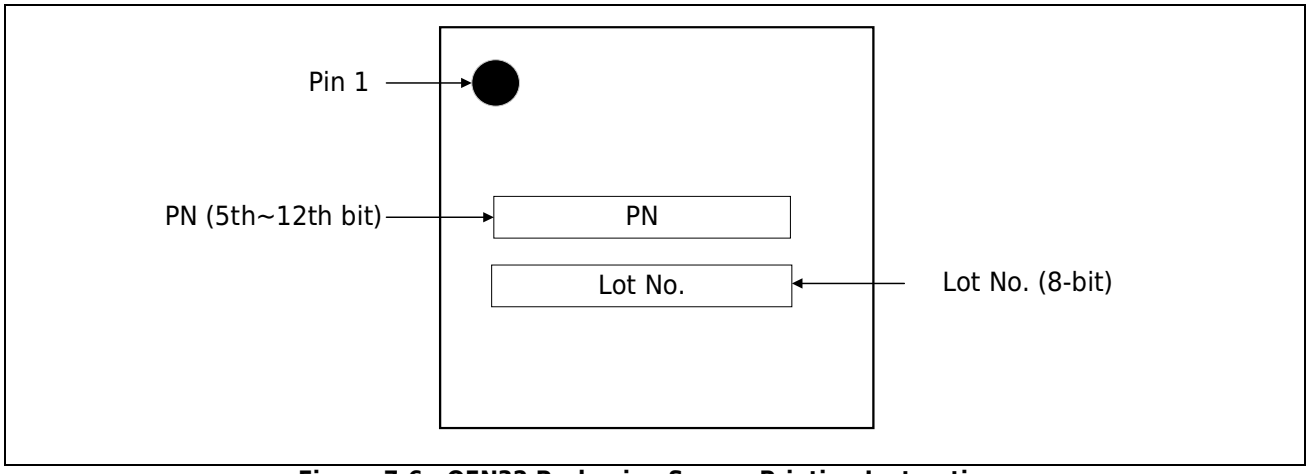


Figure 7-6 QFN32 Packaging Screen Printing Instructions

Note:

– *The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.*

7.4 Packaging Thermal Resistance Coefficient

The junction temperature T_J (℃) on the surface of a packaged chip when operating at a specified working environment temperature can be calculated according to the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD} . I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

The junction temperature T_J on the surface of the chip when operating at the specified working environment temperature cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 7-1 Thermal Resistance Coefficients of Each Package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP64 10 mm x 10 mm / 0.5 mm pitch	65 +/- 10 %	℃/W
LQFP48 7 mm x 7 mm / 0.5 mm pitch	75 +/- 10 %	℃/W
QFN48 7 mm x 7 mm / 0.5 mm pitch	30 +/- 10 %	℃/W
QFN32 4 mm x 4 mm / 0.4 mm pitch	53+/- 10 %	℃/W

8 Ordering Information

Table 8-1 Ordering Information

Product Model		HC32F420FAUB-QFN32TR	HC32F420JAUB-QFN48TR	HC32F420JATB-LQ48	HC32F420KATB-LQFP64
Main frequency (MHz)		84			
Kernel		M4			
Flash (KB)		128			
RAM (KB)		24			
GPIO		27	38	38	52
Voltage (V)		2.0 ~ 5.5			
DMA		6			
Timing and counting	Composite Timer CTIMER	3			
	Advanced Timer ATIMER	2			
	WDT	1 ch IWDT+1 ch WWDT			
Communication Interface	USART	4			
	I²C	2			
	SPI	2			
Simulation	ADC 12 bit	2 10 ch	2 10 ch	2 10 ch	2 16 ch
	VC	2			
	OTS	✓			
	LVD	✓			
Unique identification code		✓			
Working temperature (℃)		-40~105			
Packaging	Encapsulation Form:	QFN32 (4*4)	QFN48 (7*7)	LQFP48 (7*7)	LQFP64 (10*10)
	Foot Spacing	0.4 mm	0.5 mm	0.5 mm	0.5 mm
	Package style	Tape&Reel	Tape&Reel	TRAY	TRAY

Version Revision History

Version Number	Revision Date	Modify the content
Rev1.00	2023/03/31	First edition release.
Rev1.10	2024/05/06	1) 3.19 12 Bit SARADC: Modified the number of input channels from 19 to 18; Removed the description of "one built-in BGR 1.2V voltage". 2) 3.20 Voltage Comparator VC: Modified the number of internal negative input channels from 5 to 4; Removed the description of "one built-in BGR 1.2V voltage". 3) 4.2 Pin Function Table: Added the descriptions of SWDIO and SWCLK; Modified the order of BOOT0/PB11. 4) 5 Typical Application Circuit Diagram: Removed the ferrite bead and related descriptions in Figure 5-1 Typical Application Circuit Diagram; Modified RESETB in the figure to NRESET. 5) 6.2 Absolute Maximum Ratings: Modified the storage temperature range in Table 6-3 Temperature Characteristics to "-65 ~ +150". 6) 6.3.3 Embedded Reset and LVD Module Features: Added a data source description to Table 6-7 LVD Module Characteristics. 7) 6.3.6 Time to Wake up from Low Power Mode: Added a data source description to Table 6-10 Wake-up Time from Low Power Mode. 8) 6.3.14 TIM Timer Features: Modified the condition of timer resolution in Table 6-24 Composite Timer (CTIM) Characteristics to free counting. 9) 6.3.18 Temperature Sensor Characteristics: Added a new section. 10) 6.3.19 VC Characteristics: Removed the description of "1.2V BGR reference".
Rev1.11	2025/05/07	1) 3.2 32-bit CORTEX M4 core: Modified the description of the core description in Table 3-1: Added descriptions for no MPU and no Trace, removed JTAG from the debug interface; changed the number of interrupts to "NMI + 1 to 64 physical interrupts"; changed the interrupt priority to "8 priority levels"; removed the description "Optional Retention Mode with Arm Power Management Kit" from Sleep Modes; changed the number of wake-up interrupts to 64. 2) 6.3.15.2 SPI Features: Modified the parameters related to the serial clock period, the effective time of slave data output, and the hold time of slave data output in Table 6-27 SPI Interface Features; added table notes: "Data is given based on the condition of VCC = 3.0V" and "The maximum division coefficient in host mode is PCLK/2, and in slave mode is PCLK/4". 3) 3) 6.3.16 NRESET Pin Characteristics: In Table 6-28 RESET Pin Features, changed the maximum value of the input filtered pulse from "100ns" to "2μs", and changed the minimum value of the input unfiltered pulse from "300ns" to "10μs".