XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F334 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.00 June 2024

Features

ARM Cortex-M4 32bit MCU+FPU, 120MHz/ 150DMIPS, 128KB Flash, 36KB SRAM, 5KB OTP, 15Timers, 6HRPWMs, 3ADCs, 3DACs, 3CMPs, 4UARTs, 3LINs, 1SPI, 1I2C, 2CAN FDs (FD/ 2.0B)

- **ARMv7-M Architecture 32-bit Cortex-M4 CPU**
  - Integrated FPU, MPU
  - Support DSP and CoreSight standard debug unit of SIMD instructions,
  - The maximum operating frequency is 120MHz, achieving a computing performance of 150DMIPS or 410Coremarks
- **Built-in memory**
  - Maximum 128KB Flash memory
  - Maximum 36KB of single-cycle access high-speed SRAM
- System power supply: 1.8~3.63V
- **Extensive Clock and Reset Management Resources**
  - 7 Independent Clock Sources:
    - External master clock crystal (4-25MHz)
    - External secondary crystal oscillator (32.768KHz)
    - Internal high-speed RC (16/20MHz)
    - Internal medium speed RC (8MHz)
    - Internal low speed RC (32KHz)
    - PLLH clock
    - Internal WDT dedicated RC (10KHz)
  - There are 15 reset sources, each reset source has an independent flag. Reset sources include power-on reset (POR), low voltage detection reset (PVD1R/PVD2R), pin reset (NRST), etc.
- **Integrate low-power operation mode to meet power control and host computer monitoring application requirements**
  - Supports three low-power operation modes: Sleep/Stop/Power Down
  - Peripherals can be turned off or on independently
- **Flexible Peripheral Operation Support System can Significantly Reduce CPU Processing Load**
  - 8-channel single-master DMAC
  - Support mutual triggering of peripheral events (AOS)
  - Integrates 16 programmable logic blocks (PLA) to support custom wave generation design
- **Built-in High-performance Analog modules Can Effectively Reduce Peripheral BOM Devices**
  - 3 independent 12bit 2.5MSPS ADCs
  - 3 independent 12-bit 15MSPS DACs
  - 3 independent voltage comparators (CMP)
- **Rich timer and PWM Peripherals meet Various Counting/Timing and Wave Generation Requirements**
  - 6*2-channel 130ps high-resolution PWM (HRPWM), i.e. 12-channel HRPWM
  - 4 multi-function 16-bit PWM Timers (Timer6), supporting 4*2-channel PWM
  - 1 16-bit motor PWM Timer (Timer4), supports 1*8-channel PWM
  - 1 32-bit general-purpose Timer (TimerA), suppor 1*4-channel PWM
  - 4 16bit general-purpose Timers (TimerA), support4*4-channel PWM
  - 2 16-bit basic Timers (Timer0)
  - Real-time clock (RTC)
  - 2 WDTs, 1 supports internal dedicated clock
- **Featured High-precision HRPWM meets Digital Power Generation and Control Requirements**
  - It has 12 channels of 130ps high-precision PWM outputs, and the duty cycle, frequency, phase shift angle and dead zone all support high precision; and it has built-in voltage and temperature compensation functions to ensure high precision in the full temperature range
  - Flexible and diverse waveform generation modes: supporting edge-aligned, centre-aligned PWM, interleaved, and dynamic phase-shifting waveform generation modes, meeting the various waveform generation requirements of digital power supplies.
  - Independent counting mode: 6 independent 22-bit counting units, supporting sawtooth (upward) or triangular wave counting modes.
  - Rich comparison events: 6 general-purpose events, 2 dedicated events, 10 external events, zero-crossings, period points, and more, providing more flexible waveform configuration options.
  - Supports single cache global flag setting and forced shutdown function, which can effectively solve the problems of continuous wave and wave loss in variable frequency topology control (such as LLC, etc.)
  - Support capture function
  - Support external event fast asynchronous mode
  - Support EMB function
  - Support synchronous DAC function
  - Other special features: such as support for immediate idle, interval output, delayed idle, etc.
- **Up to 53 GPIOs, up to 83% GPIO Availability**
  - Up to 53 GPIOs, all support 5V-tolerant IO
- **Up to 8 communication interfaces for power control and host computer monitoring applications**
  - 4 USARTs (3 of which support LIN), supporting ISO7816-3 protocol
  - 1 SPIs
  - 1 I2C, support SMBus protocol
  - 2 CAN FD controllers (MCAN), supporting CAN2.0A/B
- **Package:**
  - LQFP64 (10×10mm)
  - LQFP48 (7×7mm)
  - QFN48 (5×5mm)
  - QFN32 (4×4mm)
- **Target Industry Applications**
  - For AC/DC, DC/DC digital power applications, such as communication and server power supplies, brick power supplies, micro-inverters, DC charging pile power modules, energy storage DC/DC, outdoor power supplies, etc.

Support Model

HC32F334KATI-LQFP64	**HC32F334K8TI-LQFP64**
HC32F334JATI-LQ48	**HC32F334J8TI-LQ48**
HC32F334JAUI-ZFN48TR	**HC32F334J8UI-ZFN48TR**
HC32F334FAUI-QFN32TR	**HC32F334F8UI-QFN32TR**

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1 Overview

The HC32F334 product family is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 120MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

The HC32F334 series integrates high-speed on-chip memory, including up to 128KB of Flash and up to 36KB of SRAM; Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus master includes CPU and DMA. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events, which can significantly reduce the transaction processing load of the CPU.

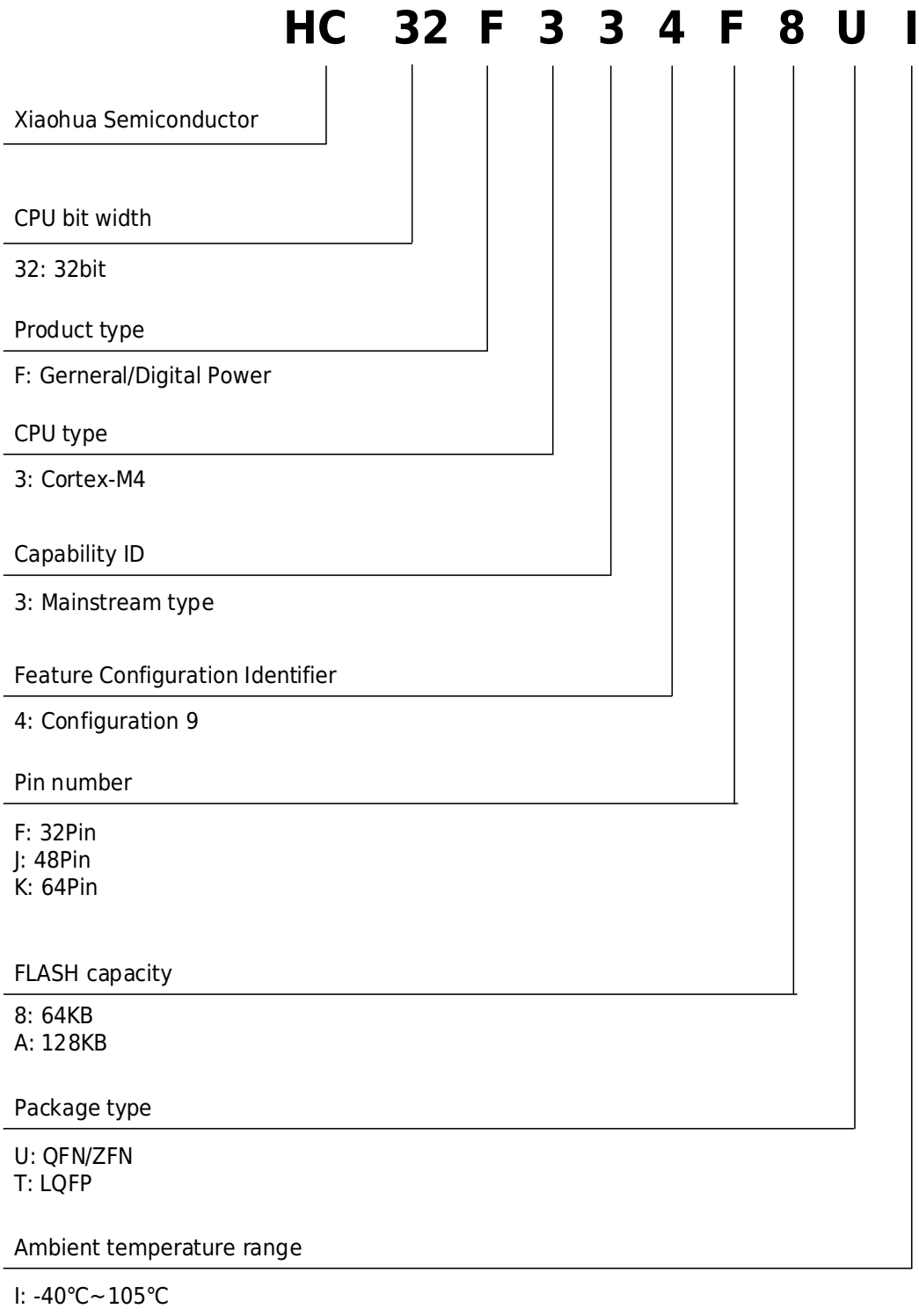
The HC32F334 series integrates a wealth of peripheral functions, including 3 independent 12bit 2.5MSPS ADCs; 3 12bit 15MSPS DACs; 3 high-speed voltage comparators (CMP); 4 multi-function PWM Timers (Timer6), supporting orthogonal encoding input and 8-channel complementary PWM output; 6 22-bit high-precision PWM (HRPWM), supporting 12-channel 130ps high-resolution PWM waveform output; 1 motor PWM Timer (Timer4), supporting 8-channel complementary PWM output; 4 16-bit universal timers (TimerA) and 1 32-bit universal timer (TimerA), supporting orthogonal encoding input and 20 channels of duty cycle adjustable PWM output; 6 serial communication interfaces (I2C/UART/SPI); 2-way MCAN controllers.

The HC32F334 series supports a wide voltage range (1.8~3.63V), a wide operating temperature range (-40~105℃) and various low power modes.

Typical Application

The HC32F334 series provides 64-pin and 48-pin LQFP packages, and 48-pin and 32-pin QFN packages, and can be used in AC/DC, DC/DC digital power applications, such as communications and server power supplies, brick power supplies, micro-inverters, charging pile modules, energy storage bidirectional DC/DC, high-performance frequency conversion control and other fields.

1.1 Part Naming Rules



1.2 Model Function Comparison Table

Table 1-1 Model Function Comparison Table

Function		Product Model							
		HC32F334F8UI-QFN32TR	HC32F334FAUI-QFN32TR	HC32F334J8UI-ZFN48TR	HC32F334JAUI-ZFN48TR	HC32F334J8TI-LQ48	HC32F334JATI-LQ48	HC32F334K8TI-LQFP64	HC32F334KATI-LQFP64
Pin number		32	32	48	48	48	48	64	64
Number of GPIOs		27	27	39	39	39	39	53	53
5V Tolerant Number of GPIOs		27	27	39	39	39	39	53	53
Package		QFN	QFN	QFN	QFN	LQFP	LQFP	LQFP	LQFP
Working Temperature Range		-40~105℃							
Supply voltage range		1.8~3.63V							
Storage Space	Flash	64KB	128KB	64KB	128KB	64KB	128KB	64KB	128KB
	OTP	5KB							
	SRAM	36KB							
DMA controller		1unit * 8ch							
External port interrupt		EIRQ * 16							
Communication Interface	USART(1)	4ch							
	SPI	1ch							
	I2C	1ch							
	CAN FD	2ch							
Timer and counter(2) (3)	Timer0	2unit							
	TimerA	5unit							
	Timer4	1unit							
	Timer6	4unit							
	HRPWM	6unit							
Timer and counter	WDT	1ch							

Function		Product Model							
		HC32F334F8UI-QFN32TR	HC32F334FAUI-QFN32TR	HC32F334J8UI-ZFN48TR	HC32F334JAUI-ZFN48TR	HC32F334J8TI-LQ48	HC32F334JATI-LQ48	HC32F334K8TI-LQFP64	HC32F334KATI-LQFP64
	SWDT	1ch							
	RTC	1ch							
Analog	12bit ADC	3unit ,9ch	3unit ,9ch	3unit ,16ch	3unit ,16ch	3unit, 16ch	3unit, 16ch	3unit, 22ch	3unit, 22ch
	12bitDAC	3ch							
	CMP	3ch							
Programmable Logic Array (PLA)		✓							
Frequency Monitoring Module (FCM)		✓							
Programmable Voltage Detection Function (PVD)		✓							
Debug Controller (DBGC)	SWD	✓							
	JTAG	✓							

Note:

1) USART_2/3/4 units with LIN function
2) Timer6, HRPWM, TimerA, Timer0 with capture input function
3) Timer6 and TimerA support 2-phase orthogonal encoding counting and 3-phase orthogonal encoding counting functions

1.3 Functional Block Diagram

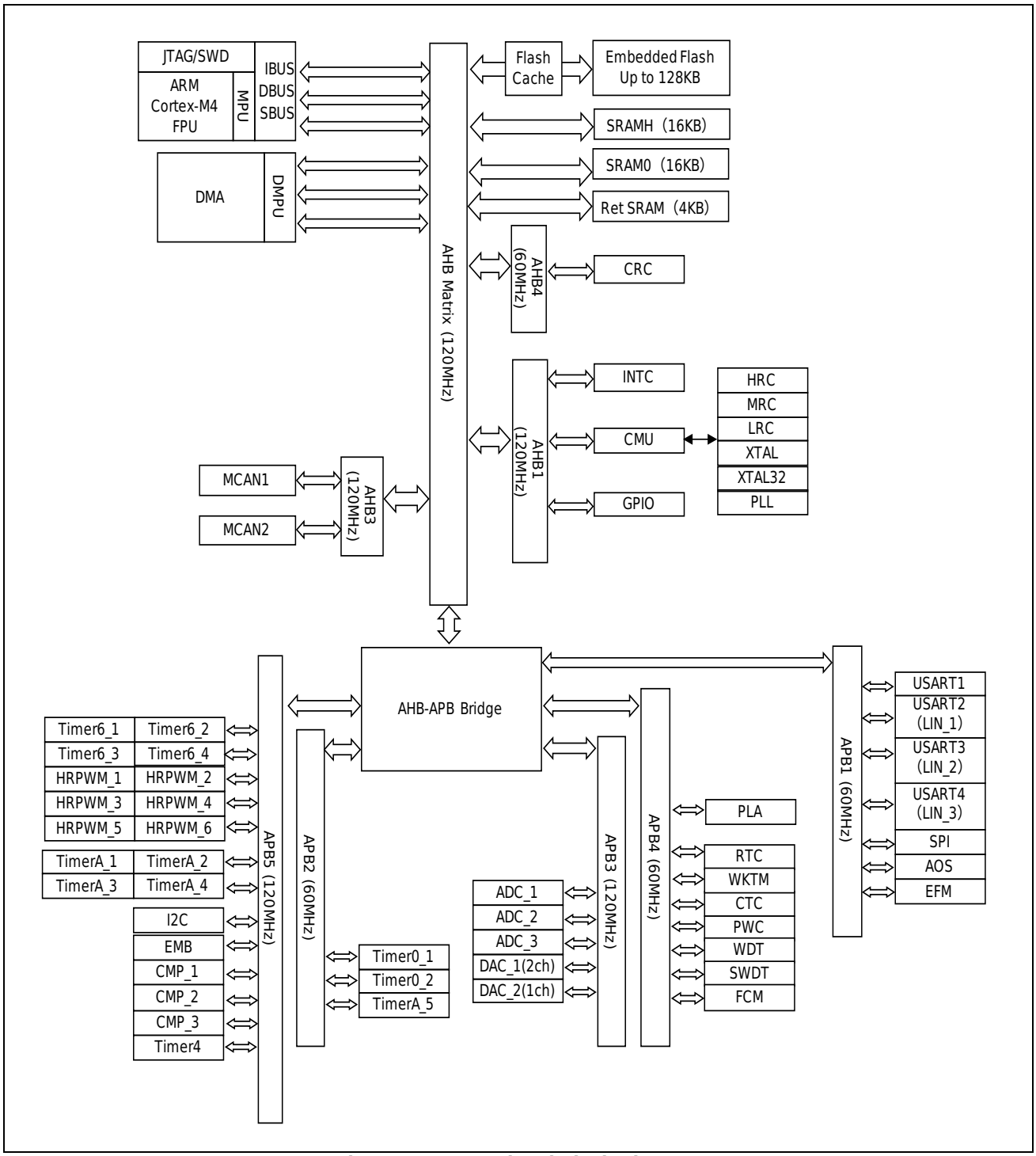


Figure 1-1 Functional Block Diagram

1.4 Feature Brief

1.4.1 CPU

The HC32F334 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit, which realizes fewer pins and lower power consumption while providing excellent computing performance and rapid interrupt response capability. Cortex-M4 command efficiency can be fully realized with integrated on-chip memory. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. The single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of 32-bit multilayer AHB bus matrix, which can interconnect the following host bus and slave bus.

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA Bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (the bus used by hosts other than the CPU to access Flash)
  - High-speed SRAMH (SRAMH 16KB) bus
  - System SRAM (SRAM0 16KB) bus
  - System SRAM (Ret SRAM 4KB) bus
  - APB1 peripheral bus (SPI/ USART/ EFM/ AOS)
  - APB2 peripheral bus (TimerA/Timer0)
  - APB3 peripheral bus (ADC/DAC)
  - APB4 peripheral bus (FCM/ WDT/ SWDT/ PWC/ CTC/ RTC/ WKTM/ PLA) KTM/)
  - APB5 peripheral bus (TimerA/ Timer4/ Timer6/ EMB/ HRPWM/ CMP/ I2C)
  - AHB1 peripheral bus (CMU/ GPIO/ DMA/ INTC/ DMPU)
  - AHB3 peripheral bus (MCAN)
  - AHB4 peripheral bus (CRC)

With the help of the bus matrix, high -efficiency concurrent access from the host bus to the slave bus can be realized.

1.4.3 Reset Control (RMU)

The chip is configured with 15 reset modes.

- Power-on Reset (POR)
- NRST pin reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock exception reset (CKFER)
- External High Speed Oscillator Abnormal Reset (XTALER)
- Cortex-M4 Lock-Up Reset (LKUPR)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including an external high-speed oscillator, an external low-speed oscillator, a PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, an SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing and clock gating circuits.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock by measuring the reference clock, and will interrupt or reset when the clock frequency exceeds the set range.

AHB, APB and Cortex-M4 clocks are all derived from the system clock. The maximum operating clock frequency of the system clock can reach 120MHz, and there are 6 selectable clock sources:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) PLLH Clock (PLLH)
4) Internal high-speed oscillator (HRC)
5) Internal Medium Speed Oscillator (MRC)
6) Internal low-speed oscillator (LRC)

For each timer, you can turn it on and off separately when not in use to reduce power consumption. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC). The real-time clock (RTC) uses an external low-speed oscillator, an internal low-speed oscillator, or an XTAL fractional clock as its clock source.

For each timer, you can turn it on and off separately when not in use to reduce power consumption.

1.4.5 Power Control (PWC)

Power controller is used to control the supply, switching and detection of multiple power domains in multiple operation modes and low power modes. The power controller is composed of power control logic (PWC) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8 V to 3.63 V. A voltage regulator (LDO) supplies power to the VDD and VDDR domains, and a VDDR voltage regulator (RLDO) supplies power the VDDR domain in power-down mode. The chip provides three low power consumption modes: sleep, stop and power-down through the power consumption control logic (PWC).

The power voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), and programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the reset action of the chip by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or

interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

After the chip enters power-down mode, the VDDR area can maintain power through RLDO to ensure that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate, and keep the data of 4KB RetSRAM.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000 0400~0x0000 045F and load the data into the initialization configuration register. Addresses 0x0000 0408~0x0000 040B, 0x0000 0410~0x0000 041F, 0x0000 0438~0x0000 045F are reserved addresses, please write all 1s to ensure the normal operation of the chip. If FLASH boot exchange is invalid, there is FLASH sector 0 in this area; if FLASH boot exchange is valid and OTP of FLASH sector 0 is not latched (0x0300 0A80~0x0300 0A83 data all 1), there is FLASH sector 1 in this area; otherwise, there is FLASH sector 0 in this area; the user can modify the initialization configuration registers (0x0000 0410~0x0000 041F) by programming or erasing sector 0 to modify the initialization configuration registers (0x0000 0410~0x0000 041F), please write all 1 to ensure the normal operation of the chip. Users can program or erase sector 0 to modify the Initialization Configuration Register (ICG). Addresses 0x0000 0420~0x0000 0437 are data security protection enable areas. The register reset value is determined by the FLASH address data.

1.4.7 Embedded Flash Interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE, and MCODE buses, and can perform programming, erasing, and full-erase operations on the FLASH; it accelerates code execution through instruction prefetching and caching mechanisms.

Main Features:

- Up to 5KBytes of OTP space
- ICODE bus 16Bytes prefetch instruction
- Two independent buffers: ICODE bus buffer space 1KBytes; DCODE bus buffer space 128Bytes
- Support boot swap function
- Support Data Security Protection

1.4.8 Built-in SRAM (SRAM)

This product has 32KB system SRAM (SRAMH/SRAM0) and 4KB power-down mode retention SRAM (Ret SRAM).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM read and write operations can be performed at the fastest CPU speed (120MHz).

Ret SRAM can provide 4KB of data retention space in Power Down mode 1/2.

SRAMH, SRAM0 and Ret SRAM have ECC (Error Checking and Correcting). The ECC check is a one-correction-two-check code, which can correct one-bit error and detect two-bit errors.

1.4.9 General IO (GPIO)

Main Features of GPIO:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up and pull-down
- Support push-pull, open-drain output mode
- Support high, medium and low drive modes
- Support CMOS/Schmitt input modes
- Support external interrupt input
- Support I/O pin peripheral function multiplexing, each I/O pin has up to 51 selectable multiplexing functions
- Individual I/O pins can be programmed independently

- Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The interrupt controller (INTC) selects interrupt events as interrupt requests to NVIC to wake up WFI; selects interrupt events as event inputs (RXEV) to wake up WFE; selects interrupt events to wake up the system in low power mode (sleep mode and stop mode); controls external interrupts and software interrupts.

The main specifications of INTC are as follows:

- NVIC interrupt request: INTC is equipped with 303 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQs). It supports 145 IRQs, and each IRQ corresponds to one or more interrupt events.
- Programmable priority: 16 programmable priorities (4-bit interrupt priority register is used).
- Non-maskable interrupts: Multiple system interrupt events can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable selection, flag, and flag clear registers.
- Equipped with 16 external pin interrupt events.
- Equipped with multiple interrupt events, please refer to the interrupt event list for details.
- Equipped with 32 software interrupt events.
- Interrupt wakes up system sleep mode and stop mode.

1.4.11 Automatic Operation System (AOS)

The automatic operation system (Automatic Operation System) is used to realize the linkage between peripheral hardware circuits without the help of the CPU. Use the events generated by the peripheral circuit as the AOS source (AOS Source), such as the comparison and matching of the timer, timing overflow, the periodic signal of the RTC, and the various states of the communication module's sending and receiving data (idle, receiving data full, sending data end, sending data empty), ADC conversion end, etc., to trigger other peripheral circuit actions. The triggered peripheral circuit action is called AOS target (AOS Target).

1.4.12 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

This chip has built-in 1 MPU unit for CPU, 1 MPU unit for CPU main stack pointer, 1 MPU unit for CPU thread stack pointer, 1 MPU unit for DMA and 1 MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

MSPMPU/PSPMPU respectively provide protection for the CPU's main stack pointer/thread stack pointer. When the pointer exceeds the set range, the MPU action can be set to non-maskable interrupt/reset.

SMPU1 provides system DMA with read and write access rights control for the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IPMPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.13 Internal Clock Calibrator (CTC)

The Clock Trimming Controller (CTC) automatically calibrates the internal high-speed oscillator (HRC). Because the influence of working environment on HRC frequency may cause deviation, CTC can automatically adjust HRC frequency by hardware based on external high precision reference clock to obtain an accurate HRC clock.

The main features of CTC are as follows:

- Hardware automatic calibration without software involvement
- Three external reference clock sources: XTAL, XTAL32, CTCREF

- Two calibration modes: continuous calibration and single calibration
- 16-bit calibration counter for frequency measurement with heavy load function
- 8-bit calibration deviation and 6-bit calibration values for frequency calibration
- Error interrupt to prompt calibration failure

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral functional modules. It can exchange data between memory, between memory and peripheral functional modules and between peripheral functional modules without CPU involvement.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus protocol.
- With 1 DMA control units, a total of 8 independent channels, which can independently operate different DMA transfer functions
- For each channel, the source of the boot request is configured via a separate trigger source
- One block per request
- The minimum data block is 1 data and the maximum is 1024 data.
- The width of each data can be configured as 8bit, 16bit or 32bit
- Can be configured to transmit 1~65535 times or unlimited times
- The source address and target address can be independently configured as fixed, auto-increment, auto-decrement, loop or jump with a specified offset
- Three types of interrupts can be generated: block transport complete interrupt, transport complete interrupt and transport error interrupt. Each interrupt can be configured with a mask or not. Among them, the block transmission is completed, and the transmission completion can be used as an event output, which can be used as a trigger source for other peripheral modules
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support channel reset triggered by external events
- You can set the module stop state to reduce power consumption when not in use
- Support software start and software triggered channel reset function

1.4.15 Voltage Comparator (CMP)

A voltage comparator (CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with two groups of 3 comparison channels: CMP1/CMP2, CMP3.

CMP has the following main features:

- 3 comparison channels can perform common comparison independently
- The combination of CMP1/CMP2 comparison channels can realize window comparison
- Each comparison channel has multiple input sources (IO/DAC) for selection of positive/negative voltage
- Configurable hysteresis voltage
- Noise filter can filter the comparator output, 7 sampling clocks are optional
- Timer PWM can be used to output the comparator blank window control
- Can generate interrupts on the changing edge of the comparison result, trigger other peripherals, and wake up the STOP mode
- The comparison result can be monitored through registers and can also be output to external pins
- Comparison results can be used for emergency brake (EMB) control events
- The comparison result can be used as an external event source for HRPWM
- The comparator output keeps on when software reset and watchdog reset occur.

1.4.16 Analog-to-Digital Converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. This MCU is equipped with 3 ADC units. Unit 1 supports a maximum of 16 channels, unit 2 supports a maximum of 12 channels, and unit 3 supports a maximum of 10 channels. It can convert analog signals from external pins and inside the chip. The analog input channels can be arbitrarily combined into a

sequence, and a sequence can be converted in a single scan or in a continuous scan. It supports multiple consecutive conversions on any specified channel and averages the conversion results. The ADC module is also equipped with an analog watchdog function to monitor the conversion result of any specified channel to detect whether it exceeds the range set by the user.

The main features of the ADC are as follows:

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of the ADC digital interface clock PCLK4 and the conversion clock PCLK2 (also called ADCLK) can be set to 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    PCLK2 can be a PLL clock asynchronous with the system clock HCLK. In this case, the frequency ratio PCLK4:PCLK2=1:1
  - PCLK2 frequency supports up to 60MHz
  - Sampling rate: 2.5MSPS (PCLK2 = 60MHz, 12 bits, sampling 11 cycles, conversion 13 cycles)
  - The sampling time of each channel is independently programmed
  - Channel-independent data register
  - Data registers can be configured with left/right alignment
  - Consecutive multiple conversion average function
  - Oversampling function
  - Analog watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Up to 22 external analog input channels
  - 1 internal analog input: internal reference voltage
- Conversion start condition
  - Software Setup Conversion Started
  - Start of Peripheral Device Synchronization Trigger Conversion
  - External Pin Triggering Start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning
  - Sequence A multiple data cache mode
  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Co-working mode (For devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A Scan End Interrupt and Event ADC _ EOCA
  - Sequence B Scan End Interrupt and Event ADC _ EOCB
  - Analog watchdog 0 compared interrupt and event ADC _ CMP0
  - Analog watchdog 1 compared interrupt and event ADC _ CMP1
  - All four of these event outputs can start the DMA

1.4.17 Digital to Analog Converter (DAC)

This MCU is equipped with two 12-bit conversion accuracy digital-to-analog converter units DAC. The DAC1 unit contains two DAC conversion channels, which can be converted independently or synchronously. The DAC2 unit contains one DAC conversion channel. The analog voltage output range can be set in two levels. Each conversion channel is equipped with an output amplifier, which can directly drive external loads without external op amps.

The main features of the DAC are as follows:

- Three D/A conversion channels
- 12-bit conversion data can be configured as left-aligned or right-aligned format
- The two conversion channels of the same DAC can be converted synchronously
- The output can be used as the negative input of the voltage comparator (CMP)
- The output is equipped with an amplifier function and can directly drive external loads

- A/D conversion priority mode can reduce interference during ADC conversion

1.4.18 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can provide rich and flexible combinations and various interrupts, events, and PWM outputs in various complex application scenarios. This series of products is equipped with 4 units of Timer6.

The main functions of Timer6 are as follows:

- Supports two counting waveform modes: sawtooth wave and triangle wave
- Various PWM waveforms can be generated (unilateral aligned independent PWM, bilateral symmetric independent PWM, bilateral symmetric complementary PWM, bilateral asymmetric PWM, etc.)
- Software synchronization and hardware synchronization can be achieved between units (synchronous start, stop, clear, refresh, etc.)
- Support cache function (single-level cache and double-level cache)
- Support pulse width measurement and period measurement
- Support 2-phase quadrature encoding counting and 3-phase quadrature encoding counting
- Support EMB function
- Support 4*2 groups of capture input

1.4.19 High-Resolution PWM (HRPWM)

The High Resolution PWM (HRPWM) is a 22-bit timer capable of generating up to 12 high-resolution PWM waveforms. This series of products HRPWM is equipped with 6 counting units and supports up to 6 pairs of high-precision PWM outputs.

The main functions of HRPWM are as follows:

- Support two waveform modes: sawtooth wave and triangle wave
- Flexible PWM output
- 130ps resolution, supports period calibration
- Software synchronization and hardware synchronization can be achieved between units (synchronous start, stop, clear, refresh, etc.);
- Support synchronous output
- Each reference value register supports cache function
- Support interval output and delayed idle
- External events support blanking and window modes
- Support fast asynchronous control
- Support EMB function
- Support synchronous DAC function
- Support interleaved phase shifting function between multi-phase units
- Support 6 * 2-channel capture input

1.4.20 General Control Timer (Timer4)

General control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. 1 unit of Timer 4 is carried in this product family.

The main functions of Timer4 are as follows:

- Support two counting waveform modes: triangle wave and sawtooth wave
- Various PWM waveforms can be generated
- Support cache function
- Support EMB function

1.4.21 Emergency Brake Module (EMB)

The emergency brake module is a functional module that generates a control event and outputs it to the timer when certain conditions are met, so as to control the timer to stop or change the PWM signal output to the external motor. The following sources can be used to generate control events:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

1.4.22 General Timer (TimerA)

General-purpose timer A (TimerA) is a timer with 16/32-bit count width and 4-channel PWM output. This series of products is equipped with 5 TimerA units (unit 1 is a 32-bit timer; units 2 to 5 are 16-bit timers), which can achieve up to 20 PWM outputs.

The main functions of TimerA are as follows:

- The timer supports two counting waveform modes: triangle wave and sawtooth wave.
- Various PWM waveforms can be generated (unilaterally aligned PWM, bilaterally symmetrical PWM)
- Support synchronous start of counter
- Support comparison reference value register cache function
- Support 32-bit cascade count
- Support 2-phase quadrature encoding counting and 3-phase quadrature encoding counting
- Support 5*4-channel capture input

1.4.23 General Timer (Timer0)

General-purpose timer 0 (Timer0) is a basic timer that can implement synchronous counting and asynchronous counting. The timer contains 2 channels (CH-A and CH-B), which can generate compare match events and count overflow events during counting. The events can trigger interrupts or be used as event outputs to control other modules. This series of products is equipped with 2 units of Timer0.

The main functions of Timer0 are as follows:

- Support hardware trigger
- Support software synchronous startup
- Support 2*2-channel capture input

1.4.24 Real Time Clock (RTC)

The real-time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24-hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 Yes according to the month and year.

1.4.25 Watchdog Counter (WDT/SWDT)

This product has two watchdog counters, one is a dedicated watchdog counter (SWDT) whose counting clock source is a dedicated internal RC (SWDTLRC: 10KHz), and the other is a general watchdog counter (WDT) whose counting clock source is PCLK3. The dedicated watchdog and general watchdog are used to 16-bit down counters used to monitor software failures due to external disturbances or unforeseen logic conditions that deviate from the normal operation of the application program.

Both watchdogs support window comparison function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

1.4.26 General Synchronous Asynchronous Transceiver (USART)

This product is equipped with 4 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly perform full-duplex data exchange with external devices.| The USART on this product supports the universal asynchronous serial communication interface (UART), clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface; supports modem operation (CTS/RTS operation), processor operation,

and Driver Enable (DE) function. Cooperate with Timer0 module to support UART receive timeout function. USART_1 supports wake-up function from STOP mode via RX pin.

The specific functions are allocated as follows:

- UART: Full channel support
- Multiprocessor communications: full channel support
- Clock synchronous communication: full channel support
- RX pin wake-up Stop mode function: USART_1 support
- Fractional baud rate: all channels support
- LIN: Supported by USART_2, USART_3, USART_4
- Smart Card: USART_1 support
- UART receive timeout function: supported by USART_1, USART_2, USART_3, USART_4
- RS485 Driver Enable: supported by USART_1, USART_2, USART_3, USART_4

1.4.27 Integrated Circuit Bus (I2C)

I2C (Integrated Circuit Bus) is used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

I2C main features:

- I2C bus mode and SMBus bus mode are optional. Host mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100Kbps, fast mode up to 400Kbps, FM+ mode up to 1Mbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected.
- Supports up to 128 slave addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be sent automatically upon reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

1.4.28 Programmable Logic Array (PLA)

The configurable logic array provides 256 programmable digital logic operations for external pins, ADC, and timers without CPU intervention. This module implements 16 independent PLA units. Each PLA unit supports the output of GPIO port.

1.4.29 Serial Peripheral Interface (SPI)

This product is equipped with a 1-channel serial peripheral interface SPI, which supports high-speed full-duplex serial synchronous transmission and can easily exchange data with peripheral devices. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

Main Features of SPI:

- Serial communication function
  - Support 4-wire SPI mode and 3-wire clock synchronization mode
  - Support full-duplex and send-only communication modes
  - Polarity and phase of adjustable communication clock SCK
- Data format
  - Selectable data shift sequence: MSB first/LSB first

  - Selectable data width: 4/ 5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/ 13/ 14/ 15/ 16/ 20/ 24/ 32 bits
  - Up to 4 frames of 32-bit data can be transmitted or received at a time
- Baud rate
  - The baud rate can be adjusted by the built-in special baud rate generator in host mode. The baud rate ranges from 2 to 256 frequency division of PCLK1.
  - Maximum Baud Rate Allowed in Slave Mode is 6 Division of PCLK1
- Data buffer
  - Data buffer area with 16 bytes
  - Support double buffering
- Error monitoring
  - Mode fault error monitoring
  - Data overload error monitoring
  - Data underload error monitoring
  - Parity error monitoring
- Chip selection signal control
  - Each channel is configured with excluding chip-selected signal line
  - The relative timing relationship between the chip select signal and the communication clock can be adjusted
  - The invalid time of the chip select signal between two consecutive communications can be adjusted
  - Polarity adjustable
- Transmission Control in Host Mode
  - Start transmission by writing data to the data register
  - Communication auto suspend function
- Interrupt
  - The receiving data area is full
  - Sending data area is empty
  - SPI error (mode/overload/underload/parity)
  - SPI Vacant
  - Transfer completed (event sources only)
- Low power control
  - Configurable module stop
- Other functions
  - SPI initialization function

1.4.30 Controller Area Network (MCAN)

This product is equipped with two-unit MCAN communication interface modules (MCAN1 and MCAN2) and is equipped with 2KB of RAM for the two MCAN controllers.

Both CAN modules (MCAN1 and MCAN2) comply with ISO 11898-1: 2015 (CAN Protocol Specification Version 2.0 Part A, B) and CAN FD Protocol Specification Version 1.0 (CAN with Flexible Data-Rate Specification Version 1.0).

2KB of RAM is freely configurable and is used to implement message filters, receive FIFOs, receive buffers, transmit event FIFOs, and transmit buffers. The message RAM is shared between the MCAN1 and MCAN2 modules.

1.4.31 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC 13239 and adopts 32-bit and 16-bit CRC respectively. The generating polynomial of CRC32 is $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$, and the 32-bit initial value is 0xFFFF FFFF. The generating polynomial of CRC16 is $X^{16}+X^{12}+X^{5}+1$, and the 16-bit initial value is 0xFFFF.

1.4.32 Debug Controller (DBGC)

The core of this MCU is Cortex-M4, which contains hardware for advanced debugging functions. With these debugging features, you can stop the kernel when fetching fingers (instruction

breakpoints) or accessing data (data breakpoints). When the kernel is stopped, the internal state of the kernel and the external state of the system can be queried. Once the query is completed, the kernel and the system are restored and program execution resumes.

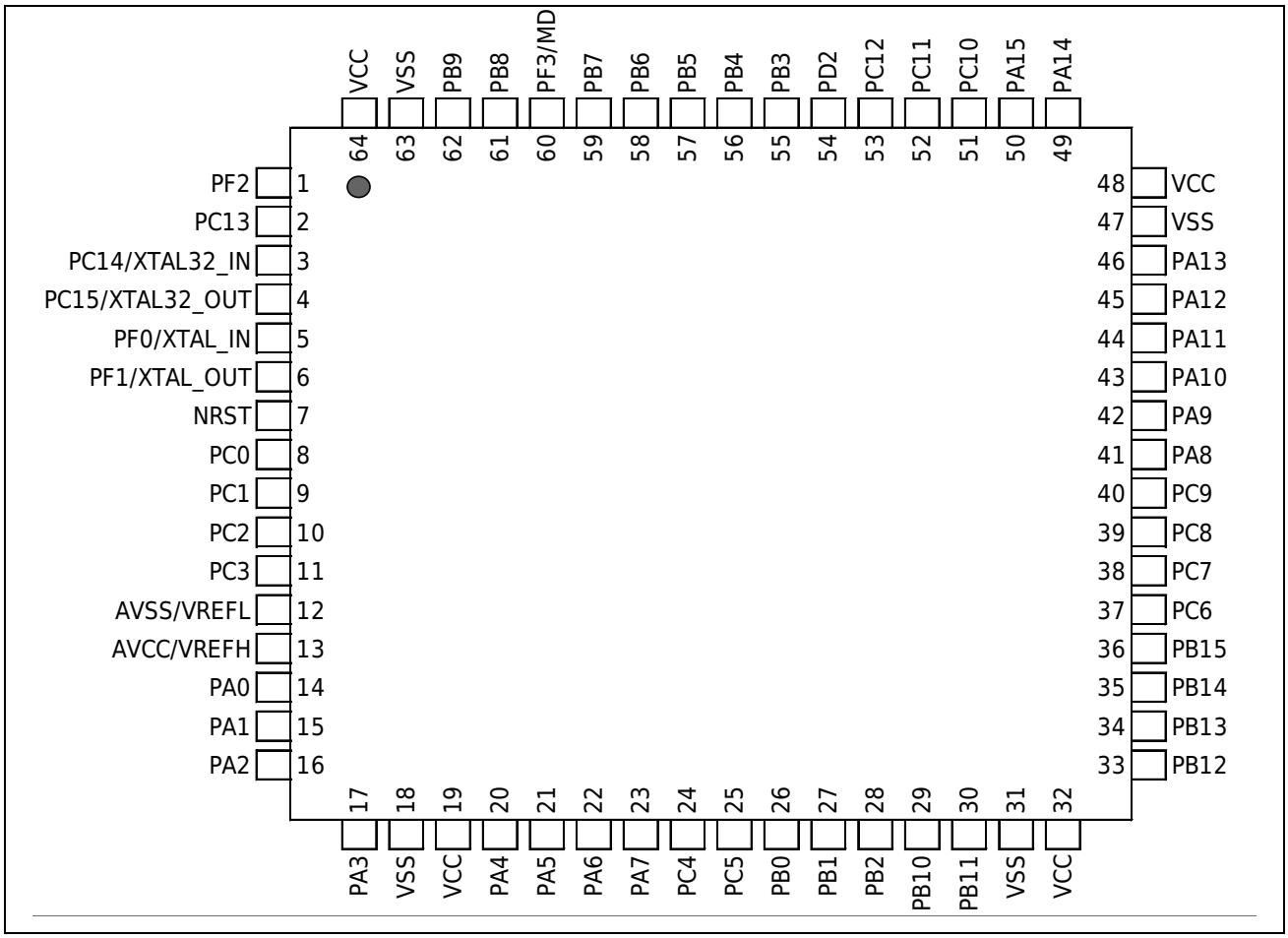
Two debugging interfaces are provided:

- Serial Debugging Tracking Interface SWD
- Parallel debug trace interface JTAG

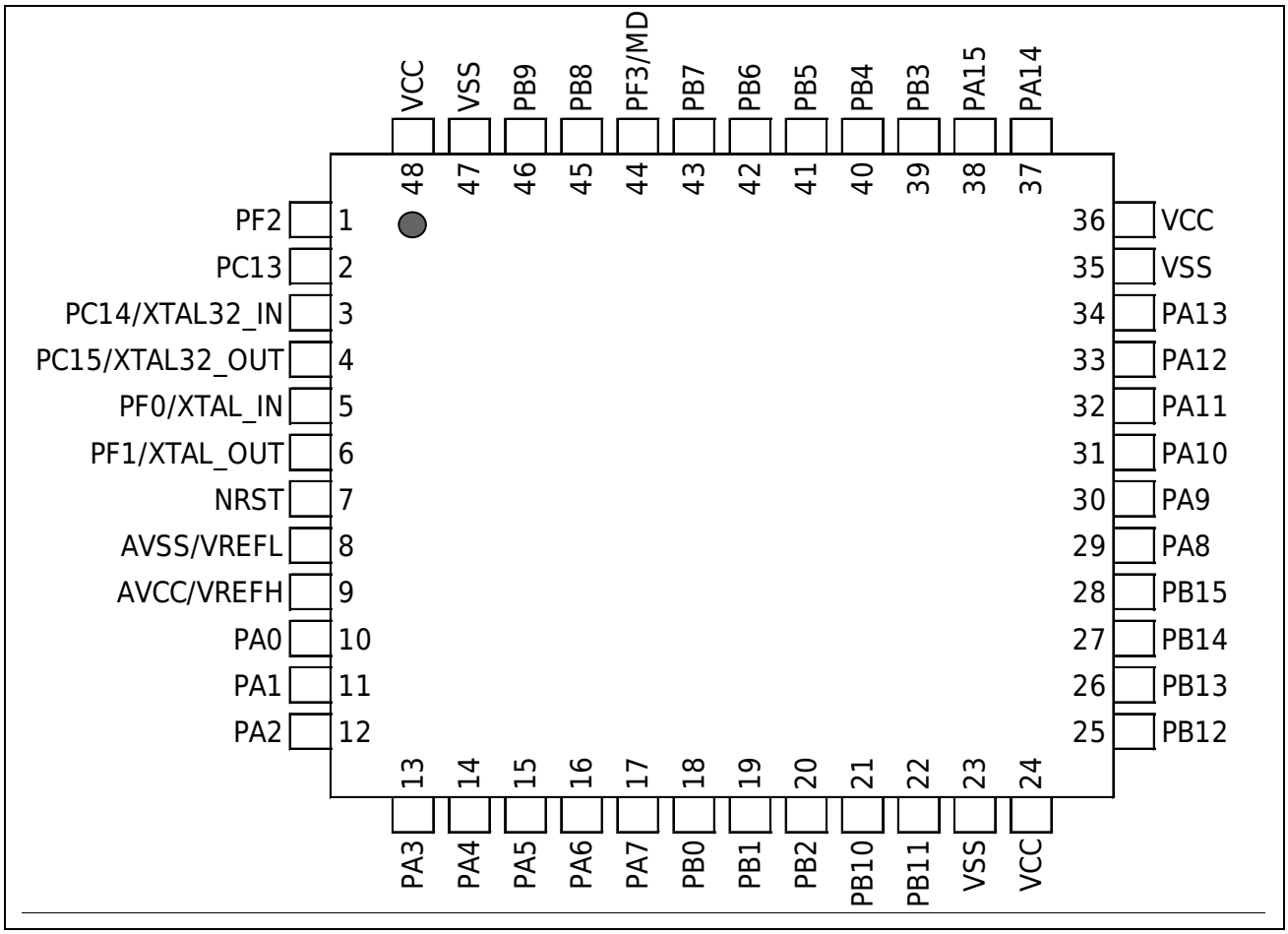
2 Pin Definitions

2.1 Pinout

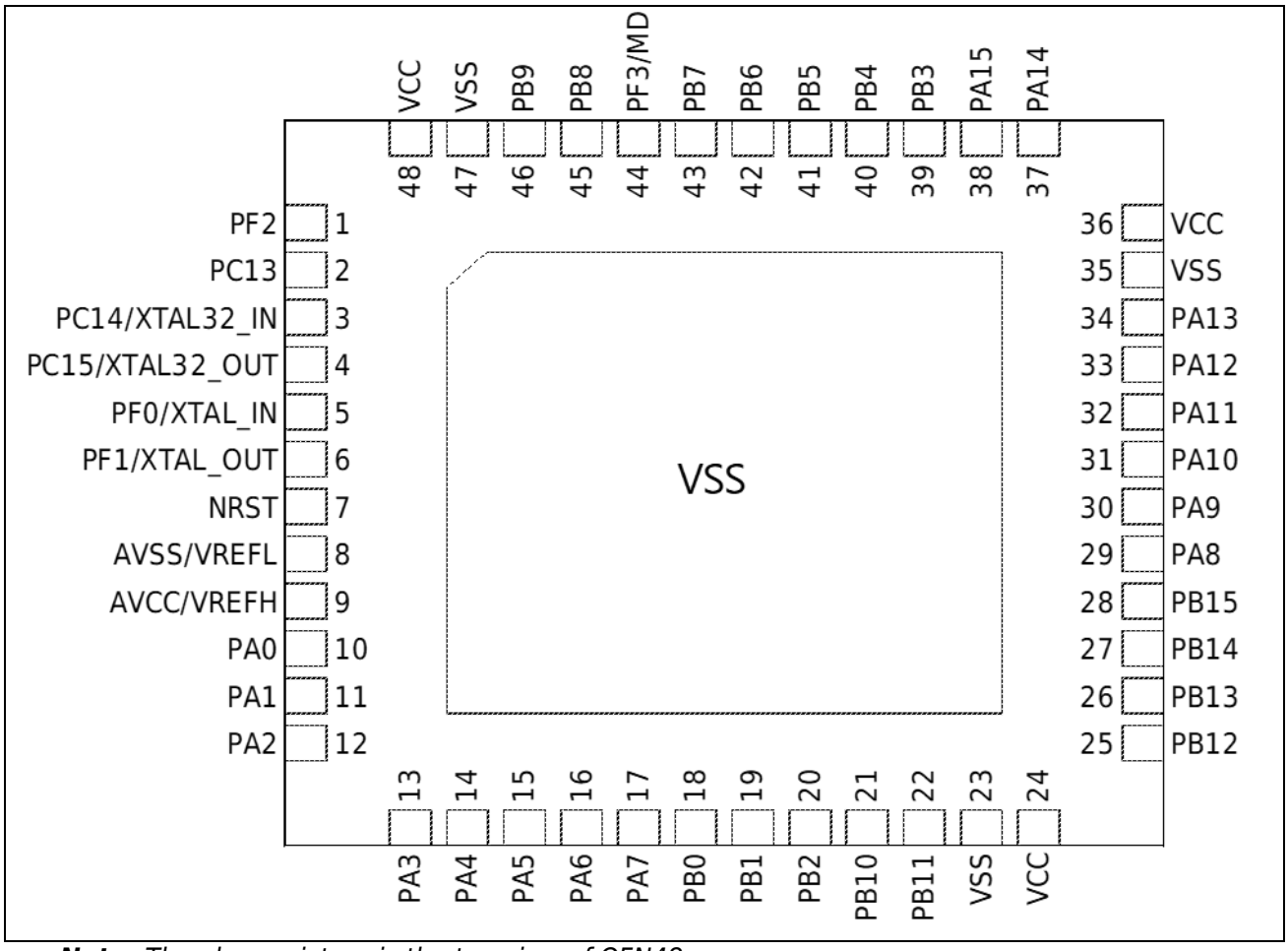
LQFP64



LQFP48

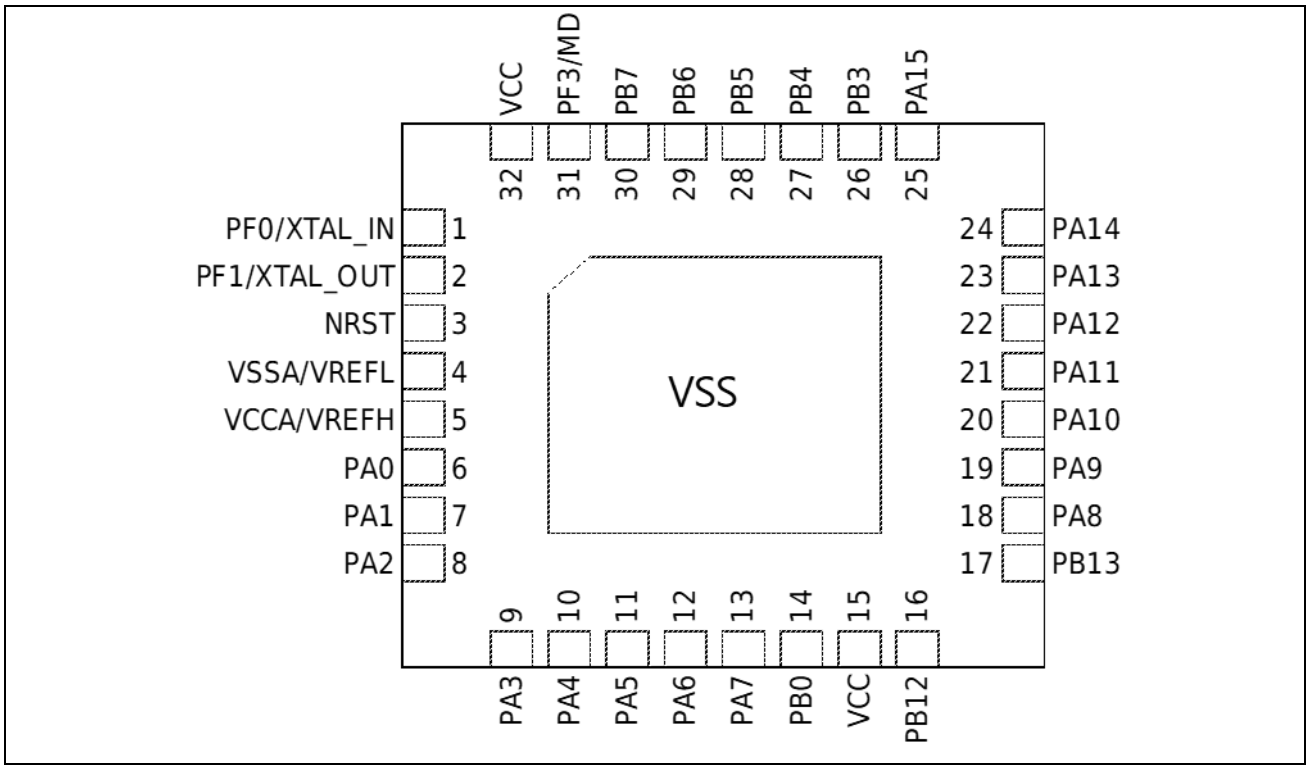

VCC 48
VSS 47
PB9 46
PB8 45
PF3/MD 44
PB7 43
PB6 42
PB5 41
PB4 40
PB3 39
PA15 38
PA14 37
PF2 1
PC13 2
PC14/XTAL32_IN 3
PC15/XTAL32_OUT 4
PF0/XTAL_IN 5
PF1/XTAL_OUT 6
NRST 7
AVSS/VREFL 8
AVCC/VREFH 9
PA0 10
PA1 11
PA2 12
36 VCC
35 VSS
34 PA13
33 PA12
32 PA11
31 PA10
30 PA9
29 PA8
28 PB15
27 PB14
26 PB13
25 PB12
13 PA3
14 PA4
15 PA5
16 PA6
17 PA7
18 PB0
19 PB1
20 PB2
21 PB10
22 PB11
23 VSS
24 VCC

QFN48



Note: *The above picture is the top view of QFN48.*

QFN32



Note: *The above picture is the Top View of QFN32.*

Figure 2-1 Pin Configuration Diagram

2.2 Pin Function Table

Table 2-1 Pin Function Table

LQFP 64	QFN/ LQFP48	QFN 32	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	HRPWM	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18~ 19	Func20	Func21	Func22	Func23	Func24	Func25	Func26	Func27~ 31	Func Group
								GPO	ADTRG	CMP	CMP	SPI	HRPWM/ EMB	HRPWM/ EMB	USART/ HRPWM	USART	PLA	PLA/HRPWM/ TIME	TIMER6	TIMER6	TMR6/ TMRA	TMR6/ TMRA	TMR6/ TMRA	TMR6, TMRA/ ADTRG	TIMERA		TIMER4/ CTC	EMB/CTC /FCM	EMB/ CMP	TMR4/ ADTRG	Other	EVENOUT	EVENTPORT/ ADTRG		
1	1	-	PF2		EIRQ2			GPO					EMB_PORT1_IN4		USART1_CK	USART4_CK	PLAIN0				TMR6_TRIGB		TMRA_4_TRIG				TMR4_OWH	EMB_PORT2_IN4		TMR4_ADSM					FG1
2	2	-	PC13		EIRQ13+WKUP3_1			GPO									PLAIN1	PLA3OUT		TMR6_1_PWMB							TMR4_OWL			TMR4_OXH	RTC_OUT		EVNTP313		FG1
3	3	-	PC14	XTAL32_IN	EIRQ14			GPO									PLAIN2										TMR4_PCT			TMR4_OXL			EVNTP314		
4	4	-	PC15	XTAL32_OUT	EIRQ15			GPO																			TMR4_ADSM			TMR4_CLK			EVNTP315		
5	5	1	PF0	XTAL_IN	EIRQ0			GPO		CMP3_OUT							PLAIN16			TMR6_3_PWMB	TMR6_TRIGC						TMR4_ADSM								
6	6	2	PF1	XTAL_OUT	EIRQ1			GPO		CMP1_OUT							PLAIN17										TMR4_PCT								
7	7	3	NRST																																
8	-	-	PC0	ADC12_IN10	EIRQ0			GPO				SPI_NSS3						PLA4OUT		TMR6_1_PWMA	TMR6_2_PWMB	TMRA_5_PWM1/CLKA										EVENTOUT	EVNTP300		FG1
9	-	-	PC1	ADC12_IN11	EIRQ1			GPO		CMP3_OUT		SPI_NSS2						PLA5OUT		TMR6_2_PWMA	TMR6_1_PWMB	TMRA_5_PWM2/CLKB										EVENTOUT	EVNTP301		FG1
10	-	-	PC2	ADC12_IN12	EIRQ2			GPO				SPI_NSS1						PLA6OUT		TMR6_3_PWMA	TMR6_4_PWMB	TMRA_5_PWM3										EVENTOUT	EVNTP302		FG1
11	-	-	PC3	ADC12_IN13	EIRQ3			GPO					EMB_PORT1_IN2					PLA7OUT		TMR6_4_PWMA	TMR6_3_PWMB	TMRA_5_PWM4						EMB_PORT2_IN2				EVENTOUT	EVNTP303		FG1
12	8	4	AVSS/VREFL																																
13	9	5	AVCC/VREFH																																
14	10	6	PA0	ADC1_IN0	EIRQ0+WKUP0_0			GPO		CMP1_OUT			EMB_PORT1_IN3	HRPWM_TRIGC			PLAIN18	TMR6_TRIGD	TMR6_1_PWMA	TMR6_1_PWMB	TMR6_TRIGB	TMRA_3_TRIG	TMRA_1_PWM1/_CLKA	TMRA_1_TRIG	TMRA_3_PWM1/CLKA			EMB_PORT2_IN3		TMR4_OXL	FCMREF	EVENTOUT	EVNTP100		FG1
15	11	7	PA1	ADC1_IN1+RTC_CLK1	EIRQ1			GPO					EMB_PORT1_IN4	HRPWM_TRIGD			PLAIN19				TMR6_TRIGA	TMRA_4_PWM2/CLKB	TMRA_1_PWM2/_CLKB		TMRA_3_PWM2/CLKB		TMR4_OUL	EMB_PORT2_IN4		TMR4_OXH		EVENTOUT	EVNTP101		FG1
16	12	8	PA2	ADC1_IN2+CMP1_INM2	EIRQ2			GPO	ADTRG1	CMP2_OUT	CMP1_OUT						PLAIN20	PLA0OUT			TMR6_5_TRIG	TMRA_5_PWM1/CLKA	TMRA_1_PWM3	TMRA_4_PWM1/CLKA	TMRA_3_PWM3		TMR4_OUH			TMR4_OUL		EVENTOUT	EVNTP102		FG1
17	13	9	PA3	ADC1_IN3+CMP1_INP2+CMP2_INP2+CMP3_INP2	EIRQ3			GPO	ADTRG2									PLA4OUT	TMR6_1_PWMA	TMR6_1_PWMB	TMRA_4_PWM3	TMRA_5_PWM2/CLKB	TMRA_1_PWM4	TMRA_5_TRIG	TMRA_3_PWM4		TMR4_CLK			TMR4_OUH		EVENTOUT	EVNTP103		FG1
18	-	-	VSS																																
19	-	-	VCC																																
20	14	10	PA4	ADC12_IN4+DAC1_OUT1+CMP1_INM1+CMP2_INM1+CMP3_INM1	EIRQ4			GPO							USART1_CK	USART2_CK		PLA5OUT					TMRA_4_TRIG	TMRA_2_PWM2/CLKB				TMR4_OVL				EVENTOUT	EVNTP104		FG1
21	15	11	PA5	ADC12_IN5+DAC1_OUT2	EIRQ5			GPO										PLA6OUT			TMRA_5_PWM3	TMRA_1_PWM1/CLKA	TMRA_1_TRIG	TMRA_3_TRIG	TMRA_3_PWM1/CLKA		TMR4_PCT			TMR4_OVH		EVENTOUT	EVNTP105		FG1
22	16	12	PA6	ADC123_IN6+DAC2_OUT1	EIRQ6			GPO		CMP1_OUT			EMB_PORT1_IN2	EMB_PORT1_IN1				PLA7OUT			TMRA_5_PWM4		TMRA_4_PWM1/_CLKA	TMRA_2_PWM1/CLKA	TMRA_5_PWM1/CLKA		TMR4_OVH	EMB_PORT2_IN2	EMB_PORT2_IN1			EVENTOUT	EVNTP106		FG1
23	17	13	PA7	ADC123_IN7+CMP1_INP1	EIRQ7			GPO	ADTRG3	CMP2_OUT								PLA1OUT	TMR6_1_PWMA		TMRA_5_PWM1/CLKA	TMR6_1_PWMB	TMRA_2_PWM2/_CLKB		TMRA_3_PWM4		TMR4_OWH					EVENTOUT	EVNTP107		FG1
24	-	-	PC4	ADC12_IN14	EIRQ4			GPO										PLA12OUT			TMR6_TRIGC	TMR6_TRIGA					TMR4_OWL			TMR4_OXH		EVENTOUT	EVNTP304		FG1
25	-	-	PC5	ADC12_IN15	EIRQ5			GPO					EMB_PORT1_IN3					PLA13OUT										EMB_PORT2_IN3		TMR4_OXL		EVENTOUT	EVNTP305		FG1
26	18	14	PB0	ADC123_IN8+CMP2_INP1	EIRQ0			GPO	ADTRG1								PLAIN8	PLA1OUT		TMR6_2_PWMA	TMR6_2_PWMB			TMRA_2_PWM3	TMRA_3_PWM1/CLKA		TMR4_ADSM				RTC_OUT	EVENTOUT	EVNTP200		FG1
27	19	-	PB1	ADC123_IN9	EIRQ1+WKUP0_1			GPO	ADTRG2	CMP1_OUT	CMP2_OUT			HRPWM_SCOUT			PLAIN9		TMR6_3_PWMA			TMR6_3_PWMB		TMRA_2_PWM4	TMRA_3_PWM2/CLKB		TMR4_PCT			TMR4_OWH	MCO_1	EVENTOUT	EVNTP201		FG1
28	20	-	PB2	ADC3_IN10+CMP2_INM2	EIRQ2+WKUP0_2			GPO	ADTRG3					HRPWM_TRIGA	USART1_CK	USART4_CK	PLAIN10			TMR6_TRIGB	TMR6_TRIGC	TMR6_TRIGD	TMRA_2_TRIG		TMRA_3_PWM3		TMR4_OWL				MCO_2	EVENTOUT	EVNTP202		FG1
29	21	-	PB10	ADC3_IN11	EIRQ10			GPO					HRPWM_EEV9	EMB_PORT1_IN3							TMR6_TRIGC		TMRA_1_PWM3	TMRA_3_PWM3								EVENTOUT	EVNTP210		FG1
30	22	-	PB11	CMP3_INP1	EIRQ11			GPO					HRPWM_EEV7	EMB_PORT1_IN4					TMR6_4_PWMA	TMR6_4_PWMB			TMRA_1_PWM4	TMRA_3_PWM4								EVENTOUT	EVNTP211		FG1
31	23	-	VSS																																
32	24	15	VCC																																
33	25	16	PB12	ADC3_IN0	EIRQ12		HRPWM_4_PWMA	GPO					EMB_PORT1_IN1		USART1_CK	USART3_CK	PLAIN10	PLA8OUT		TMR6_3_PWMB	TMR6_TRIGB	TMR6_3_PWMA			TMRA_4_PWM3			EMB_PORT2_IN1				EVENTOUT	EVNTP212		FG1

LQFP 64	QFN/ LQFP48	QFN 32	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	HRPWM	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18~ 19	Func20	Func21	Func22	Func23	Func24	Func25	Func26	Func27~ 31	Func Group
								GPO	ADTRG	CMP	CMP	SPI	HRPWM/ EMB	HRPWM/ EMB	USART/ HRPWM	USART	PLA	PLA/HRPWM/ TIME	TIMER6	TIMER6	TMR6/ TMRA	TMR6/ TMRA	TMR6/ TMRA	TMR6, TMRA/ ADTRG	TIMERA		TIMER4/ CTC	EMB/CTC /FCM	EMB/ CMP	TMR4/ ADTRG	Other	EVENOUT	EVENTPORT/ ADTRG		
34	26	17	PB13	ADC3_IN1	EIRQ13		HRPWM_4_PWMB	GPO									PLAIN11	PLA9OUT		TMR6_3_PWMA		TMR6_3_PWMB			TMRA_4_PWM4							EVENTOUT	EVNTP213		FG1
35	27	-	PB14	ADC3_IN2	EIRQ14		HRPWM_5_PWMA	GPO									PLAIN12	PLA10OUT		TMR6_4_PWMB		TMR6_4_PWMA	TMRA_3_PWM1/_CLKA		TMRA_4_PWM1/CLKA		TMR4_OUH					EVENTOUT	EVNTP214		FG1
36	28	-	PB15	ADC3_IN3+CMP3_INM2+RTC_CLK2	EIRQ15		HRPWM_5_PWMB	GPO		CMP1_OUT							PLAIN13	PLA11OUT		TMR6_4_PWMA		TMR6_4_PWMB	TMRA_3_PWM2/_CLKB	TMRA_4_PWM3	TMRA_4_PWM2/CLKB		TMR4_OUL					EVENTOUT	EVNTP215		FG1
37	-	-	PC6		EIRQ6		HRPWM_1_PWMA	GPO		CMP3_OUT				HRPWM_EEV10			PLAIN14	PLA12OUT		TMR6_1_PWMB	TMR6_TRIGD	TMR6_1_PWMA		TMRA_2_PWM1/CLKA			TMR4_OVH					EVENTOUT	EVNTP306		FG1
38	-	-	PC7		EIRQ7		HRPWM_1_PWMB	GPO						EMB_PORT1_IN5			PLAIN15	PLA13OUT		TMR6_2_PWMB		TMR6_2_PWMA		TMRA_2_PWM2/CLKB			TMR4_OVL					EVENTOUT	EVNTP307		FG1
39	-	-	PC8		EIRQ8		HRPWM_6_PWMA	GPO									PLAIN16	PLA14OUT		TMR6_3_PWMB		TMR6_3_PWMA		TMRA_2_PWM3			TMR4_OWH				MCO_2	EVENTOUT	EVNTP308		FG1
40	-	-	PC9		EIRQ9		HRPWM_6_PWMB	GPO									PLAIN17	PLA15OUT		TMR6_4_PWMB		TMR6_4_PWMA		TMRA_2_PWM4			TMR4_OWL				MCO_1	EVENTOUT	EVNTP309		FG1
41	29	18	PA8	EXVREF	EIRQ8+WKUP2_0	TRACED0	HRPWM_2_PWMA	GPO							USART2_CK	USART1_CK	PLAIN11	PLA0OUT	TMR6_1_PWMB		TMR6_1_PWMA				TMRA_2_PWM1/CLKA		CTCREF			TMR4_OXH	MCO_1	EVENTOUT	EVNTP108		FG1
42	30	19	PA9		EIRQ9	TRACECLK	HRPWM_2_PWMB	GPO					EMB_PORT1_IN3				PLAIN12	PLA1OUT	TMR6_1_PWMA		TMR6_1_PWMB		TMRA_1_PWM3	TMRA_3_PWM3	TMRA_2_PWM2/CLKB		TMR4_ADSM	EMB_PORT2_IN3		TMR4_OXL	MCO_2	EVENTOUT	EVNTP109		FG1
43	31	20	PA10		EIRQ10+WKUP2_2	TRACED1	HRPWM_3_PWMA	GPO		CMP3_OUT			EMB_PORT1_IN5				PLAIN13	PLA2OUT	TMR6_2_PWMB		TMR6_2_PWMA		TMRA_1_PWM4	TMRA_3_PWM4	TMRA_2_PWM3		TMR4_CLK	EMB_PORT2_IN5		TMR4_OWH		EVENTOUT	EVNTP110		FG1
44	32	21	PA11		EIRQ11+WKUP2_3	TRACED2	HRPWM_3_PWMB	GPO		CMP1_OUT			EMB_PORT1_IN2				PLAIN14	PLA3OUT					TMR6_2_PWMB	TMR6_2_PWMA	TMRA_2_PWM4		TMR4_OWL	EMB_PORT2_IN2				EVENTOUT	EVNTP111		FG1
45	33	22	PA12		EIRQ12+WKUP3_0	TRACED3		GPO		CMP2_OUT	CMP1_OUT	SPI_NSS1	HRPWM_EEV2	EMB_PORT1_IN1			PLAIN15	PLA7OUT	TMR6_TRIGC	TMR6_TRIGB	TMR6_TRIGA		TMRA_1_TRIG	TMRA_5_PWM1/CLKA			TMR4_OVH				FCMREF	EVENTOUT	EVNTP112		FG1
46	34	23	PA13		EIRQ13	JTMS_SWDIO		GPO					EMB_PORT1_IN5	HRPWM_EEV3	USART4_CK			PLA8OUT			TMR6_TRIGD			TMRA_5_PWM2/CLKB			TMR4_OVL		CMP3_OUT	ADTRG3		EVENTOUT	EVNTP113		FG1
47	35	-	VSS																																
48	36	-	VCC																																
49	37	24	PA14		EIRQ14+WKUP3_2	JTCK_SWCLK		GPO											TMR6_4_PWMB	TMR6_4_PWMA							TMR4_OUH	EMB_PORT2_IN1		ADTRG2		EVENTOUT	EVNTP114		FG1
50	38	25	PA15		EIRQ15+WKUP3_3	JTDI		GPO					HRPWM_EEV1	EMB_PORT1_IN2			PLAIN0	PLA3OUT			TMR6_TRIGC	TMRA_1_PWM1/CLKA	TMRA_1_TRIG	TMRA_3_TRIG	TMRA_3_PWM1/CLKA		TMR4_OUL		EMB_PORT2_IN1			EVENTOUT	EVNTP115		FG1
51	-	-	PC10		EIRQ10			GPO										PLA2OUT	TMR6_1_PWMA	TMR6_1_PWMB												EVENTOUT	EVNTP310		FG1
52	-	-	PC11		EIRQ11			GPO						HRPWM_EEV2				PLA14OUT													TMR4_OXH		EVENTOUT	EVNTP311		FG1
53	-	-	PC12		EIRQ12			GPO						HRPWM_EEV1	USART1_CK	USART3_CK		PLA15OUT													TMR4_OXL		EVENTOUT	EVNTP312		FG1
54	-	-	PD2		EIRQ2			GPO		CMP3_OUT				HRPWM_EEV10					TMR6_3_PWMB	TMR6_3_PWMA	TMR6_TRIGD				TMRA_2_TRIG			EMB_PORT2_IN5				EVENTOUT	EVNTP402		FG1
55	39	26	PB3		EIRQ3+WKUP0_3	JTDO_TRACESWO		GPO						HRPWM_EEV9	HRPWM_SCOUT		PLAIN1	PLA0OUT			TMR6_TRIGC	TMRA_1_PWM2/CLKB	TMRA_3_PWM2/_CLKB	TMRA_2_TRIG	TMRA_4_PWM1/CLKA		TMR4_OWL			TMR4_OVL		EVENTOUT	EVNTP203		FG1
56	40	27	PB4		EIRQ4+WKUP1_0	NJTRST		GPO						HRPWM_EEV7			PLAIN2	PLA1OUT	TMR6_2_PWMB	TMR6_2_PWMA		TMRA_5_PWM1/CLKA		TMRA_2_PWM1/CLKA	TMRA_4_PWM2/CLKB		TMR4_OVH	EMB_PORT2_IN5		TMR4_OWH	MCO_2	EVENTOUT	EVNTP204		FG1
57	41	28	PB5		EIRQ5+WKUP1_1			GPO						HRPWM_EEV6	USART1_CK	USART2_CK	PLAIN3	PLA2OUT	TMR6_4_PWMB	TMR6_4_PWMA				TMRA_2_PWM2/CLKB	TMRA_4_PWM3		TMR4_OWH	EMB_PORT2_IN4		TMR4_OXH	MCO_1	EVENTOUT	EVNTP205		FG1
58	42	29	PB6		EIRQ6+WKUP1_2			GPO				SPI_NSS2		HRPWM_EEV4			PLAIN4	HRPWM_TRIGB	TMR6_TRIGA		TMR6_TRIGC	TMRA_5_PWM2/CLKB	TMR6_TRIGD	TMRA_4_PWM1/CLKA	TMRA_4_PWM4		TMR4_OVL	CTCREF	CMP1_OUT	TMR4_OXL	ADTRG1	EVENTOUT	EVNTP206		FG1
59	43	-	PB7		EIRQ7+WKUP1_3			GPO					EMB_PORT1_IN1	HRPWM_EEV3			PLAIN5				TMR6_TRIGD	TMRA_5_PWM3		TMRA_4_PWM2/CLKB	TMRA_2_PWM4		TMR4_OWL	FCMREF	CMP2_OUT		ADTRG2	EVENTOUT	EVNTP207		FG1
60	44	31	PF3					GPO	ADTRG3				EMB_PORT1_IN2	HRPWM_EEV2			PLAIN7				TMR6_TRIGC	TMRA_4_TRIG	TMRA_3_TRIG	TMRA_2_TRIG	TMRA_1_TRIG		TMR4_OWH		CMP3_OUT			EVENTOUT			FG1
61	45	-	PB8	PVD2EXINP	EIRQ8			GPO				SPI_NSS3	EMB_PORT1_IN3	HRPWM_EEV8			PLAIN6	PLA3OUT			TMR6_TRIGB	TMRA_4_PWM1/CLKA	TMRA_5_PWM1/_CLKA	ADTRG1	TMRA_4_PWM3		TMR4_OVH	EMB_PORT2_IN1			FCMREF	EVENTOUT	EVNTP208		FG1
62	46	-	PB9		EIRQ9+WKUP2_1			GPO		CMP2_OUT	CMP1_OUT		EMB_PORT1_IN4	HRPWM_EEV5			PLAIN7		TMR6_1_PWMA	TMR6_1_PWMB		TMRA_5_PWM4	TMRA_5_PWM2/_CLKB	TMRA_4_TRIG	TMRA_4_PWM4		TMR4_OWH			TMR4_ADSM		EVENTOUT	EVNTP209		FG1
63	47	-	VSS																																
64	48	32	VCC																																

Note:

– *In the above table, Func32~57 are mainly serial communication functions (including USART, SPI, I2C, MCAN), which are a group of FunctionGroup, referred to as FG1.* Please refer to Table 22 *Table 2-2* for details.

Table 2-2 Func32~63 table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART1_RTS_DE	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS_DE	USART2_CTS	USART3_TX	USART3_RX	USART3_RTS_DE	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS_DE	USART4_CTS

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
FG1	SPI_NSS0	SPI_SCK	SPI_MOSI	SPI_MISO	I2C1_SDA	I2C1_SCL	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX	-	-	-	-	-	-

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	53
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortF	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	o	4	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	39
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortF	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	o	4	
QFN48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	39
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortF	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	o	4	
QFN32	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	27
	PortB	-	-	o	o	-	-	-	-	o	o	o	o	o	-	-	o	8	
	PortF	-	-	-	-	-	-	-	-	-	-	-	-	o	-	o	o	3	
-	-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-	-

Table 2-4 General Functional Specifications

Port		Pull-up / Pull-down	Open-Drain Output	Driving Capacity	5V Withstand Voltage
PortA	PA0~PA15	Support	Support	Low Medium High	Support
PortB	PB0~PB15	Support	Support	Low Medium High	Support
PortC	PC0~PC15	Support	Support	Low Medium High	Support
PortD	PD2	Support	Support	Low Medium High	Support
PortF	PF0~PF3	Support	Support	Low Medium High	Support

Note:

– *Input voltage must not be higher than AVCC/VREFH when used as an analog function.*

2.3 Pin Function Description

Table 2-5 Pin Function Description

Categories	Functional Name	I/O	Description
Power System	VCC	I	Power supply
	VSS	I	Source ground
	AVCC/ VREFH	I	Analog power supply/analog reference voltage
	AVSS/ VREFL	I	Analog power ground/analog reference voltage
	NRST	I	Reset terminal, low level valid
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External master clock oscillator interface
	XTAL_EXT/ XTAL_OUT	O	XTAL_EXT external clock input
	XTAL32_IN	I	External sub-clock (32KHz) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1~2)	O	Internal clock output
GPIO	GPIOxy (x=A~D, F y=0~15)	IO	General input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Shielded external interrupt
	WKUPx_y (x=0~3 y=0~3)	I	Power Down mode external wake-up input
Event Port	EVNTPxy (x=1~4 y=0~15)	IO	Event port input and output functions
JTAG/ SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECLK	O	Trace debug sync clock output
	TRACEDx (x=0~3)	O	Trace debug data output
FCM	FCMREF	I	External pin input reference clock for clock frequency measurement function
RTC	RTC_OUT	O	1Hz clock output
	RTC_CLK x (x=1~2)	I	External clock input
Timer4	TMR4_CLK	I	Counting clock port input
	TMR4_OUH	IO	PWM port U-phase output
	TMR4_OUL	IO	PWM port U-phase output
	TMR4_OVH	IO	PWM port V-phase output
	TMR4_OVL	IO	PWM port V-phase output
	TMR4_OWH	IO	PWM port W-phase output
	TMR4_OWL	IO	PWM port W-phase output
	TMR4_OXH	IO	PWM port X phase output

Categories	Functional Name	I/O	Description
Timer4	TMR4_OXL	IO	PWM port X phase output
	TMR4_ADSM	O	Dedicated event output monitoring
	TMR4_PCT	O	PWM cycle output monitoring
Timer6 (<t>=1~4)	TMR6_TRIGA	I	External event trigger A input
	TMR6_TRIGB	I	External event trigger B input
	TMR6_TRIGC	I	External event trigger C input
	TMR6_TRIGD	I	External event trigger D input
	TMR6_<t>_PWMA	IO	External Event Trigger Input or PWM Port Output
	TMR6_<t>_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA (<t>=1~5)	TMRA_<t>_TRIG	I	External event trigger input
	TMRA_<t>_PWM1/ CLKA	IO	External event trigger input or PWM port output or count clock port input
	TMRA_<t>_PWM2/ CLKB	IO	External event trigger input or PWM port output or count clock port input
	TMRA_<t>_PWMy (y=3~4)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_PORT1_INx (x=1~5)	I	Port input control signal
	EMB_PORT2_INx (x=1~5)	I	Port input control signal
HRPWM	HRWPM_x_PWMA (x=1~6)	O	PWM output port
	HRWPM_x_PWMB (x=1~6)	O	PWM output port
	HRPWM_TRIGx (x=A~D)	I	Hardware start, stop, clear, refresh condition synchronization input port
	HRPWM_EEVx (x=1~10)	I	External event input port
	HRPWM_SCOUT	O	Synchronous output port
USARTx (x=1~4)	USARTx_TX	IO	Send data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx_RTS	O	Request to send a signal
	USARTx_CTS	I	clear send signal
SPI	SPI_MISO	IO	Primary input/secondary output data transfer pin
	SPI_MOSI	IO	Primary output/slave input data transfer pin
	SPI_SCK	IO	Transmission clock
	SPI_NSS0	IO	Select input/output pin from machine
	SPI_NSSy (y=1~3)	O	Slave select output pin
I2C	I2C_SCL	IO	Clock line
	I2C_SDA	IO	Data line
MCANx (x=1~2)	MCANx_TX	O	Send data
	MCANx_RX	I	Receiving data
CMP	CMP1_OUT	O	CMP1 result output
	CMP2_OUT	O	CMP2 result output
	CMP3_OUT	O	CMP3 result output

Categories	Functional Name	I/O	Description
	CMPx_INPy (x=1~3 y=1~2)	I	CMPx positive analog input
	CMPx_INMy (x=1~3 y=1~2)	I	CMPx negative analog input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADTRG3	I	ADC3 AD conversion external start source
	ADC123_INx (x=6~9)	I	ADC1/2/3 share external analog input port
	ADC12_INx (x=4~5,10~15)	I	ADC1/2 share external analog input port
	ADC1_INx (x=0~3)	I	ADC1 external analog input port
	ADC3_INx (x=0~3,10,11)	I	ADC3 external analog input port
DAC	DAC_OUTy (y=1,2)	O	DAC analog output

2.4 Pin Instruction

Table 2-6 Pin Instruction

Pin Name	Usage Notes
VCC	Power supply, connect 1.8V~3.63V voltage, and connect a decoupling capacitor to the VSS pin nearby (refer to [Electrical Specifications])
VSS	Source ground, connected to 0V
AVCC	Analog power supply, power the analog module, connect to the same voltage as VCC (refer to [Electrical Specifications]) When not using the analog module, please short it with VCC
AVSS	Analog power ground, powering the analog module, connected to the same voltage as VSS (refer to [Electrical Specifications]) When not using the analog module, please short it with VSS
PF3/MD	Mode input. When the reset pin (NRST) is released (from low to low, the pin must be fixed at low level. Recommended resistance (4.7 KΩ) to VSS (Pull-down)
NRST	Reset pin, low level valid. Resistance to VCC when not in use (pull-up)
Pxy (x=A~D, F y=0~15)	General pin. When used as input function, the input voltage of the pin that supports 5V voltage tolerance should not exceed 5V. When the input voltage exceeds VCC, the internal pull-up/pull-down is prohibited. The input voltage of the pin that does not support 5V voltage tolerance should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Floating when not in use or connect to VCC (Pull-up)/VSS (Pull-down)

3 Electrical Specifications

3.1 Testing Conditions

All voltages are VSS-based unless otherwise specified.

3.1.1 Minimum and Maximum

Unless otherwise stated, the minimum and maximum values of all devices are obtained through comprehensive evaluation through sample testing under the worst-case ambient temperature, supply voltage and clock frequency conditions.

3.1.2 Typical Value

Unless otherwise specified, typical data are obtained through comprehensive evaluation of sample tests at TA=25°C, VCC=3.3V.

3.1.3 Typical Curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load Capacitance

Figure 3-1(Left) shows the load conditions used to measure the pin parameters.

3.1.5 Pin Input Voltage

Figure 3-1 (Right) shows how to measure the input voltage at the device pins.

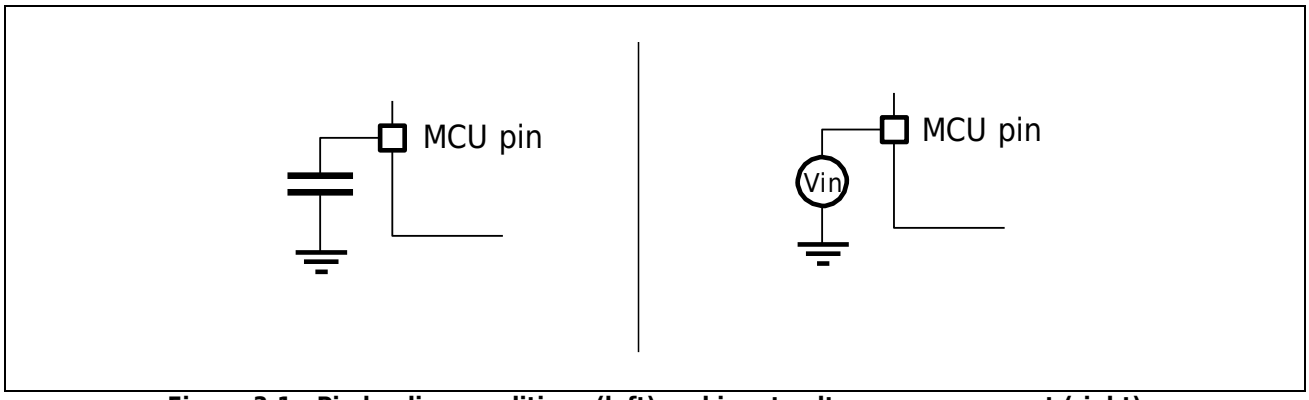


Figure 3-1 Pin loading conditions (left) and input voltage measurement (right)

3.1.6 Power Supply Scheme

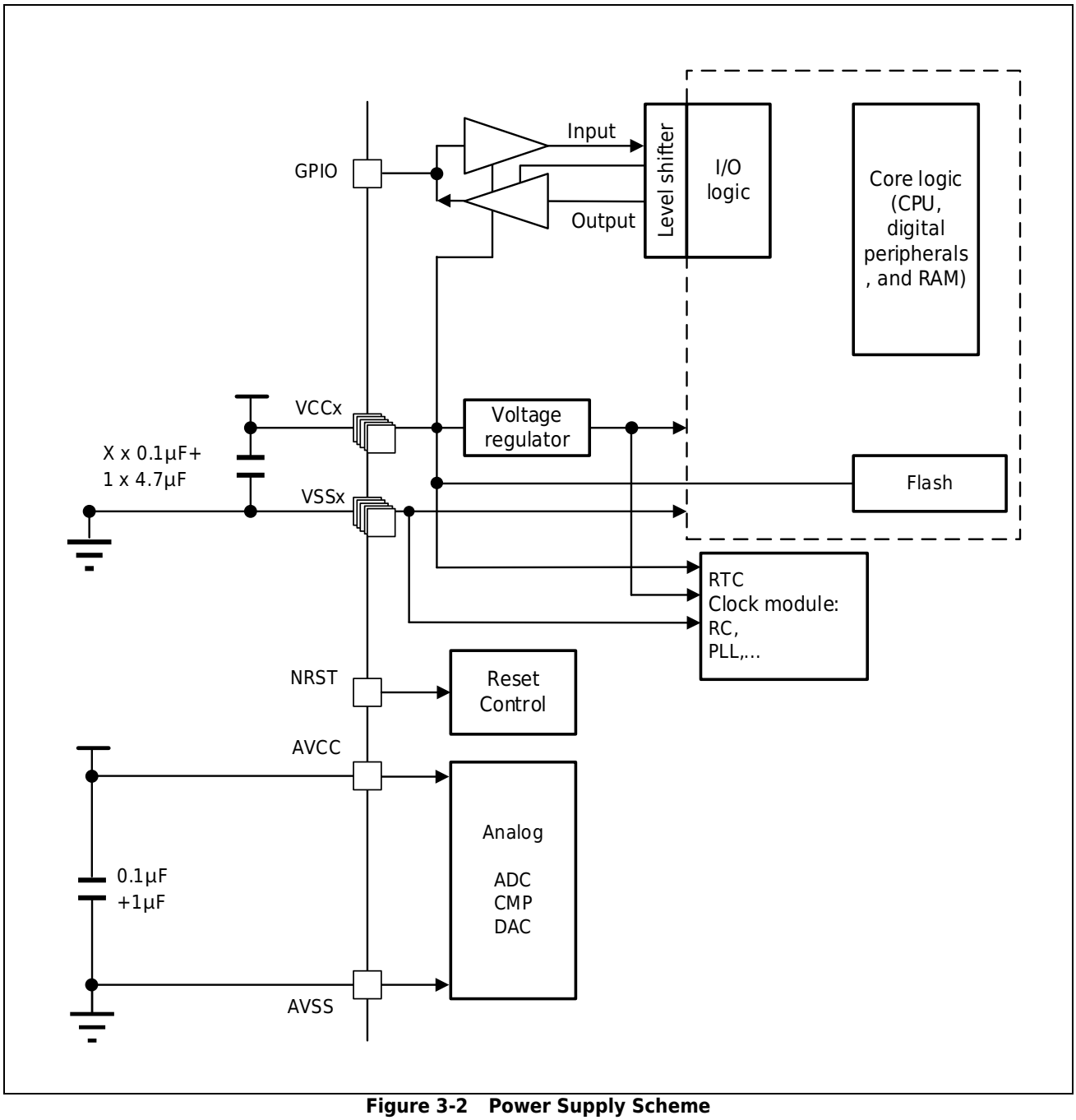


Figure 3-2 Power Supply Scheme

1. A 4.7µF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS.
3. These capacitors must be placed as close as possible to or underneath the power pair pins on the underside of the PCB to ensure proper operation of the device. These capacitors must be placed as close as possible to or underneath the power pair pins on the underside of the PCB to ensure proper operation of the device. Removing the filter capacitors to reduce PCB size or cost is not recommended and may cause the device to not operate properly.

3.1.7 Current Consumption Measurement

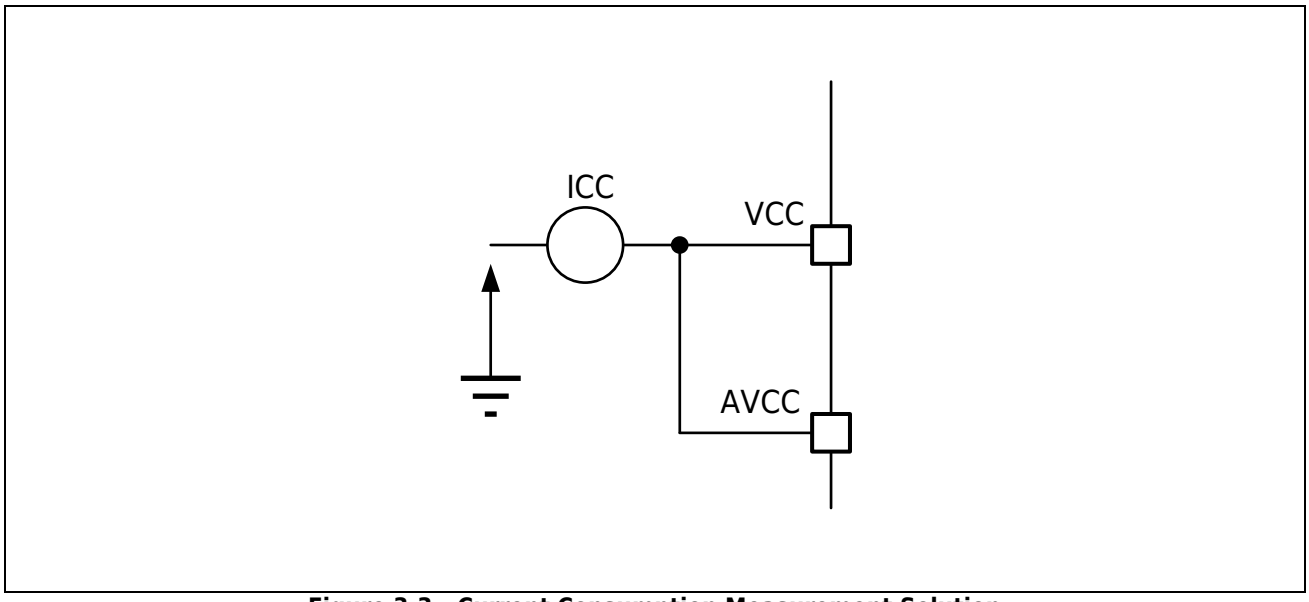


Figure 3-3 Current Consumption Measurement Solution

3.2 Absolute Maximum Ratings

Permanent damage to the device may result if loads exceeding the absolute maximum ratings listed in Table 3-1, Table 3-2 and Table 3-3 are applied to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability.

Table 3-1 Voltage Features

Symbol	Item	Minimum Value	Max	Unit
V_{CC}-V_{SS}	External main supply voltage (including AVCC, VCC) (1)	-0.3	4.0	V
V_{IN}	Input voltage on pin (2)	V_{SS}–0.3	V_{CC}+4.0 (Maximum 5.8V)	
|VSSx-VSS|	Voltage difference between different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage	Please refer to 'Electrical Sensitivity'		-

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. The maximum value of VIN must always be followed. For information on the maximum permissible current values, See Table 3-2.

Table 3-2 Current Characteristic

Symbol	Item	Max	Unit
∑IVCC	Total current flowing into all VCCX supply lines (source current) (1)	240	mA
∑IVSS	Total current flowing (sinking) out of all VSSX ground wires (1)	-240	
IVCC	Maximum current flowing into each VCCX power line (source current) (1)	100	
IVSS	Maximum current flowing out of each VSSX ground line (sink current) (1)	-100	
IIO	Output current sinking on any I/O and control pin	20	
	Output current sourced by any I/O and control pin	-20	
∑IIO	Total output sink current on all I/O and control pins (2)	120	
	Total output source current on all I/O and control pins (2)	-120	

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. This total output current must be correctly distributed across all power domains; this total output current applies to the 64 PINs package. For the 48 PINs package, the maximum total output current is ±80mA, and for the 32 PINs package, the maximum total output current is ±40mA.

Table 3-3 Thermal Features

Symbol	Item	Numerical Value	Unit
T_{STG}	Storage temperature range	–65~150	°C
T_J	Junction temperature range	-40~125	°C

3.3 Operating Conditions

3.3.1 General Working Conditions

Table 3-4 General Operating Conditions

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	120	MHz
V_{CC}	Standard operating voltage	-	1.8	-	3.63	V
V_{AVCC}	Analog working voltage	-	1.8	-	3.63	V
V_{IN}	Input voltage on 5V tolerant pin(2)(3)(4)	2V ≤ V_{CC} ≤ 3.63V 2V ≤ V_{AVCC} ≤ 3.63V	–0.3	-	5.5	
		V_{CC} < 2V V_{AVCC}< 2V	–0.3	-	5.2	
T_J	Junction temperature range	-	-40	-	125	°C
T_A	Working Temperature Range	-	-40	-	105	°C

1. Guarantee of mass production test.
2. To keep the voltage above VCC + 0.3V, the internal pull-up/pull-down resistors must be disabled.
3. It is necessary to ensure that the power supply (VCC, AVCC) of the device is stable before adding this voltage to the 5V withstand voltage pin of the device.
4. Direct connection of this input voltage to an external power supply is prohibited. It is recommended to connect the external power supply in series through a resistor of 100Ω or more.

3.3.2 Operating Conditions During Power Up/Down

Table 3-5 Operating Conditions in Case of Power-on/Power-off

Symbol	Parameter	Min	Max	Unit
t_{VCC}	VCC Rise Time Rate	20	20000	μs/V
	VCC Fall Time Rate	20	20000	

3.3.3 Reset and Power Control Block Features

Table 3-6 Reset and Power Control Block Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
V_{BOR}	Monitoring Voltage of BOR	ICG1.BOR_LEV[1:0]=0b00	1.70(1)	1.90	2.10	V
		ICG1.BOR_LEV [1:0]=0b01	1.80	2.00	2.20	V
		ICG1.BOR_LEV [1:0]=0b10	1.90	2.10	2.30	V
		ICG1.BOR_LEV [1:0]=0b11	2.10(1)	2.30	2.50	V
V_{PVD1}	PVD1 Monitoring Voltage (3)	PVD1LVL[2:0]=0b000	1.80	2.00	2.20	V
		PVD1LVL[2:0]=0b001	1.90	2.10	2.30	V
		PVD1LVL[2:0]=0b010	2.10	2.30	2.50	V
		PVD1LVL[2:0]=0b011	2.33	2.55	2.77	V
		PVD1LVL[2:0]=0b100	2.43	2.65	2.87	V
		PVD1LVL[2:0]=0b101	2.53	2.75	2.97	V
		PVD1LVL[2:0]=0b110	2.63	2.85	3.07	V
		PVD1LVL[2:0]=0b111	2.73	2.95	3.17	V
V_{PVD2}	PVD2 Monitoring Voltage (3)	PVD2LVL[2:0]=0b000	1.90	2.10	2.30	V
		PVD2LVL[2:0]=0b001	2.10	2.30	2.50	V
		PVD2LVL[2:0]=0b010	2.33	2.55	2.77	V
		PVD2LVL[2:0]=0b011	2.43	2.65	2.87	V
		PVD2LVL[2:0]=0b100	2.53	2.75	2.97	V
		PVD2LVL[2:0]=0b101	2.63	2.85	3.07	V
		PVD2LVL[2:0]=0b110 (1)	2.73	2.95	3.17	V
		PVD2LVL[2:0]=0b111(1)(5)	0.90	1.10	1.30	V
V_{pvd}hyst	Hysteresis of PVD1,2 (4)	-	-	100	-	mV
V_{POR}	Power-on/power-off reset threshold (1)	Rising edge VPOR	1.56	1.68	1.80	V
		Falling edge VPDR	1.52	1.64	1.76	V
V_{POR}hyst	POR Hysteresis	-	-	40	-	mV
I_{RUSH}	Surge current when the voltage regulator is powered on (POR or awakens from standby)	-	-	100	150	mA
T_{NRST}	NRST reset minimum width	-	10	-	-	μs
T_{IPVD1}	PVD1 reset release time (2)	-	300	380	460	μs
T_{IPVD2}	PVD2 reset release time (2)	-	300	380	460	μs
T_{INRST}	NRST reset release time (2)	-	25	35	50	μs
T_{RIPT}	NRST reset release time (2)	-	140	160	200	μs
T_{RSTBOR}	BOR reset release time (2)	-	440	520	610	μs
T_{RSTPOR}	Power-on reset release time (2)	-	-	2500	3000	μs

1. Guarantee of mass production test.
2. Design guaranteed.

3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL[2:0] is set to 0b111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops; when PVD2LVD[2:0] is set to a value other than 0b111, the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1/2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.
   PVD1 monitors voltage when VCC rises=V_{pvd1}+V_{pvd}hyst.
   PVD2 monitors voltage when VCC rises=V_{pvd2}+V_{pvd}hyst.
5. When PVD2LVDL[2:0]=0b111, the comparison voltage is the external input comparison voltage of the PVD2EXINP pin.

3.3.4 Supply Current Features

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

The method for measuring the current consumption is described in Figure 3-3. The current consumption measurements in the various modes described in this section are obtained under laboratory conditions using a set of test codes running in FLASH.

The specific conditions are as follows:

1) All I/O pins are in high-impedance mode (no load).
2) Clock frequency selection f_{HCLK}=120MHz/ 60MHz/ 24MHz/ 8MHz/ 1MHz.
3) The power consumption modes are divided into: normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power-down mode ICC_PD, and Dhrystone working mode ICC_DHRYSTONE.
4) Please refer to the specific current condition description for peripheral clock ON/OFF.
5) The PLL is turned on in high-speed mode f_{HCLK}=120MHz/ 60MHz.

Table 3-7 Run Mode Current Consumption1

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Classic Value(1)	Max (2)	
Operating mode	f_{HCLK}= 120MHz	ICC_RUN	while(1), all modules clock OFF(3)	-40	-	14.0	-	mA
			while(1), all modules clock ON(3)	-40	-	25.0	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	14.0	-	mA
			CACHE ON	-40	-	14.0	-	mA
		ICC_SLEEP	All modules clocks OFF(3)	-40	-	9.0	-	mA
			All modules clocks ON(3)	-40	-	20.0	-	mA
		ICC_RUN	while(1), all modules clock OFF(3)	25	-	14.0	-	mA
			while(1), all modules clock ON(3)	25	-	25.0	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	14.0	-	mA
			CACHE ON	25	-	14.0	-	mA
		ICC_SLEEP	All modules clocks OFF(3)	25	-	9.0	-	mA
			All modules clocks ON(3)	25	-	20.0	-	mA
		ICC_RUN	while(1), all modules clock OFF(3)	85	-	-	18.0	mA
			while(1), all modules clock ON(3)	85	-	-	30.0	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	17.5	mA
			CACHE ON	85	-	-	18.0	mA
		ICC_SLEEP	All modules clock OFF	85	-	-	13.0	mA
			All modules clock ON	85	-	-	25.0	mA
		ICC_RUN	while(1), all modules clock OFF(3)	105	-	-	23.0	mA
			while(1), all modules clock ON(3)	105	-	-	36.0	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	23.6	mA
			CACHE ON	105	-	-	24.0	mA
		ICC_SLEEP	All modules clocks OFF(3)	105	-	-	17.5	mA
			All modules clocks ON(3)	105	-	-	30.5	mA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.
3. Guarantee of mass production test.

Table 3-8 Run Mode Current Consumption 2

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Classic Value(1)	Max (2)	
Operating mode	f_{HCLK}= 60MHz	ICC_RUN	while(1) all modules clocks are OFF	-40	-	9.0	-	mA
			While (1), all modules clock ON	-40	-	15.0	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	9.0	-	mA
			CACHE ON	-40	-	9.0	-	mA
		ICC_SLEEP	All modules clock OFF	-40	-	6.0	-	mA
			All modules clock ON	-40	-	12.0	-	mA
		ICC_RUN	While (1), all modules clock OFF	25	-	9.0	-	mA
			While (1), all modules clock ON	25	-	15.0	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	9.0	-	mA
			CACHE ON	25	-	9.0	-	mA
		ICC_SLEEP	All modules clock OFF	25	-	6.0	-	mA
			All modules clock ON	25	-	12.0	-	mA
		ICC_RUN	While (1), all modules clock OFF	85	-	-	12.0	mA
			While (1), all modules clock ON	85	-	-	19.0	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	12.1	mA
			CACHE ON	85	-	-	12.3	mA
		ICC_SLEEP	All modules clock OFF	85	-	-	10.0	mA
			All modules clock ON	85	-	-	16.5	mA
		ICC_RUN	While (1), all modules clock OFF	105	-	-	17.0	mA
			While (1), all modules clock ON	105	-	-	24.5	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	17.6	mA
			CACHE ON	105	-	-	17.8	mA
		ICC_SLEEP	All modules clock OFF	105	-	-	14.0	mA
			All modules clock ON	105	-	-	21.5	mA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.

Table 3-9 Run Mode Current Consumption 3

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Classic Value(1)	Max (2)	
Operating mode	f_{HCLK}= 24MHz	ICC_RUN	While (1), all modules clock OFF	-40	-	4.5	-	mA
			While (1), all modules clock ON	-40	-	8.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	4.6	-	mA
		ICC_SLEEP	All modules clock OFF	-40	-	3.5	-	mA
			All modules clock ON	-40	-	7.5	-	mA
		ICC_RUN	While (1), all modules clock OFF	25	-	4.5	-	mA
			While (1), all modules clock ON	25	-	8.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	4.6	-	mA
		ICC_SLEEP	All modules clock OFF	25	-	3.5	-	mA
			All modules clock ON	25	-	7.5	-	mA
		ICC_RUN	While (1), all modules clock OFF	85	-	-	9.0	mA
			While (1), all modules clock ON	85	-	-	12.0	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	9.0	mA
		ICC_SLEEP	All modules clock OFF	85	-	-	7.5	mA
			All modules clock ON	85	-	-	11.1	mA
		ICC_RUN	While (1), all modules clock OFF	105	-	-	14.0	mA
			While (1), all modules clock ON	105	-	-	18.0	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	15.0	mA
		ICC_SLEEP	All modules clock OFF	105	-	-	12.5	mA
			All modules clock ON	105	-	-	17.0	mA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.

Table 3-10 Running Speed Mode Current Consumption 4

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typical Value (1)	Max (2)	
Operating mode	f_{HCLK}= 8MHz	ICC_RUN	While (1), all modules clock OFF	-40	-	3.2	-	mA
			While (1), all modules clock ON	-40	-	5.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3.3	-	mA
		ICC_SLEEP	All modules clock OFF	-40	-	2.8	-	mA
			All modules clock ON	-40	-	5.0	-	mA
		ICC_RUN	While (1), all modules clock OFF	25	-	3.3	-	mA
			While (1), all modules clock ON	25	-	5.0	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3.3	-	mA
		ICC_SLEEP	All modules clock OFF	25	-	2.8	-	mA
			All modules clock ON	25	-	4.6	-	mA
		ICC_RUN	While (1), all modules clock OFF	85	-	-	7.1	mA
			While (1), all modules clock ON	85	-	-	8.2	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	7.5	mA
		ICC_SLEEP	All modules clock OFF	85	-	-	6.5	mA
			All modules clock ON	85	-	-	7.8	mA
		ICC_RUN	While (1), all modules clock OFF	105	-	-	12.2	mA
			While (1), all modules clock ON	105	-	-	13.8	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	13.0	mA
		ICC_SLEEP	All modules clock OFF	105	-	-	11.4	mA
			All modules clock ON	105	-	-	13.3	mA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.

Table 3-11 Run Mode Current Consumption5

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typical Value (1)	Max(2)	
Operating mode	f_{HCLK}= 1MHz	ICC_RUN	While (1), all modules clock OFF	-40	-	2.7	-	mA
			While (1), all modules clock ON	-40	-	4.9	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	2.7	-	mA
		ICC_SLEEP	All modules clock OFF	-40	-	2.5	-	mA
			All modules clock ON	-40	-	4.0	-	mA
		ICC_RUN	While (1), all modules clock OFF	25	-	2.7	-	mA
			While (1), all modules clock ON	25	-	3.6	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	2.7	-	mA
		ICC_SLEEP	All modules clock OFF	25	-	2.5	-	mA
			All modules clock ON	25	-	3.3	-	mA
		ICC_RUN	While (1), all modules clock OFF	85	-	-	6.4	mA
			While (1), all modules clock ON	85	-	-	6.6	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	6.5	mA
		ICC_SLEEP	All modules clock OFF	85	-	-	6.1	mA
			All modules clock ON	85	-	-	6.5	mA
		ICC_RUN	While (1), all modules clock OFF	105	-	-	11.5	mA
			While (1), all modules clock ON	105	-	-	12.1	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	12.1	mA
		ICC_SLEEP	All modules clock OFF	105	-	-	11.0	mA
			All modules clock ON	105	-	-	12.0	mA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.

Table 3-12 Low Power Mode Current Consumption

Mode	Parameter	Symbol	Condition (VCC = 3.3 V)	Ta(°C)	Product Specifications			Unit
					Min	Typical Value(1)	Max(2)	
Stop mode	-	ICC_STP	Stop mode	-40	-	46	-	μA
				25	-	71	-	μA
				85	-	-	2.5	mA
				105	-	-	5.2	mA
Power Down Mode	-	ICC_PD	Power down mode 1	-40	-	9.0	-	μA
			Power down mode 2	-40	-	4.0	-	μA
			Power down mode 3	-40	-	2.0	-	μA
			Power down mode 4	-40	-	2.0	-	μA
			Power down mode 2+XTAL32+RTC	-40	-	6.0	-	μA
			Power down mode 2+LRC+RTC	-40	-	9.0	-	μA
			Power down mode 1	25	-	10.0	-	μA
			Power down mode 2	25	-	4.0	-	μA
			Power down mode 3	25	-	2.0	-	μA
			Power down mode 4	25	-	2.0	-	μA
			Power down mode 2+XTAL32+RTC	25	-	7.0	-	μA
			Power down mode 2+LRC+RTC	25	-	10.0	-	μA
			Power down mode 1	85	-	-	17.0	μA
			Power down mode 2	85	-	-	9.0	μA
			Power down mode 3	85	-	-	6.0	μA
			Power down mode 4	85	-	-	6.0	μA
			Power down mode 2+XTAL32+RTC	85	-	-	16.0	μA
			Power down mode 2+LRC+RTC	85	-	-	21.0	μA
			Power down mode 1	105	-	-	30.0	μA
			Power down mode 2	105	-	-	22.0	μA
			Power down mode 3	105	-	-	19.0	μA
			Power down mode 4[3]	105	-	-	19.0	μA
			Power down mode 2+XTAL32+RTC	105	-	-	44.0	μA
			Power down mode 2+LRC+RTC	105	-	-	49.0	μA

1. Typical voltage condition VCC=3.3V.
2. Maximum voltage condition VCC=1.8~3.63V.
3. Guarantee of mass production test.

Table 3-13 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)		T_A(°C)	Product Specifications			Unit
						Min	Typical Value	Max	
Module current	-	ICC_MODULE	XTAL oscillator mode high drive 24MHz		25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode		25	-	1.0	-	mA
			Oscillator mode low drive 10MHz		25	-	0.8	-	mA
			Oscillator mode ultra low drive 8MHz		25	-	0.6	-	mA
			XTAL 32.768KHz		25	-	1.1	-	μA
			HRC		25	-	0.3	-	mA
			PLLH (VCO=480MHz)		25	-	3.5	-	mA
			PLLH (VCO=240MHz)		25	-	1.8	-	mA
			ADC		25	-	1.3	-	mA
			DAC	Amplifier allowed	25	-	0.8	-	mA
				Amplifier Disable	25	-	0.2	-	mA
			CMP		25	-	0.3	-	mA

3.3.5 Low Power Mode Wake-up Timing

The wake-up time measurement method is from the wake-up event triggering to the CPU execution of the first instruction:

- For stop or sleep mode: Wakeup event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All the timings are measured at ambient temperature and VCC=3.3V.

Table 3-14 Low Power Mode Wake Up Time

Symbol	Parameter	Conditions	Typical Value	Max	Unit
T_{STOP}	Wakeup from stop mode	System clock is MRC	20.4	35	μs
T_{PD1}	Wake up from power-down mode 1	-	70	76	
T_{PD2}	Wake up from power-down mode 2	-	125	135	
T_{PD3}	Wake up from power-down mode 3	-	2140	2397	
T_{PD4}	Wake up from power-down mode 4	-	181	194	

3.3.6 External Timer Characteristic

3.3.6.1 High-speed External Subscriber Clock Generated by External Source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/O. The external clock signal must take into account the requirements for external input clock Features in Table3-15.

Table 3-15 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
f_{XTAL_EXT}	User external clock frequency	-	1	-	25(1)	MHz
V_{IH_XTAL}	XTAL_EXT input pin high level voltage		0.8×V_{CC}	-	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low level voltage		V_{SS}	-	0.2×V_{CC}	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_EXT rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	Duty Ratio	-	40	-	60	%

1. Guarantee of mass production test.

3.3.6.2 High-speed External Clock Generated by Crystal/Ceramic Resonator

High-speed external (XTAL) clocks can be produced using a 4 to 25 MHz crystal oscillator/ceramic resonator oscillator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator Features (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-16 XTAL 4-25 MHz Oscillator Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
f_{XTAL_IN}	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback Resistance(1)	-	-	300	-	kΩ
A_{XTAL}	XTAL Accuracy(2)(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm(2)	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$	Start time (4)	VCC is stable, crystal oscillator=8MHz	-	2.0	-	ms
		VCC is stable, crystal oscillator=4MHz	-	4.0	-	ms

1. Guarantee of mass production test.
2. Design guaranteed.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the start-up time, which is measured from the time XTAL is enabled by software until a stable oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications that meet crystal or resonator requirements (see figure below). C_{L1} and C_{L2} are usually the same size, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the sum of parasitic capacitance between PCB and MCU pins (XTAL_IN, XTAL_OUT). C_L is the load capacitance of the crystal or ceramic resonator. Please consult the crystal resonator manufacturer.

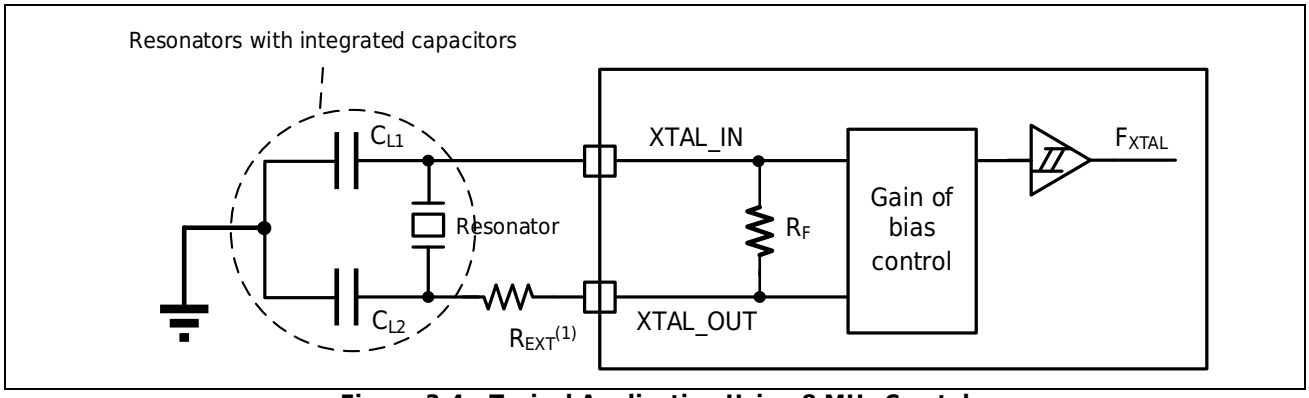


Figure 3-4 Typical Application Using 8 MHz Crystal

1. The value of REXT depends on the crystal oscillator Features.

3.3.6.3 Low-speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

Low-speed external clocks can be produced using an oscillator composed of 32.768KHz crystal oscillator/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator Features (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-17 XTAL32 Oscillator Features

Symbol	Parameter	Conditions	Specifications			Unit
			Min	Typical Value	Max	
F_{XTAL32}	Frequency	-	-	32.768	-	KHz
R_F	Feedback Resistance(1)	-	-	15	-	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=0b000	-	0.8	-	μA
A_{XTAL32}	XTAL32 precision(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm(2)	XTAL32DRV[2:0]=0b000	5.6	-	-	μA/V
$T_{SUXTAL32}$	Start time (4)	VCC Stabilization	-	2	-	s

1. Mass production test guarantee.
2. Design guaranteed.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the start-up time, which is measured from the time when the software enables XTAL32 until a stable 32.768KHz oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, high quality external ceramic capacitors are recommended (see figure below). C_{L1} and C_{L2} are usually the same size, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the sum of parasitic capacitance between PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} or C_{L2} are greater than 18 pF, it is recommended to set XTAL32DRV[2:0]=0b001 (high drive, the typical value of power consumption increases by 0.2μA). C_L is the load capacitance of the crystal or ceramic resonator. Please consult the crystal resonator manufacturer.

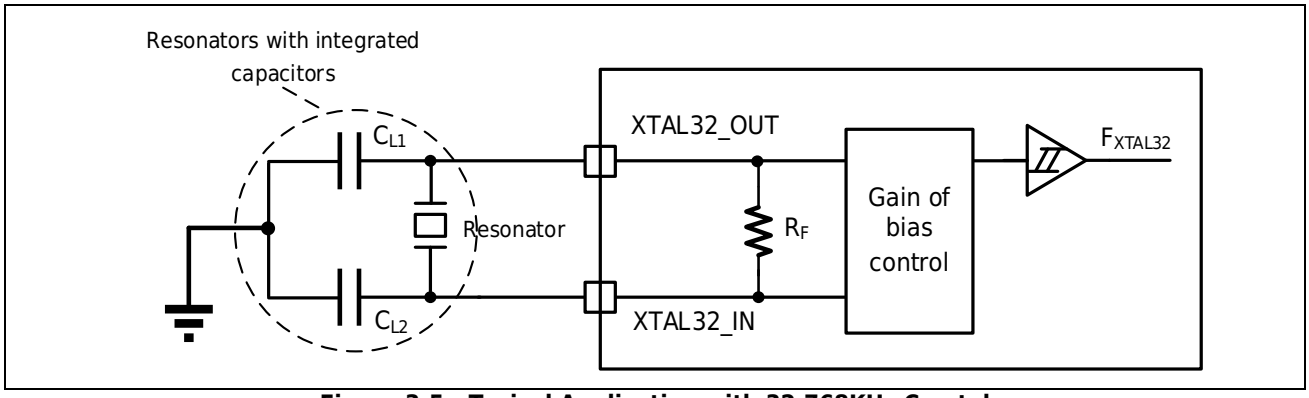


Figure 3-5 Typical Application with 32.768KHz Crystal

3.3.7 Internal Timer Features

3.3.7.1 Internal High Speed (HRC) Oscillator

Table 3-18 HRC Oscillator Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
f_{HRC}	Frequency(1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User Adjustment Scale	-	-	-	0.2	%
	Frequency accuracy	T_A = -40 to 105℃(1)	-2	-	2	%
		T_A = 25℃(1)	-1.5	-	1.5	%
$t_{st(HRC)}$	HRC oscillator oscillation stabilization time(1)	-	-	-	15	μs

1. Guarantee of mass production test.

3.3.7.2 Internal Medium Speed (MRC) Oscillator

Table 3-19 MRC Oscillator Features

Symbol	Parameter	Min	Typical Value	Max	Unit
f_{MRC}	Frequency(1)	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time(1)	-	-	3	μs

1. Guarantee of mass production test.

3.3.7.3 Internal Low Speed (LRC) Oscillator

Table 3-20 LRC Oscillator Features

Symbol	Parameter	Min	Typical Value	Max	Unit
f_{LRC}	Frequency(1)	27.853	32.768	37.683	KHz
$t_{st(LRC)}$	LRC oscillator stabilization time(1)	-	-	36	μs

1. Guarantee of mass production test.

3.3.7.4 SWDT Dedicated Internal Low-speed (SWDTLRC) Oscillator

Table 3-21 SWDTLRC Oscillator Features

Symbol	Parameter	Min	Typical Value	Max	Unit
$f_{SWDTLRC}$	Frequency(1)	9	10	11	KHz
$t_{st(SWDTLRC)}$	SWDTLRC oscillator stabilization time(1)	-	-	57.1	μs

1. Guarantee of mass production test.

3.3.8 PLL Characteristic

Table 3-22 PLLH Main Performance Indicators

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
f_{PLL_IN}	Input Clock of PLL Phase Frequency Detector (PFD)(1)(2)	-	1	-	25	MHz
f_{PLL_OUT}	Output Clock of PLL Multiplier	-	15	-	120	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output(1)	-	240	-	480	MHz
t_{LOCK}	PLL lock time	-	-	80	120	μs
$Jitter_{PLL}$	Periodic Jitter	PLL PFD input clock is 8MHz, system clock is 120MHz, peak to peak	-	±100	-	ps
	Cycle-to-cycle jitter	PLL PFD input clock is 8MHz, system clock is 120MHz, peak to peak-	-	±150	-	

1. Guarantee of mass production test.
2. A higher input clock is recommended to obtain good jitter Features.

3.3.9 Memory (Flash) Features

Flash memory was erased when the device was delivered to the customer.

Table 3-23 Flash Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
I_{VCC}	Power supply current(1)	Read mode, V_{CC}=1.8 V~3.63V	-	-	5	mA
		Programming mode, V_{CC}=1.8 V~3.63V	-	-	10	
		Block erase mode, V_{CC}=1.8 V~3.63V	-	-	10	
		Full erase mode, V_{CC}=1.8 V~3.63V	-	-	10	

1. Design guaranteed.

Table 3-24 Flash Program Erase Time

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
T_{prog}	Word programming time(1)	Single programming mode	$43+2\times T_{hclk}$(2)	$48+4\times T_{hclk}$(2)	$53+6\times T_{hclk}$(2)	μs
	Word programming time(1)	Continuous programming mode	$12+2\times T_{hclk}$(2)	$14+4\times T_{hclk}$(2)	$16+6\times T_{hclk}$(2)	μs
T_{erase}	Block erase time(1)	-	$16+2\times T_{hclk}$(2)	$18+4\times T_{hclk}$(2)	$20+6\times T_{hclk}$(2)	ms
T_{mas}	Full erase time(1)	-	$16+2\times T_{hclk}$(2)	$18+4\times T_{hclk}$(2)	$20+6\times T_{hclk}$(2)	ms

1. Guarantee of mass production test.
2. T_{hclk} is one cycle of CPU clock.

Table 3-25 Flash Memory Erasability and Data Retention Period

Symbol	Parameter	Conditions	Numerical Value	Unit
			Min	
N_{end}	Programming, block erase times, full erase times	T_A = 85℃	10	Thousands of times
T_{ret}	Data retention period	T_A = 85℃, after 10 kcycles	10	Year

3.3.10 Electrical Sensitivity

The chip is tested differently (ESD, LU) using specific measurement methods to determine its performance in terms of electrical susceptibility.

3.3.10.1 Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with JS001 and JS002 standards.

Table 3-26 ESD Features

Symbol	Parameter	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage	T_A =+25°C, meet JS001 standard	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A =+25°C, meet JS002 standard	1000	

3.3.10.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output, and configurable I/O pins

These tests met the EIA/JESD 78A IC Latch-up standard.

Table 3-27 Static Latch-up Features

Symbol	Parameter	Conditions	Max	Unit
LU	Static Latch-up	T_A =+105°C compliant with JESD78A	200	mA

3.3.11 I/O Port Features

General Input/Output Features

Table 3-28 I/O Static Features

Symbol	Parameter		Conditions	Min	Typical Value	Max	Unit
V_{IL}	Schmitt input low level(1)		1.8≤V_{CC}≤3.63	-	-	0.3V_{CC}	V
V_{IH}	Schmitt input high level(1)		1.8≤V_{CC}≤3.63	0.7V_{CC}	-	-	V
V_{HYS}	Schmitt input hysteresis		1.8≤V_{CC}≤3.63	0.1	0.2	-	V
V_{IL}	CMOS Input low level(1)		1.8≤V_{CC}≤3.63	-	-	0.3V_{CC}	V
V_{IH}	CMOS input high level(1)		1.8≤V_{CC}≤3.63	0.7V_{CC}	-	-	V
TTL_V_{IL}	CMOS/ Schmitt compatible TTL input low level(1)		2.7≤V_{CC}≤3.63	-	-	0.8	V
TTL_V_{IH}	CMOS/ Schmitt compatible TTL input high level(1)		2.7≤V_{CC}≤3.63	2.2	-	-	V
$F_{max(in)}$	Schmitt input maximum frequency		2.7≤V_{CC}≤3.63	-	-	40	MHz
			1.8≤V_{CC}≤2.7	-	-	20	MHz
	CMOS input maximum frequency		2.7≤V_{CC}≤3.63	-	-	80	MHz
			1.8≤V_{CC}≤2.7	-	-	40	MHz
I_{LKG}	I/O input leakage current(1)		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN} = 5.5V(2)	-	-	10	μA
R_{PU}	Weak pull-up Equivalant resistance(1)(3)		V_{IN} = V_{SS} 1.8≤V_{CC}≤3.63	10	30	150	KΩ
R_{PD}	Weak pull-down Equivalant resistance(1)(3)		V_{IN} = V_{cc} 1.8≤V_{CC}≤3.63	5	20	50	KΩ
C_{IO}	I/O Pin Capacitance(2)	PB6, PB7 (I2C) PF3/MD	-	-	10	-	pF
		Input pins other than those mentioned above	-	-	5	-	pF

1. Guarantee of mass production test.
2. Design guaranteed.
3. To keep the voltage above VCC + 0.3V, the internal pull-up/pull-down resistors must be disabled.

Output Current

The GPIO (General Purpose Input/Output) can source or sink current up to ±20mA.

The output voltage

Table 3-29 Output Voltage Features

Driver Settings	Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
Low drive	V_{OL}	Low level output(1)(2)	I_{IO}=±1.5mA, 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±3mA, 2.7≤V_{CC}≤3.63	-	-	0.6	
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±6mA, 2.7≤V_{CC}≤3.63	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
Medium drive	V_{OL}	Low level output(1)(2)	I_{IO}=±3mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±5mA, 2.7≤V_{CC}≤3.63	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±12mA, 2.7≤V_{CC}≤3.63	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
High drive	V_{OL}	Low level output(1)(2)	I_{IO}=±6mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±8mA, 2.7≤V_{CC}≤3.63	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20mA, 2.7≤V_{CC}≤3.63	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20mA, 2.97≤V_{CC}≤3.63	-	-	0.88	
	V_{OH}	High level output(1)(3)		V_{CC}-0.88	-	-	
IIC/ FM+	VOLFM+	Low level output(1)(2)	I_{IO}=20 mA, 2.7≤V_{CC}≤3.63	-	-	0.4	V

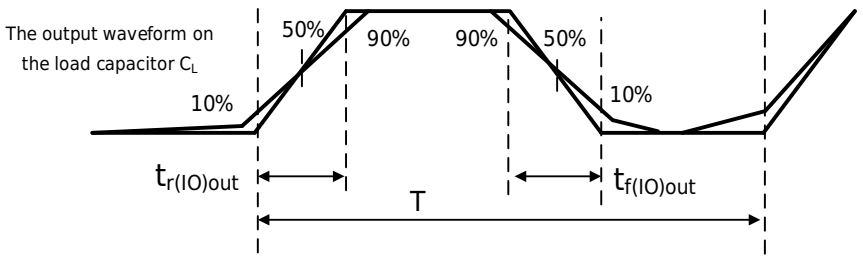
1. Guarantee of mass production test.
2. The I_{IO} current sunk by the device must always consider the absolute maximum ratings specified in Table 3-2. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} source current of the device must always adhere to the absolute maximum ratings listed in Table 3-2, and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Input/output AC Features

Table 3-30 I/O AC Features

Driver Settings	Symbol	Parameter	Condition(3)	Min	Typical Value	Max	Unit
Low drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	40	
			C_L=10pF, V_{CC}≥1.8V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	15	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	25	
			C_L=10pF, V_{CC}≥2.7V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	15	
medium drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	45	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7V	-	-	90	
			C_L=10pF, V_{CC}≥1.8V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	6	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	4	
			C_L=10pF, V_{CC}≥1.8V	-	-	6	
High drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	100	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	50	
			C_L=10pF, V_{CC}≥1.8V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	4	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	6	
			C_L=10pF, V_{CC}≥2.7V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	3.5	

1. The maximum frequency is defined in Figure 3-6.
2. The load capacitance CL must take into account the capacitance of the PCB and MCU pins (the capacitance between the I2C pins PB6, PB7 and the MD pin PF3 and the circuit board can be roughly estimated as 15pF; the capacitance between other pins and the circuit board can be roughly estimated as 10pF).



Maximum frequency condition: (tr+tf)≤(2/3)T and Duty cycle=50%±5% (Load capacitance C_L is indicated in the "Conditions" column of the "Input/Output AC Features" table)

Figure 3-6 I/O AC Features Definition

3.3.12 HRPWM Features

Table 3-31 HRPWM Features

Symbol	Parameter	Min	Typical Value	Max	Unit
f_{PCLK0}	HRPWM calibration clock input	-	120	-	MHz
		-	8.33	-	ns
Tres(HRPWM)	Timer resolution time	-	130	-	ps
Res_{HRPWM}	Timer resolution	-	22	-	bit

Table 3-32 HRPWM EMB Response Time

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
$T_{LAT\ (DEMB)}$	Digital EMB response time	Delay from EMB_PORT1_INx input to HRPWM_<t>_PWMA/B output port	-	15	25	ns
$T_{W\ (EMB)}$	Minimum EMB pulse width	-	12.5	-	-	ns
$T_{LAT\ (AEMB)}$	Analog EMB response time	-	-	30	50	ns

Table 3-33 HRPWM External Events 1~5 Response Time (2) (Fast Asynchronous Mode)

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
$T_{LAT(DEEV)}$	Digital external event response time	Delay from HRPWMEEVy input to HRPWM_<t>_PWMA/B output port (30pF load)	-	15	25	ns
$T_{W(EEV)}$	Minimum external event pulse width	-	12.5	-	-	ns
$T_{LAT(AEEV)}$	Analog external event response time	Delay from CMPy_INPz input to HRPWM_<t>_PWMA/B output port (30pF load)	-	30	50	ns
$T_{JIT\ (EEV)}$	External event response jitter	Jitter from HRPWM_EEVy input to HRPWM_<t>_PWMA/B output port	-	-	0	t_{PCLK0}(1)

1. $t_{PCLK0} = 1/f_{PCLK0}$.
2. The fast asynchronous mode is set by the HRPWM_EECR1.EEyFAST register bit and only supports external events 1~5.

Table 3-34 HRPWM External Events 1~5 Response Time (Synchronous Mode)

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
$T_{LAT(DEEV)}$	Digital external event response time	Delay from HRPWMEEVy input to HRPWM_<t>_PWMA/B output port (30pF load)	-	60	70	ns
$T_{W(EEV)}$	Minimum external event pulse width	-	12.5	-	-	ns
$T_{LAT(AEEV)}$	Analog external event response time	Delay from CMPy_INPz input to HRPWM_<t>_PWMA/B output port (30pF load)	-	75	85	ns
$T_{JIT\ (EEV)}$	External event response jitter	Jitter from HRPWM_EEVy input to HRPWM_<t>_PWMA/B output port	-	-	1	t_{PCLK0}

Table 3-35 HRPWM Synchronous Input and Output Features

Symbol	Parameter	Min	Typical Value	Max	Unit
$T_{w(TRGA-D)}$	Synchronous input signal HRPWM_TRGA~D Minimum pulse width	2	-	-	t_{PCLK0}
$T_{RES(TRGA-D)}$	Synchronous request response time	-	-	4	t_{PCLK0}
$T_{w(SYNCOUT)}$	Synchronous output signal HRPWM_SYNCOUT Minimum pulse width	16	-	65535	t_{PCLK0}

3.3.13 I2C Interface Features

Table 3-36 I2C Electrical Features

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Fast Mode Plus (FM+)(3)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	0.26	-	μs
t_{LOW}	SCL Low Level	4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	SCL High Level	4	-	0.6	-	0.26	-	μs
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	0.26	-	μs
$t_{HD;DAT}$	Data Hold(1)	0	-	0	-	0	-	μs
$t_{SU;DAT}$	Data setup(1)	30+ $t_{I2C\ reference\ clock\ period}$(2)	-	30+ $t_{I2C\ reference\ clock\ period}$(2)	-	30+ $t_{I2C\ reference\ clock\ period}$(2)	-	ns
t_R	Rising time of SCL/SDA	-	1000	-	300	-	120	ns
t_F	Falling time of SCL/SDA	-	300	-	300	-	120	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	0.26	-	μs
t_{BUF}	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	0.5	-	μs
C_b	Load Capacitance	-	400	-	400	-	550	pF

1. Guarantee of mass production test.
2. $t_{I2C\ reference\ clock\ period}$ is the I2C reference clock period, which is set by the I2C_CCR.CKDIV[2:0] bits.
3. In FM+ mode, the I2C function needs to be configured on ports PB6 and PB7.

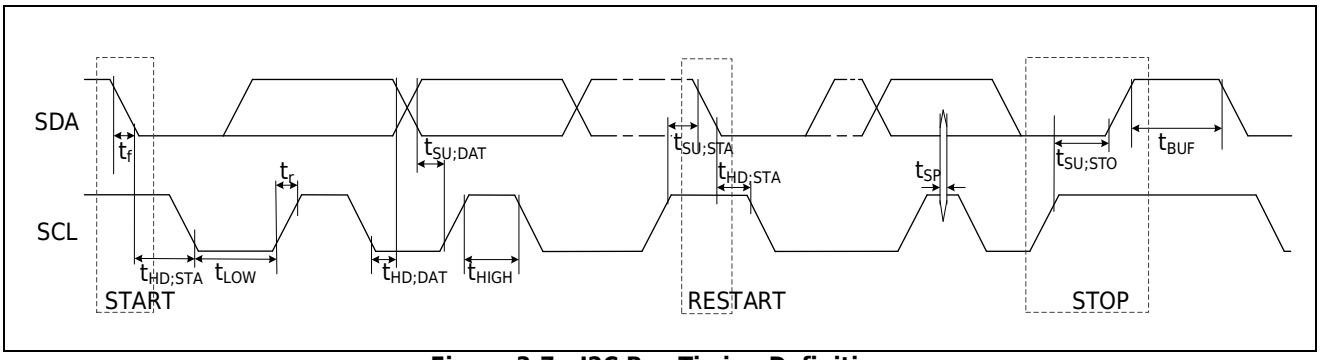


Figure 3-7 I2C Bus Timing Definition

3.3.14 SPI Interface Features

Table 3-37 SPI Electrical Features

Symbol	Parameter	Conditions	Min	Max	Unit
t_w(SCKH)	SCK high level time	Master Mode(4), 1.8V≤Vcc≤3.63V	T_{pclk1}-1(5)	T_{pclk1}+1(5)	ns
		Slave Mode(4), 1.8V≤Vcc≤3.63V	3xT_{pclk1}-1(5)	3×T_{pclk1}+1(5)	ns
t_w(SCKL)	SCK low level time	Master Mode(4), 1.8V≤Vcc＜3.63V	T_{pclk1}-1(5)	T_{pclk1}+1(5)	ns
		Slave Mode(4), 1.8V≤Vcc＜ 3.63V	3×T_{pclk1}-1(5)	3×T_{pclk1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave Mode, 1.8V≤Vcc≤3.63V(1)	4	-	ns
t_h(SI)	Data input hold time	Slave Mode, 1.8V≤Vcc≤3.63V(1)	3	-	ns
t_v(SO)	Data output valid time	Slave Mode, 2.7V≤Vcc≤3.63V(1)	-	15	ns
		Slave Mode, 1.8V≤Vcc＜2.7V(1)	-	26	ns
t_{su}(MI)	Data input setup time	Master Mode, 2.7V≤Vcc≤3.63V(1)	5	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V(1)	9	-	ns
t_h(MI)	Data input hold time	Master Mode, 2.7V≤Vcc≤3.63V	5	-	ns
		Master Mode, 1.8V≤Vcc≤2.7V	15	-	ns
t_{su}(SS)	SS setup time	Slave Mode, 1.8V≤Vcc≤3.63V	6×T_{pclk1} (5)	-	ns
		Master Mode, 2.7V≤Vcc≤3.63V	-5+N×T_{sck} (2)(5)	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck} (2)(5)	-	ns
t_h(SS)	SS hold time	Slave Mode, 1.8V≤Vcc≤3.63V	6×T_{pclk1} (5)	-	ns
		Master Mode, 2.7V≤Vcc≤3.63V	-5+N×T_{sck} (3)(5)	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck} (3)(5)	-	ns
t_v(MO)	Data output valid time	Master Mode, 2.7V≤Vcc≤3.63V(1)	-	4	ns
		Master Mode, 1.8V≤Vcc≤2.7V(1)	-	9	ns

1. Guarantee of mass production test.
2. N=1~8, determined by register SPI_CFG1.MSSI[2:0].
3. N=1~8, determined by register SPI_CFG1.MSSDL[2:0].
4. The values of t_w(SCKH) and t_w(SCKL) are determined by SPI_CFG2.MBR. The values listed in the table are those when SPI_CFG2.MBR=0.
5. T_{pclk1} refers to one cycle of the clock PCLK1, and T_{sck} refers to one cycle of the SPI communication clock.

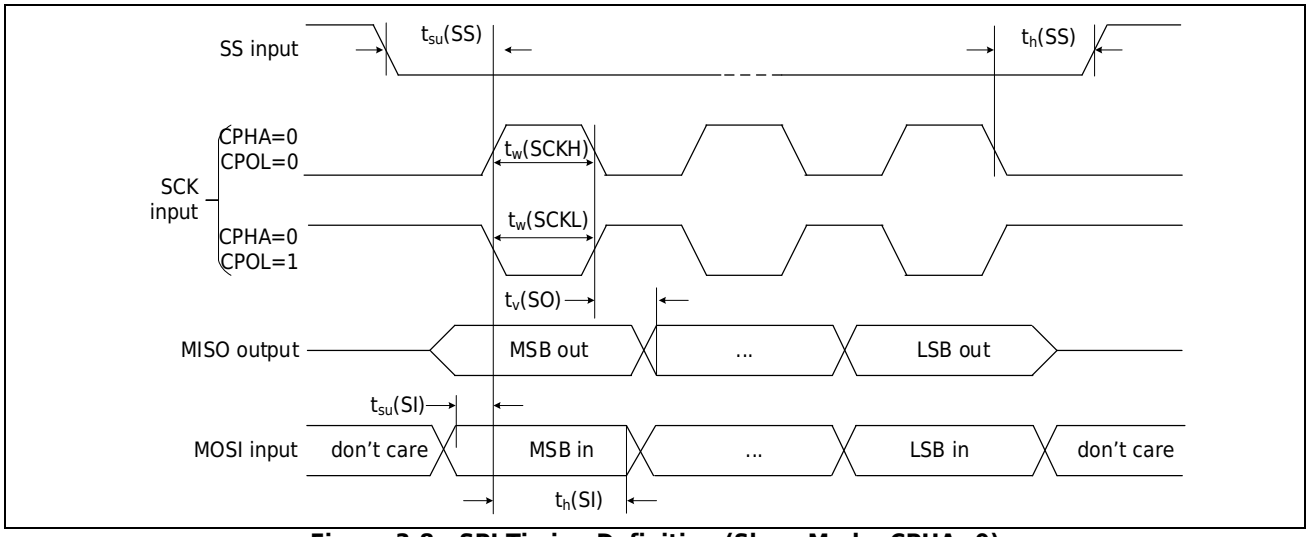


Figure 3-8 SPI Timing Definition (Slave Mode, CPHA=0)

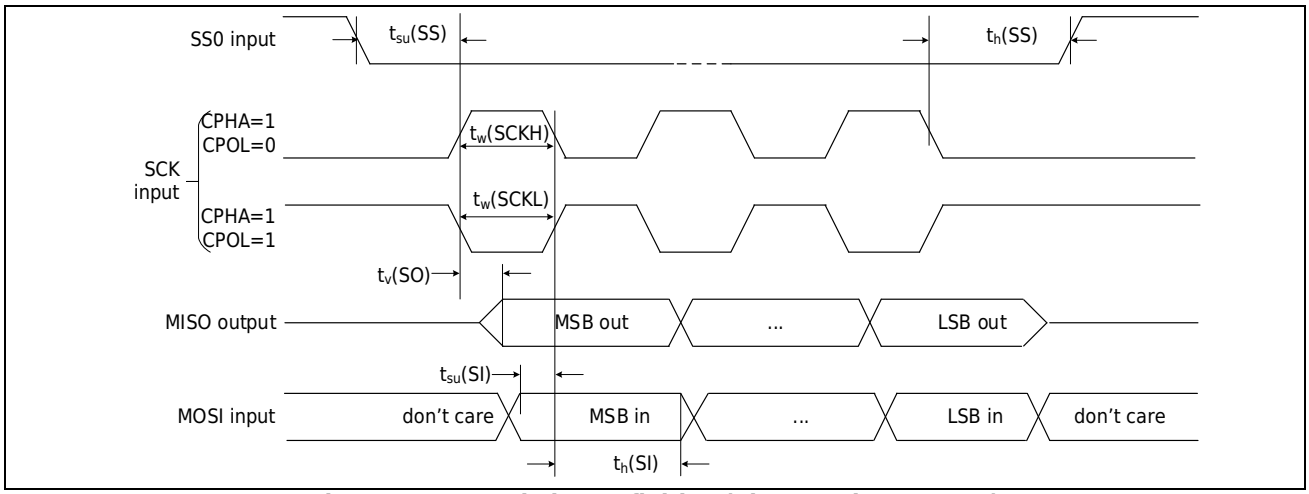


Figure 3-9 SPI Timing Definition (Slave Mode, CPHA=1)

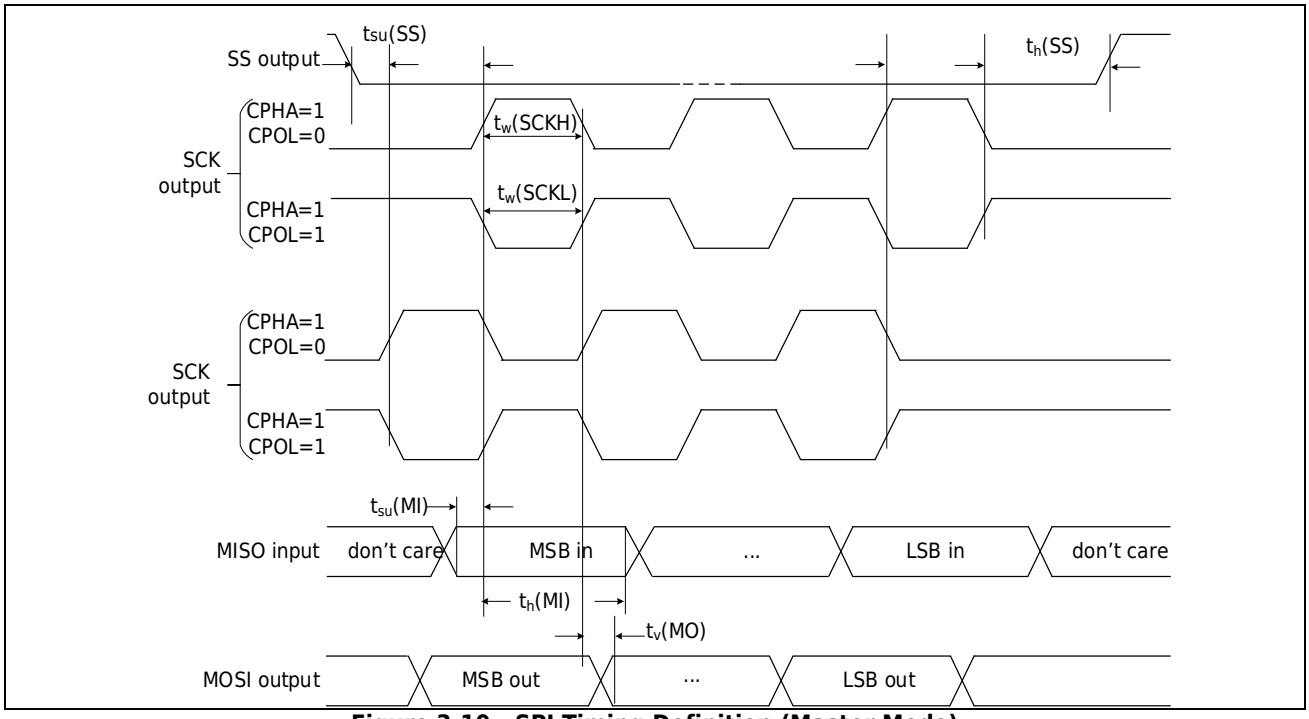


Figure 3-10 SPI Timing Definition (Master Mode)

3.3.15 USART Interface Features

Table 3-38 USART AC Timing

Symbol	Parameter		Min	Max	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock synchronization mode	6	-	
t_{CKw}	Input Clock Width		0.4	0.6	t_{cyc}
t_{CKr}	Input Clock Rise Time		-	5	ns
t_{CKf}	Input Clock Fall Time		-	5	ns
t_{TD}	Send delay time 2.7V≤Vcc≤3.63V(1)	Clock synchronization mode	-	23	ns
	Send delay time 1.8V≤Vcc＜2.7V	Clock synchronization mode	-	30	ns
t_{RDS}	Receive data setup time 2.7V≤Vcc≤3.63V(1)	Clock synchronization mode	17	-	ns
	Receive data setup time 1.8V≤Vcc＜2.7V	Clock synchronization mode	23	-	ns
t_{RDH}	Receive data hold time	Clock synchronization mode	5	-	ns

1. Guarantee of mass production test.

Table 3-39 USART Highest Baud Rate

Mode		Highest baud rate
UART	Internal timer	PCLK1/8
	External timer	PCLK1/32
Clock synchronization mode 2.7V≤Vcc≤3.63V		6.0Mbps
Clock synchronization mode 1.8V≤Vcc<2.7V		4.0Mbps

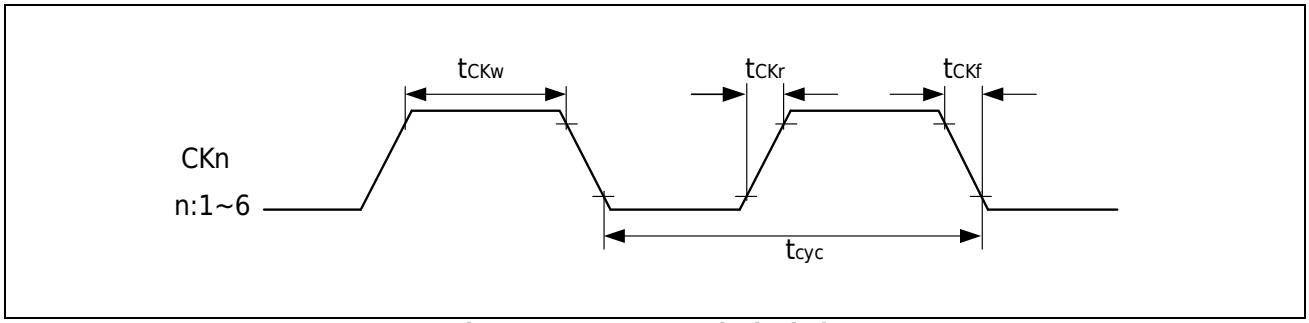


Figure 3-11 USART Clock Timing

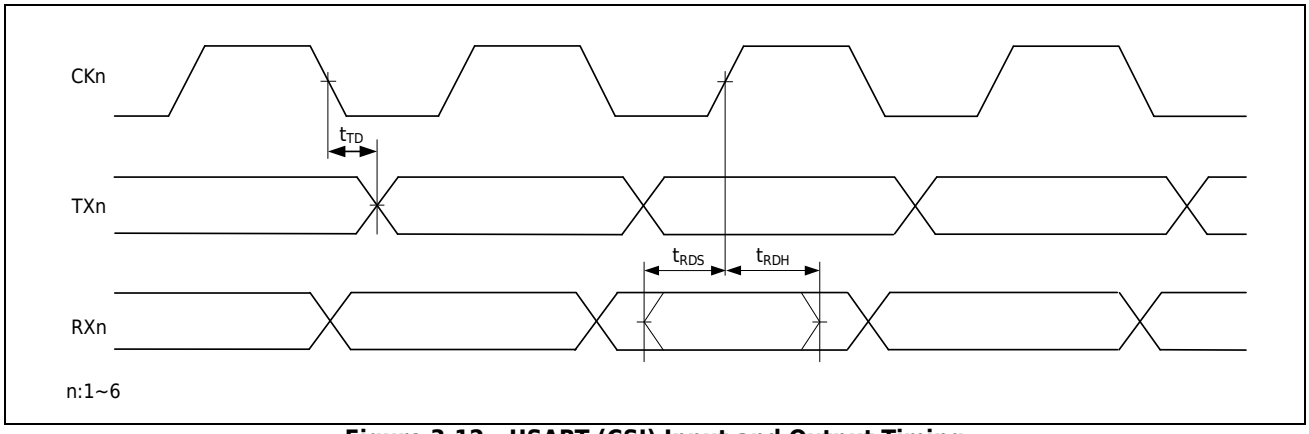


Figure 3-12 USART (CSI) Input and Output Timing

3.3.16 JTAG Interface Features

Table 3-40 JTAG Interface Features

Symbol	Parameter	Min	Typical Value	Max	Unit
t_{TCKcyc}	JTCK clock cycle	50	-	-	ns
t_{TCKH}	JTCK clock high level	15	-	-	ns
t_{TCKL}	JTCK clock low level	15	-	-	ns
t_{TCKr}	Clock Rise time	-	-	5	ns
t_{TCKf}	JTCK Clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time(1)	10	-	-	ns
t_{TMSh}	JTMS hold time(1)	10	-	-	ns
t_{TDIs}	JTDI setup time(1)	10	-	-	ns
t_{TDIh}	JTDI hold time(1)	10	-	-	ns
t_{TDOd}	JTDO data delay(1)	-	-	25	ns

1. Guarantee of mass production test.

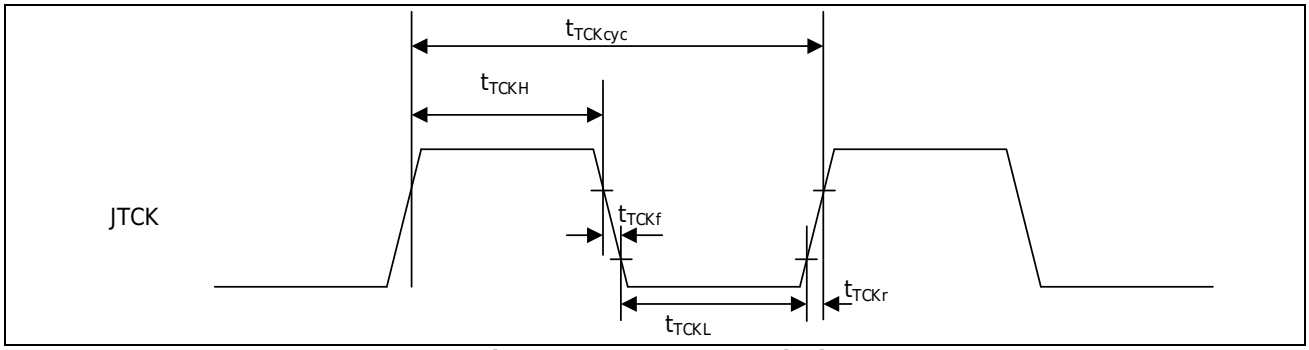


Figure 3-13 JTAG JTCK Clock

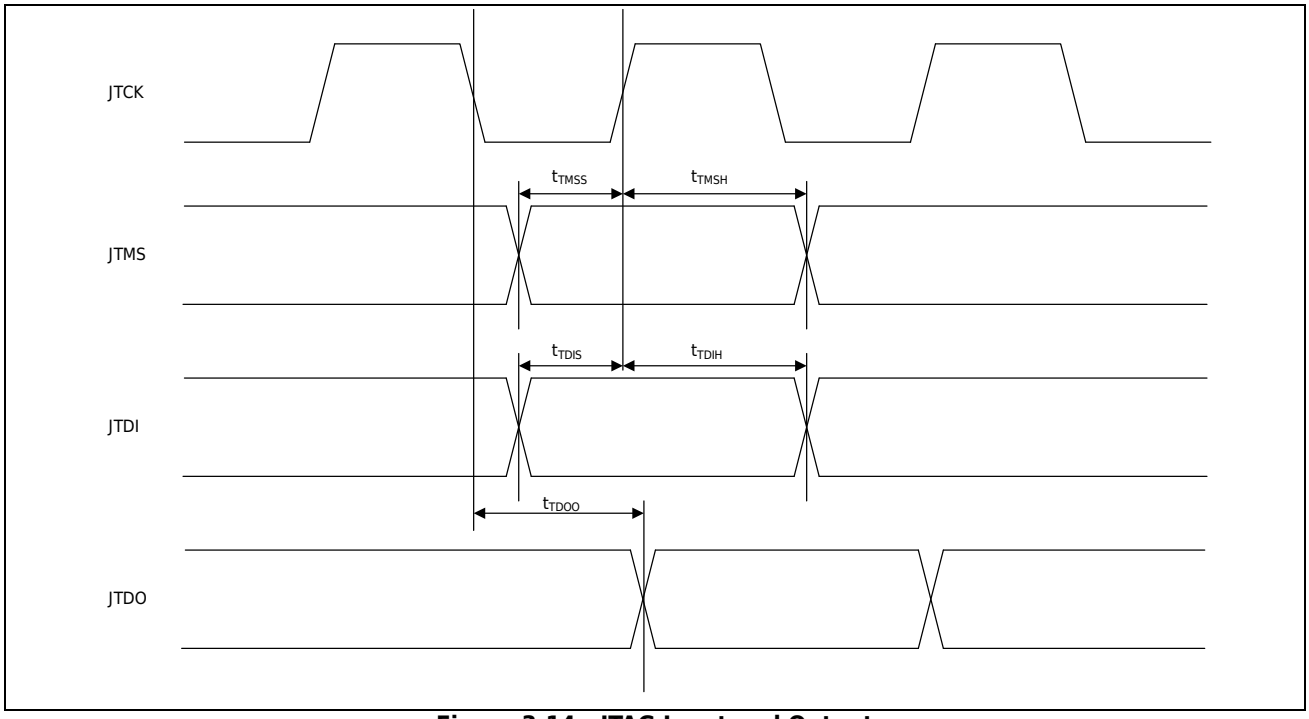


Figure 3-14 JTAG Input and Output

3.3.17 SWD Interface Features

Table 3-41 SWD Interface Features

Symbol	Parameter	Min	Typical Value	Max.	Unit
$t_{SWCLKcyc}$	SWCLK clock cycle	50	-	-	ns
t_{SWCLKH}	SWCLK clock high level	15	-	-	ns
t_{SWCLKL}	SWCLK clock low level	15	-	-	ns
t_{SWCLKr}	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time(1)	10	-	-	ns
t_{SWDIh}	SWDI hold time(1)	10	-	-	ns
t_{SWDOd}	SWDO data delay(1)	2	-	25	ns

1. Mass Production Test Guarantee.

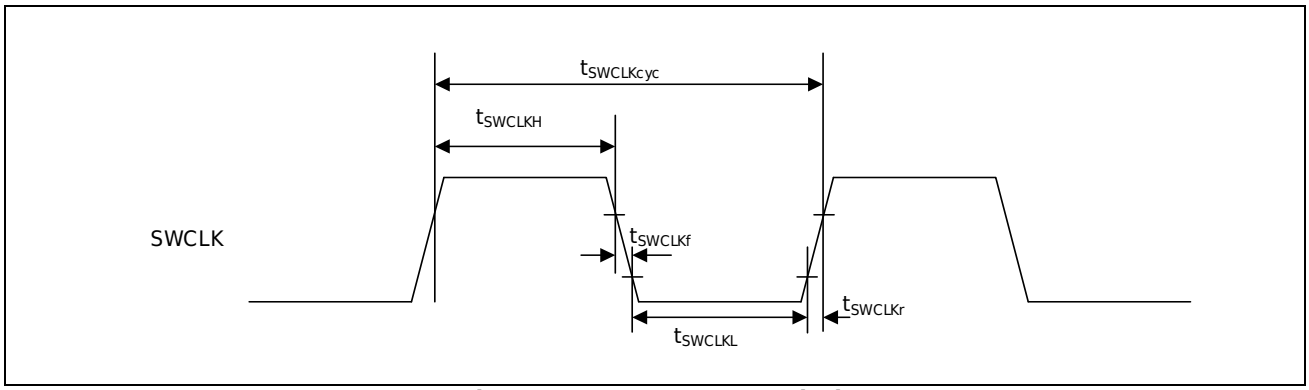


Figure 3-15 SWD SWCLK Clock

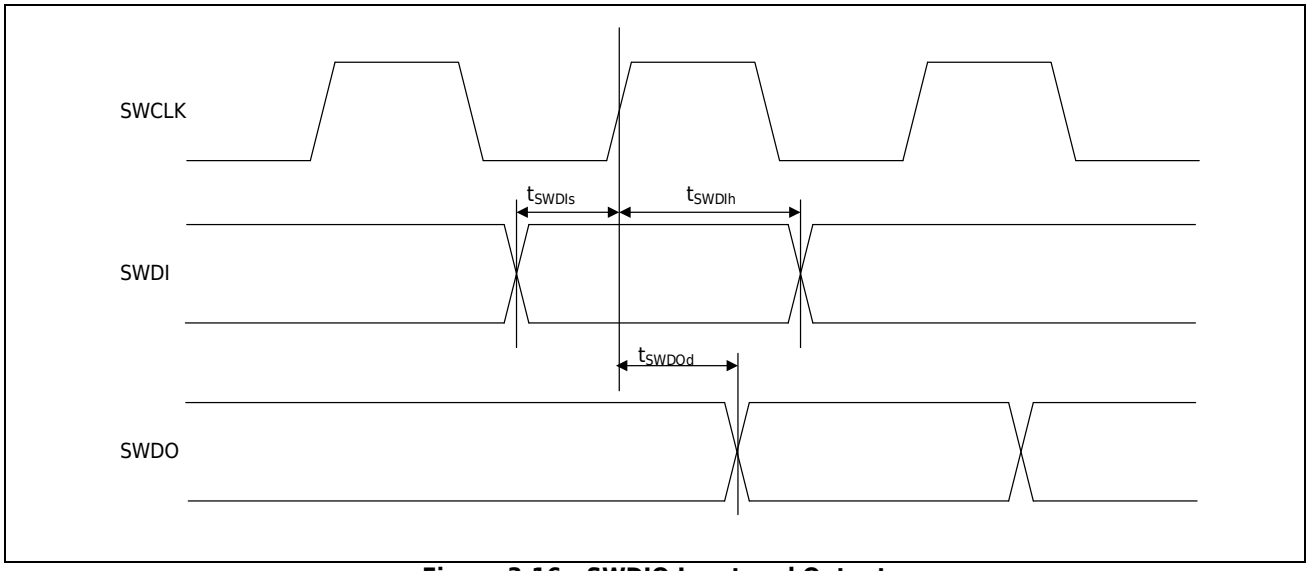


Figure 3-16 SWDIO Input and Output

3.3.18 TRACE Interface Features

Table 3-42 TRACE Interface Features

Symbol	Parameter	Min	Typical Value	Max	Unit
$t_{TRCLKcyc}$	TRACECK clock cycle	20	-	-	ns
t_{TRCKH}	TRACECK clock high level	7	-	-	ns
t_{TRCKL}	TRACECK clock low level	7	-	-	ns
t_{TRCKr}	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf}	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED0~3 data delay(1)	1.6	-	8.4	ns

1. Guarantee of mass production test.

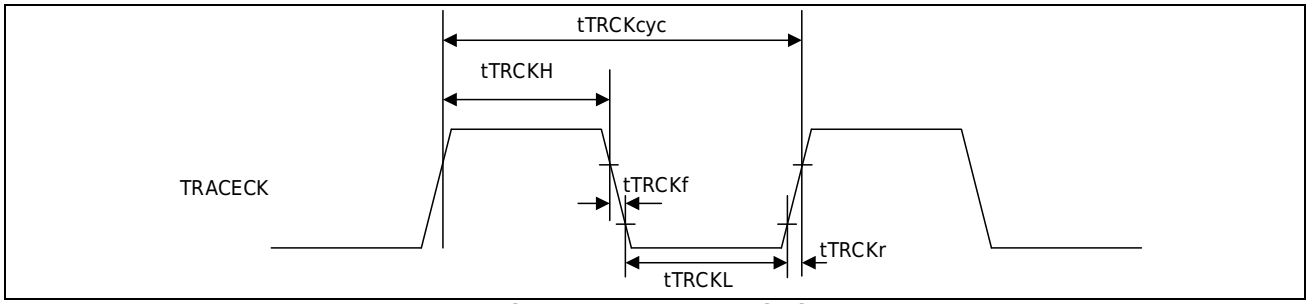


Figure 3-17 TRACE Clock

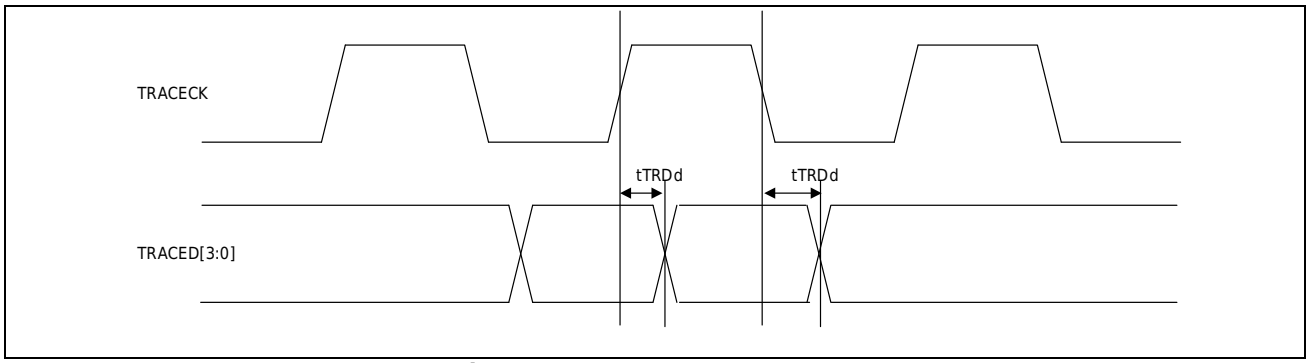


Figure 3-18 TRACE Data Output

3.3.19 12-bit ADC Features

Table 3-43 ADC Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
$V_{AVCC/REFH}$	Power supply	-	1.8	-	3.63	V
f_{ADC}	ADC conversion clock frequency	High-speed working mode V_{AVCC}=2.4 ~3.63V	1	-	60	MHz
		Low speed working mode V_{AVCC}=1.8 ~2.4V	1	-	30	
		Ultra-low speed working mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{AVSS}	-	$V_{AVCC/REFH}$	V
R_{AIN}	External input impedance(1)	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance(1)	-	-	3	6	kΩ
C_{ADC}	Internal sampling and retention capacitance(1)	-	-	4	7	PF
t_D	Trigger conversion delay(1)	f_{ADC}=60MHz	-	-	0.3	μs
t_S	Sampling time	f_{ADC}=60MHz	0.183	-	4.266	μs
			11	-	255	1/ f_{ADC}
t_{CONV}	Single channel total conversion time(1) (Including sampling time)	f_{ADC}=60MHz 12-bit resolution	0.4	-	-	μs
		f_{ADC}=60MHz 10-bit resolution	0.37	-	-	μs
		f_{ADC}=60MHz 8-bit resolution	0.34	-	-	μs
		20 to 268 (sampling time Ts + successive approximation n-bit resolution + 1)				1/ f_{ADC}
f_S	Sampling rate(1) f_{ADC}=60MHz	12-bit resolution single ADC	-	-	2.5	Msps
t_{ST}	Start time(1)	-	-	1	2	μs

1. Design guaranteed.

Formula 1: RAIN Maximum Value Formula

$$R_{AIN}=\frac{k}{f_{ADC}\times C_{ADC}\times \ln(2^{N+2})}-R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance to make the error lower than 1/ 4LSB. Where N = 12 (12-bit resolution), k is the number of sampling cycles defined in the ADC _ SSTR register.

Table 3-44 Input Channel Static Accuracy @f_{ADC}=60MHz

Symbol	Parameter	Conditions	Typical Value	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=60MHz Input source impedance<1KΩ V_{AVCC}=2.4~3.63V T_A=-40℃~105℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinearity error		±1.5	±3	LSB
E_L	Integral nonlinearity error		±2.0	±4	LSB

Table 3-45 Input Channel Static Accuracy @f_{ADC}=8MHz/ 30MHz

Symbol	Parameter	Conditions	Typical Value	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=8/30MHz Input source impedance<1KΩ V_{AVCC}=1.8V T_A=-40℃~105℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinearity error		±1.5	±3	LSB
E_L	Integral nonlinearity error		±2.0	±4	LSB

Table 3-46 Input Channel Dynamic Accuracy @f_{ADC}=60MHz

Symbol	Parameter	Conditions	Min	Max	Unit
ENOB	Significant digits	f_{ADC}=60MHz Input signal frequency = 2KHz Input source impedance<1KΩ V_{AVCC}=2.4 ~3.63V T_A=-40℃~105℃	10.5	-	Bits
SINAD	Signal-to-Noise Harmonic Ratio		65.0	-	dB
SNR	Signal-to-Noise Ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Table 3-47 Input Channel Dynamic Accuracy @f_{ADC}=8MHz/ 30MHz

Symbol	Parameter	Conditions	Min	Max	Unit
ENOB	Significant digits	f_{ADC}=8/30MHz Input signal frequency = 2KHz Input source impedance<1KΩ V_{AVCC}=1.8V T_A=-40℃~105℃	10.5	-	Bits
SINAD	SNR		65.0	-	dB
SNR	Signal-to-Noise Ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

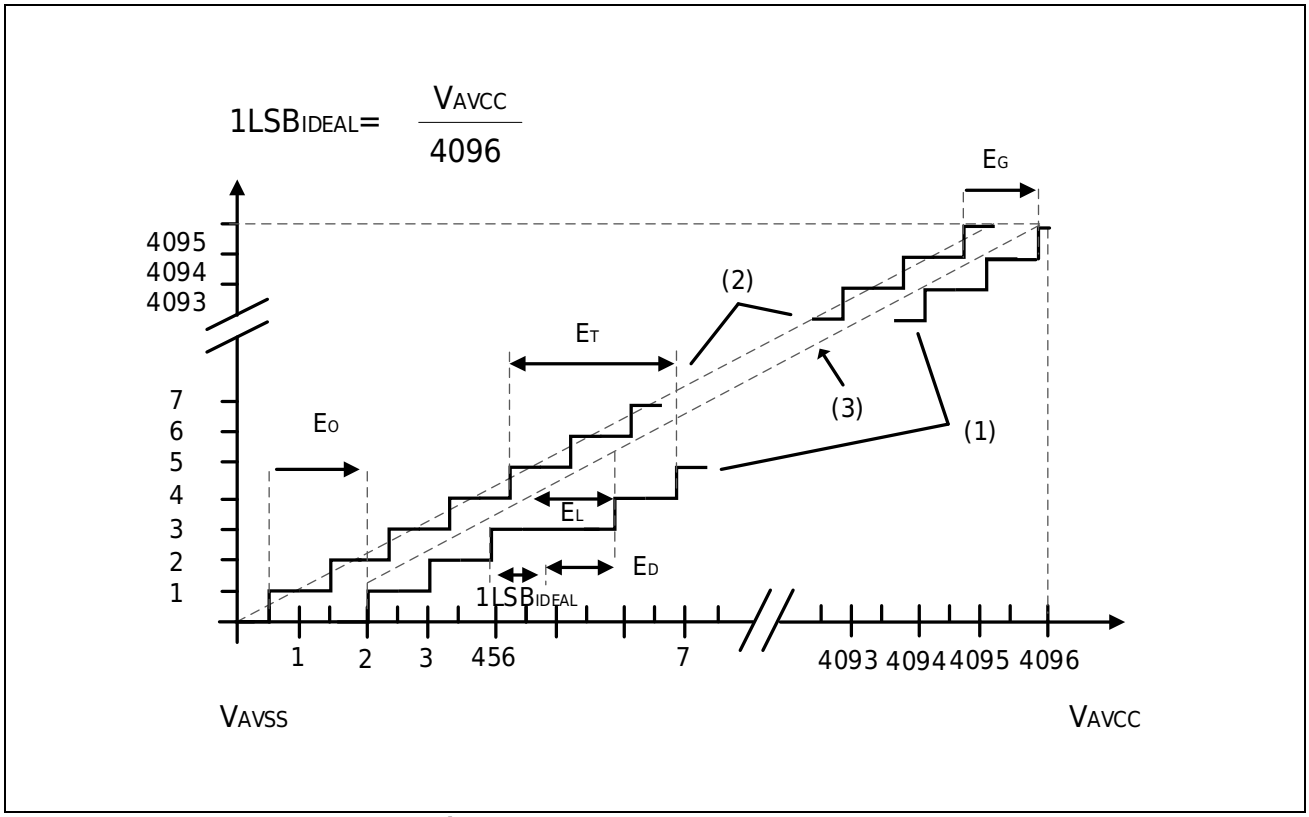


Figure 3-19 ADC Accuracy Features

1. Refer to also table above.
2. Examples of actual transmission curves.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.
   E_O = Offset Error: The deviation between the first actual transition and the first ideal transition.
   E_G = Gain Error: The deviation between the last ideal transition and the last actual transition.
   E_D = Differential nonlinearity error: The maximum deviation between the actual step and the ideal value.
   E_L = Integral Nonlinearity Error: The maximum deviation between any actual transition and the endpoint correlation line.

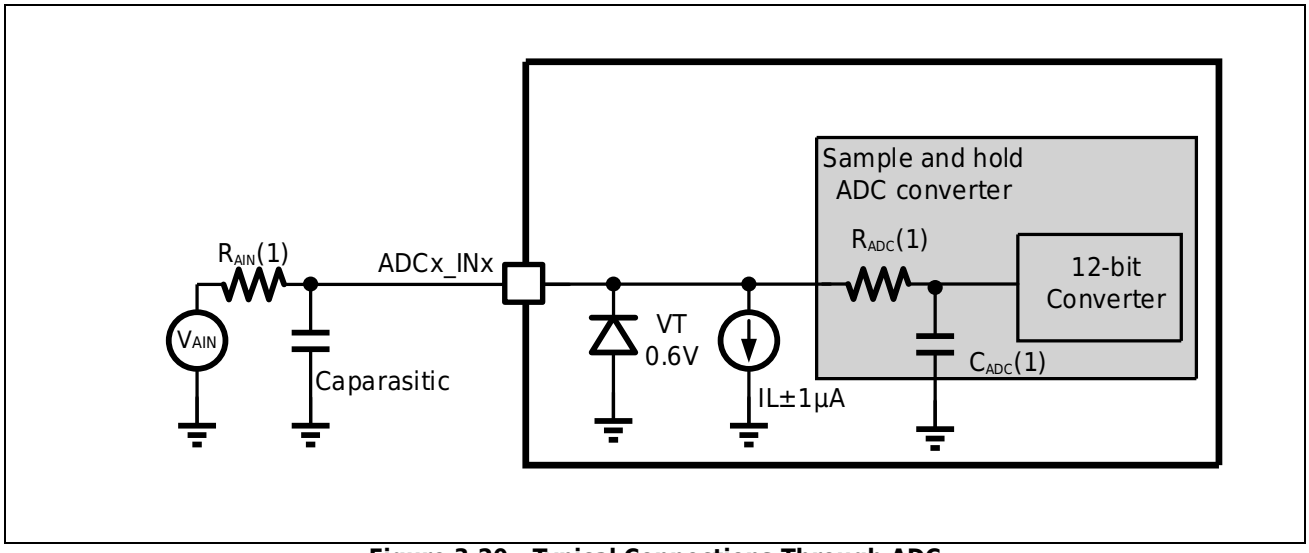


Figure 3-20 Typical Connections Through ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 3-43.
2. Cparasitic represents the PCB capacitance (depending on soldering and PCB routing quality) and pad capacitance (about 5pF). Higher values of Cparasitic result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the following figure. The 0.1μF capacitor should be a (good quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

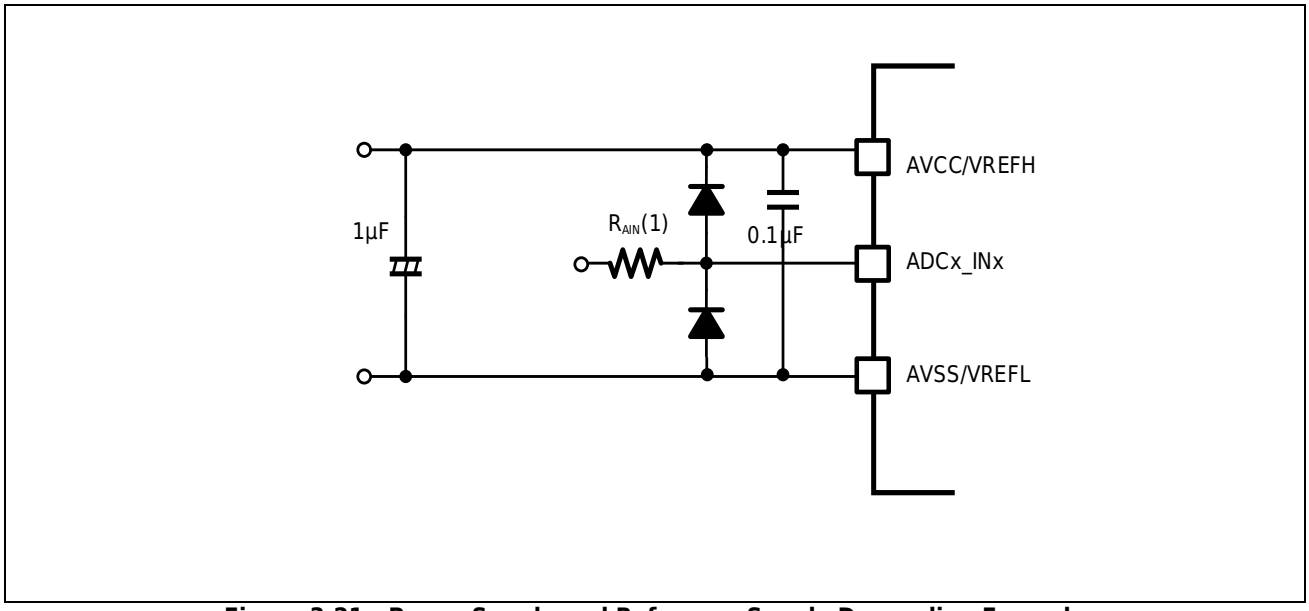


Figure 3-21 Power Supply and Reference Supply Decoupling Example

1. For information on RADC values, refer to Table 3-43.

3.3.20 12-bit DAC Features

Table 3-48 Features When 12-bit DAC Port Output Enabled and Output Amplifier Enabled

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.63	V
AO	Output voltage range	-	0.2	-	V_{AVCC}-0.2	-
RL	Load resistance	-	100	-	-	kΩ
CL	Load Capacitance	-	-	-	50	pF
DNL	Differential Nonlinearity Error (deviation between two consecutive codes -1 LSB)(1)	RL=100kΩ	-	-	±3	LSB
INL	Integral nonlinearity error (the difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095) (1)	RL=100kΩ	-	-	±5	LSB
OE	Offset Error (Difference between measured value and ideal value VREF+/2 at code 2048)	-	-	-	±15	LSB
GE	Gain error	-	-	-	±1	%
T_{st}	Settling Time (Full Scale: Applies to 12-bit input code transition between lowest input code and highest input code until the DAC output reaches ±4 LSB of final value) (2)	-	-	2	3	μs

1. Guarantee of mass production test.
2. Design guaranteed.

Table 3-49 12-bit DAC Port Output Enabled and Output Amplifier Disabled Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.63	V
AO	Output voltage range (1)	-	0	-	V_{AVCC}-1LSB	V
CL	Load Capacitance	-	-	-	20	pF
RO	Output resistance (2)	-	-	8.6	12	kΩ
DNL	Differential Nonlinearity Error (deviation between two consecutive codes -1 LSB)(1)	-	-	-	±2	LSB
TUE	Total unadjusted error	-	-	-	±24	LSB
T_{st}	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±4 LSB of final value, CL = 10 pF)	-	-	1.5	2.5	μs

1. Guarantee of mass production test.
2. Design guaranteed.

Table 3-50 12-bit DAC Port Output Disabled and Output Amplifier Disabled Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.63	V
AO	Output voltage range	-	0	-	V_{AVCC}-1 LSB	-
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB) (1)	-	-	-	±2	LSB
TUE	Total unadjusted error	-	-	-	±5	LSB
T_{st}	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±1 LSB of final value, Vavcc ≥ 2.7) (1)	-	-	95.5	117.3	ns
	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±32 LSB of final value, Vavcc ≥ 2.7)(1)	-	-	57.2	70.5	ns
	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±1 LSB of final value, Vavcc < 2.7) (1)	-	-	-	121.6	ns
	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±32 LSB of final value, Vavcc < 2.7) (1)	-	-	-	79.1	ns

1. Design guaranteed.

3.3.21 Comparator Features

Table 3-51 Comparator Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.63	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Comparing Time (1)	Step=200mV with overdrive 100mV Input Slew Rate ≥ 4mV/ns	-	-	60	ns
T_{set}	Input channel switching stabilization time	-	-	100	200	ns
Vhyst	Hysteresis voltage	HYST[2:0]=0b000	-	0	-	mv
		HYST[2:0]=0b001	-	10	-	mv
		HYST[2:0]=0b010	-	20	-	mv
		HYST[2:0]=0b011	-	30	-	mv
		HYST[2:0]=0b100	-	40	-	mv
		HYST[2:0]=0b101	-	50	-	mv
		HYST[2:0]=0b110	-	60	-	mv
		HYST[2:0]=0b111	-	70	-	mv
Voffset	Comparator input offset voltage	-	-15	-	+15	mV
I_{AVCC}	Comparator Current Consumption (Single Comparator)	-	-	400	500	μA

1. The performance test calculation method is to input voltage from the CMP input pin and output the comparison result from the CMP output pin.

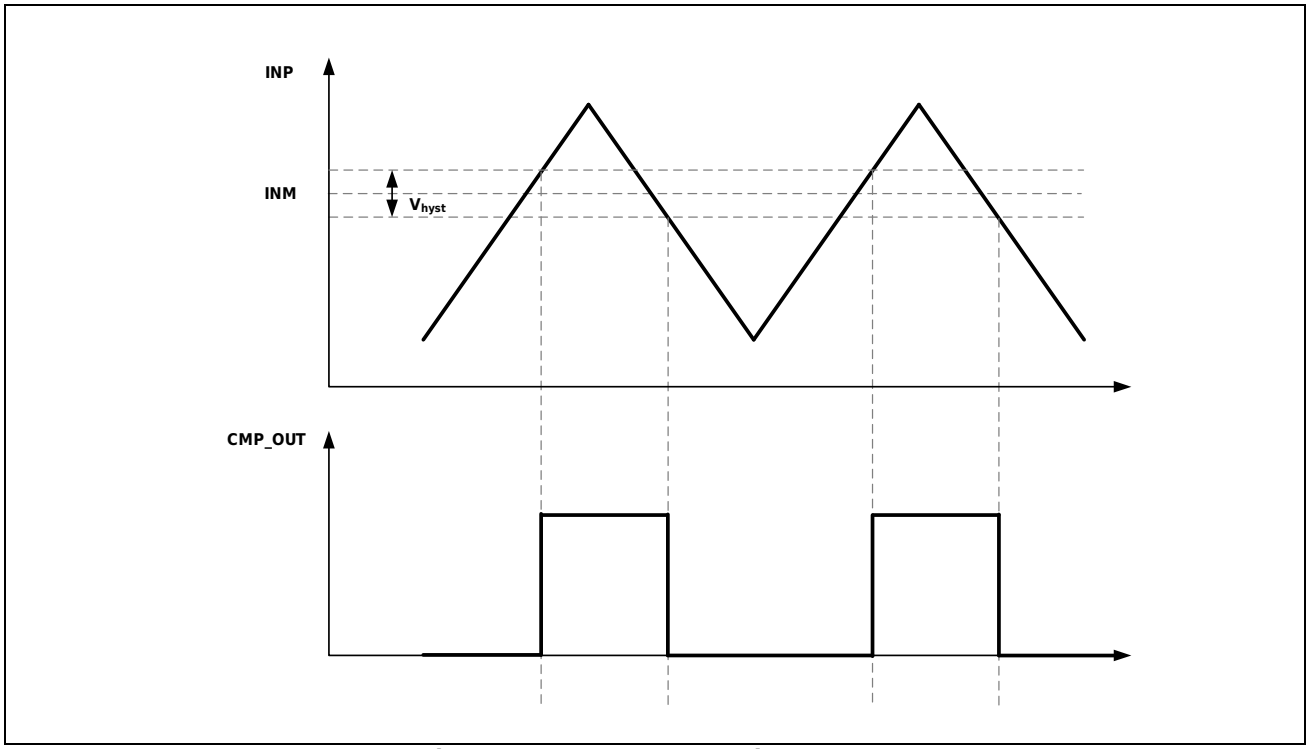


Figure 3-22 CMP Hysteresis Features

3.3.22 EIRQ Filter Features

Table 3-52 EIRQ Filter Features

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
W_{F_EIRQ}	EIRQ Input Filter Width	INTC_EIRQCR.NOCSEL[1:0] = 0b00	0.4	-	1.2	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b01	0.8	-	2.3	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b10	1.7	-	4.5	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b11	3.4	-	8.9	μs

3.3.23 USART1 RX Filter Features in Stop Mode

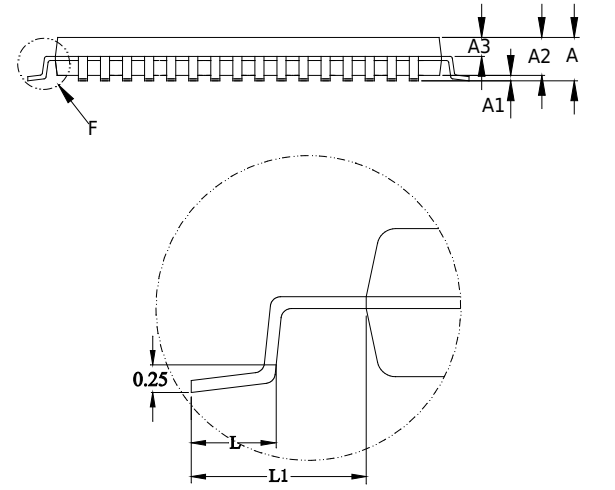
Table 3-53 USART1 RX Filter Features in STOP Mode

Symbol	Parameter	Conditions	Min	Typical Value	Max	Unit
W_{F_USART1}	USART1 input filter width	USART1_NFC.USART1_NFS[1:0] = 0b00	0.4	-	1.2	μs
		USART1_NFC.USART1_NFS[1:0] = 0b01	0.8	-	2.3	μs
		USART1_NFC.USART1_NFS[1:0] = 0b10	1.7	-	4.5	μs
		USART1_NFC.USART1_NFS[1:0] = 0b11	3.4	-	8.9	μs

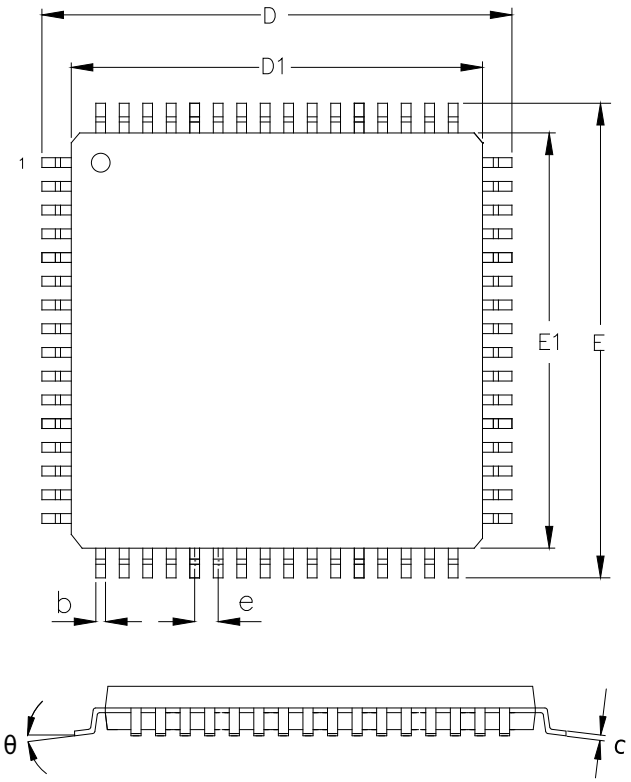
4 Package Specifications

4.1 Package Dimensions

LQFP64 packaging



DETAIL: F

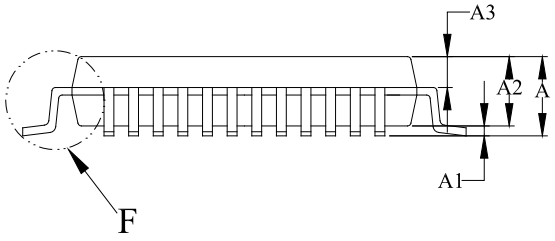


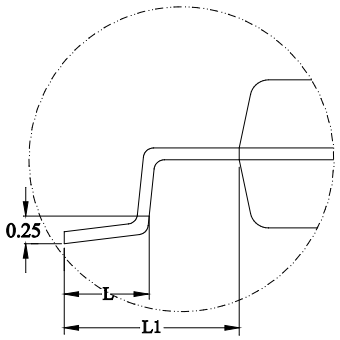
Symbol	10x10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

Note:

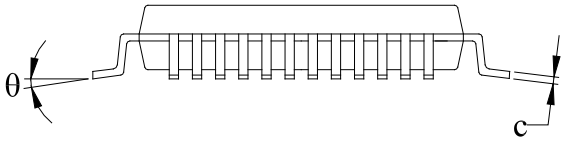
– *Dimensions "D1" and "E1" do not include mold protrusions*

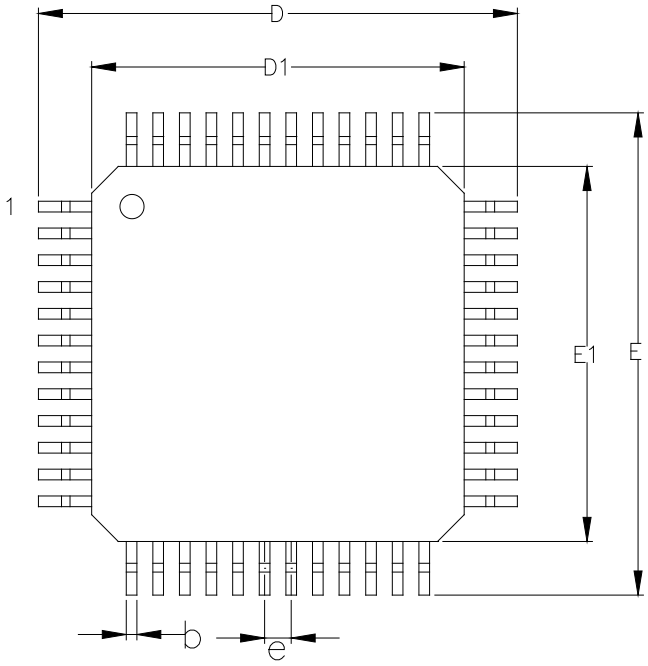
LQFP48 Packaging





DETAIL: F



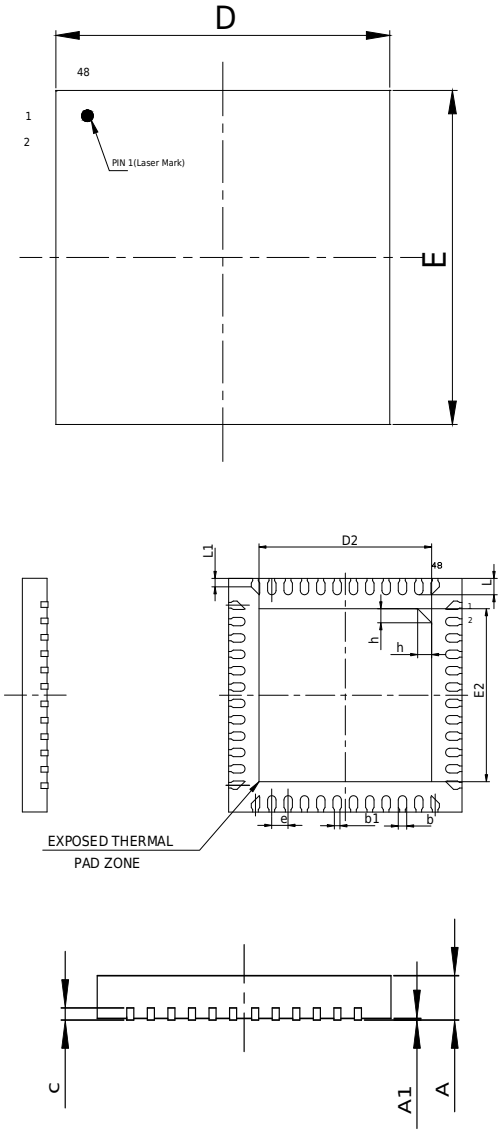


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

Note:

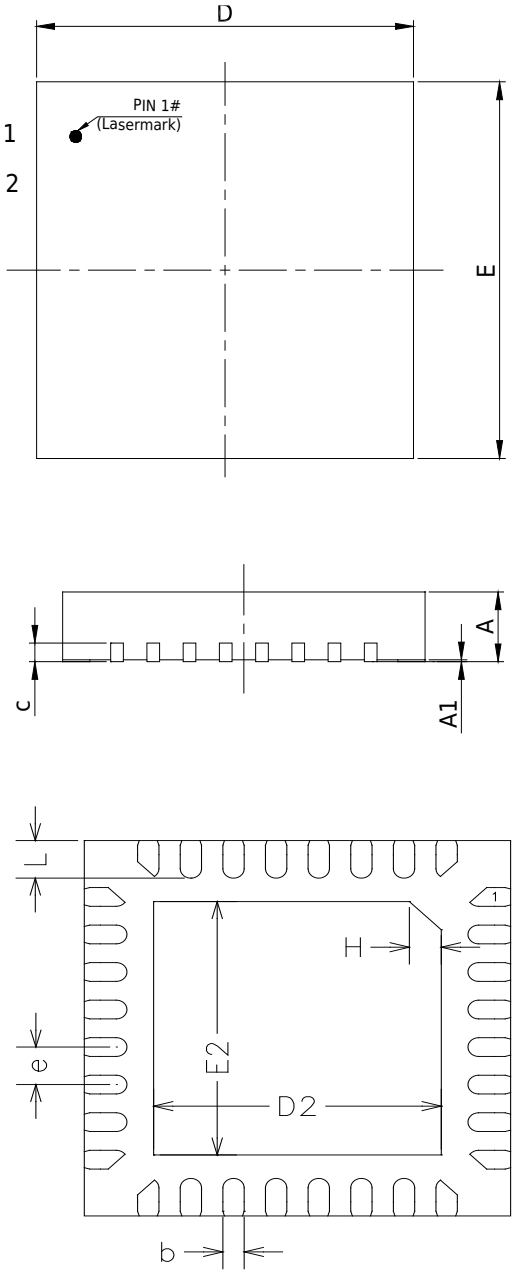
– *Dimensions "D1" and "E1" do not include mold protrusions*

QFN48 Packaging



Symbol	5x5 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35

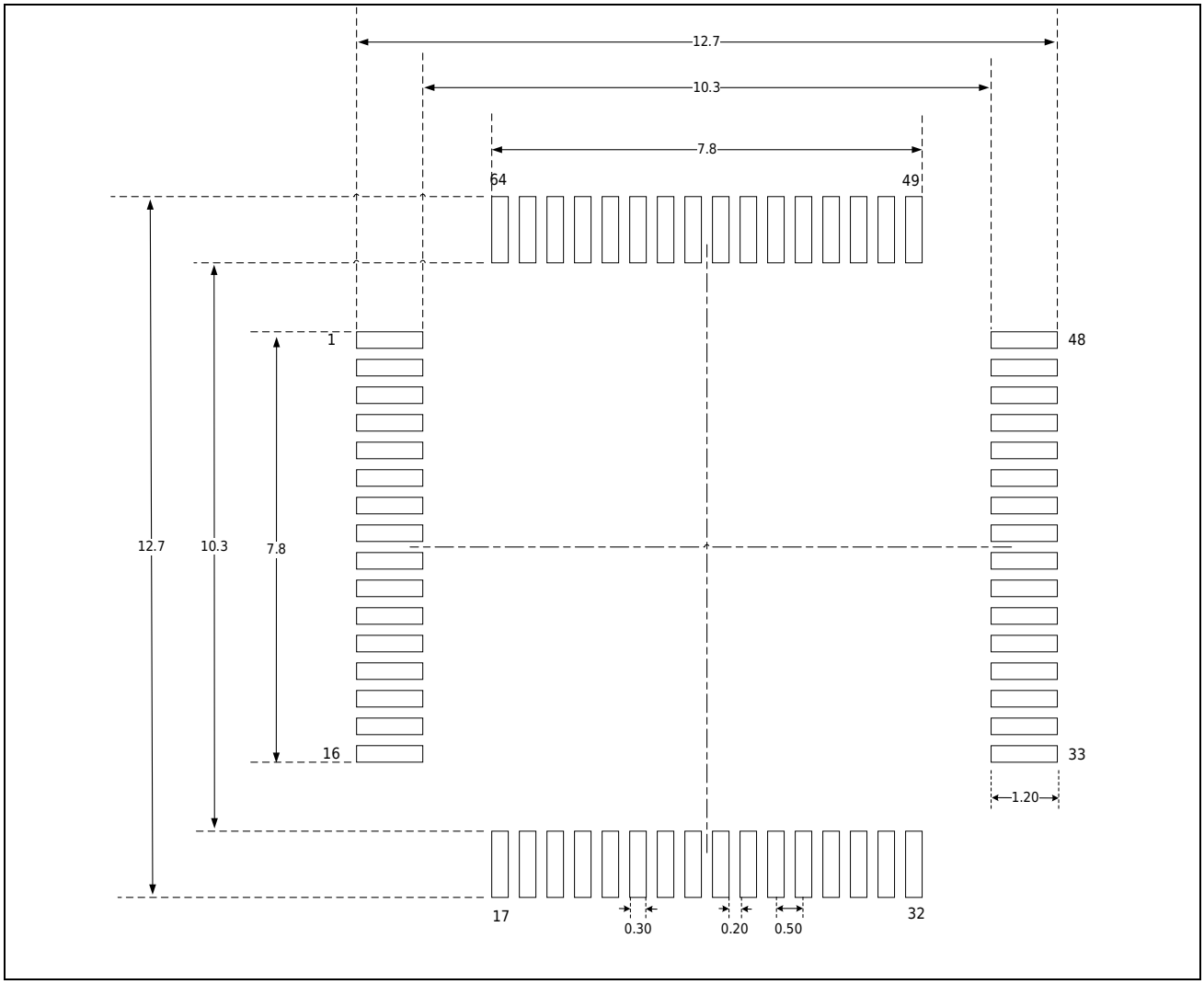
QFN32 Packaging



Symbol	4x4 Millimeter		
	Min	Nom	Max
A	0.7	0.75	0.8
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.50	2.70	2.90
e	0.40BSC		
E	3.90	4.00	4.10
E2	2.50	2.70	2.90
L	0.25	0.35	0.50
H	0.25	--	0.40

4.2 PCB Land Pattern

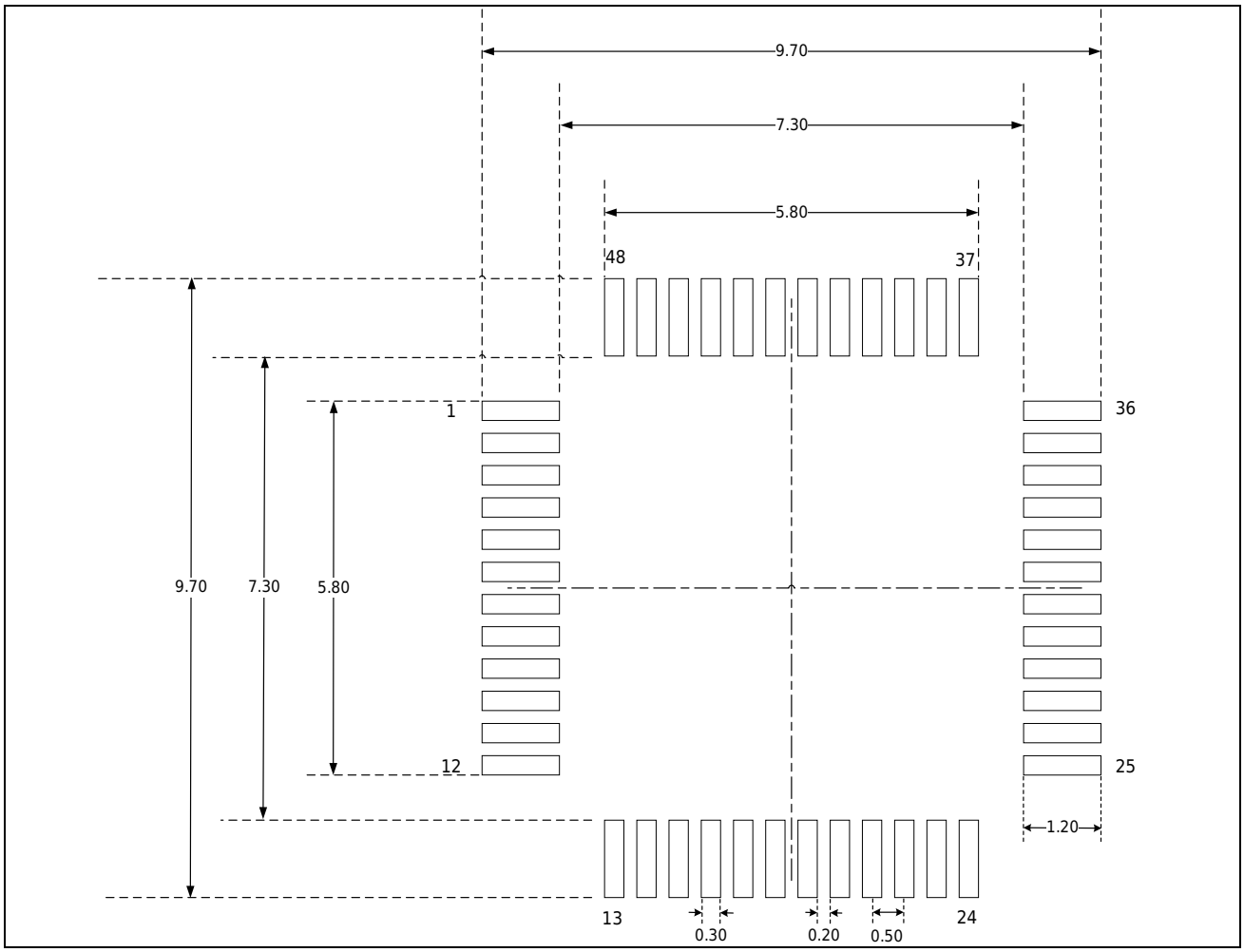
LQFP64 Packaging (10mm x 10mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

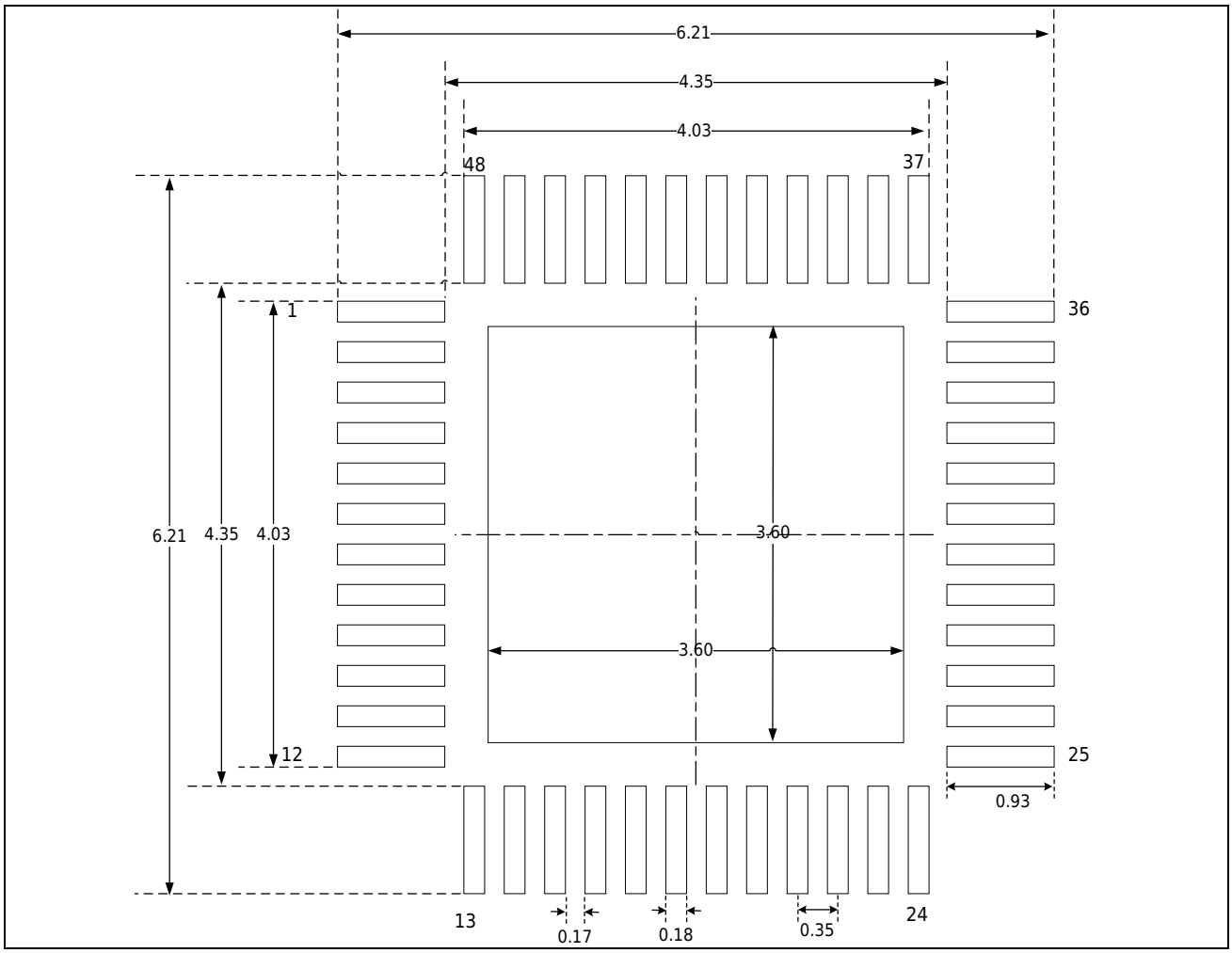
LQFP48 Packaging (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

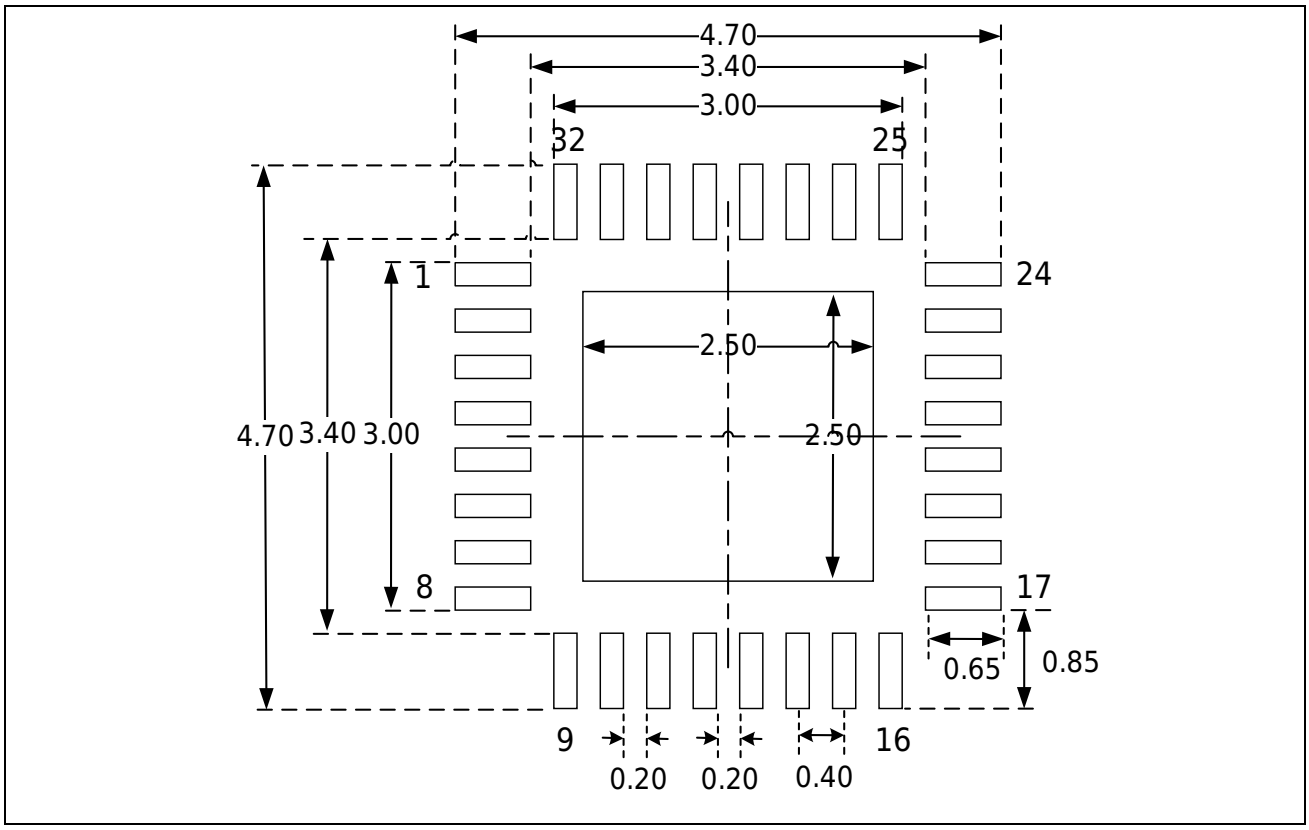
QFN48 Packaging (5mm x 5mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

QFN32 Packaging (4mm x 4mm)



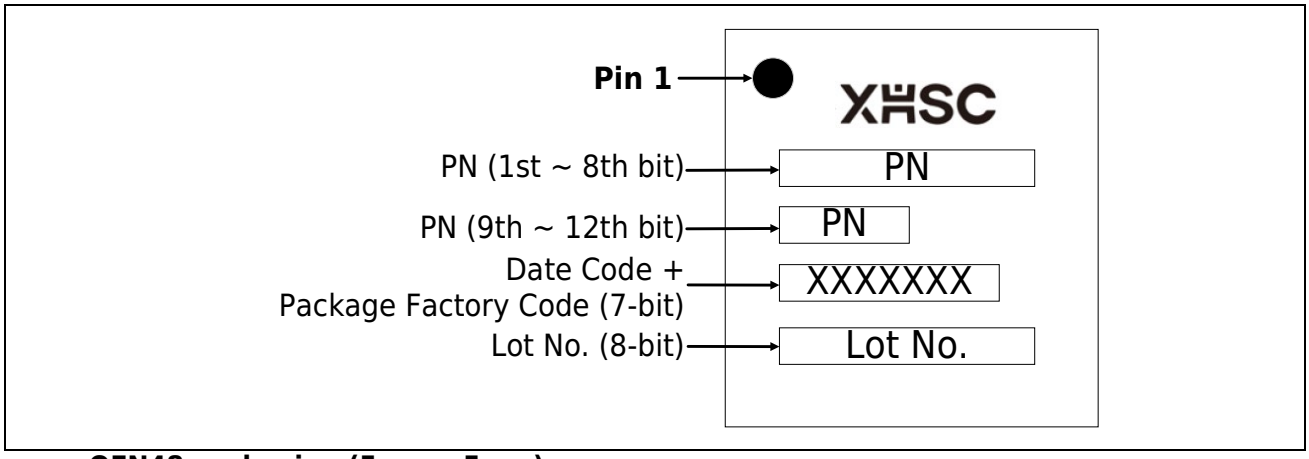
NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

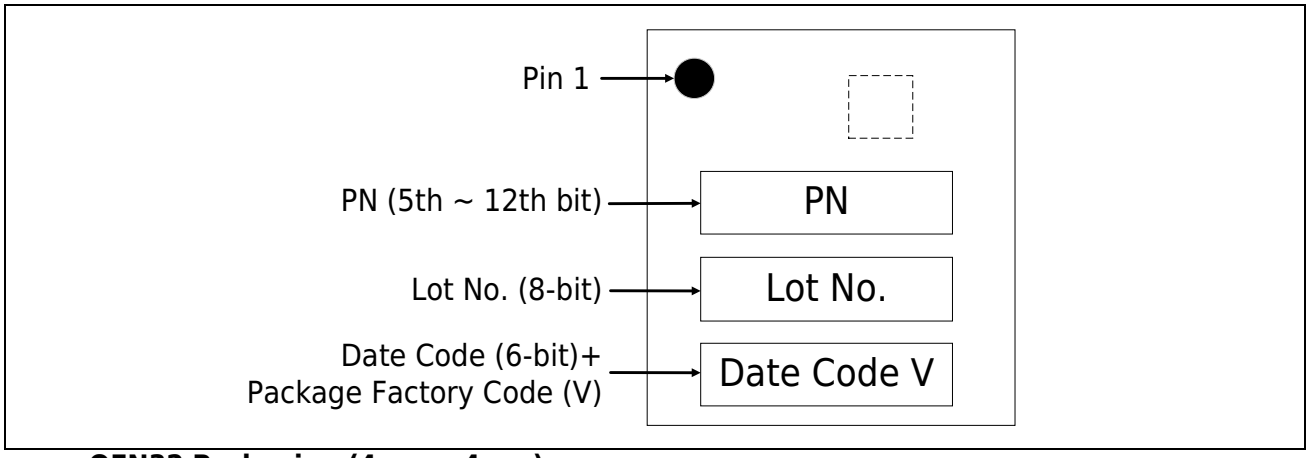
4.3 Package Marking

The position and information of Pin 1 printed on the front of each package are given below.

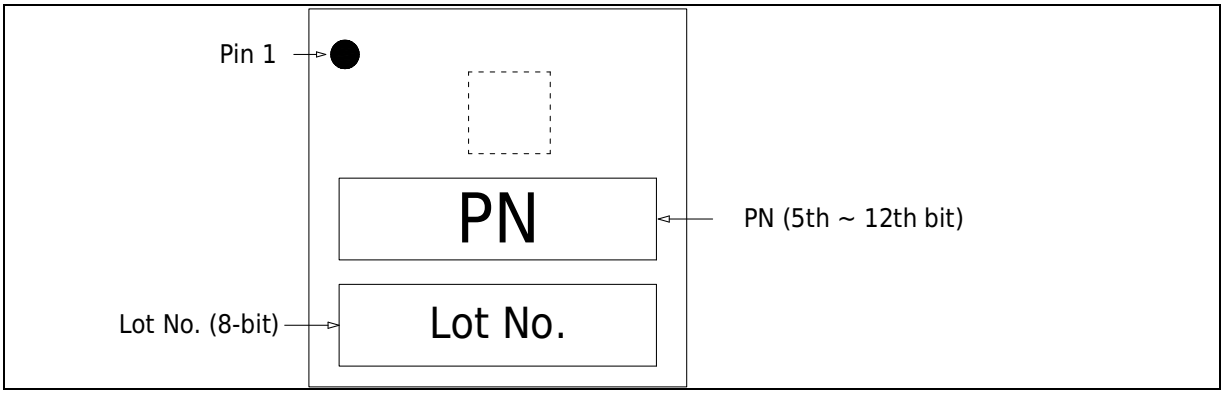
LQFP64 packaging (10mm x 10mm)/LQFP48 packaging (7mm x 7mm)



QFN48 packaging (5mm x 5mm)



QFN32 Packaging (4mm x 4mm)



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

4.4 Packaging Thermal Resistance Coefficient

When the packaged chip works at a specified operating ambient temperature, the junction temperature Tj (°C) on the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D \times \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of the internal power consumption of the chip (P_{INT}) and the power consumption generated by the I/O pin when the chip is working ($P_{I/O}$), and the unit is W.
  $P_{INT} = I_{CC} \times V_{CC}$
  $P_{I/O} = \sum(V_{OL} \times I_{OL}) + \sum((V_{CC} - V_{OH}) \times I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 4-1 Thermal Resistance Coefficient Table for Each Package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP64 10*10*1.4 e=0.5	65 +/- 10%	℃/W
LQFP48 7*7*1.4 e=0.5	75 +/- 10%	℃/W
QFN32 4*4*0.75 e=0.4	53 +/- 10%	℃/W
QFN48 5*5*0.55 e=0.35	42 +/- 10%	℃/W

5 Ordering Information

Function		Product Model							
		HC32F334F8UI-QFN32TR	HC32F334FAUI-QFN32TR	HC32F334J8UI-ZFN48TR	HC32F334JAUI-ZFN48TR	HC32F334J8TI-LQ48	HC32F334JATI-LQ48	HC32F334K8TI-LQFP64	HC32F334KATI-LQFP64
Main Frequency (MHz)		120							
Kernel		M4							
Number of GPIOs		27	27	39	39	39	39	53	53
Supply voltage range (V)		1.8~3.63							
Flash (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		36							
DMA		1unit * 8ch							
Communication Interface	USART (1)	4ch							
	SPI	1ch							
	I2C	1ch							
	CAN FD	2ch							
Timers and Counters (2) (3)	Timer0	2unit							
	TimerA	5unit							
	Timer4	1unit							
	Timer6	4unit							
	HRPWM	6unit							
	WDT	1ch							
	SWDT	1ch							
	RTC	1ch							
Analog	12bit ADC	3unit ,9ch	3unit ,9ch	3unit ,16ch	3unit ,16ch	3unit, 16ch	3unit, 16ch	3unit, 22ch	3unit, 22ch
	12bit DAC	3ch							

Function		Product Model							
		HC32F334F8UI-QFN32TR	**HC32F334FAUI-QFN32TR**	**HC32F334J8UI-ZFN48TR**	**HC32F334JAUI-ZFN48TR**	**HC32F334J8TI-LQ48**	**HC32F334JATI-LQ48**	**HC32F334K8TI-LQFP64**	**HC32F334KATI-LQFP64**
Analog	CMP	3ch							
	PVD	✓							
Working temperature		-40~105℃							
Package information (mm)	Package Type	QFN32 (4*4)	QFN32 (4*4)	QFN48 (5*5)	QFN48 (5*5)	LQFP48 (7*7)	LQFP48 (7*7)	LQFP64 (10*10)	LQFP64 (10*10)
	Thickness	0.75	0.75	0.55	0.55	1.6	1.6	1.6	1.6
	Packaging	Tape	Tape	Tape	Tape	tray	tray	tray	tray

Note:

1) USART_2/3/4 units with LIN function
2) Timer6, HRPWM, TimerA, Timer0 with capture input function
3) Timer6 and TimerA support 2-phase orthogonal encoding counting and 3-phase orthogonal encoding counting functions

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version Number	Revision Date	Modify the content
Rev1.00	12/06/2024	First edition release.