XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F030 Series

32-bit ARM® Cortex® -M0+ Microcontroller

Datasheet

Rev2.23 March 2025

Features

- **48MHz Cortex-M0+ 32-bit CPU platform**
- **HC32F030 series has a flexible power management system**
  - 5 μA @ 3 V Deep-sleep mode: all clocks off, power-on reset active, IO state retained, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 12 μA @32.768 kHz low-speed working mode: CPU and peripherals running, running programs from Flash
  - 35 μA/MHz@3V@24MHz sleep mode: CPU stops, peripherals run, main clock runs
  - 130 μA/MHz@3V@24MHz working mode: CPU and peripherals running, running programs from Flash
  - 4 μs wake-up time, making mode switching more flexible and efficient, and system response more agile
- 64K bytes Flash memory, with erase and write protection function
- 8K bytes RAM memory with parity check to enhance system stability
- General I/O pins (56IO/64pin, 40IO/48pin, 38IO/44pin, 26IO/32pin ,23IO/28pin)
- Clock, crystal
  - External high-speed crystal oscillator 8 ~ 32 MHz
  - External low-speed crystal 32.768 kHz
  - Internal high-speed clock 4/8/16/22.12/24 MHz
  - Internal low-speed clock 32.8/38.4 kHz
  - PLL clock 8 ~ 48 MHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
  - Three 1- channel complementary general-purpose 16- bit timers
  - 1 x 3 -channel complementary output 16- bit timer
  - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
  - 1 programmable 16-bit timer PCA, support capture compare, PWM output
  - 1 20-bit programmable watchdog circuit, built-in dedicated 10 kHz oscillator to provide WDT counting
- Communication Interface
  - 2-channel UART standard communication interface
  - 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware CRC-16/32 module
- Hardware 32-bit divider
- AES-128 hardware coprocessor
- TRNG true random number generator
- 2- channel DMAC
- Globally unique 10-byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in op amp, can measure external weak signals
- Integrates 3 multifunctional operational amplifiers
- 2- way voltage comparator VC with integrated 6 -bit DAC and programmable reference input
- Integrated low voltage detector LVD, can be configured with 16-step comparison level, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40 ~ 85 ℃, 1.8 ~ 5.5 V
- Package form: QFN32, LQFP64/48/44/32, TSSOP28

Support Model

HC32F030K8TA	HC32F030F8UA
HC32F030J8TA	HC32F030E8PA
HC32F030F8TA	HC32F030H8TA

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1 Introduction

The HC32F030 series is a general-purpose MCU with a wide operating voltage range. Integrated 12-bit 1Msps high-precision SARADC and integrated comparator, operational amplifier, built-in high-performance PWM timer, multi-channel UART, SPI, I2C and other rich communication peripherals, built-in AES, TRNG and other information security modules, It has the characteristics of high integration, high anti-interference and high reliability. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

General-Purpose MCU typical applications

- Smart transportation, smart city, smart home
- E-cigarettes, aircraft models, Wireless chargers and other consumer industries
- Electric tools and other motor control industries

32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

64K Byte FlASH

The built-in fully integrated Flash controller does not require external high voltage input, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP functions.

8K Byte RAM

According to different power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24 MHz. Under the configuration of 24 MHz, the wake-up time from deep sleep mode to working mode is 4 us, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8-32 MHz.

An external crystal oscillator XTL with a frequency of 32.768 kHz.

An internal clock RCL with a frequency of 32.8/38.4kHz.

A PLL with 8-48MHz output frequency.

Working mode

1) Running mode (Active Mode): CPU running, peripheral function modules running.
2) Sleep mode (Sleep Mode): The CPU stops running, and the peripheral function modules run.
   Deep sleep mode (Deep sleep Mode): The CPU stops running, the high-speed clock stops, and some function modules run.

Port controller GPIO

It can provide up to 56 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various deep sleep modes. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 20 mA. 56 general-purpose IOs can support external asynchronous interrupts.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

Interrupt vector number	Interrupt source
[0]	GPIO_PA
[1]	GPIO_PB

Interrupt vector number	Interrupt source
[2]	GPIO_PC
[3]	GPIO_PD
[4]	DMA
[5]	TIM3
[6]	UART0
[7]	UART1
[8]	-
[9]	-
[10]	SPI0
[11]	SPI1
[12]	I2C0
[13]	I2C1
[14]	TIM0
[15]	TIM1
[16]	TIM2
[17]	-
[18]	TIM4
[19]	TIM5
[20]	TIM6
[21]	PCA
[22]	WDT
[23]	-
[24]	ADC
[25]	-
[26]	VC0
[27]	VC1
[28]	LVD
[29]	-
[30]	RAM FLASH
[31]	CLK TRIM

Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset, and the program counter PC will be reset to point to start address.

	Reset source
[0]	Power-on and power-down reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

DMA controller DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

Timer TIM

Types	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
General timer	TIM0	16/32	1/2/4/8/16 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM1	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM2	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	No
Advanced timer	TIM4	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM5	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM6	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1

The general timer includes four timers TIM0/1/2/3.

General timer features:

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2. It can generate 3 sets of PWM complementary outputs or 6 channels of PWM independent output, and a maximum of 6 channels of input capture. With dead zone control function.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 is a high-performance counter with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or Period measurement.

The basic functions and features of Advanced Timer are shown in the table:

Waveform mode	Sawtooth wave, triangular wave
Basic functions	• Direction of increments and decrements
	• Software synchronization
	• Hardware synchronization
	• Cache function
	• Orthogonal coding count
	• General PWM output
	• Protection mechanism
	• AOS related actions

Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt

Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10kHz low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

Universal synchronous asynchronous transceiver UART0~UART1

2-channel universal asynchronous receiver/transmitter, UART0/UART1.

Basic functions of universal UART:

- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control

Serial Peripheral Interface SPI

2-channel synchronous serial interface (Serial Peripheral Interface).

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is PCLK/8, and the maximum communication rate is 6M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit

- Support DMA software/hardware access

I2C bus

Two-way I2C (Inter-Integrated Circuit), supporting both master and slave modes.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

Buzzer

4 general-purpose timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 20mA sink current, complementary output, no additional transistor is needed.

Clock calibration circuit module CLKTRIM

The built-in clock calibration circuit can calibrate the internal RC clock through an external precise crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID addresses are: 0x00100E74 – 0x00100E7D.

Cyclic Redundancy Check (CRC)

CRC16 conforms to the polynomial given in ISO/IEC13239 $=X^{16} + X^{12} + X^5 + 1$

CRC32 conforms to the polynomial given in ISO/IEC13239 $= x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8 +x^7 +x^5 +x^4+x^2 +x+1$

Hardware Divider Module HDIV

HDIV (Hardware Divider) is a 32-bit signed/unsigned integer hardware divider.

Basic characteristics of HDIV hardware divider:

- Configurable signed/unsigned integer division calculation
- 32-bit dividend, 16-bit divisor
- Output 32-bit quotient and 32-bit remainder
- Divide by zero warning flag, division end flag
- 10 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division operation
- Automatically wait for the end of the calculation when reading the quotient register/remainder register

Advanced Encryption Standard Module AES

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length of AES is fixed at 128 Bit, and the key length supports 128 Bit.

True Random Number Generator TRNG

TRNG is a true random number generator, used to generate true random numbers.

Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5 V or 2.5 V) or from an external input or power supply voltage. 29 input channels, including 24 external pin inputs, 1 internal temperature sensor voltage, 1/3 supply voltage, and 3 OPA outputs. Built-in configurable input signal amplifier to detect weak signals.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;
- 29 input channels, including 24 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, and 3 OPA outputs;
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5 V reference voltage, built-in 2.5 V reference voltage;
- ADC voltage input range: 0~Vref;
- 4 conversion modes: single conversion, sequential scan continuous conversion, queue scanning continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in signal amplifier, can convert high impedance signal;
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

Analog Voltage Comparator VC

Chip pin voltage monitoring / comparison circuit. 16 configurable positive external input channels, 11 configurable negative external input channels; 4 internal negative input channels, including 1 internal temperature sensor voltage, 1 -channel built-in BGR 2.5V reference voltage, 1 channel 64-step resistor divider. VC output can be used for general-purpose timer TIM0/1/2/3,programmable counting array PCA for capturing, gating, and external counting clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

Low voltage detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3 V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3 V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

Operational Amplifier OPA

OPA module can be flexibly configured and is suitable for simple filter and buffer applications. The three internal op amps can be configured as combined op amps with different gains in the opposite direction and in the same direction, or can be cascaded with external resistors.

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

Programming mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

ISP protocol programming interface: PA9, PA10 or PA13, PA14.

SWD protocol programming interface: PA13, PA14.

When reset, BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and FLASH can be programmed through ISP protocol.

When reset, BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in FLASH, and FLASH can be programmed through SWD protocol.

Note:

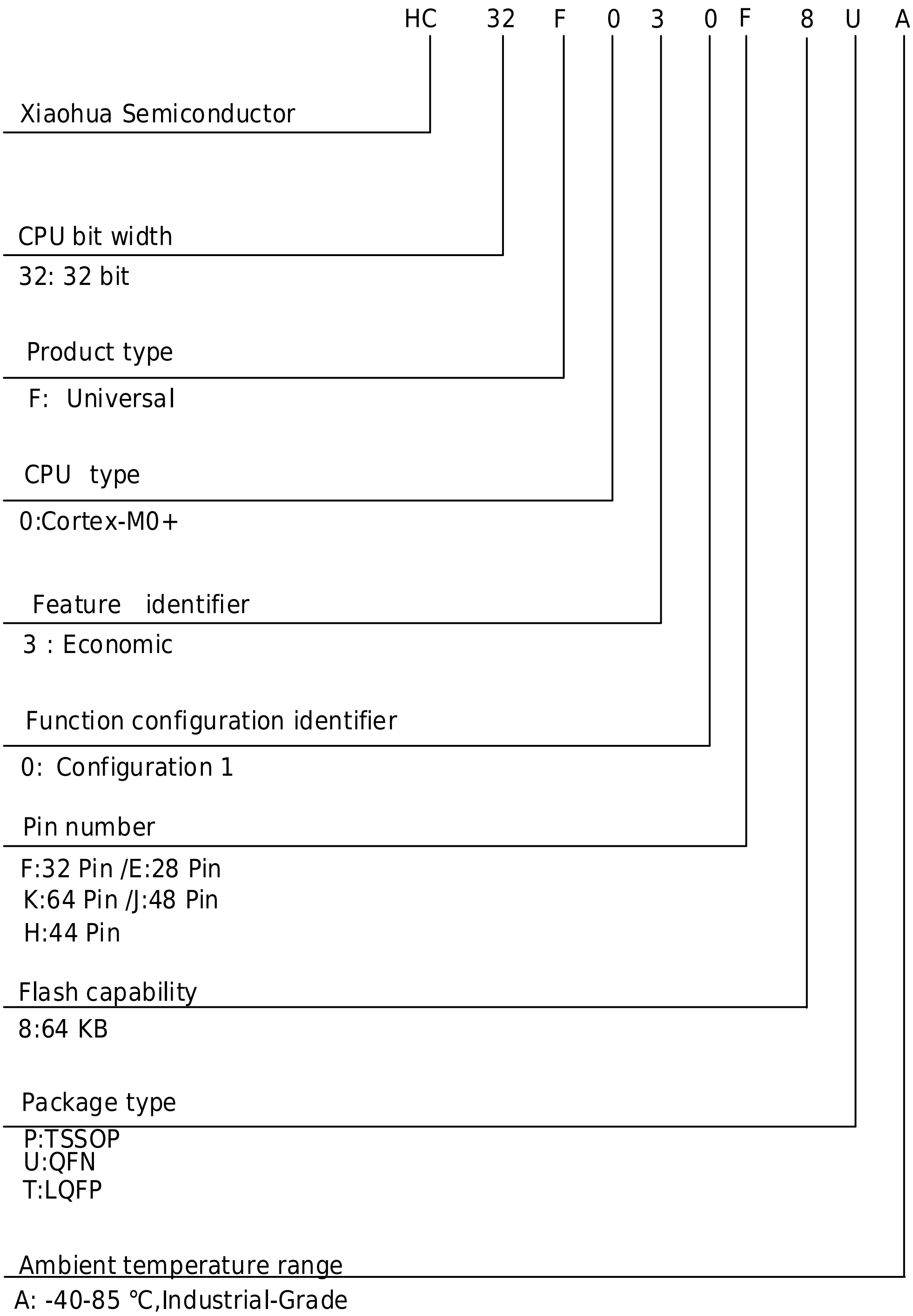
– ***It is recommended to reserve PA9 and PA10 as the ISP programming interface. If you need to use PA13 and PA14 as the ISP programming interface, please refer to PCN: PCN20191230-1_HC32L130HC32F030HC32L136 to increase the programming speed.***

High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product Lineup

2.1 Product Name



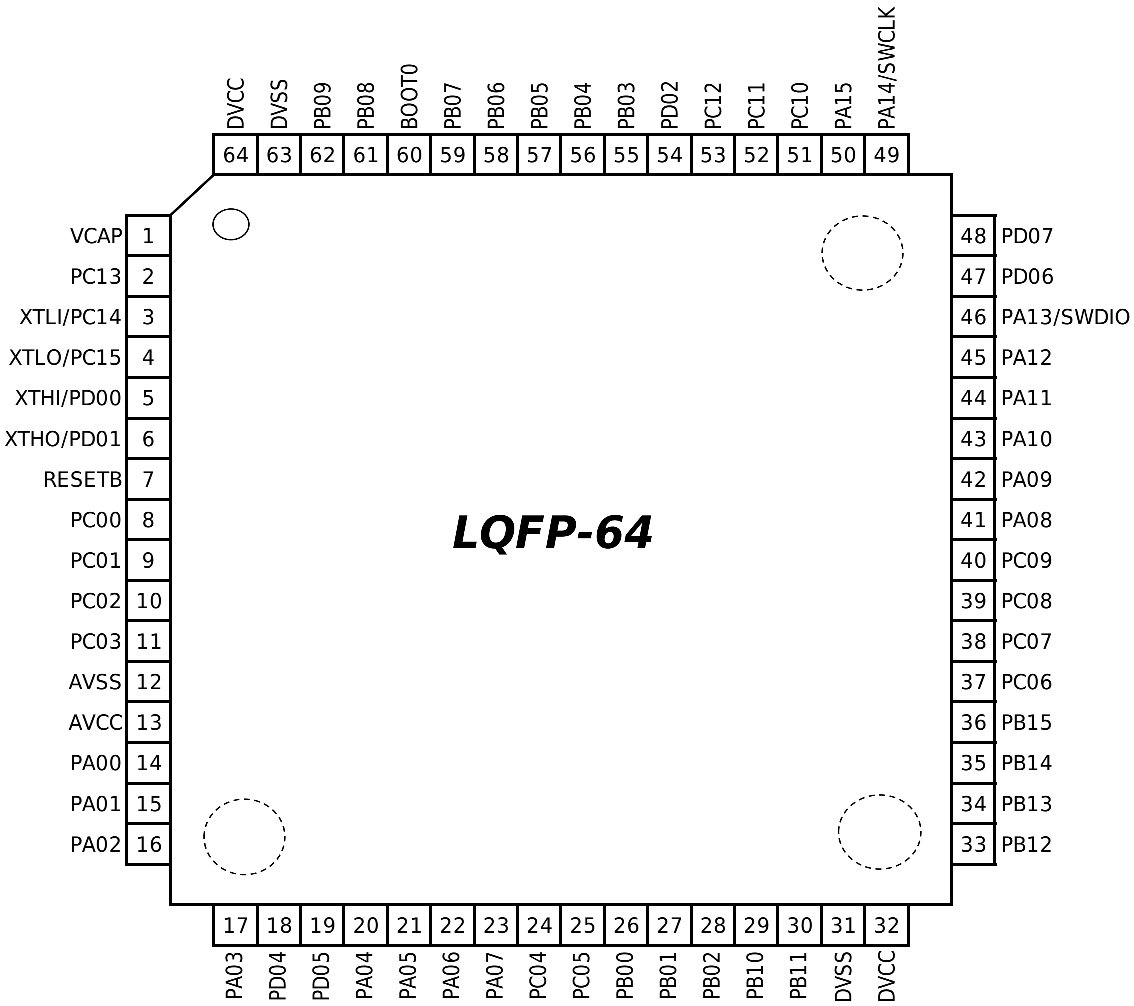
2.2 Function

Product name		HC32F030K8TA	HC32F030J8TA	HC32F030H8TA	HC32F030F8TA HC32F030F8UA	HC32F030E8PA
Pin number		64	48	44	32	28
GPIO pin number		56	40	38	26	23
CPU	Kernel	Cortex M0+				
	Frequency	48MHz				
Supply voltage range		1.8 ~5.5V				
Single / dual power supply		Single power supply				
Temperature range		-40 ~ 85℃				
Debug function		SWD debug interface				
Unique identification code		Support				
Communication Interface		UART0/1 SPI0/1 I2C0/1			UART0/1 SPI0 I2C0/1	
Timer		General timer TIM0/1/2 General timer TIM3 Advanced timer TIM4/5/6				
12-bit A/D converter		24ch	17ch		10ch	11ch
Analog voltage comparator		VC0/1				
Port interrupt		56	40	38	26	23
Low voltage detection reset		1				
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz				
	Internal low-speed oscillator	RCL 32.8/38.4kHz				
	PLL	8~48MHz				
	External high-speed crystal oscillator	8~32MHz				
buzzer		Max 4ch				
Flash security protection		Support				
RAM parity		Support				

3 Pin Configuration and Function

3.1 Pin Configuration Diagram

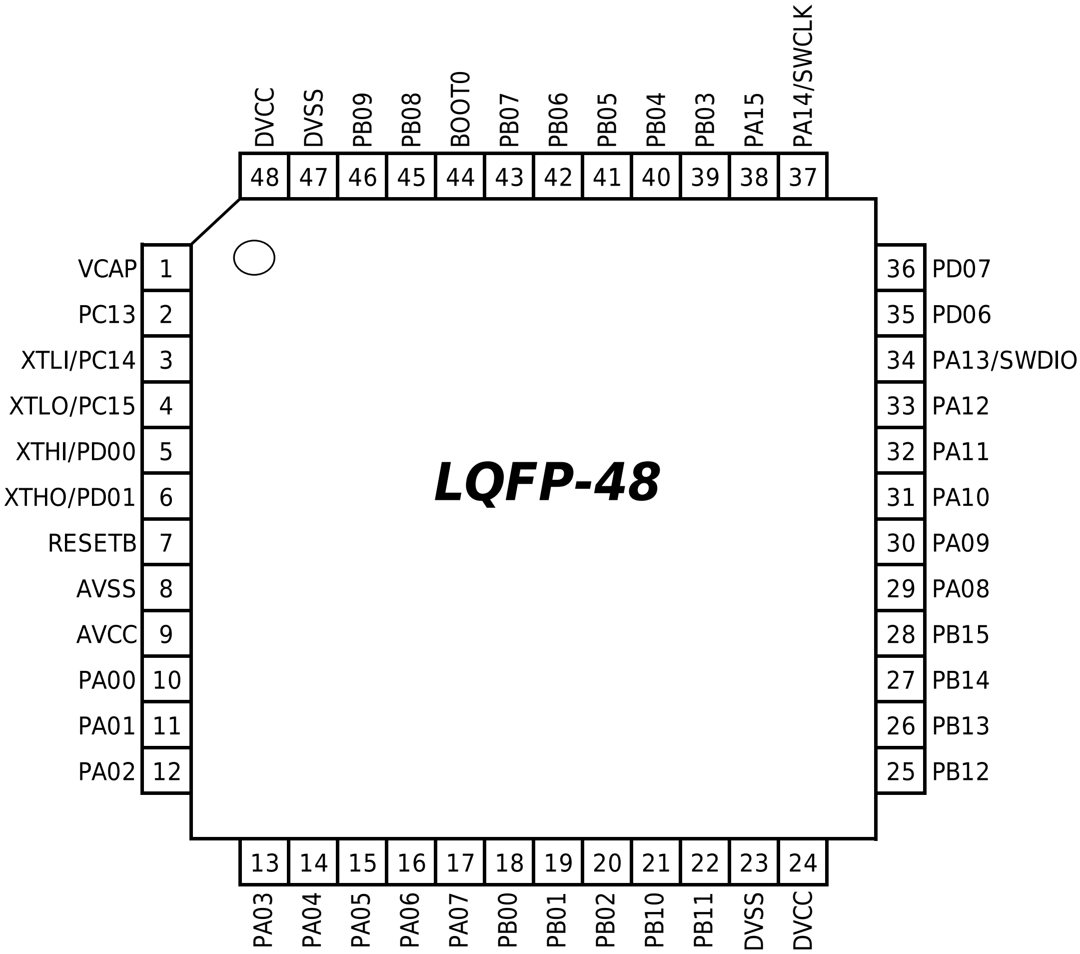
HC32F030K8TA



Note:

- ***The BOOT0 pin is used to control FLASH programming, see [Module Signal Description].***

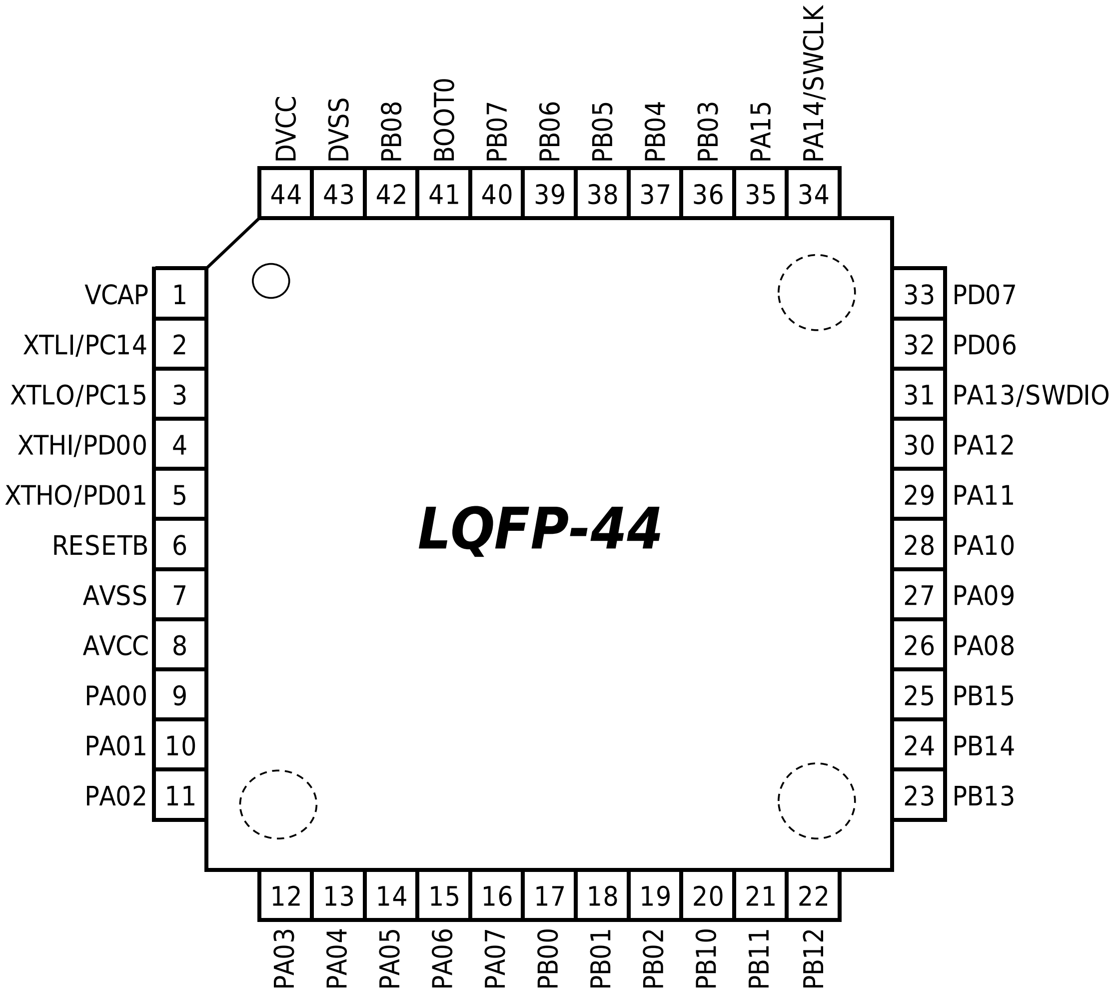
HC32F030J8TA



Note:

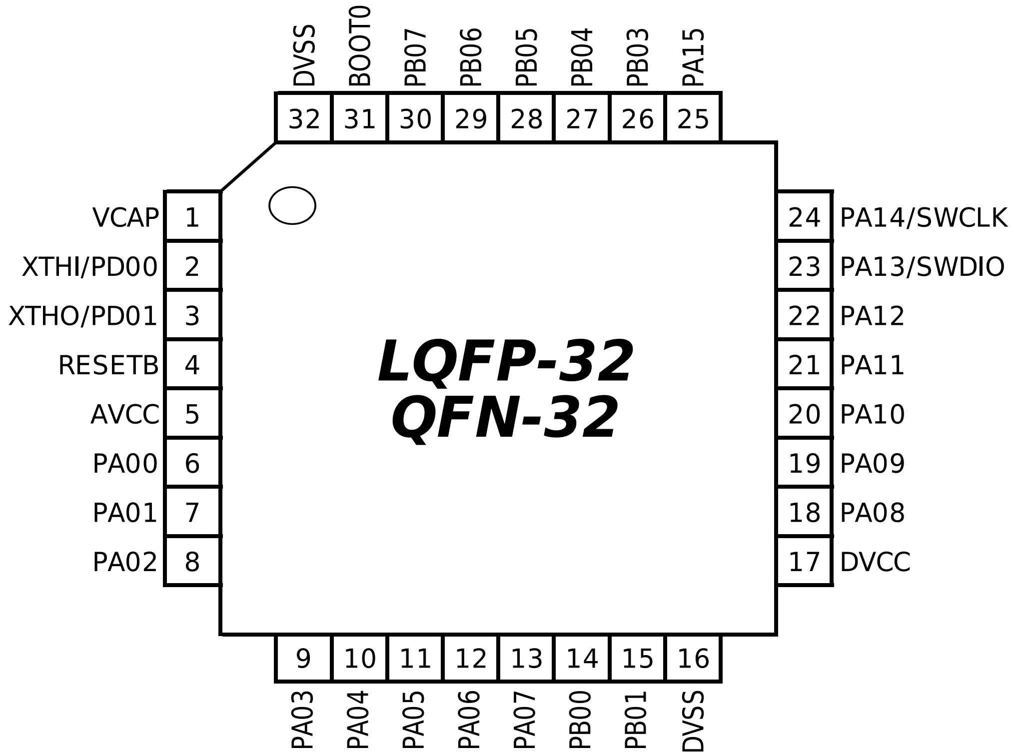
- ***In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.***
- ***For details on the IOs not brought out in this package, please refer to the [Pin Function Description].***
- ***The BOOT0 pin is used to control FLASH programming, see [Module Signal Description].***

HC32F030H8TA



Note:

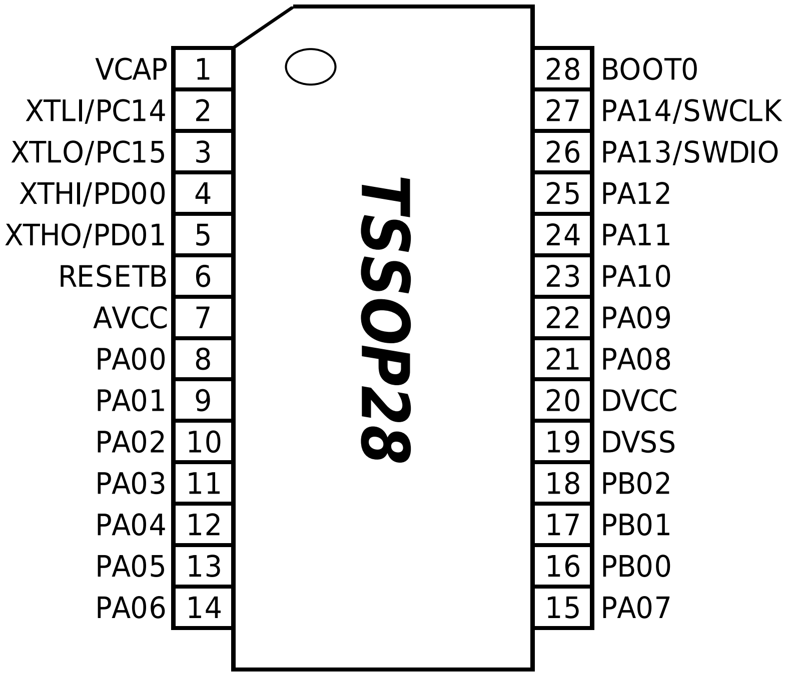
- ***In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.***
- ***For details on the IOs not brought out in this package, please refer to the [Pin Function Description].***
- ***The BOOT0 pin is used to control FLASH programming, see [Module Signal Description].***



Note:

- ***In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.***
- ***For details on the IOs not brought out in this package, please refer to the [Pin Function Description].***
- ***The BOOT0 pin is used to control FLASH programming, see [Module Signal Description].***

HC32F030E8PA



Note:

- ***In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.***
- ***For details on the IOs not brought out in this package, please refer to the [Pin Function Description].***
- ***The BOOT0 pin is used to control FLASH programming, see [Module Signal Description].***

3.2 Pin Function Description

64	48	44	32	28	NAME	DIGITAL	ANALOG
1	1	1	1	1	VCAP		
2	2				PC13	TIM3_CH1B	LVD_IN0
3	3	2		2	PC14		XTLI
4	4	3		3	PC15		XTLO
5	5	4	2	4	PD00	I2C0_SDA UART1_TXD	XTHI
6	6	5	3	5	PD01	I2C0_SCL TIM4_CHB UART1_RXD	XTHO
7	7	6	4	6	RESETB		
8					PC00	UART1_CTS	AIN10 VC0_INP0 VC1_INN0
9					PC01	TIM5_CHB UART1_RTS	AIN11 VC0_INP1 VC1_INN1
10					PC02	SPI1_MISO	AIN12 VC0_INP2 VC1_INN2
11					PC03	SPI1_MOSI	AIN13 VC0_INP3 VC1_INN3
12	8	7			AVSS		
13	9	8	5	7	AVCC		
14	10	9	6	8	PA00	UART1_CTS TIM0_ETR VC0_OUT TIM1_CHA TIM3_ETR TIM0_CHA	AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4
15	11	10	7	9	PA01	UART1_RTS TIM0_CHB TIM1_ETR TIM1_CHB HCLK_OUT SPI1_MOSI	AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5
16	12	11	8	10	PA02	UART1_TXD TIM0_CHA VC1_OUT TIM1_CHA TIM2_CHA PCLK_OUT SPI1_MISO	AIN2 VC0_INP6 VC0_INN2 VC1_INP2
17	13	12	9	11	PA03	UART1_RXD TIM0_GATE TIM1_CHB TIM2_CHB SPI1_CS TIM3_CH1A TIM5_CHA	AIN3 VC0_INP7 VC0_INN3 VC1_INP3
18					PD04		
19					PD05		
20	14	13	10	12	PA04	SPI0_CS UART1_TXD PCA_CH4	AIN4 VC0_INP8

64	48	44	32	28	NAME	DIGITAL	ANALOG
						TIM2_ETR TIM5_CHA LVD_OUT TIM3_CH2B	VC0_INN4 VC1_INP4
21	15	14	11	13	PA05	SPI0_CLK TIM0_ETR PCA_ECI TIM0_CHA TIM5_CHB XTL_OUT XTH_OUT	AIN5 VC0_INP9 VC0_INN5 VC1_INP5
22	16	15	12	14	PA06	SPI0_MISO PCA_CH0 TIM3_BK TIM1_CHA VC0_OUT TIM3_GATE	AIN6 VC0_INP10 VC0_INN6
23	17	16	13	15	PA07	SPI0_MOSI PCA_CH1 HCLK_OUT TIM3_CH0B TIM2_CHA VC1_OUT TIM4_CHB	AIN7 VC0_INP11 VC0_INN7
24					PC04	TIM2_ETR IR_OUT	AIN14 VC0_INN8
25					PC05	TIM6_CHB PCA_CH4	AIN15 VC0_INN9
26	18	17	14	16	PB00	PCA_CH2 TIM3_CH1B TIM5_CHB RCH_OUT RCL_OUT PLL_OUT	AIN8 VC0_INN10 VC1_INN6
27	19	18	15	17	PB01	PCA_CH3 PCLK_OUT TIM3_CH2B TIM6_CHB	AIN9/EXVREF VC1_INP6 VC1_INN7
28	20	19		18	PB02	PCA_ECI TIM4_CHA TIM1_BK TIM0_BK TIM2_BK	AIN16 VC1_INP7 VC1_INN8 OP2_INN
29	21	20			PB10	I2C1_SCL SPI1_CLK TIM1_CHA TIM3_CH1A UART1_RTS	AIN17 VC1_INP8 OP2_INP
30	22	21			PB11	I2C1_SDA TIM1_CHB TIM2_GATE TIM6_CHA UART1_CTS	AIN18 OP2_OUT
31	23		16	19	DVSS		
32	24		17	20	DVCC		
33	25	22			PB12	SPI1_CS TIM3_BK TIM0_BK TIM6_CHA	AIN19 VC1_INP9 OP1_INN
34	26	23			PB13	SPI1_CLK I2C1_SCL TIM3_CH0B	AIN20 VC1_INP10 OP1_INP

64	48	44	32	28	NAME	DIGITAL	ANALOG
						TIM1_CHA TIM1_GATE TIM6_CHB	
35	27	24			PB14	SPI1_MISO I2C1_SDA TIM3_CH1B TIM0_CHA TIM1_BK	AIN21 VC1_INP11 OP1_OUT
36	28	25			PB15	SPI1_MOSI TIM3_CH2B TIM0_CHB TIM0_GATE	AIN22 OP0_INN
37					PC06	PCA_CH0 TIM4_CHA TIM2_CHA	AIN23 OP0_INP
38					PC07	PCA_CH1 TIM5_CHA TIM2_CHB	OP0_OUT
39					PC08	PCA_CH2 TIM6_CHA TIM2_ETR	
40					PC09	PCA_CH3 TIM4_CHB TIM1_ETR	
41	29	26	18	21	PA08	UART0_TXD TIM3_CH0A TIM1_GATE TIM4_CHA TIM3_BK	
42	30	27	19	22	PA09	UART0_TXD TIM3_CH1A TIM0_BK I2C0_SCL HCLK_OUT TIM5_CHA	
43	31	28	20	23	PA10	UART0_RXD TIM3_CH2A TIM2_BK I2C0_SDA TIM2_GATE PCLK_OUT TIM6_CHA	
44	32	29	21	24	PA11	UART0_CTS TIM3_GATE I2C1_SCL VC0_OUT SPI0_MISO TIM4_CHB	
45	33	30	22	25	PA12	UART0_RTS TIM3_ETR I2C1_SDA VC1_OUT SPI0_MOSI	
46	34	31	23	26	PA13	IR_OUT UART0_RXD LVD_OUT TIM3_ETR SWDIO	
47	35	32			PD06	I2C1_SCL UART0_CTS	
48	36	33			PD07	I2C1_SDA UART0_RTS	
49	37	34	24	27	PA14	UART1_TXD	

64	48	44	32	28	NAME	DIGITAL	ANALOG
						UART0_TXD TIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT SWCLK	
50	38	35	25		PA15	SPI0_CS UART1_RXD TIM0_ETR TIM0_CHA TIM3_CH1A	
51					PC10	PCA_CH2	
52					PC11	PCA_CH3	
53					PC12	PCA_CH4	
54					PD02	PCA_ECI TIM1_ETR	
55	39	36	26		PB03	SPI0_CLK TIM0_CHB TIM1_GATE TIM3_CH0A XTL_OUT XTH_OUT	VC1_INN9
56	40	37	27		PB04	SPI0_MISO PCA_CH0 TIM2_BK UART0_CTS TIM2_GATE TIM3_CH0B	VC0_INP12 VC1_INP12 VC1_INN10
57	41	38	28		PB05	SPI0_MOSI TIM1_BK PCA_CH1 UART0_RTS	VC0_INP13 VC1_INP13
58	42	39	29		PB06	I2C0_SCL UART0_TXD TIM1_CHB TIM0_CHA TIM3_CH0A	VC0_INP14 VC1_INP14
59	43	40	30		PB07	I2C0_SDA UART0_RXD TIM2_CHB TIM0_CHB	VC0_INP15 VC1_INP15 LVD_IN2
60	44	41	31	28	PD03	BOOT0	
61	45	42			PB08	I2C0_SCL TIM1_CHA TIM2_CHA TIM0_GATE TIM3_CH2A UART0_TXD	LVD_IN1
62	46				PB09	I2C0_SDA IR_OUT SPI1_CS TIM2_CHA TIM2_CHB UART0_RXD	
63	47	43	32		DVSS		
64	48	44			DVCC		

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

PSEL	1	2	3	4	5	6	7
PA00	UART1_CTS		TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS		TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A			TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL		HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL		VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA		VC1_OUT	SPI0_MOSI	
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR			
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD		TIM0_ETR	TIM0_CHA	TIM3_CH1A	
PB00	PCA_CH2	TIM3_CH1B		TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB			
PB02		PCA_ECI		TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A		XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	
PB05	SPI0_MOSI		TIM1_BK	PCA_CH1			UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA		TIM3_CH0A	
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB		TIM0_CHB		
PB08	I2C0_SCL	TIM1_CHA		TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA		TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA		TIM3_CH1A		UART1_RTS
PB11	I2C1_SDA	TIM1_CHB		TIM2_GATE	TIM6_CHA		UART1_CTS
PB12	SPI1_CS	TIM3_BK		TIM0_BK			TIM6_CHA
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B		TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA			TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE			
PC00			UART1_CTS				
PC01		TIM5_CHB	UART1_RTS				
PC02	SPI1_MISO						
PC03	SPI1_MOSI						
PC04		TIM2_ETR	IR_OUT				

PSEL	1	2	3	4	5	6	7
PC05		TIM6_CHB	PCA_CH4				
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA				
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB				
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR				
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR				
PC10			PCA_CH2				
PC11			PCA_CH3				
PC12			PCA_CH4				
PC13			TIM3_CH1B				
PC14							
PC15							
PD00	I2C0_SDA		UART1_TXD				
PD01	I2C0_SCL	TIM4_CHB	UART1_RXD				
PD02	PCA_ECI		TIM1_ETR				
PD03							
PD04							
PD05							
PD06	I2C1_SCL		UART0_CTS				
PD07	I2C1_SDA		UART0_RTS				

3.3 Module Signal Description

Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	VCAP	LDO core power output (only for internal circuit use, external decoupling capacitor no less than 1 µF is required)
ISP	BOOT0	When reset, BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and FLASH can be programmed through ISP protocol. When reset, the BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in the FLASH, and the FLASH can be programmed through the SWD protocol.
ADC	AIN0~AIN23	ADC input channel 0-23
	ADC_VREF	ADC external reference voltage
	ADC_RDY	ADC Ready output signal
VC	VCIN0~VCIN15	VC input 0-15
	VC0_OUT	VC0 comparison output
	VC1_OUT	VC1 comparison output
LVD	LVDIN0	Voltage detection input 0
	LVDIN1	Voltage detection input 1
	LVDIN2	Voltage detection input 2
	LVD_OUT	Voltage detection output
OPA x=0,1,2	OPx_INN	OPA negative input
	OPx_INP	OPA positive input
	OPx_OUT	OPA output
UART x=0,1	UARTx_TXD	UARTx data transmitter
	UARTx_RXD	UARTx data receiver
	UARTx_CTS	UARTx CTS
	UARTx_RTS	UARTx RTS
SPI x=0,1	SPIx_MISO	SPI module host input and slave output data signal
	SPIx_MOSI	SPI module master output slave input data signal
	SPIx_SCK	SPI module clock signal
	SPIx_CS	SPI chip select
I2C x=0,1	I2Cx_SDA	I2C module data signal
	I2Cx_SCL	I2C module clock signal
General timer TIMx x=0,1,2	TIMx_CHA	Timer capture input compare output A
	TIMx_CHB	Timer's capture input compare output B
	TIMx_ETR	Timer's external count input signal
	TIMx_GATE	Timer gate signal
General timer	TIM3_CHyA	Timer capture input compare output A

Modules	Pin name	Description
TIM3 y=0,1,2	TIM3_CHyB	Timer's capture input compare output B
	TIM3_ETR	Timer's external count input signal
	TIM3_GATE	Timer gate signal
Programmable counting array PCA	PCA_ECI	External clock input signal
	PCA_CH0	Capture input/comparison output/PWM output 0
	PCA_CH1	Capture input/comparison output/PWM output 1
	PCA_CH2	Capture input/comparison output/PWM output 2
	PCA_CH3	Capture input/comparison output/PWM output 3
	PCA_CH4	Capture input/comparison output/PWM output 4
Advanced Timer	TIM4_CHA	Advanced Timer4 compare output/capture input A
	TIM4_CHB	Advanced Timer4 compare output/capture input B
	TIM5_CHA	Advanced Timer5 compare output/capture input A
	TIM5_CHB	Advanced Timer5 compare output/capture input B
	TIM6_CHA	Advanced Timer6 compare output/capture input A
	TIM6_CHB	Advanced Timer6 compare output/capture input B
	TIMTRIA	Hardware count clock input port or capture input port Hardware start, stop, clear condition input port, port selection refer to user manual advanced timer chapter register control
	TIMTRIB	
	TIMTRIC	
	TIMTRID	
	TIMBK	Brake input, port selection refer to user manual advanced timer chapter register control

Note:

- *The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.*

4 Block Diagram

Functional module

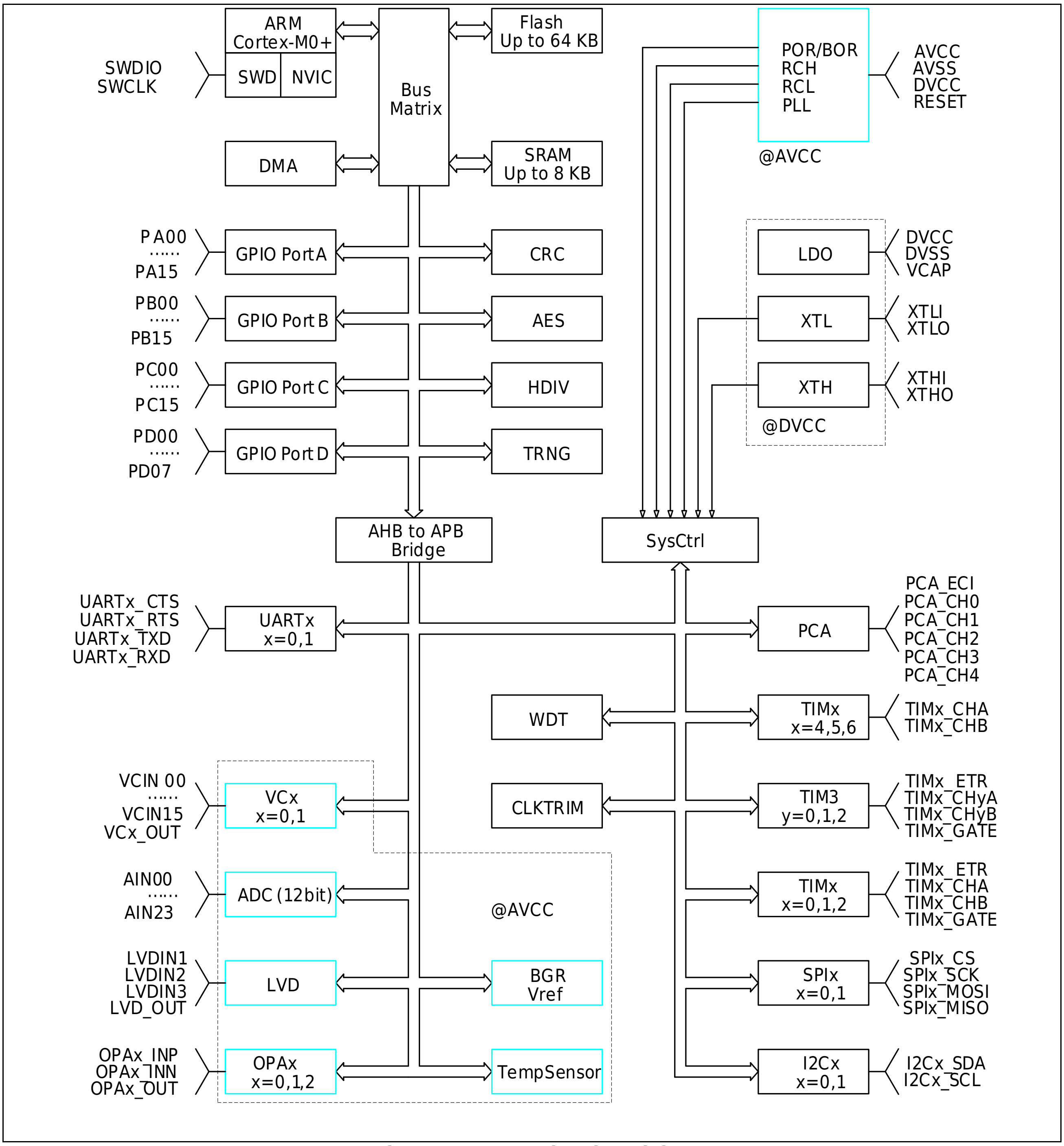
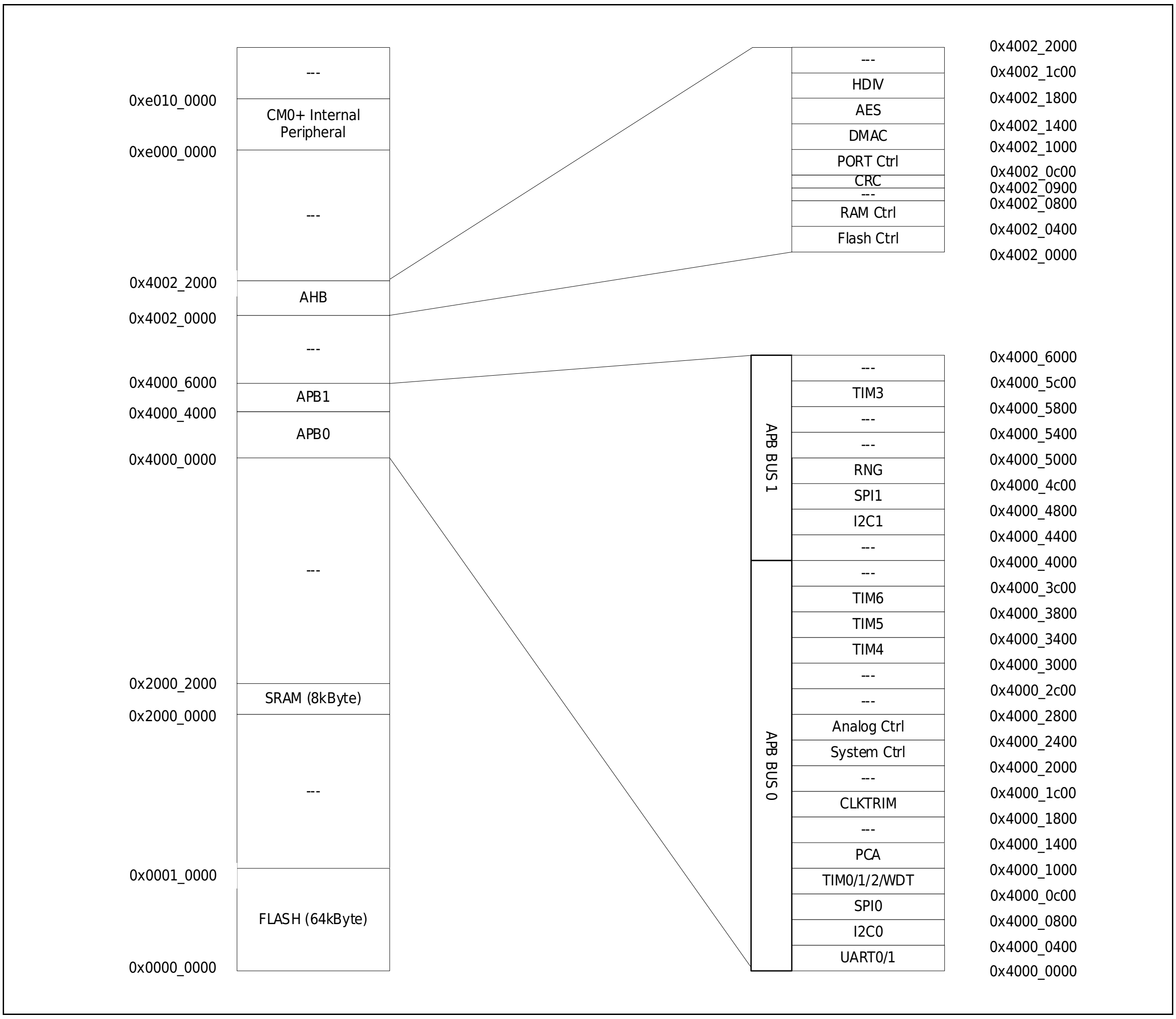
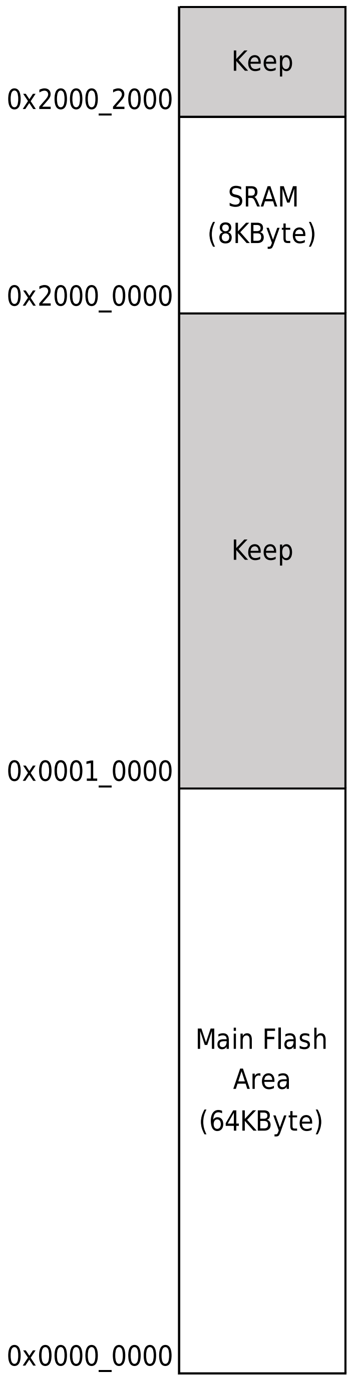


Figure 4-1 Functional modules

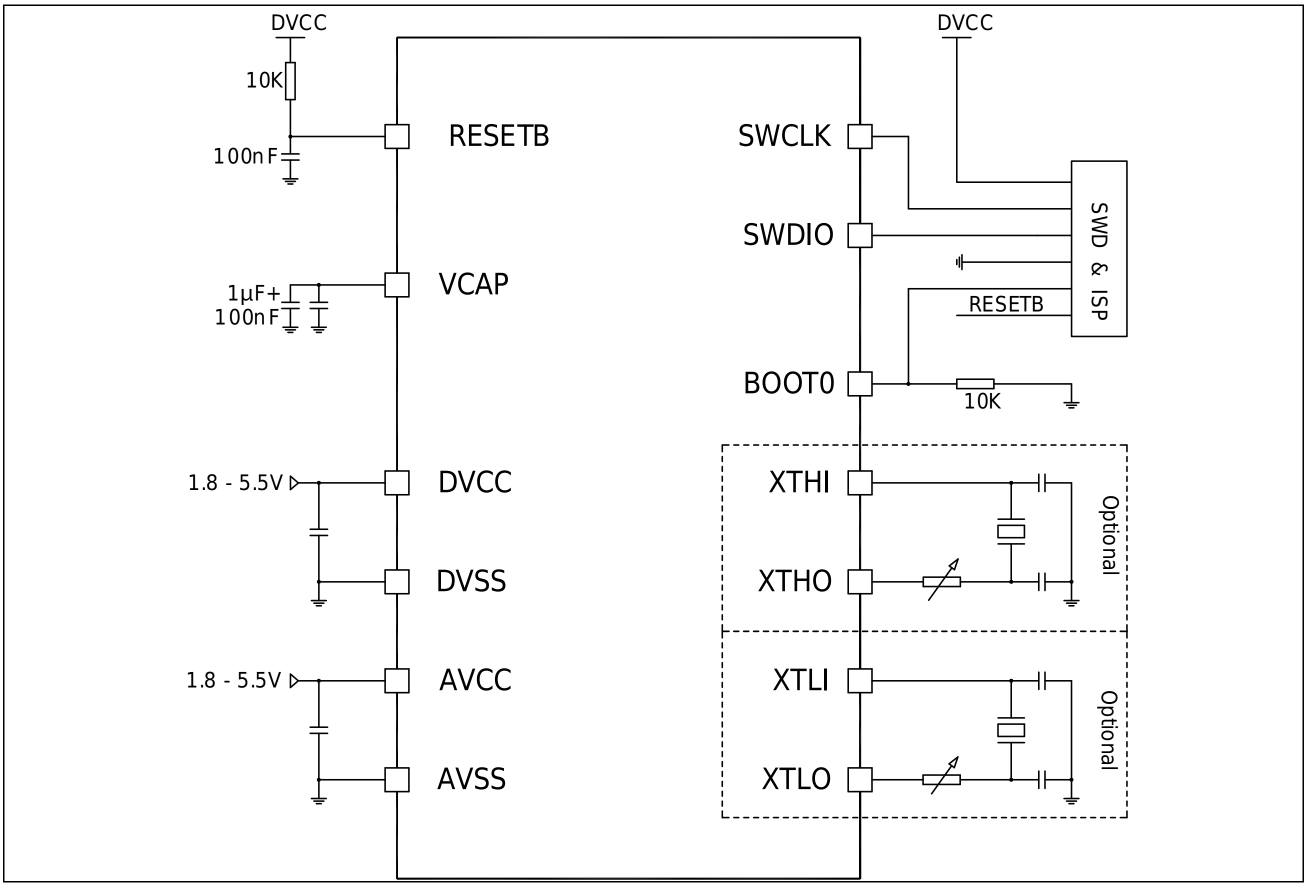
5 Storage Area Map



HC32F030K8TA HC32F030J8TA
HC32F030F8TA HC32F030F8UA
HC32F030E8PA HC32F030H8TA



6 Typical Application Circuit Diagram



Note:

- *AVCC and DVCC voltage must be the same.*
- *Each group of power supplies requires a decoupling capacitor, and the decoupling capacitor should be as close as possible to the corresponding power supply pin.*

7 Electrical Characteristics

7.1 Test Conditions

All voltages are referenced to VSS unless otherwise noted.

7.1.1 Minimum and Maximum Values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100 % of the products in the production line at ambient temperature T_A=25 °C and T_A=$T_A$max ($T_A$max matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3Σ).

7.1.2 Typical Value

Unless otherwise specified, typical data is based on T_A=25 °C and VCC=3.3V (1.8 V ≤ VCC ≤ 5.5 V voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95 % of the products is less than or equal to the given value (average ± 2Σ).

7.2 Absolute Maximum Ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins		50	mV
| VSSx - VSS |	Voltage difference between different ground pins		50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

Table 7-2 Voltage Characteristics

Symbol	Description	Max (1)	Unit
I_{VCC}	The total current (supply current) through the DVCC/AVCC power cord (1)	300	mA
I_{VSS}	The total current through the VSS ground wire (outflow current) (1)	300	mA
I_{IO}	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
$I_{INJ(PIN)}$(2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
$\sum I_{INJ(PIN)}$ (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the

instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	105	℃

7.3 Operating Conditions

7.3.1 General Working Conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	MHz
DVCC	Working voltage of digital part		1.8	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	1.8	5.5	V
P_D	Power dissipation T_A=85 ℃	LQFP64		455	mW
	Power dissipation T_A=85 ℃	LQFP48		364	mW
	Power dissipation T_A=85 ℃	LQFP32		357	mW
	Power dissipation T_A=85 ℃	TSSOP28		283	mW
T_A	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption (3)	-40	105	℃
T_J	Junction temperature range		-40	105	℃

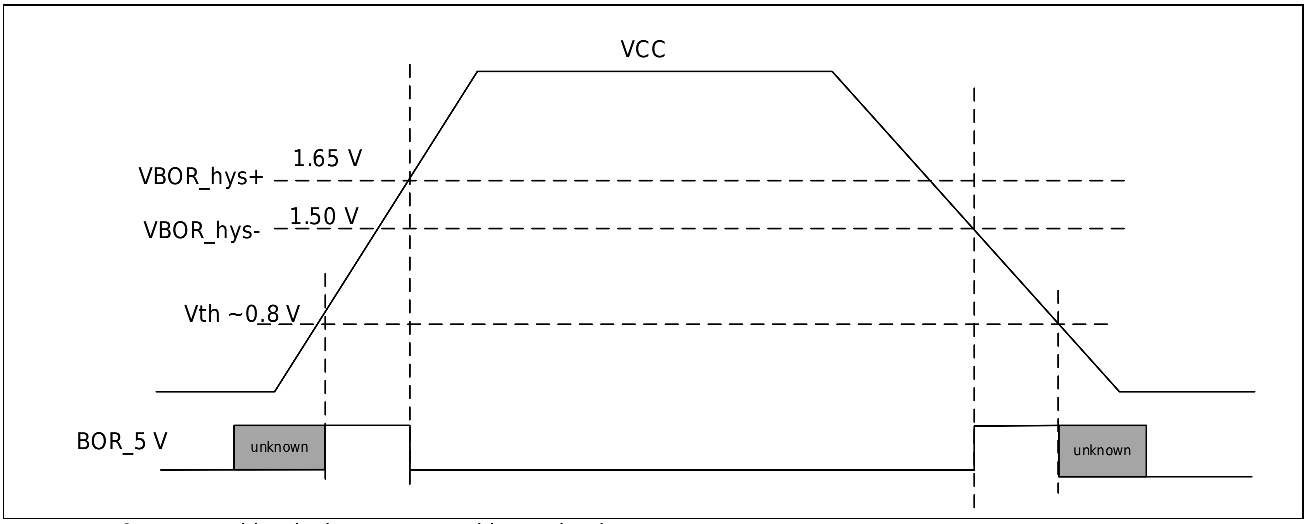
1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax} , T_A can be extended to this range.

7.3.2 Working Conditions at Power-up and Power-down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{VCC}	VCC rising rate		0	∞	μs/V
t_{VCC}	VCC falling rate		10	∞	μs/V

7.3.3 Embedded Reset and LVD Module Features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out Schematic

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{por}	POR release voltage (power-on process) BOR detection voltage (power-down process)		1.45	1.50	1.65	V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS=0001 LVD_CR.VTDS=0010 LVD_CR.VTDS=0011 LVD_CR.VTDS=0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111	1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2	1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3	1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4	V
Icomp	Power consumption			0.12		μA
Tresponse	Response time			80		μs
Tsetup	Establishment time			400		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.4 Built-in Reference Voltage

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5 V Reference Voltage	Room temperature 25°C 3.3 V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5 V Reference Voltage	-40~85 °C 2.8~5.5V	2.463	2.5	2.525	V[1]
V_{REF15}	Internal 1.5 V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5 V Reference Voltage	-40~85 °C 1.8~5.5V	1.477	1.5	1.519	V[1]
T_{Coeff}	Internal 2.5 V 1.5 V temperature coefficient	-40 ~ 85°C			120	ppm/°C

1. The data is based on the assessment results and is not tested in production.

7.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24 MHz, 1 wait cycle for 24~48 MHz).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$，$f_{PCLK1} = f_{HCLK}$.

Table 7-8 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V_{CAP}=1.5 V V_{CC}=3.3 V T_A=2xC	RCH clock source	4 M	655		μA
				8 M	1290		
				16 M	2470		
				22.12 M	3500		
				24 M	3790		
			PLL RCH4M to xxM clock source	32 M	5090		
				48 M	7580		
	All peripherals clock OFF, Run while(1) in RAM	V_{CAP}=1.5 V V_{CC}=3.3 V T_A=2xC	RCH clock source	4 M	270		μA
				8 M	510		
				16 M	950		
				22.12 M	1320		
				24 M	1420		
			PLL RCH4M to xxM clock source	32 M	1980		
				48 M	2920		
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	V_{CAP}=1.5 V V_{CC}=3.3 V T_A=2xC	RCH clock source	4 M	735		μA
				8 M	1415		
				16 M	2643		
				22.12 M	3573		
				24 M	3808		
			PLL RCH4M to xxM	48 M FlashWait=1	5815		
I_{DD} (Run mode)	All peripherals clock ON,	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	RCH clock source	4 M	1000	1300	μA
				8 M	1910	2420	
				16 M	3650	4590	

Symbol	Parameter	Conditions			Typ[1]	Max[2]	Unit
	Run while(1) in Flash			22.12 M	5080	6330	
				24 M	5440	6820	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH4M to xxM clock source	16 M	3960	4850	µA
				24 M	5700	7000	
				32 M FlashWait=1	6600	7480	
				40 M FlashWait=1	8140	9190	
				48 M FlashWait=1	9550	10860	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH8M to xxM clock source	16 M	4030	4940	µA
				24 M	5780	7060	
				32 M FlashWait=1	6670	7560	
				40M FlashWait=1	8240	9340	
				48 M FlashWait=1	9630	10970	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	RCH clock source	4 M	610	875	µA
				8 M	1330	1570	
				16 M	2110	2900	
				22.12 M	2860	3860	
				24 M	3060	4120	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH4M to xxM clock source	16 M	2360	3110	µA
				24 M	3360	4330	
				32 M FlashWait=1	3490	4010	
				40 M FlashWait=1	4240	4890	
				48M FlashWait=1	4910	5720	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH8M to xxM clock source	16 M	2430	3190	µA
				24 M	3420	4405	
				32 M FlashWait=1	3560	4090	
				40 M FlashWait=1	4320	4960	
				48 M FlashWait=1	4980	5760	
I_{DD} (Sleep mode)	All peripherals clock ON	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	RCH clock source	4 M	545	625	µA
				8 M	1060	1200	
				16 M	2030	2290	
				22.12 M	2870	3230	
				24 M	3100	3470	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH4M to xxM clock source	16 M	2280	2560	µA
				24 M	3350	3745	
				32 M FlashWait=1	4190	4690	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
				40 M FlashWait=1	5210	5830	
				48 M FlashWait=1	6210	6935	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH8M to xxM clock source	16 M	2340	2625	µA
				24 M	3410	3810	
				32 M FlashWait=1	4260	4760	
				40 M FlashWait=1	5290	5900	
				48 M FlashWait=1	6290	7020	
	All peripherals clock OFF	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	RCH clock source	4 M	155	190	µA
				8 M	280	338	
				16 M	500	586	
				22.12 M	680	800	
				24M	735	855	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH4M to xxM clock source	16 M	715	820	µA
				24 M	1005	1150	
				32 M FlashWait=1	1060	1210	
				40M FlashWait=1	1290	1470	
				48 M FlashWait=1	1520	1730	
		V_{CAP}=1.5 V V_{CC}=1.8-5.5 V T_A=N40C-85C	PLL RCH8M to xxM clock source	16 M	775	888	µA
				24 M	1060	1210	
				32 M FlashWait=1	1120	1280	
				40M FlashWait=1	1345	1530	
				48M FlashWait=1	1580	1800	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.5 V V_{CC}=1.8-5. 5V	XTL32K clock source Driver=0x0	T_A=N40-25C	15.3	20.5	µA
				T_A=50C	16	20.5	
				T_A=85C	19.3	25	
				T_A=105C	25.3	33	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V	XTL32K clock source Driver=0x0	T_A=N40-25C	12.1	17	µA
				T_A=50C	12.7	17	
				T_A=85C	16	21	
I_{DD} (LP Sleep)	All peripherals clock ON	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	10.6	11.2	µA
				T_A=50C	11	11.8	
				T_A=85C	14.2	16	
	All peripherals clock OFF	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V	XTL32K clock source Driver=0x0	T_A=N40-25C	7.4	7.7	µA
				T_A=50C	7.8	8.3	
				T_A=85C	11	12.7	
(DeepSleep)				T_A=N40-25C	5.8	6	µA

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
	XTL32K +DeepSleep	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V	XTL32K Driver=0x0	T_A=50C	6.2	6.5	
				T_A=85C	8.5	9.5	
	IRC32K +DeepSleep	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V		T_A=N40-25C	5.7	5.9	μA
				T_A=50C	6.1	6.4	
				T_A=85C	8.4	9.4	
	WDT +DeepSleep	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V		T_A=N40-25C	5.5	5.7	μA
				T_A=50C	5.9	6.1	
				T_A=85C	8.1	9.1	
	DeepSleep	V_{CAP}=1.5 V V_{CC}=1.8-5.5 V		T_A=N40-25C	5.4	5.6	μA
				T_A=50C	5.8	6	
				T_A=85C	8.1	9	

1. If there are no other specified conditions, the value of this Typ is measured at 25℃ & V_{CC} = 3.3 V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC} = 1.8-5.5 & Temperature = N40 – 85 ℃
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to Wake Up from Low Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time			1.8		μs
	Deep sleep wake-up time	F_{MCLK} = 4MHz		9.0		μs
		F_{MCLK} = 8MHz		6.0		μs
		F_{MCLK} = 16MHz		5.0		μs
		F_{MCLK} = 24MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External Timer Characteristic

7.3.7.1 External Input High-speed Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTH_ext}	User external clock frequency (1)		0	8	32	MHz
V_{XTHH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTHL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTH)}$	Rise time (1)				20	ns
$T_{f(XTH)}$	Falling time (1)				20	ns
$T_{w(XTH)}$	Enter high or low time (1)		16			ns
$C_{in(XTH)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		40		60	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

7.3.7.2 External Input Low-speed Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTL_ext}	User external clock frequency (1)		0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTLL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTL)}$	Rise time (1)				50	ns
$T_{f(XTL)}$	Falling time (1)				50	ns
$T_{w(XTL)}$	Enter high or low time (1)		450			ns
$C_{in(XTL)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		30		70	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

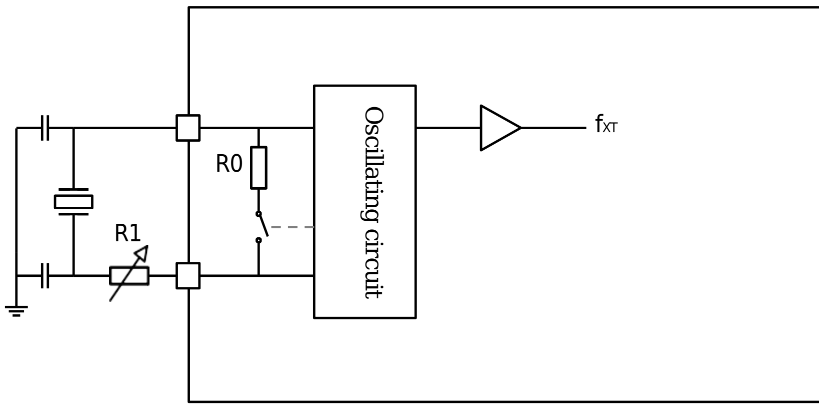
7.3.7.3 High-speed External Clock XTH

The high-speed external clock (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C_{LX}(3)	Load capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I_{dd}(4)	Current	XTH_CR [3:0] = 0b1111	-	1000	-	μA
		XTH_CR [3:0] = 0b1110	-	600	-	
		XTH_CR [3:0] = 0b1010	-	370	-	
		XTH_CR [3:0] =0b0110	-	300	-	
		XTH_CR [3:0] = 0b0010	-	160	-	
g_m	transconductance	XTH_CR [3:0] = 0b1111	-	11.75	-	mA/V
		XTH_CR [3:0] = 0b1110（32MHz，24MHz recommended value）	-	6.34	-	
		XTH_CR [3:0] = 0b1101	-	4.38	-	
		XTH_CR [3:0] = 0b1100	-	3.38	-	
		XTH_CR [3:0] = 0b1011	-	7.41	-	
		XTH_CR [3:0] = 0b1010（16MHz recommended value）	-	4.01	-	
		XTH_CR [3:0] = 0b1001	-	2.77	-	
		XTH_CR [3:0] = 0b1000	-	2.14	-	
		XTH_CR [3:0] = 0b0111	-	5.59	-	
		XTH_CR [3:0] = 0b0110（12MHz recommended value）	-	3.01	-	
		XTH_CR [3:0] = 0b0101	-	2.08	-	
g_m		XTH_CR [3:0] = 0b0100	-	1.60	-	mA/V

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
	transconductance	XTH_CR [3:0] = 0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010(8MHz recommended value)	-	1.30	-	
		XTH_CR [3:0] = 0b0001	-	0.93	-	
		XTH_CR [3:0] = 0b0000	-	0.72	-	
T_{start}(5)	Start time	32MHz，CL=16pF @ XTH_CR [3:0] = 0b1110	-	500	-	μs
		8MHz，CL=16pF @ XTH_CR [3:0] = 0b0010	-	2	-	ms

1. The characteristic parameters of the resonator are provided by the crystal/ceramic resonator manufacturer.
2. According to comprehensive evaluation, it is not tested in production.
3. CLX refers to the two pin load capacitors CL1 and CL2of XTAL. For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications and select crystals or resonators that meet the requirements. Usually, CL1and CL2have the same parameters. Crystal manufacturers typically provide the parameters of load capacitance in a serial combination of CL1and CL2. When selecting CL1and CL2, the frequency and ESR parameters of the crystal oscillator should be taken into account, and the capacitance impedance of the PCB and MCU pins should be taken into account.
4. The current varies with the choice of frequency and driving capability. The higher the frequency, the stronger the driving ability, and the greater the current consumption.
5. Tstart is the startup time, which is measured from the software enabling XTH until a stable oscillation of 32MHz/8MHz is obtained. This value was measured using a standard crystal resonator with XTH_CR [5:4] = 0b10 setting, and it may vary greatly depending on the crystal manufacturer and model.



Note：

- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
  If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.
- *The chip has integrated feedback resistor R0.*
- *Damping resistor R1 is optional, and the value of the resistance depends on the crystal characteristics, with a default value of 0 Ω.*

7.3.7.4 Low-speed External Clock XTL

The low-speed external clock (XTH) can be generated using a 32.768MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{Lx} (2)	Load capacitance	Configure as required by the crystal manufacturer.	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
I_{dd}(3)	Current	XTL_CR [3:0] =0b1111	-	1330	-	nA
		XTL_CR [3:0] =0b1011	-	1230	-	
		XTL_CR [3:0] =0b0111	-	1140	-	
		XTL_CR [3:0] =0b0011	-	1050	-	
		XTL_CR [3:0] =0b1110	-	630	-	
		XTL_CR [3:0] =0b1010 (recommended value)	-	580	-	
		XTL_CR [3:0] =0b0110	-	530	-	
		XTL_CR [3:0] =0b0010	-	490	-	
g_m	transconductance	XTL_CR [3:0] =0b1111	-	14.64	-	μA/V
		XTL_CR [3:0] =0b1011	-	13.17	-	
		XTL_CR [3:0] =0b0111	-	11.67	-	
		XTL_CR [3:0] =0b0011	-	10.15	-	
		XTL_CR [3:0] =0b1110	-	7.37	-	
		XTL_CR [3:0] =0b1010(recommended value)	-	6.62	-	
		XTL_CR [3:0] =0b0110	-	5.87	-	
		XTL_CR [3:0] =0b0010	-	5.10	-	
T_{start}(4)	Start time	ESR=30kΩ C_L=12pF XTL_CR [3:0] =0b1010	-	2000	-	ms

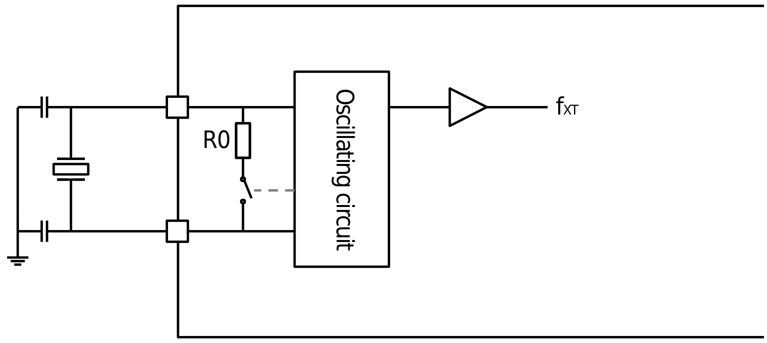
1. Based on comprehensive evaluation, it is determined that testing will not be conducted during production.
2. CLX refers to the load capacitance of the two pins of XTAL. Users suggest selecting the capacitance value of this capacitor according to the requirements of the crystal manufacturer.
   If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of

the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used。

Example：

When the crystal manufacturer provides a load capacitance of 8pF for the crystal, the capacitance value of the matching capacitor should be 16pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 15pF or 12pF.
When the crystal manufacturer provides a matching capacitance of 12pF for the crystal, the capacitance value of the matching capacitance should be 12pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 10pF or 8pF.

3. Choosing a high-quality oscillator with a smaller ESR value (such as MSIV-TIN32.768kHz) can optimize current consumption by adjusting the XTL_CR [3:0] setting. The current consumption is proportional to the transconductance gm) provided by the circuit。
4. Tstart is the startup time, which is measured from the software enabling XTL until a stable 32768Hz oscillation is obtained. This value was measured using a standard crystal resonator with XTL_CR [3:0]=0b1010 and XTL_CR [5:4]=0b11 settings, and it may vary greatly depending on the crystal manufacturer and model。



Note：

- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
- *If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.*
- *The chip has integrated feedback resistor R0.*

7.3.8 Internal Timer Characteristics

7.3.8.1 Internal RCH Oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions		0.25		%
		VCC = 1.8 ~ 5.5 V T_{AMB} = -40 ~ 85 °C	-3.5		+3.5	%
		VCC = 1.8 ~ 5.5 V T_{AMB} = -20 ~ 50 °C	-2.0		+2.0	%
F_{CLK}	Oscillation frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I_{CLK}	Power consumption	F_{MCLK} = 4 MHz		80		μA
		F_{MCLK} = 8 MHz		100		μA
		F_{MCLK} = 16 MHz		120		μA
		F_{MCLK} = 24 MHz		140		μA
DC_{CLK}	Duty Cycle (1)		45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL Oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions		0.5		%
		VCC = 1.8 ~ 5.5 V T_{AMB} = -40 ~ 85 °C	-5		+5	%
		VCC = 1.8 ~ 5.5 V T_{AMB} = -20 ~ 50 °C	-3		+3	%
F_{CLK}	Oscillation frequency			38.4 32.768		kHz
T_{CLK}	Start time			150		μs
DC_{CLK}	Duty Cycle (1)		25	50	75	%
I_{CLK}	Power consumption			0.35		μA

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.3 Internal Low-speed Clock 10k Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8		5.5	V
Dev	Oscillator accuracy (1)	VCC = 1.8 ~ 5.5 V T_{AMB} = -20 ~ 50 °C	-50	-	50	%
F_{CLK}	Oscillation frequency	VCC=3.3 V T_{AMB} = 25 °C		10		KHz

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 PLL Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Fin(1)	Input clock		4	4	24	MHz
	Input clock duty cycle		40		60	%
Fout	Output frequency		8	-	48	MHz
Duty(1)	Output duty cycle		48%	-	52%	
Tlock(1)	Lock time	Input frequency 4MHz	-	100	200	μs

1. Resulted from comprehensive evaluation, not tested in production.

7.3.10 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EC_{FLASH}	Erase times	Regulator voltage=1.5 V, T_{AMB} = 25 ℃	20			kcycles
RET_{FLASH}	Data retention period	T_{AMB} = 85 ℃, after 20 kcycles	20			Years
T_{b_prog}	Programming time (bytes)		22		30	μs
T_{w_prog}	Programming time (words)		40		52	μs
T_{p_erase}	Page erase time		4		5	ms
T_{m_erase}	Whole chip erase time		30		40	ms

7.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4A
EFT to Power (IEC61000-4-4)	Class:2A（4B)

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode			4		KV
$VESD_{CDM}$	ESD @ Charge Device Mode			1		KV
$VESD_{MM}$	ESD @ machine Mode			200		V
Ilatchup	Latch up current			100		mA

7.3.13 I/O Port Characteristics

7.3.13.1 Output Characteristics——Ports

Table 7-9 Port output characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 5 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing10 mA, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V_{OL}	Low level output voltage Sink Current	Sinking 6 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 15 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing10 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 20 mA, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 10 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 20 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V

NOTES:

1. *The maximum total current, I_{OH} (max) and I_{OL} (max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.*
2. *The maximum total current, I_{OH} (max) and I_{OL} (max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.*

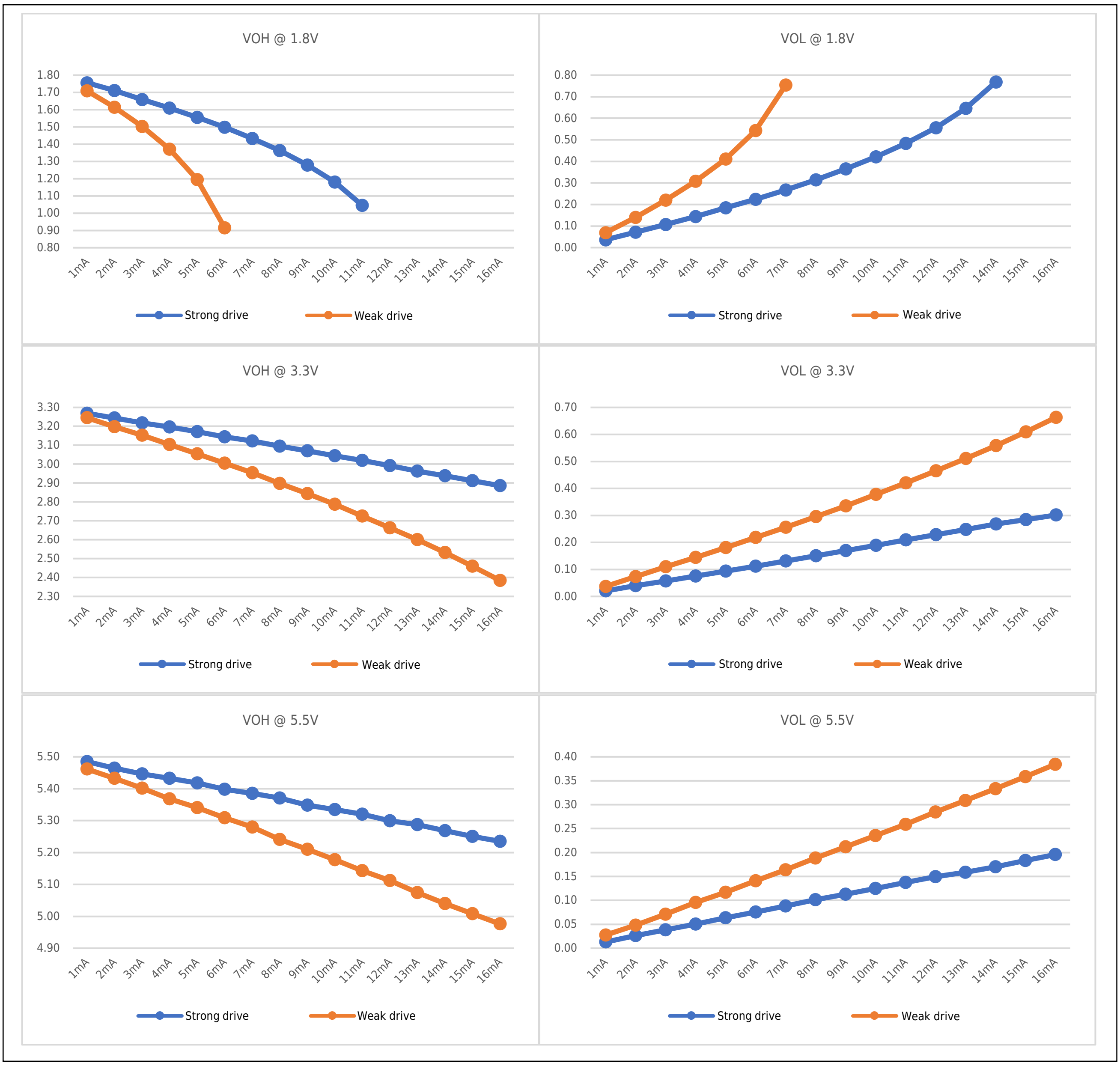


Figure 7-2 Output port VOH/VOL measured curve

7.3.13.2 Input Characteristics - Ports PA, PB, PC, PD

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8 V	0.7VCC			V
		VCC=3.3 V	0.7VCC			V
		VCC=5.5 V	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=1.8 V			0.3VCC	V
		VCC=3.3 V			0.3VCC	V
		VCC=5.5 V			0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IT+} - V_{IT-})	VCC=1.8 V		0.3		V
		VCC=3.3 V		0.4		V
		VCC=5.5 V		0.6		V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3 V		80		kΩ
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3 V		40		kΩ
C_{input}	Input capacitance			5		pf

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.3 Port External Input Sampling Requirements——Timer Gate/Timer Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8 V	30		ns
			3.3 V	30		ns
			5.5 V	30		ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8 V	0.5		μs
			3.3 V	0.5		μs
			5.5 V	0.5		μs
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8 V		PCLK/2	MHz
			3.3 V		PCLK/2	MHz
			5.5 V		PCLK/2	MHz
t(pca)(2)	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8 V		PCLK/8	MHz
			3.3 V		PCLK/8	MHz
			5.5 V		PCLK/8	MHz

NOTES:

1. *The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.*
2. *Based on comprehensive evaluation, not tested in production.*

7.3.13.4 Port Leakage Characteristics - PA, PB, PC, PD

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1,2)		±50		nA

NOTES:

1. *The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.*
2. *The port pin must be selected as input.*

7.3.14 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

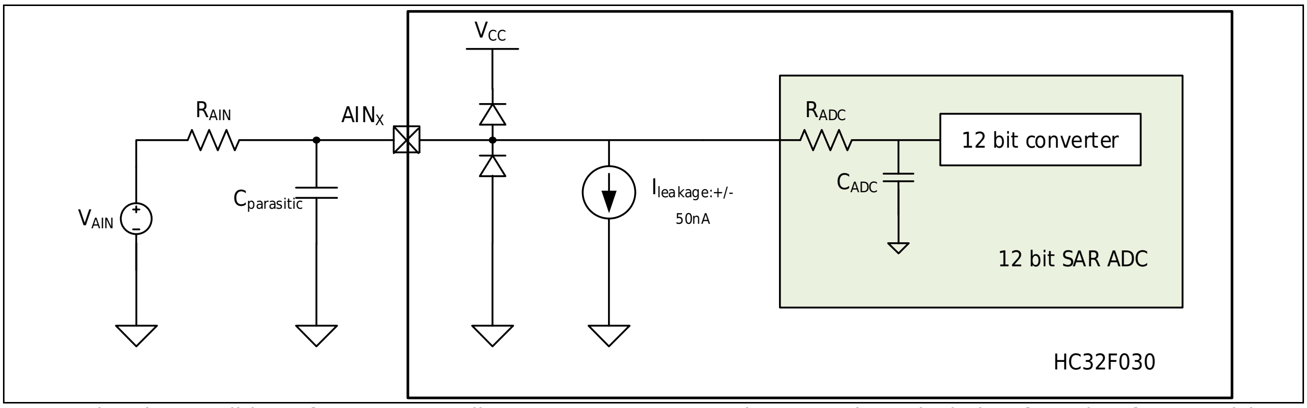
Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(RESETB)}$ (1)	Input low level voltage		-0.3		0.3VCC	V V
$V_{IH(RESETB)}$	Input high level voltage		0.7VCC		VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$		80		KΩ
$V_{F(RESETB)}$ (1)	Input filter pulse				2	µs
$V_{NF(RESETB)}$ (1)	Input unfiltered pulse		10			µs

1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0		AVCC	V
$DEV_{AVCC/3}$	AVCC/3 precision			3		%
I_{ADC1}	Active current including reference generator and buffer	200Ksps		2		mA
I_{ADC2}	Active current without reference generator and buffer	1Msps		0.5		mA
C_{ADCIN}	ADC input capacitance			16	19.2	pF
R_{ADC}(1)	ADC sampling switch impedance			1.5		KΩ
R_{AIN}(1)	ADC external input resistor(2)				100	KΩ
F_{ADCCLK}	ADC clock Frequency				24 M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			30		µs
$T_{ADCCONV}$	Conversion time		20	24	28	cycles
ENOB	Effective Bits	1Msps@VCC>=2.7 V 500Ksps@VCC>=2.4 V 200Ksps@VCC>=1.8 V REF=EXREF		10.3		Bit
		1Msps@VCC>=2.7 V 500Ksps@VCC>=2.4 V 200Ksps@VCC>=1.8 V REF=VCC		10.3		Bit
		200Ksps@VCC>=1.8 V REF=internal 1.5 V		9.4		Bit
		200Ksps@VCC>=2.8 V REF=internal 2.5 V		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7 V 500Ksps@VCC>=2.4 V 200Ksps@VCC>=1.8 V REF=EXREF		68.2		dB
		1Msps@VCC>=2.7 V 500Ksps@VCC>=2.4 V 200Ksps@VCC>=1.8 V REF=VCC		68.2		dB
		200Ksps@VCC>=1.8 V REF=internal 1.5 V		60		dB
		200Ksps@VCC>=2.8 V REF=internal 2.5 V		60		dB
DNL(1)	Differential non-linearity	200Ksps; VREF=EXREF/AVCC	-1		1	LSB
INL(1)	Integral non-linearity	200Ksps; VREF=EXREF/AVCC	-3		3	LSB
E_o	Offset error			0		LSB
E_g	Gain error			0		LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

Among them F_{ADC} is the ADC clock frequency, the register ADC_CR0<3:2> can set the relationship between it and PCLK, as shown in the following table:

The following table shows the ADC clock frequency F_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0<3:2>	**N**
00	1
01	2
10	4
11	8

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the relationship between sampling time t_{sa} and ADC clock frequency F_{ADC}:

ADC_CR0<13:12>	**M**
00	4
01	6
10	8
11	12

The following table shows the relationship between ADC clock frequency F_{ADC} and external resistance R_{AIN} (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} **(kΩ)**	F_{ADC}**(kHz)**
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{PARACITIC}$;
- In addition to considering R_{AIN} the value, if the internal resistance of the signal source V_{AIN} is large, it also needs to be considered.

7.3.16 VC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range		0		5.5	V
Vincom	Input common mode range		0		VCC-0.2	V
Voffset	Input offset	Normal temperature 25 °C 3.3 V	-10		+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20		μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Twarmup	From main bandgap enable to Temp sensor voltage, ADC internal 1.5 V, 2.5 V reference stable			20		μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.17 OPA Characteristic

OPA: (AVCC=2.2 V ~ 5.5 V, AVSS=0 V, Ta=- 40 °C ~ +85 °C)

Symbol	Parameter	Operating Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vi	Input voltage		0	-	AVCC	V
Vo	Output voltage (1)		0.1	-	AVCC-0.1	V
Io	Output current (1)				0.5	mA
RL	Load resistance (1)		10K			Ohm
Tstart	Initialization time (2)				20	μs
Vio	Input offset voltage	Vic=AVCC/2, Vo=AVCC/2, RL=10 kΩ, Rs=50 Ω		±6		mV
PM	Phase Range(1)	RL=10 kΩ, CL=20 pF		65	-	deg
GM	Gain Range(2)	RL=10 kΩ, CL=20 pF		15	-	dB
UGBW	Unity gain bandwidth (1)	CL=20 pF		2.5		MHz
SR	Slew rate (1)	CL=15 pF		2.6		V/μs
CMRR	Common Mode Rejection Ratio(1)			70		dB

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR<0>=1 at the same time.

7.3.18 TIM Timer Features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ADVTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs
T_{MAX_COUNT}	Maximum possible count			67108864	t_{TIMCLK}
		f_{TIMCLK}=48MHz		1.4	s

1. Guaranteed by design, not tested in production.

Table 7-11 General Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
		Mode 0 free counting		32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count (reload mode)			16777216	t_{TIMCLK}
		f_{TIMCLK}=48MHz		349.5	ms

1. Guaranteed by design, not tested in production.

Table 7-12 PCA Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count			2097152	t_{TIMCLK}
		f_{TIMCLK}=48MHz		43.69	ms

1. Guaranteed by design, not tested in production.

Table 7-13 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

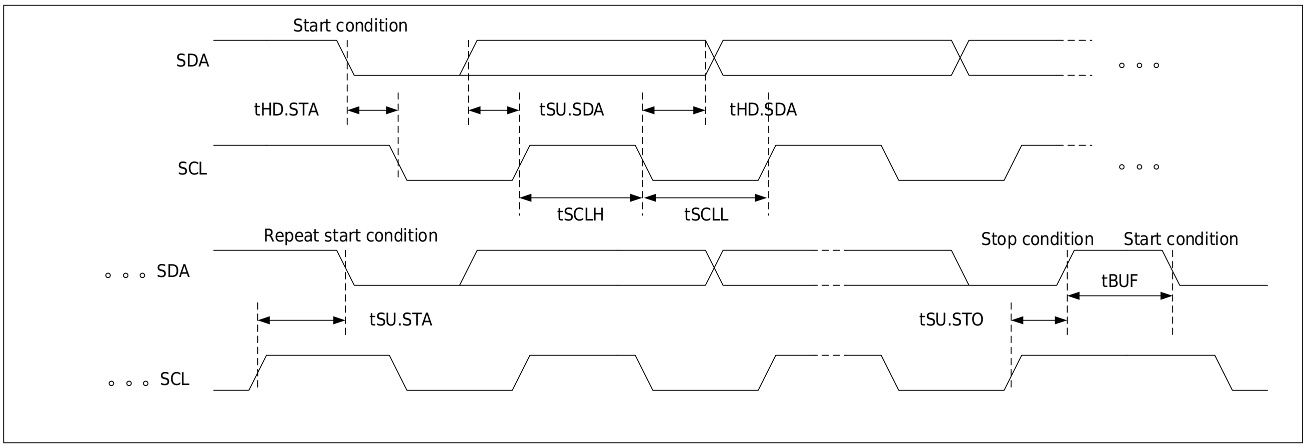
7.3.19 Communication Interface

7.3.19.1 I2C Features

I2C interface characteristics are as follows:

Table 7-14 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100 K)		Fast mode (400 K)		High speed mode (1 M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7		1.25		0.5		µs
t_{SCLH}	SCL clock high time	4.0		0.6		0.26		µs
$t_{SU.SDA}$	SDA establishment time	250		100		50		ns
$t_{HD.SDA}$	SDA hold time	0		0		0		µs
$t_{HD.STA}$	Start condition hold time	2.5		0.625		0.25		µs
$t_{SU.STA}$	Repeated start condition establishment time	2.5		0.6		0.25		µs
$t_{SU.STO}$	Stop condition establishment time	0.25		0.25		0.25		µs
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		µs



1. Guaranteed by design, not tested in production.

Figure 7-3 I2C Interface Timing

7.3.19.2 SPI Features

Table 7-15 SPI Interface Features[1][2]

Symbol	Parameter	Conditions	Minimum value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period[3]	Host Transmit Mode f_{PCLK} = 32MHz	62.5	-	ns
		Host Receive Mode f_{PCLK} = 48MHz	160	-	ns
		Slave Transmit Mode f_{PCLK} = 48MHz	160	-	ns
		Slave Receive Mode f_{PCLK} = 48MHz	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output	-	-	3	ns
$t_{h(MO)}$	Hold time of host data output	-	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$1.5*T_{pclk}+20$	ns
$t_{h(SO)}$	Hold time of slave data output	-	$0.5*T_{pclk}+10$	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

1. Guaranteed by design and not tested in production.
2. The data is based on the condition of VCC = 3.0 V.
3. The maximum prescaler factor in host mode is PCLK/2, and in slave mode, it is PCLK/4.

The waveform and timing parameters of the SPI interface signal are as follows:

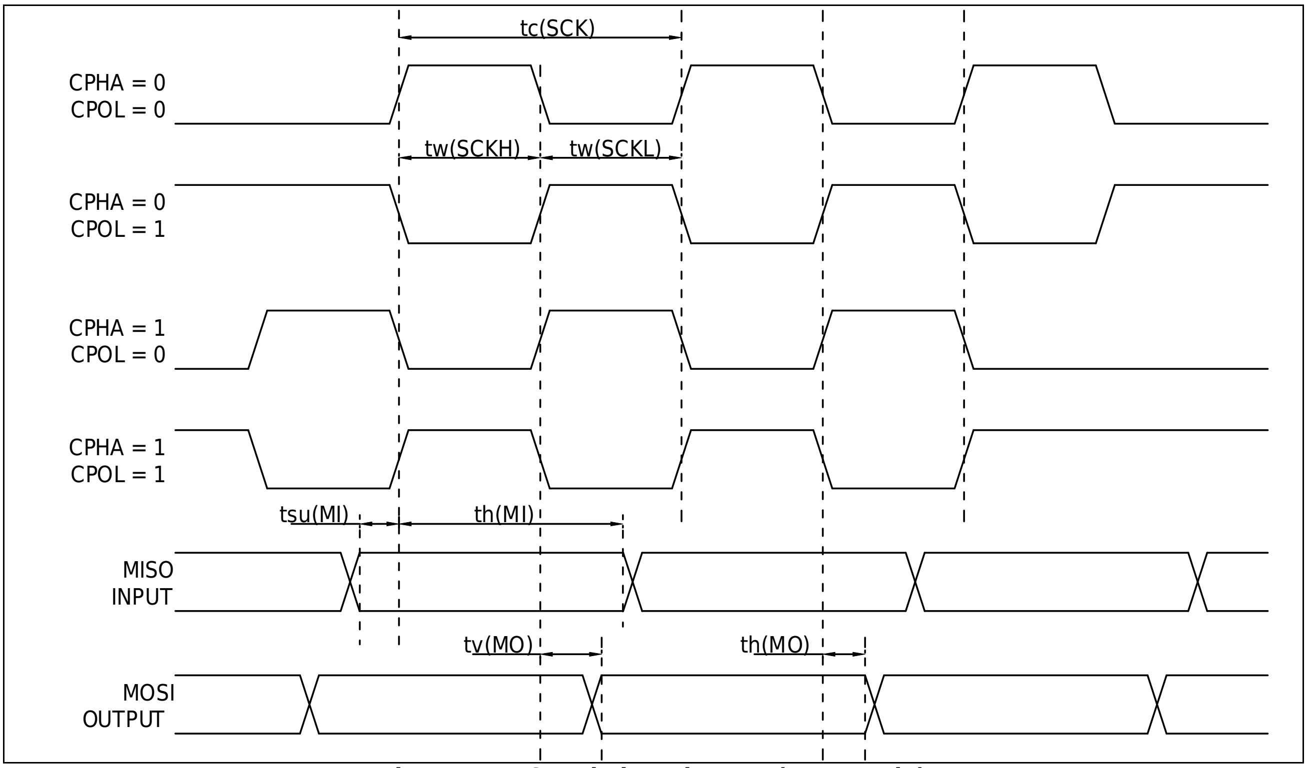


Figure 7-4 SPI Timing Diagram (Host Mode)

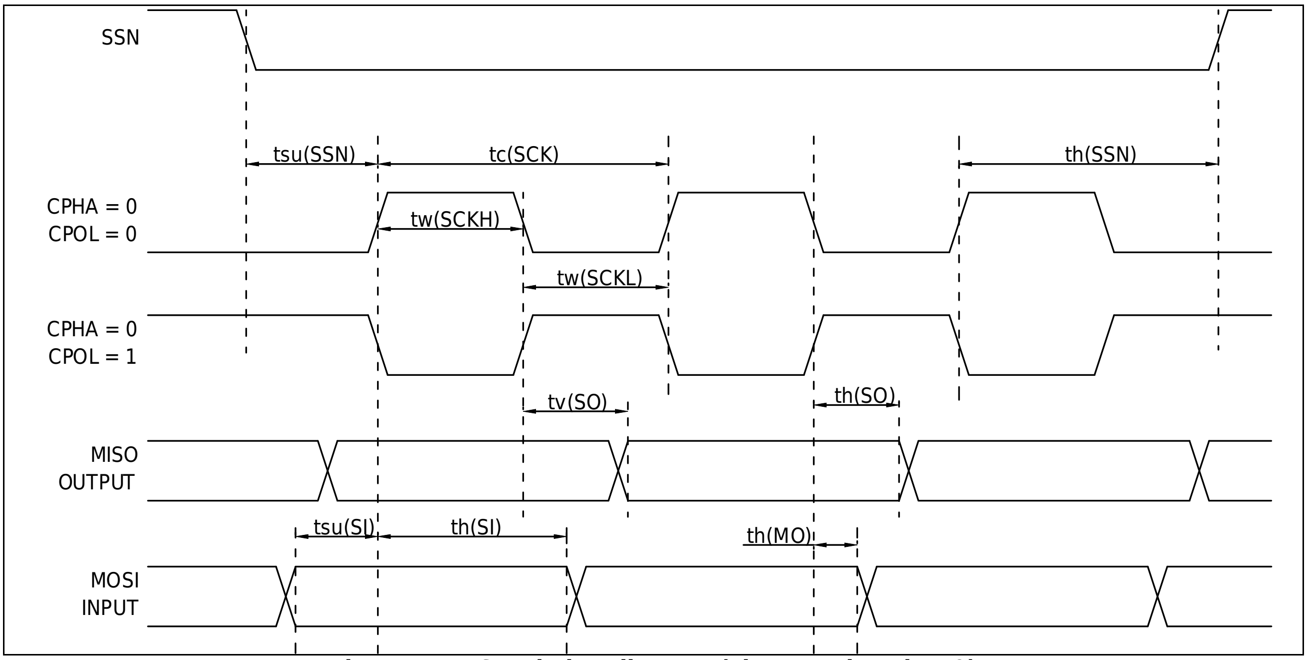


Figure 7-5 SPI timing diagram (slave mode cpha=0)

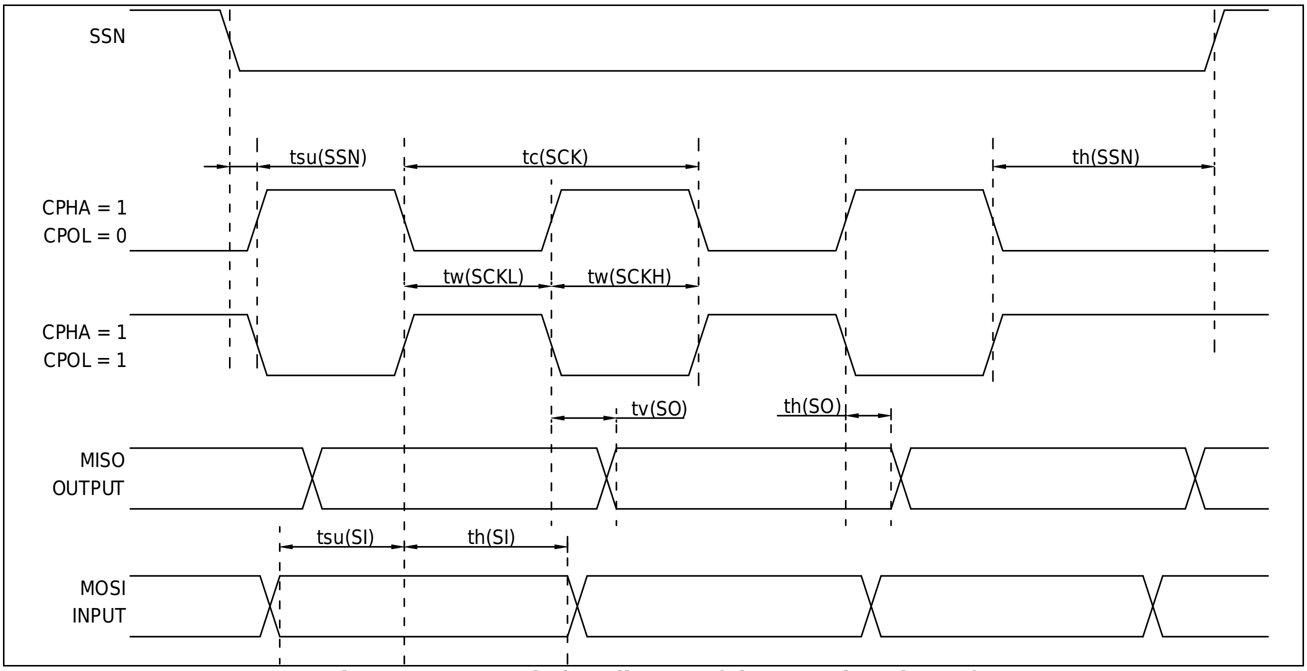
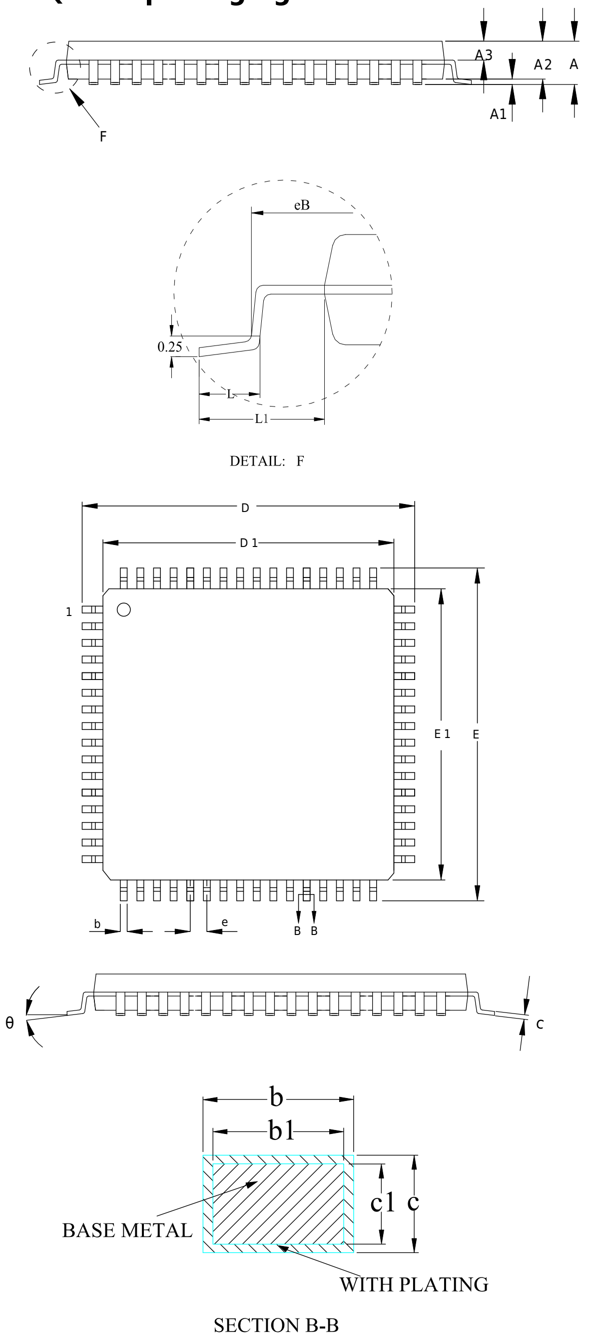


Figure 7-6 SPI timing diagram (slave mode cpha =1)

8 Packaging Information

8.1 Packaging Size

LQFP64 packaging

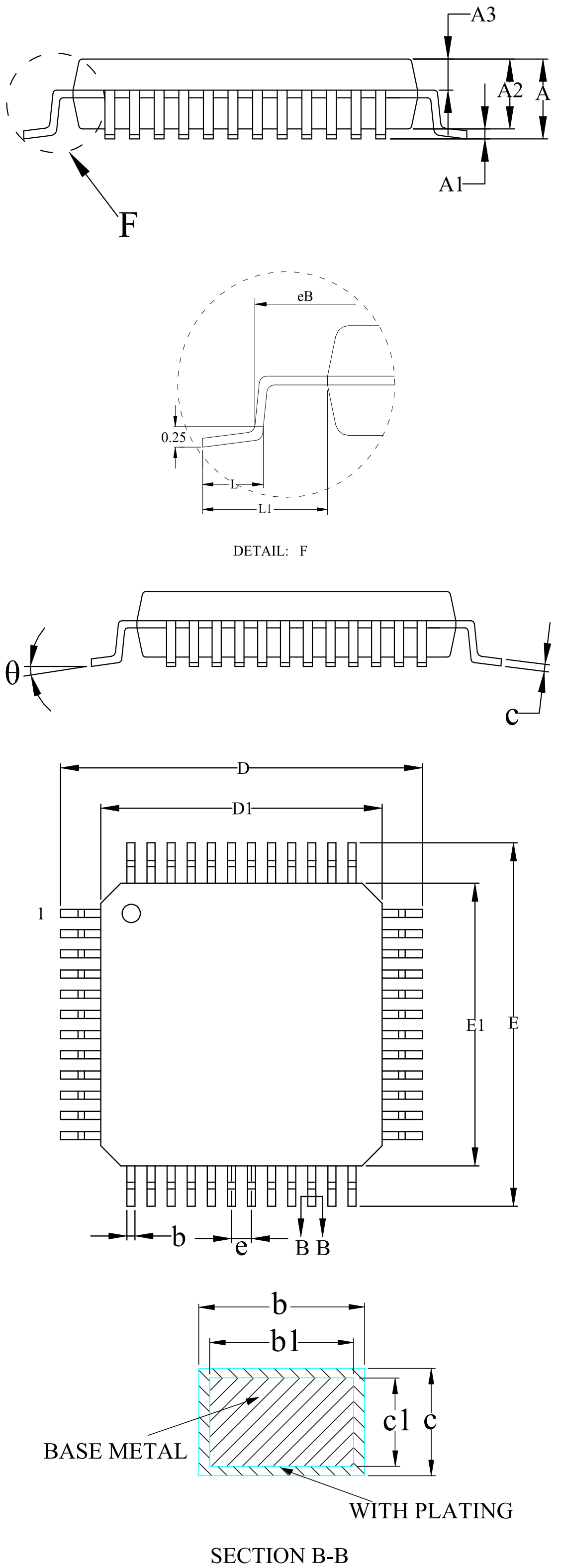


Symbol	10x10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0°	--	7°

NOTE:

- ***Dimensions "D1" and "E1" do not include mold flash.***

LQFP48 packaging

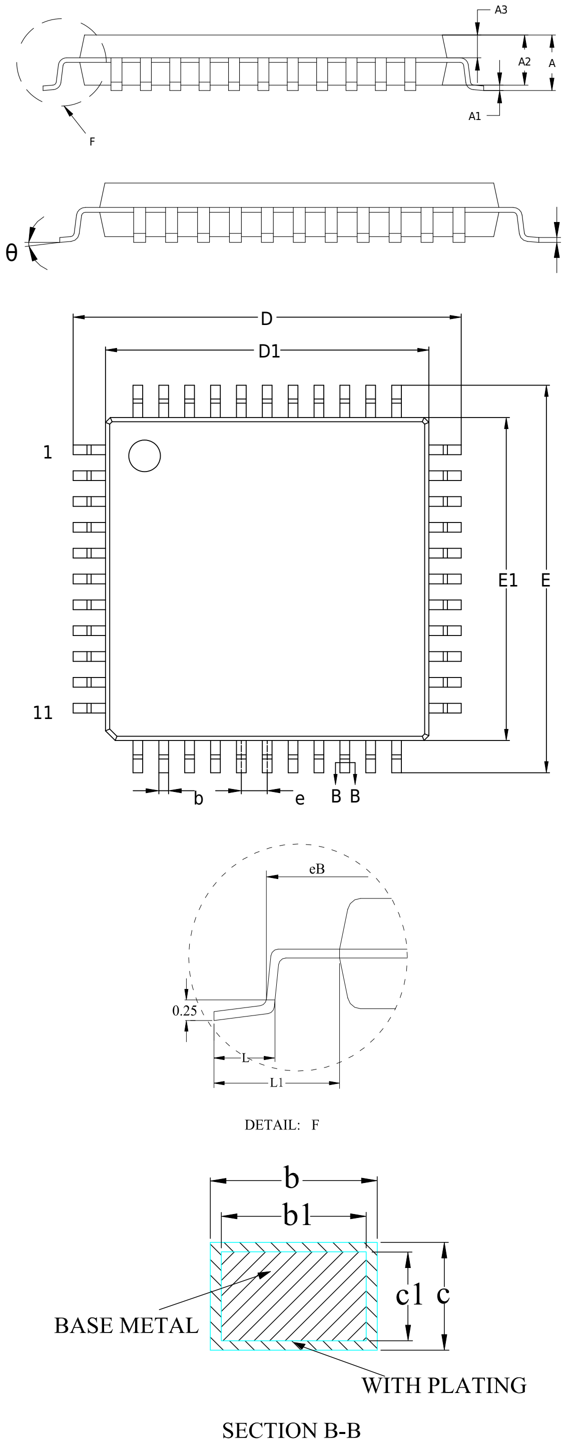


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.50BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

NOTE:

- ***Dimensions "D1" and "E1" do not include mold flash.***

LQFP44 packaging

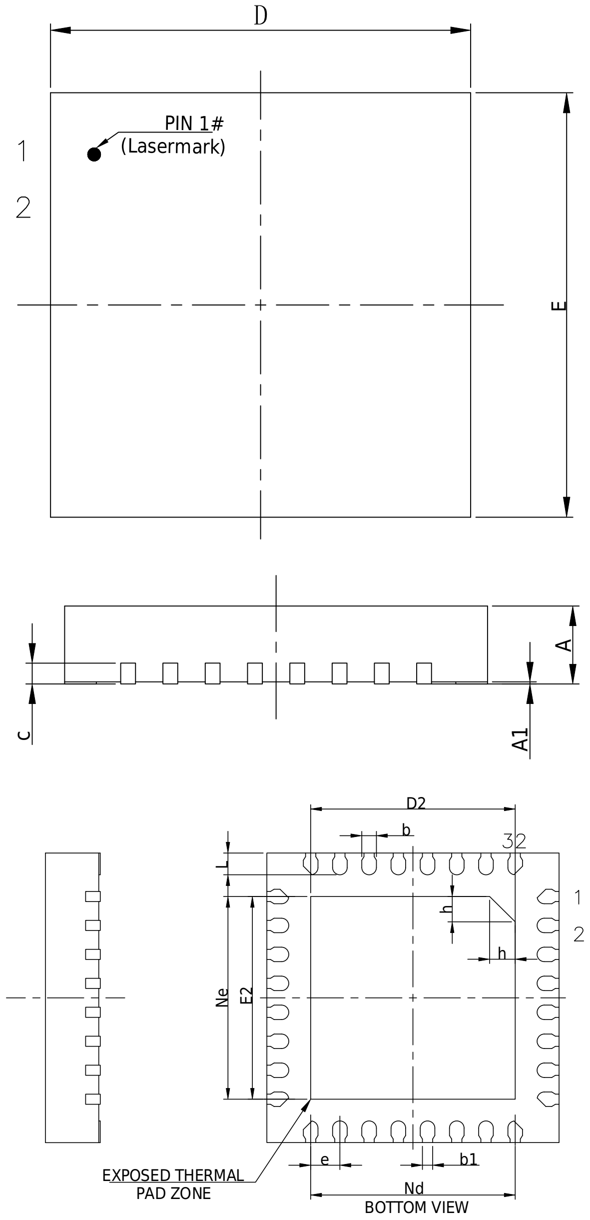


Symbol	10x10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	--	0.36
b1	0.27	0.30	0.33
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	--	11.25
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

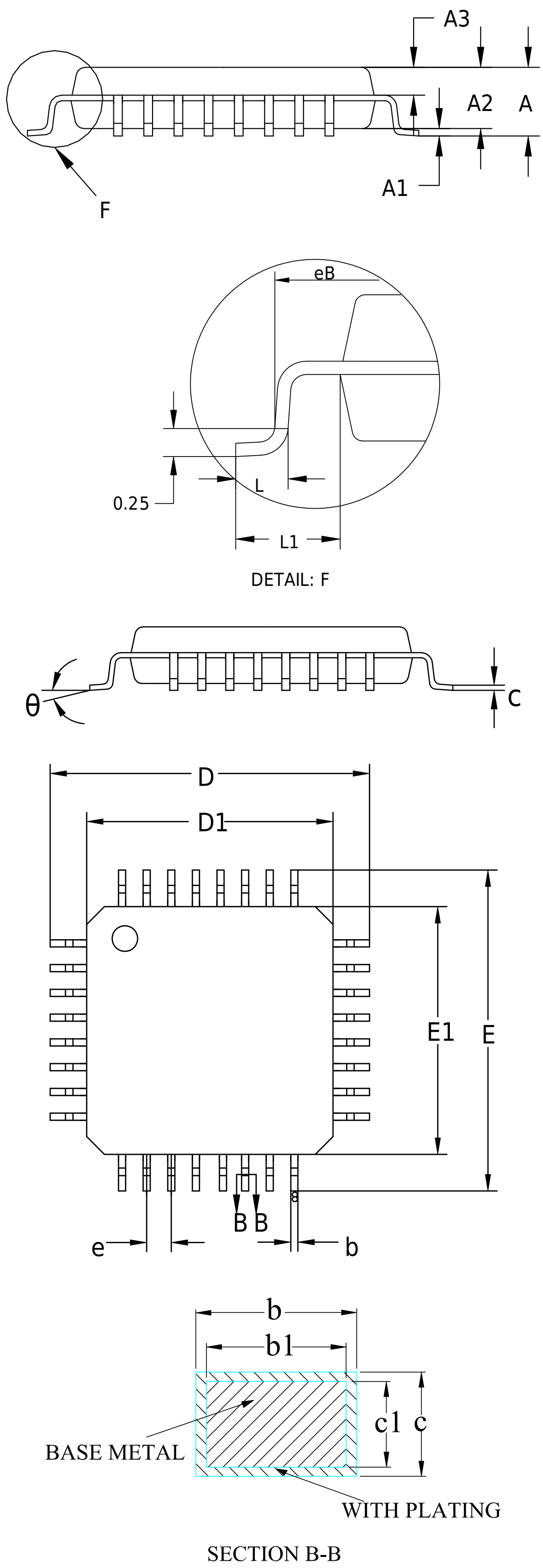
- ***Dimensions "D1" and "E1" do not include mold flash.***

QFN32 packaging



Symbol	5x5 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
e	0.50BSC		
Ne	3.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F Carrier Dimensions	4.10 x 4.10		

LQFP32 packaging

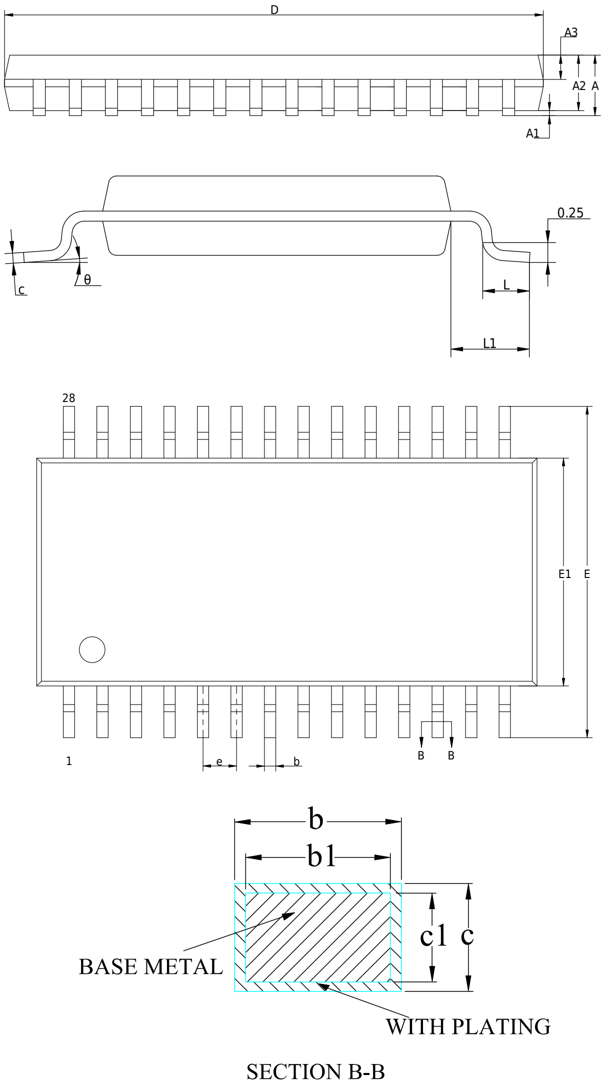


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	--	0.41
b1	0.32	0.35	0.38
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0°	--	7°

NOTE:

- ***Dimensions "D1" and "E1" do not include mold flash.***

TSSOP28 packaging



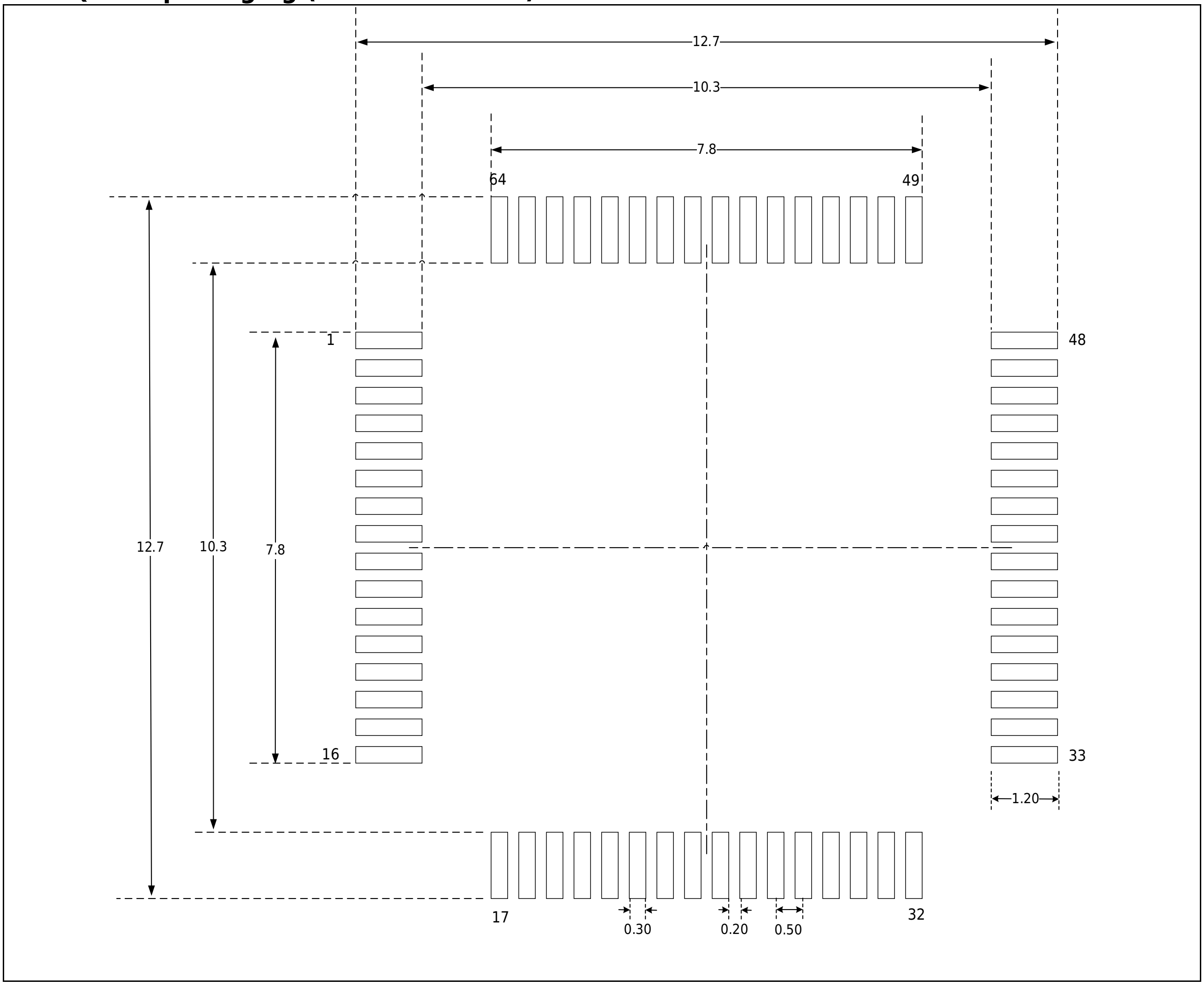
Symbol	Millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	--	1.00
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	--	8°

NOTE:

- ***Dimensions “D” and “E1” do not include mold flash.***

8.2 Schematic Diagram of Pad

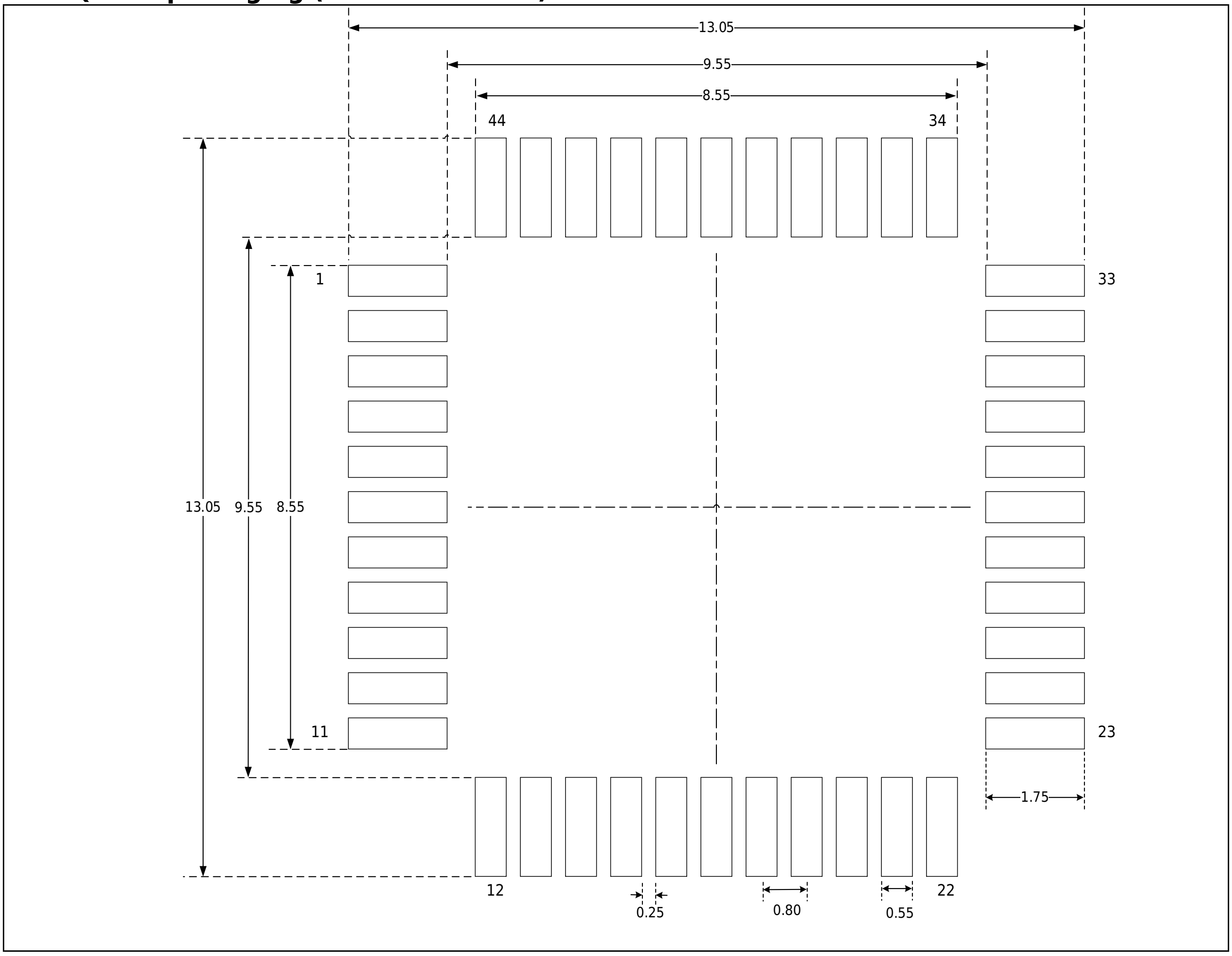
LQFP64 packaging (10 mm x 10 mm)



NOTE:

- ***Dimensions are expressed in millimeters.***
- ***Dimensions are for reference only.***

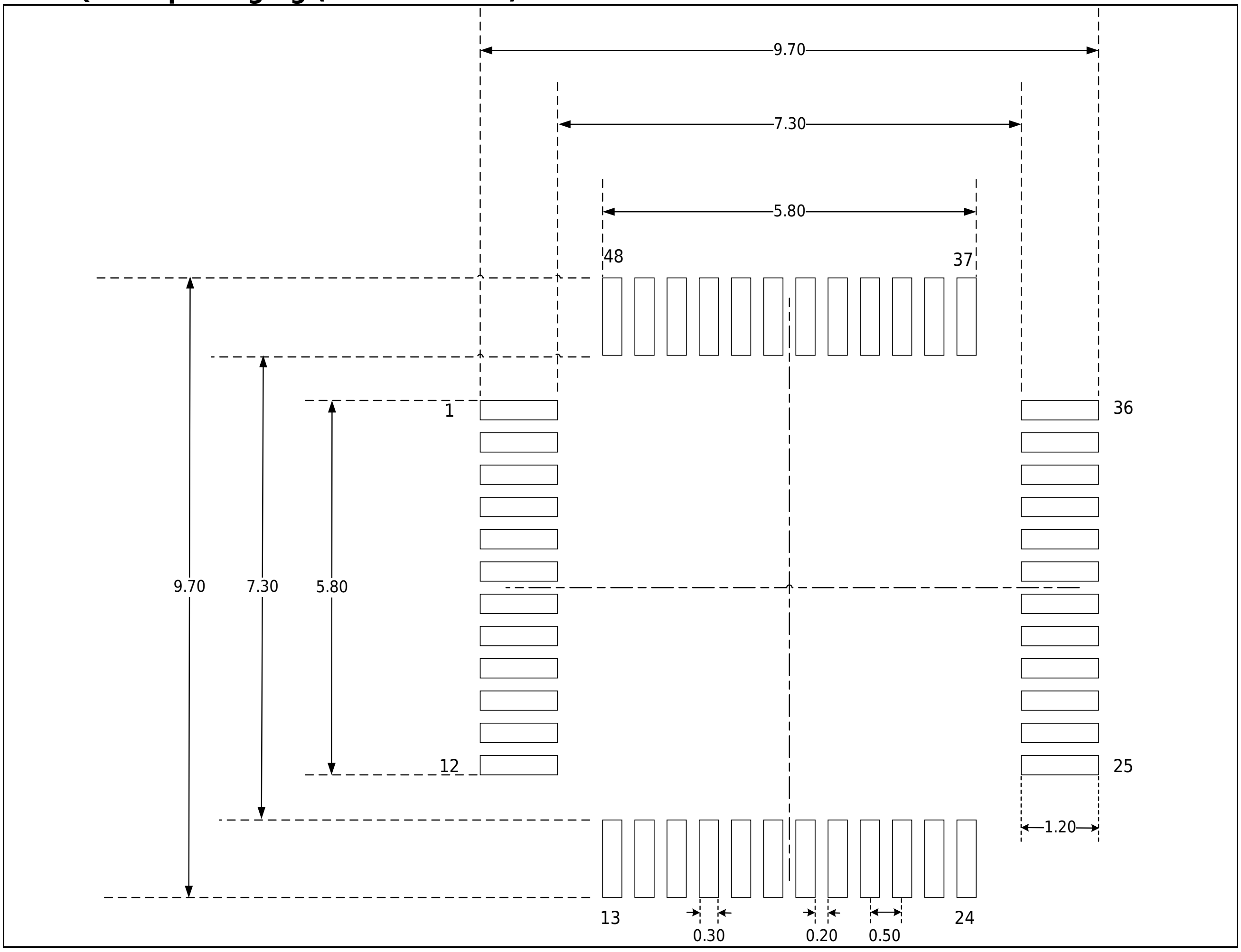
LQFP44 packaging (10 mm x 10 mm)



NOTE:

- ***Dimensions are expressed in millimeters.***
- ***Dimensions are for reference only.***

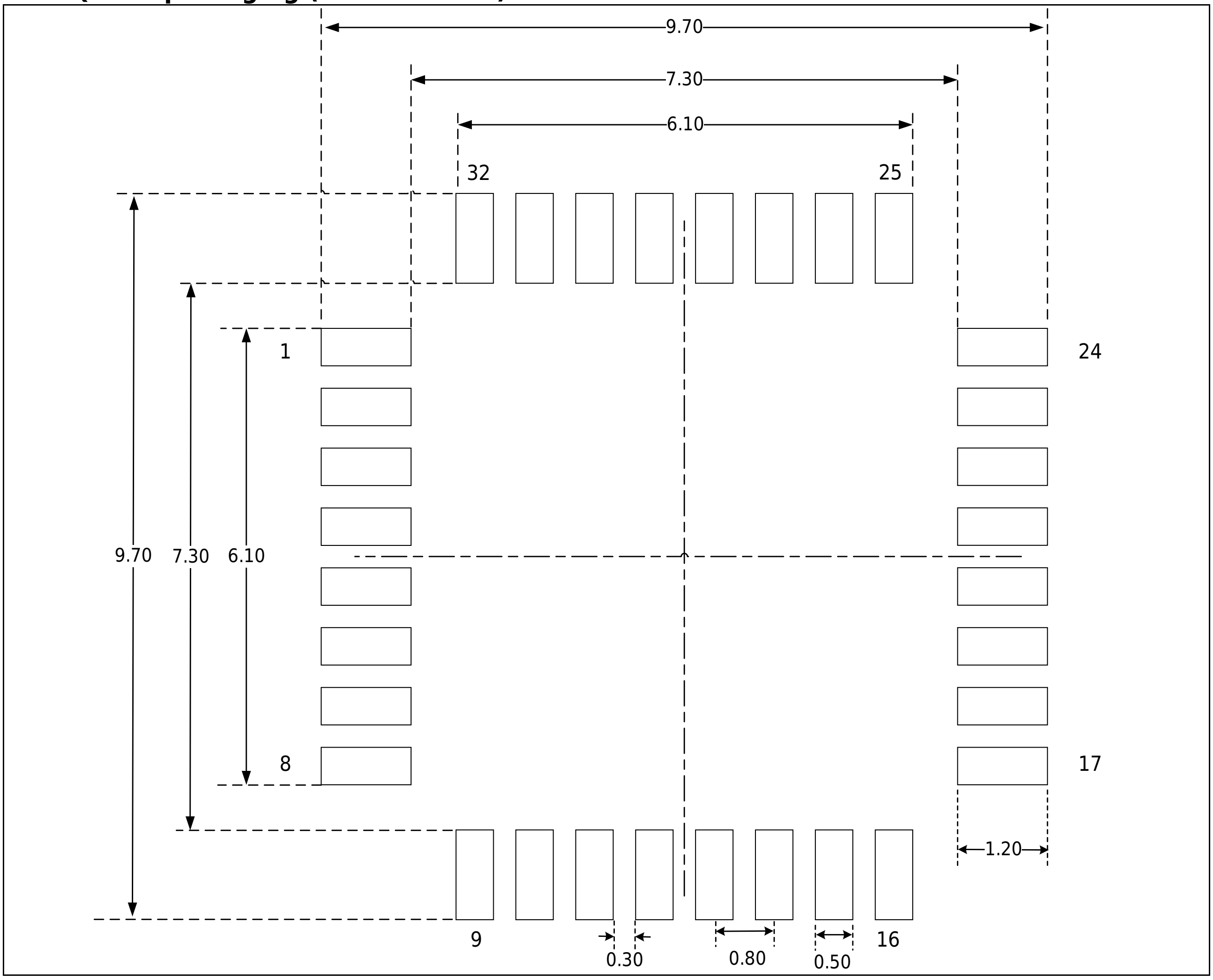
LQFP48 packaging (7 mm x 7 mm)



NOTE:

– ***Dimensions are expressed in millimeters.***
– ***Dimensions are for reference only.***

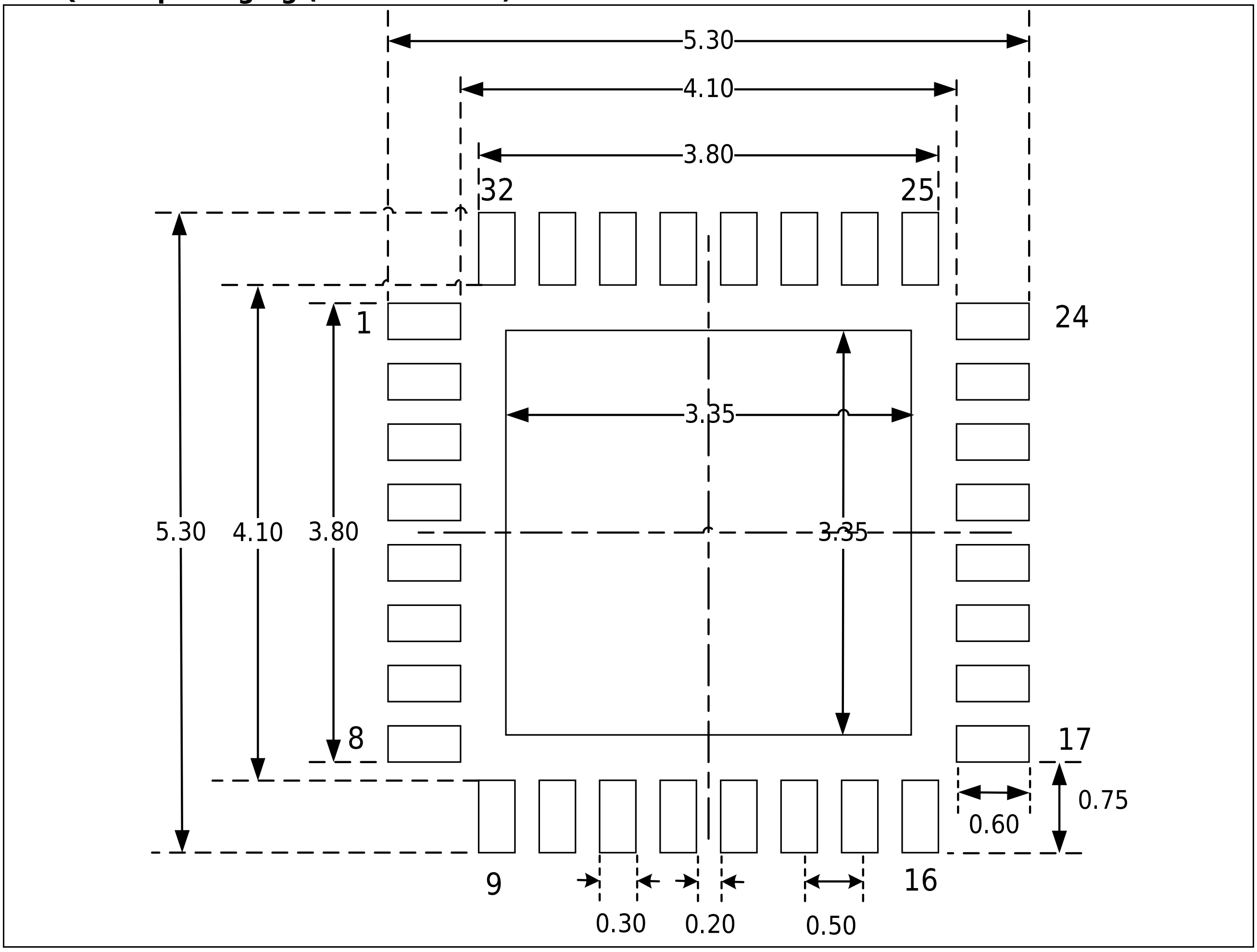
LQFP32 packaging (7 mm x 7 mm)



NOTE:

- ***Dimensions are expressed in millimeters.***
- ***Dimensions are for reference only.***

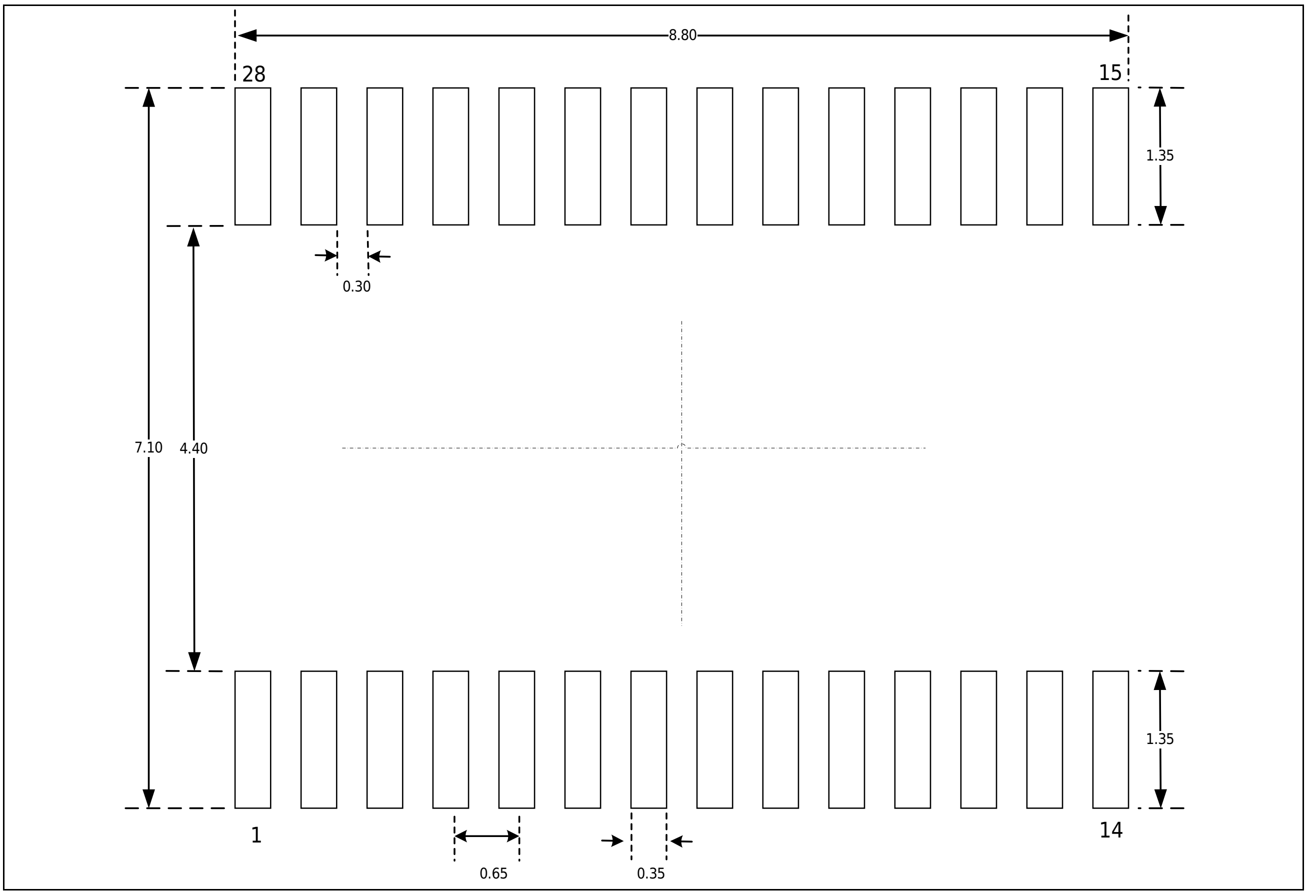
QFN32 packaging (5 mm x 5 mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

TSSOP28



NOTE:

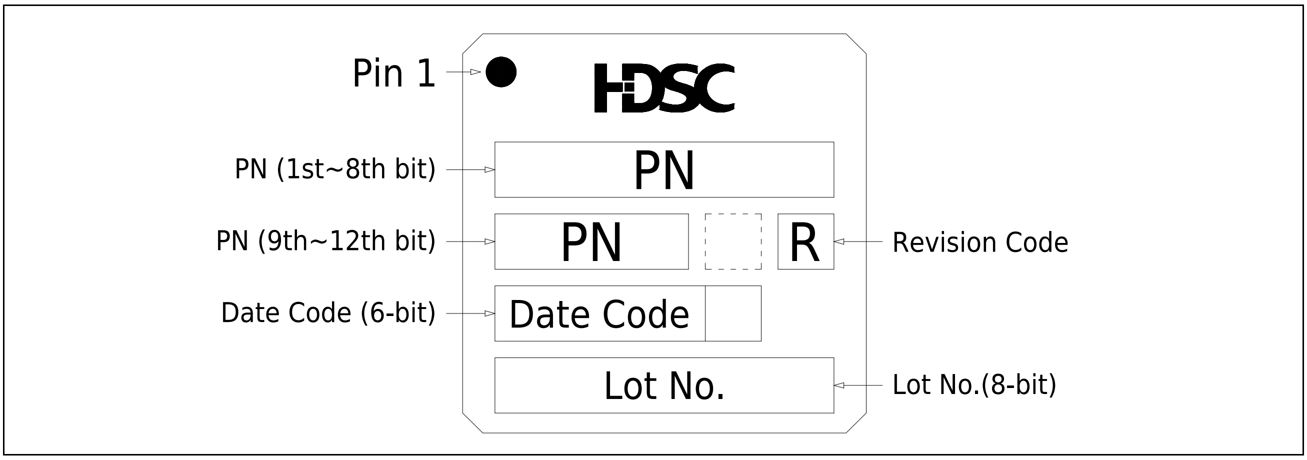
- ***Dimensions are expressed in millimeters.***
- ***Dimensions are for reference only.***

8.3 Silkscreen Instructions

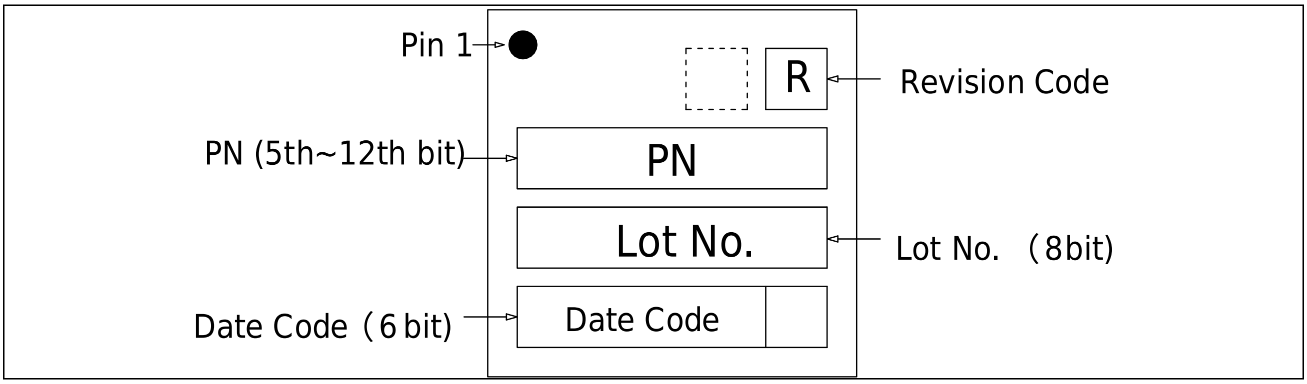
The position and information of Pin 1 printed on the front of each package are given below.

LQFP64 packaging（10 mm x 10 mm） / LQFP44 packaging（10 mm x 10 mm）

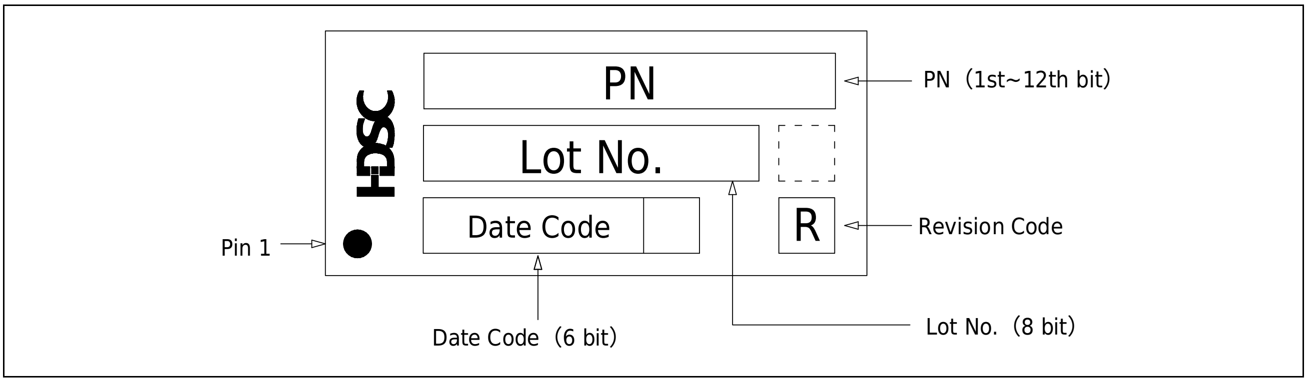
LQFP48 packaging（7 mm x 7 mm） / LQFP32 packaging（7 mm x 7 mm）



QFN32 packaging (5mm x 5mm)



TSSOP28



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

8.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's $I_{DD} \times V_{DD}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 8-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP64 10 mm x 10 mm / 0.5 mm pitch	65 +/- 10 %	℃/W
LQFP44 10 mm x 10 mm / 0.8 mm pitch	65 +/- 10 %	℃/W
LQFP48 7 mm x 7 mm / 0.5 mm pitch	75 +/- 10 %	℃/W
LQFP32 7 mm x 7 mm / 0.8 mm pitch	80 +/- 10 %	℃/W
QFN32 5 mm x 5 mm / 0.5 mm pitch	42 +/- 10 %	℃/W
TSSOP28	64 +/- 10 %	℃/W

9 Ordering Information

Part Number	HC32F030K8TA-LQFP64	HC32F030J8TA-LQ48	HC32F030H8TA-LQ44	HC32F030F8TA-LQ32	HC32F030F8UA-QN32TR	HC32F030E8PA-TSSOP28	HC32F030E8PA-TSSOP28TR
Flash	64K	64K	64K	64K	64K	64K	64K
RAM	8K	8K	8K	8K	8K	8K	8K
UART	2	2	2	2	2	2	2
SPI	2	2	2	1	1	1	1
I2C	2	2	2	2	2	2	2
ADC	24*12	17*12	17*12	10*12	10*12	11*12	11*12
PWM	23	18	18	12	12	12	12
Comp	2	2	2	2	2	2	2
OP	3	2	2	0	0	0	0
I/O	56	40	38	26	26	23	23
LVD	✓	✓	✓	✓	✓	✓	✓
LVR	✓	✓	✓	✓	✓	✓	✓
AES	✓	✓	✓	✓	✓	✓	✓
Vdd	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v
Package	LQFP64(10*10)	LQFP48(7*7)	LQFP44(10*10)	LQFP32(7*7)	QFN32(5*5)	TSSOP28	TSSOP28
Packaging Form	Tray	Tray	Tray	Tray	Tape and Reel	Tubing	Tape and Reel
Pin Pitch	0.5mm	0.5mm	0.8mm	0.8mm	0.5mm	0.65mm	0.65mm

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version number	Revision date	Modify the content
Rev1.00	2018/08/21	Initial release.
Rev1.10	2018/10/18	Corrected unique ID to 10 bytes; updated functionality table in "Product Lineup"; corrected RESETB pin characteristic parameters.
Rev1.20	2019/02/27	Corrected the following data: ① ADC characteristics; ② QFN32 package dimensions; ③ LQFP32 package dimensions; ④ added silk screen instructions; ⑤ removed product selection table, added ordering information; ⑥ added NOTE in package dimensions; ⑦ updated product name; ⑧ pin configuration for HC32F030F8TA / HC32F030F8UA pins; ⑨ ESD characteristics; ⑩ minimum value for EC_{FLASH} in memory characteristics.
Rev1.30	2019/03/22	Added commercial numbers HC32F030H8TA-LQ44 and HC32F030E8PA-TSSOP28TR.
Rev1.40	2019/07/15	Corrected the following data: ① programming mode; ② ESD characteristics; ③ memory characteristics.
Rev1.50	2019/12/12	Corrected the following data: ① BOOT0 pin in pin configuration diagram; ② added new descriptions in module signal description; ③ typical application circuit diagram; ④ illustrations and notes for high-speed external clock XTH and low-speed external clock XTL.
Rev1.60	2020/01/17	Corrected the following data: ① silk screen instructions.
Rev1.70	2020/03/05	Added notes in the introduction regarding "programming mode."
Rev1.80	2020/04/30	Corrected the following data: ① added AVCC/3 accuracy in ADC characteristics; ② corrected clerical error in section 7.3.7.2; ③ corrected RCL oscillator accuracy in section 7.3.8.2.
Rev1.90	2020/07/31	Corrected the following data: ① added sections 7.3.18, 7.3.19, 8.2, and 8.4; ② levels in section 7.3.11; ③ V_{IH} and V_{IL} values in section 7.3.13.2.
Rev2.00	2020/09/30	Corrected the following data: ① clock system description in the introduction; ② RCH oscillator accuracy in section 7.3.8.1; ③ V_{IL} and V_{IH} in section 7.3.14; ④ added SPI characteristics.
Rev2.10	2021/05/31	Corrected the following data: ① modified declaration; ② $t_{HD.STA}$ and $t_{SU.STO}$ parameters in I2C characteristics; ③ serial peripheral interface SPI in the introduction; ④ data retention period in memory characteristics; ⑤ added g_m parameter in external clock source characteristics.
Rev2.20	2022/03/09	Updated company logo.
Rev2.21	2024/07/05	Corrected the following data: ① modified ADC and VC channel numbers in the introduction, removed 1.2V related descriptions; ② modified storage temperature range in Table 7-3 temperature characteristics; ③ added section "7.3.8.3 Internal Low-speed Clock 10k Oscillator"; ④ removed 1.2V related descriptions in section 7.3.16 VC characteristics.
Rev2.22	2024/12/12	Updated content in sections "7.3.7.3 High-speed External Clock XTH" and "7.3.7.4 Low-speed External Clock XTL."
Rev2.23	2025/03/28	Corrected the following data: ① updated parameters in Table 7-15 SPI interface characteristics; ② modified maximum input filter pulse and minimum non-filter pulse values in section 7.3.14 RESETB pin characteristics.