XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F002 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.21 June 2023

Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32F002 series has a flexible power management system
  - 5μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retained, IO interrupt active, all registers, RAM, and CPU data save state power consumption
  - 15μA/MHz@3V@48MHz sleep mode: CPU stops, peripherals are in runnable state, main clock runs
  - 100μA/MHz@3V@48MHz working mode: CPU and peripherals can run, run programs from FLASH
- 18K bytes FLASH memory, with erase and write protection function, support ISP, ICP, IAP, 4 -level security protection
- 2K bytes RAM memory
- General I/O pins (22IO/24PIN, 18IO/20PIN)
- Clock
  - Internal high-speed clock 44.24/48MHz
  - Internal low-speed clock 32.8/38.4KHz
  - External input 1-16MHz
- Timer/counter
  - 1 composite timer, which can be configured as a general-purpose 16 -bit timer / counter or three 16 -bit basic timers; when used as a general-purpose timer, it supports 4 -channel capture comparison and 4 - channel PWM output; when used as a basic timer, each timing The device supports two inverted output
  - 1 advanced 16 -bit timer supporting 3 complementary PWM outputs
  - 1 independent watchdog circuit, the internal low-speed clock oscillator provides WDT counting
  - 1 window watchdog circuit, using the system clock
  - 1 low-power 16 -bit timer, support automatic wake-up
  - 1 CM0+ built-in 24 - bit SysTick timer
- Communication Interface
  - 2 -way LPUART communication interface
  - 1-channel SPI standard communication interface
  - 1-channel I2C standard communication interface
- Timer as buzzer frequency generator
- Globally unique 10-byte ID number
- 128 bytes OTP memory, can only be written by programmer
- 10 -bit SARADC up to 1Msps sampling rate
- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -20 ~ 105 ℃, 1.7 ~ 5.5V
- Package form: QFN24/20, TSSOP24/20

Support Model:

HC32F002C4PZ-TSSOP20	HC32F002C4UZ-ZFN20TR
HC32F002D4PZ-TSSOP24	HC32F002D4UZ-QFN24TR
HC32F002C4PZ-TSSOP20TR	HC32F002D4PZ-TSSOP24TR

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Table of Contents

Table Index

Graph Index

1 Overview

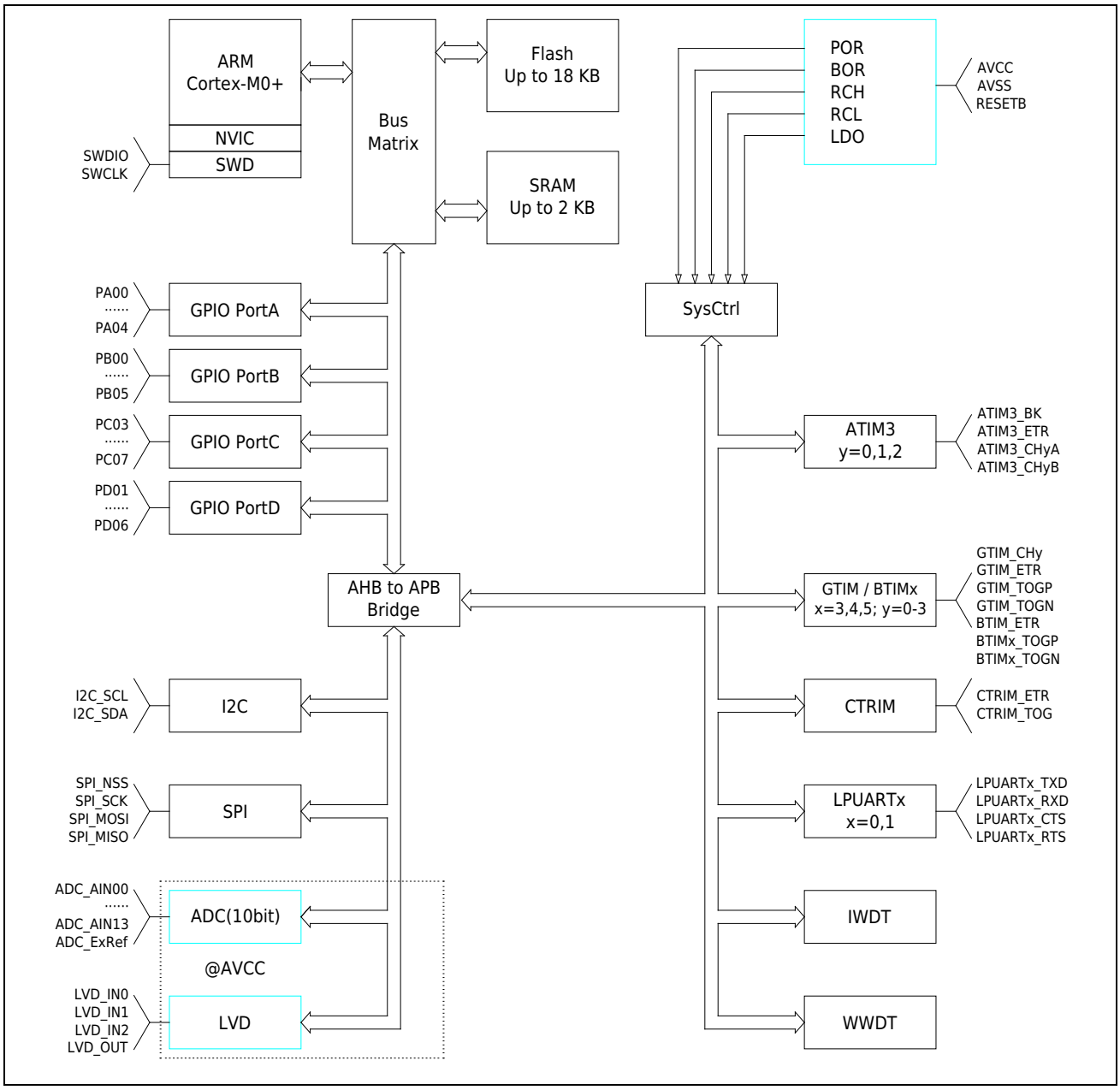
The HC32F002 series is a basic general-purpose 32 -bit MCU with a wide operating voltage range. The chip integrates a 10 -bit SARADC with a sampling rate of up to 1Msps, a high-performance PWM timer, LPUART, SPI, I2C and other rich peripherals, and has the characteristics of low power consumption, high reliability, and high integration. The HC32F002 series adopts the Cortex-M0+ core, the main frequency is up to 48MHz, cooperates with the mature Keil and IAR debugging and development software, and supports the use of C language and assembly language development.

Typical application

- Motor Control, Battery Management
- Smart home, medical equipment
- Security alarm, intelligent transportation
- Sensor modules, wireless modules, shelf labels

2 Functional Module

2.1 Block diagram of functional modules



2.2 32 -bit Cortex M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	15 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Multi-cycle 32 -bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 1 watch points (watch points)

2.3 memory

2.3.1 18 Kbytes FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming Support ISP, IAP, ICP functions. With 4 levels of security protection.

2.3.2 2 Kbytes RAM

RAM data will not be lost in any power consumption mode.

2.4 Clock System

A high-precision internal clock RCH with a frequency of 44~48MHz. Calibration values of 44.24MHz and 48MHz have been preset at the factory.

An internal clock RCL with a frequency of 32.8KHz/38.4KHz.

An external high-speed clock EXTCLK with a frequency of 1~16MHz.

2.5 Operating Mode

- Operating mode (Active Mode): CPU is running, and on-chip peripherals are running.
- Sleep Mode (Sleep Mode): The CPU stops running, and the on-chip peripherals run.
- Deep sleep mode (Deep sleep Mode): The CPU stops running, and the low-power on-chip peripherals run.

2.6 Port Controller GPIO

It can provide up to 22 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by an independent control register bit. All pins support edge-triggered interrupts and level-triggered interrupts, which can wake up the MCU from various sleep modes to work mode. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor with Schmitt trigger function. Each IO supports a maximum current drive capability of 18mA.

2.7 Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 15 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

2.8 Reset Controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset again, and the program counter PC will point to the starting address.

2.9 Timer TIM

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Advanced timer	ATIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Universal timer	GTIM	16	1~32768	Up count	4	4	No
	BTIM3-5	16	1~32768	Up count	No	No	No
clock calibrator	CTRIM	16	1~32768	Up count	No	No	No

The general- purpose timer is a timer that supports 4 -way compare and capture functions, and can be configured into 3 basic timers.

The low-power timer is an asynchronous 16 -bit timer / counter, which can still time / count through RCL after the system clock is turned off. Wake up the system in low-power mode through interrupts.

Advanced timers include timer ATIM3, whose characteristics are as follows:

- PWM independent output, complementary output

- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

ATIM3 is a multi-channel general-purpose timer, which can generate 3 sets of PWM complementary outputs or 6 channels of PWM independent output, and a maximum of 6 channels of input capture. With dead zone control function.

2.10Watchdog WDT

IWDT is a configurable 12 -bit timer that provides reset in case of MCU exception; RCL clock input is used as counter clock. The WDT can only be restarted by writing a specific sequence.

WWDT is a 7 -bit timer that is usually used to monitor software failures caused by external disturbances or unforeseen logic conditions that cause the application program to deviate from the normal operating sequence.

2.11Low Power Synchronous Asynchronous Transceiver LPUART

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1, its basic functions are as follows:

- Transmission clock SCLK (SCLK can choose RCL or PCLK, the clock precision is the same as RCL or PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- Hardware flow control
- Support single line mode

2.12 Serial Peripheral Interface SPI

- Can be configured as master or slave, support multi-machine mode
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 12M bps
- The maximum frequency division factor of slave mode is PCLK/4, and the maximum communication rate is 8M bps
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- Two transmission orders: send and receive MSB first or send and receive LSB first
- Various data frame lengths: 4bit ~ 16bit
- Two NSS methods: hardware control, software control
- Configurable serial clock polarity and phase

2.13 I2C bus

One-way I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

2.14 Clock Calibrator CTRIM

The clock calibration timer can adjust the calibration RC clock frequency, and can also adjust the calibration clock frequency of other RC oscillators. It can also be used as a general-purpose timer or an automatic wake-up timer.

2.15 Buzzer

A timer function multiplexed output provides a programmable drive frequency for the buzzer. The buzzer port can provide 18mA sink current, complementary output, no additional transistor is needed.

2.16 Analog-to-digital Converter (ADC)

External analog signals need to be converted into digital signals to be further processed by the MCU. A 10 -bit successive approximation analog-to-digital converter (SAR ADC) module with high precision and high conversion rate is integrated inside. Has the following properties:

- 10-bit conversion accuracy;
- 1M SPS conversion speed;
- Support single conversion and continuous conversion;
- 2 reference sources: AVCC voltage, ExRef pin;
- 15 input channels, including 14 external pin inputs and 1 built- in BGR 0.9V voltage;

Note: Select AVCC as the reference source, measure BGR 0.9V; AVCC voltage can be calculated.

- ADC voltage input range: 0~Vref;
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

2.17 Low voltage detector LVD

Detect chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 monitoring sources, AVCC, PA03, PC03, PD04;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

2.18 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

2.19 Programming Mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

Support unified programming interface: ISP protocol and SWD protocol share SWD port.

2.20 Device Electronic Signature

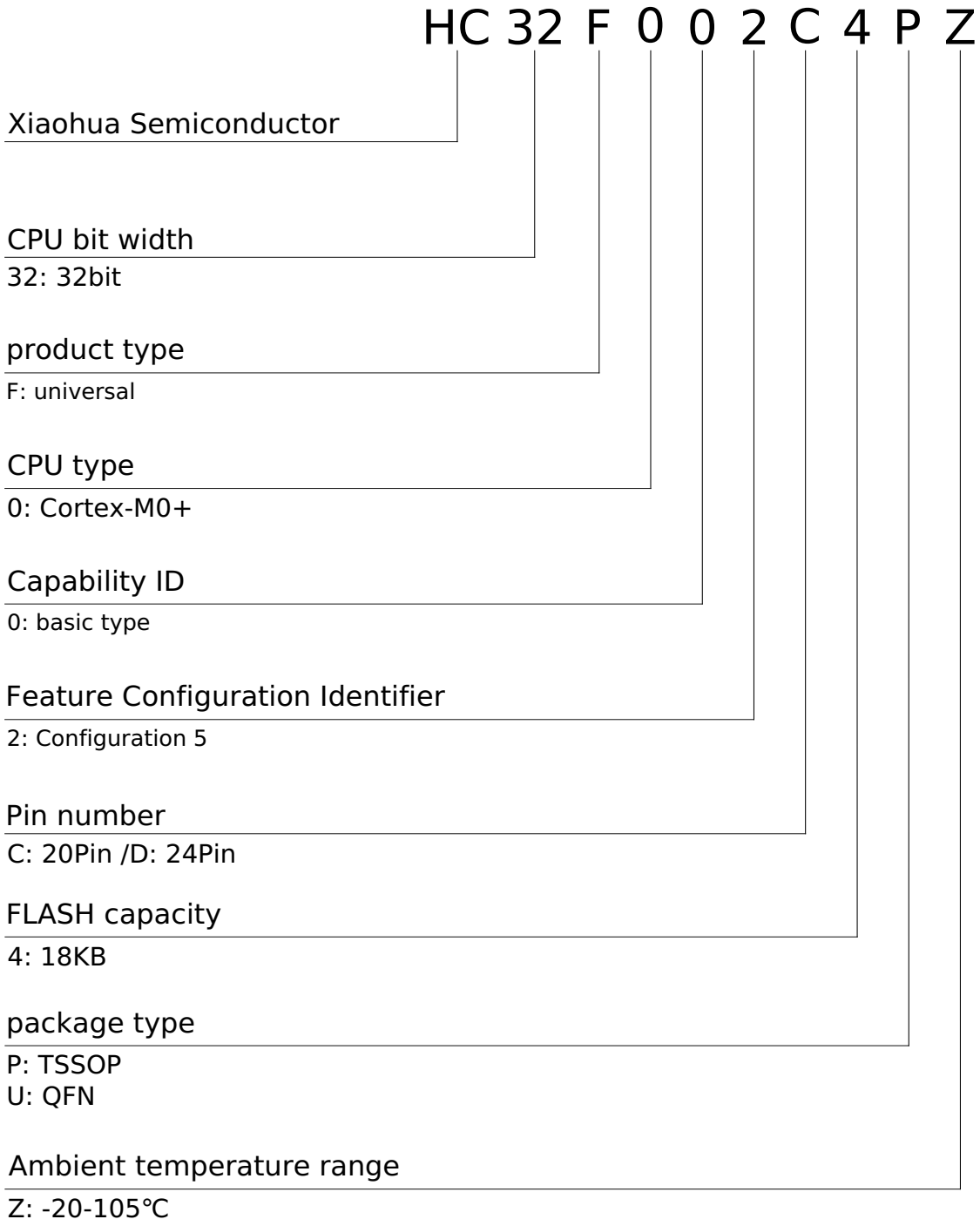
Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. Built -in 128 -byte OTP, which can only be written once by a programmer.

2.21 High Security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Product Lineup

3.1 Product Name



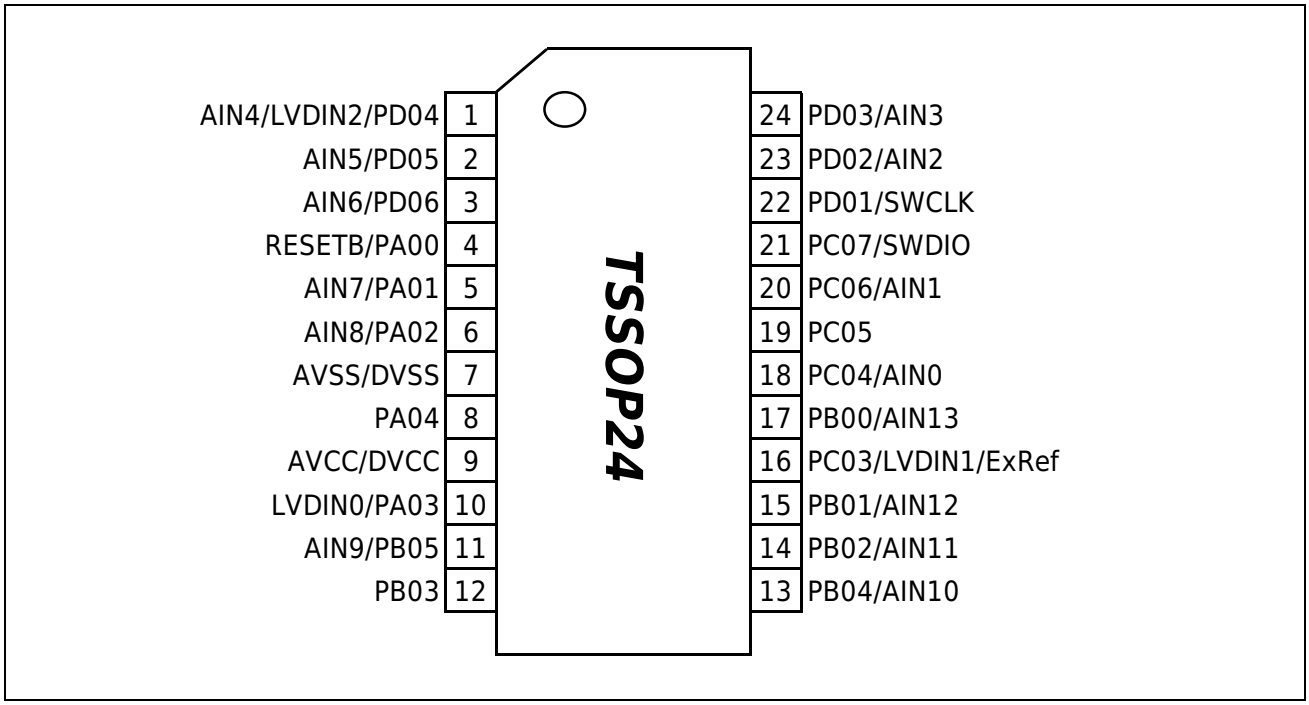
3.2 Function

Product Name		HC32F002C4PZ	HC32F002C4UZ	HC32F002D4PZ	HC32F002D4UZ
Pin number		20	20	24	24
GPIO pin number		18	18	22	22
CPU	Kernel	Cortex M0+			
	Frequency	48MHz			
Supply voltage range		1.7 ~5.5V			
Temperature range		-20 ~ 105℃			
Debug function		SWD debug interface			
Unique identification code		Support			
Communication Interface		LPUART0/1 SPI I2C			
Timer		Advanced Timer ATIM3 General purpose timer GTIM or BTIM3/4/5 Low Power Timer CTRIM			
10-bit A/D converter		14ch+1ch(internal)			
Port interrupt		18	18	22	22
Low voltage detection reset		1			
Clock	Internal high-speed oscillator	RCH 44.24/48MHz			
	Internal low-speed oscillator	RCL 32.8/38.4kHz			
buzzer		Max 4ch			
Flash security protection		Support			

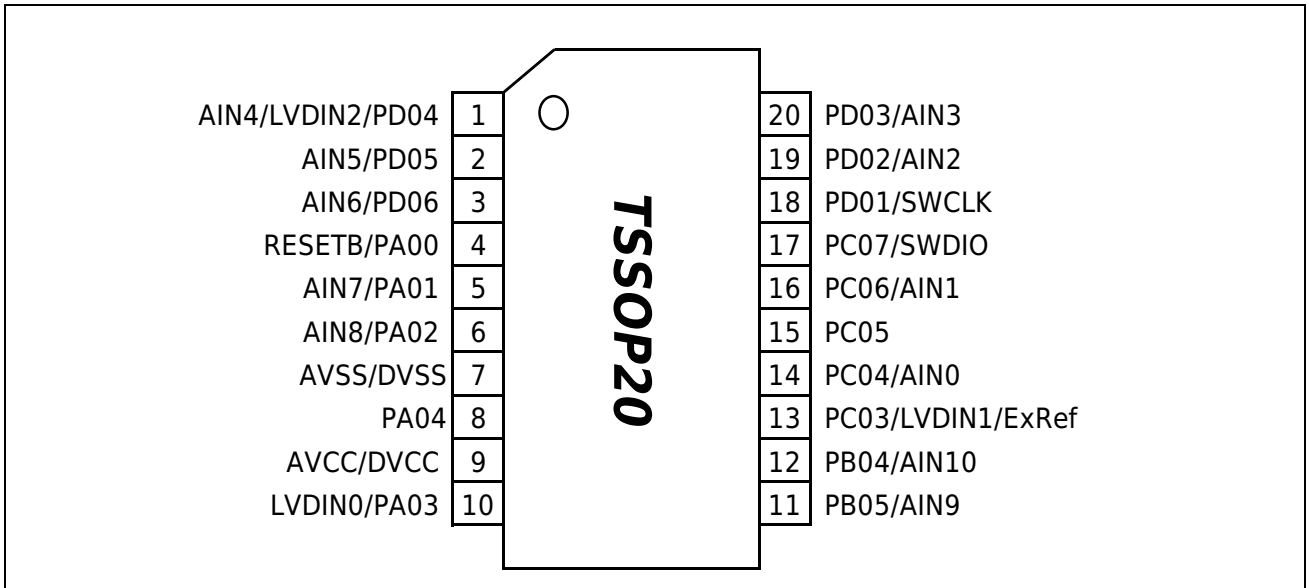
4 Pin configuration and function

4.1 Pin configuration diagram

HC32F002D4PZ-TSSOP24/ HC32F002D4PZ-TSSOP24TR



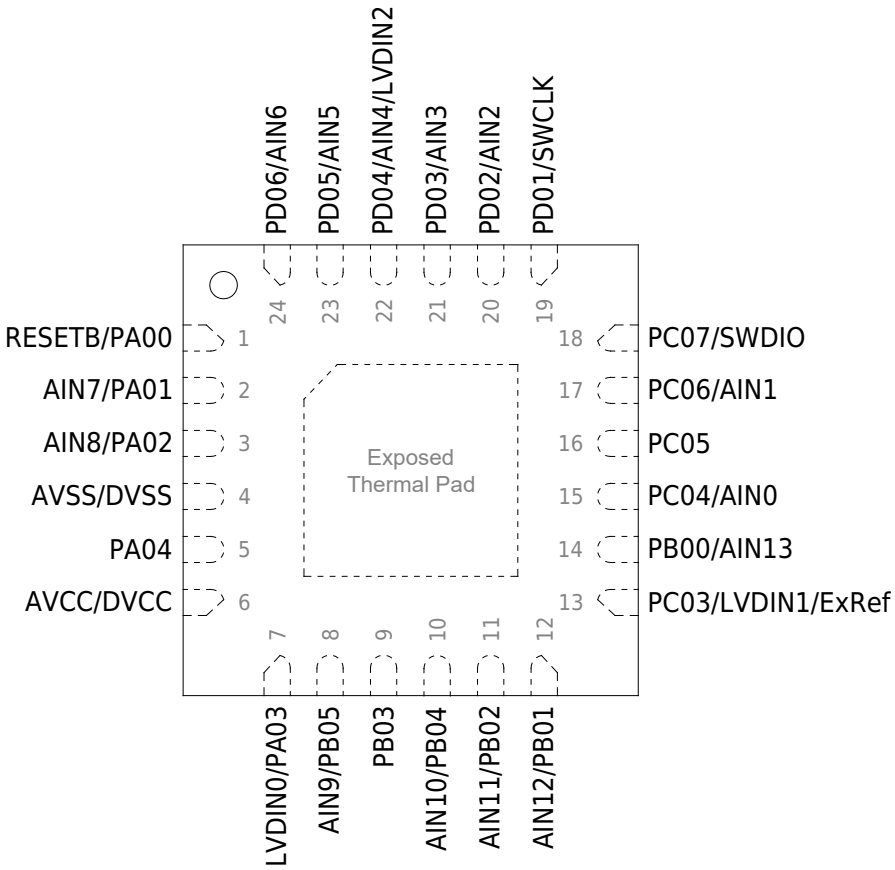
HC32F002C4PZ-TSSOP20/ HC32F002C4PZ-TSSOP20TR



Note:

- In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.
- For details about the IOs not exported by this package, see Pin function description

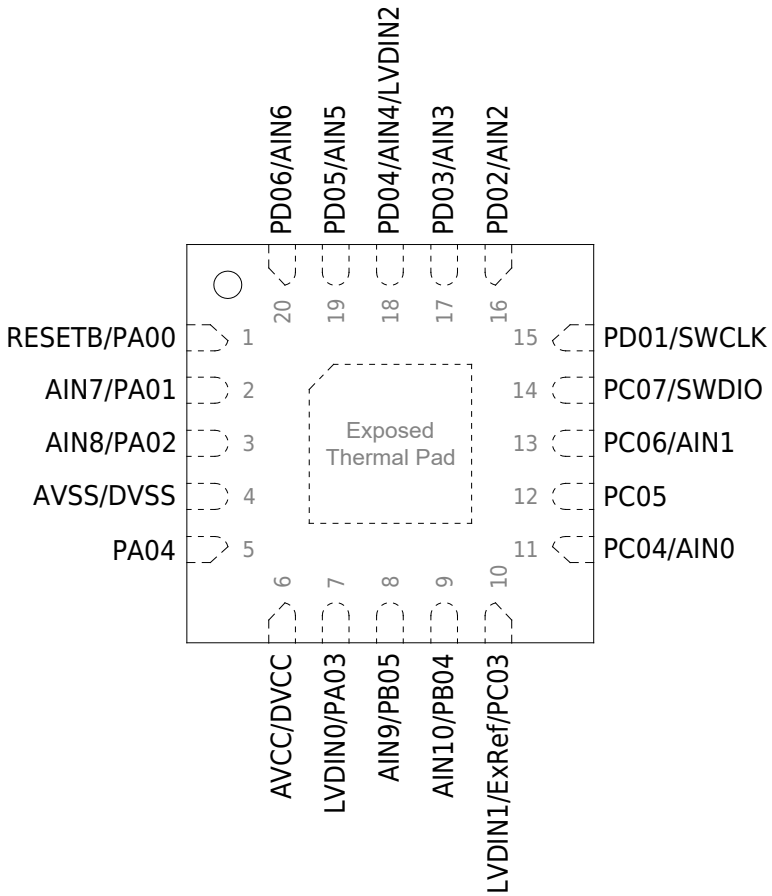
HC32F002D4UZ-QFN24TR



Note:

– The Exposed Thermal Pad needs to be connected to the DVSS.

HC32F002C4UZ-ZFN20TR



Note:

- In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.
- For details about the IOs not exported by this package, see Pin function description.

Figure 4-1 Pin Configuration Diagram

4.2 Pin function description

QFN20	QFN24	TSSOP20	TSSOP24	NAME	DIGITAL	ANALOG
1	1	4	4	PA00	-	RESETB
2	2	5	5	PA01	LPUART0_RXD I2C_SDA GTIM_TOGP HCLK_OUT	ADC_AIN7 EXTCLK
3	3	6	6	PA02	LPUART0_TXD I2C_SCL GTIM_TOGN LVD_OUT	ADC_AIN8
4	4	7	7	AVSS/DVSS		
5	5	8	8	PA04	GTIM_TOGP LVD_OUT SPI_NSS	-
6	6	9	9	AVCC/DVCC		
7	7	10	10	PA03	GTIM_CH2 SPI_NSS CTRIM_ETR CTIRM_TOG	LVD_IN0
8	8	11	11	PB05	I2C_SDA ATIM3_BK CTRIM_ETR CTIRM_TOG	ADC_AIN9
	9		12	PB03	ATIM3_ETR GTIM_CH0 LPUART1_CTS	-
9	10	12	13	PB04	I2C_SCL ATIM3_CH2B LPUART0_CTS	ADC_AIN10
	11		14	PB02	ATIM3_CH2B GTIM_CH1 LPUART1_RTS	ADC_AIN11
	12		15	PB01	ATIM3_CH1B GTIM_CH2 LPUART0_CTS	ADC_AIN12
10	13	13	16	PC03	ATIM3_CH2A ATIM3_CH0B LPUART0_RTS	LVD_IN1 ADC_ExRef
	14		17	PB00	ATIM3_CH0B GTIM_CH3 LPUART0_RTS	ADC_AIN13
11	15	14	18	PC04	ATIM3_CH0B ATIM3_CH1B TCLK_OUT	ADC_AIN0
12	16	15	19	PC05	SPI_SCK GTIM_CH3 ATIM3_ETR	-
13	17	16	20	PC06	SPI_MOSI ATIM3_CH0A LPUART1_RTS	ADC_AIN1
14	18	17	21	PC07 SWDIO	SPI_MISO ATIM3_CH1A LPUART0_RXD	-
15	19	18	22	PD01 SWCLK	GTIM_ETR ATIM3_BK LPUART0_TXD	-
16	20	19	23	PD02	GTIM_CH2 ATIM3_CH2A LPUART1_CTS	ADC_AIN2

QFN20	QFN24	TSSOP20	TSSOP24	NAME	DIGITAL	ANALOG
17	21	20	24	PD03	GTIM_CH1 ATIM3_CH1A LPUART1_RXD	ADC_AIN3
18	22	1	1	PD04	GTIM_CH0 LPUART1_TXD SPI_SCK	ADC_AIN4 LVD_IN2
19	23	2	2	PD05	LPUART1_TXD ATIM3_CH0A SPI_MISO	ADC_AIN5
20	24	3	3	PD06	LPUART1_RXD GTIM_ETR SPI_MOSI	ADC_AIN6

The digital function of each pin is controlled by the AFRx register, see the GPIO chapter for details.

4.3 Module Signal Description

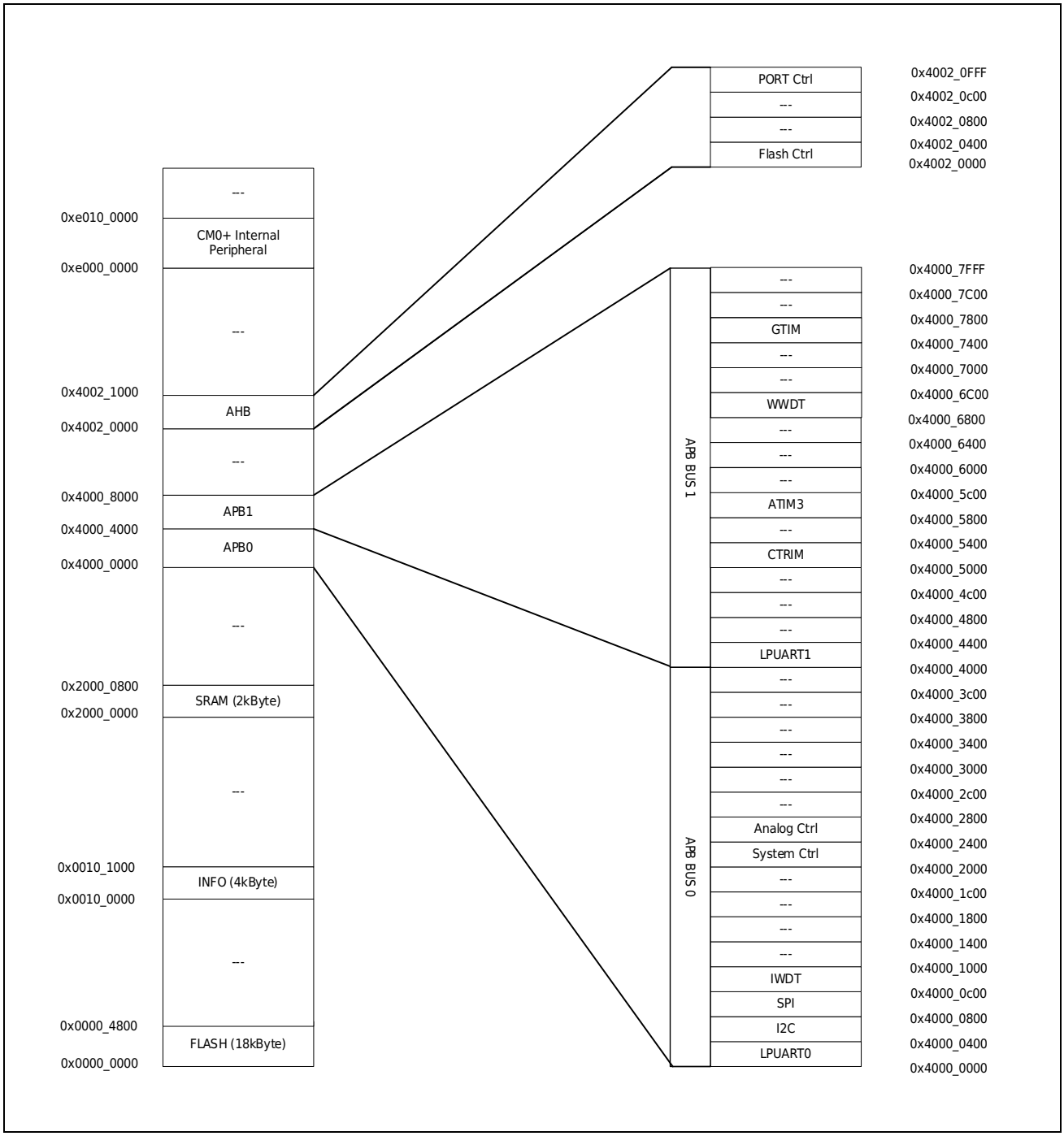
Table 4-1 Module Signal Description

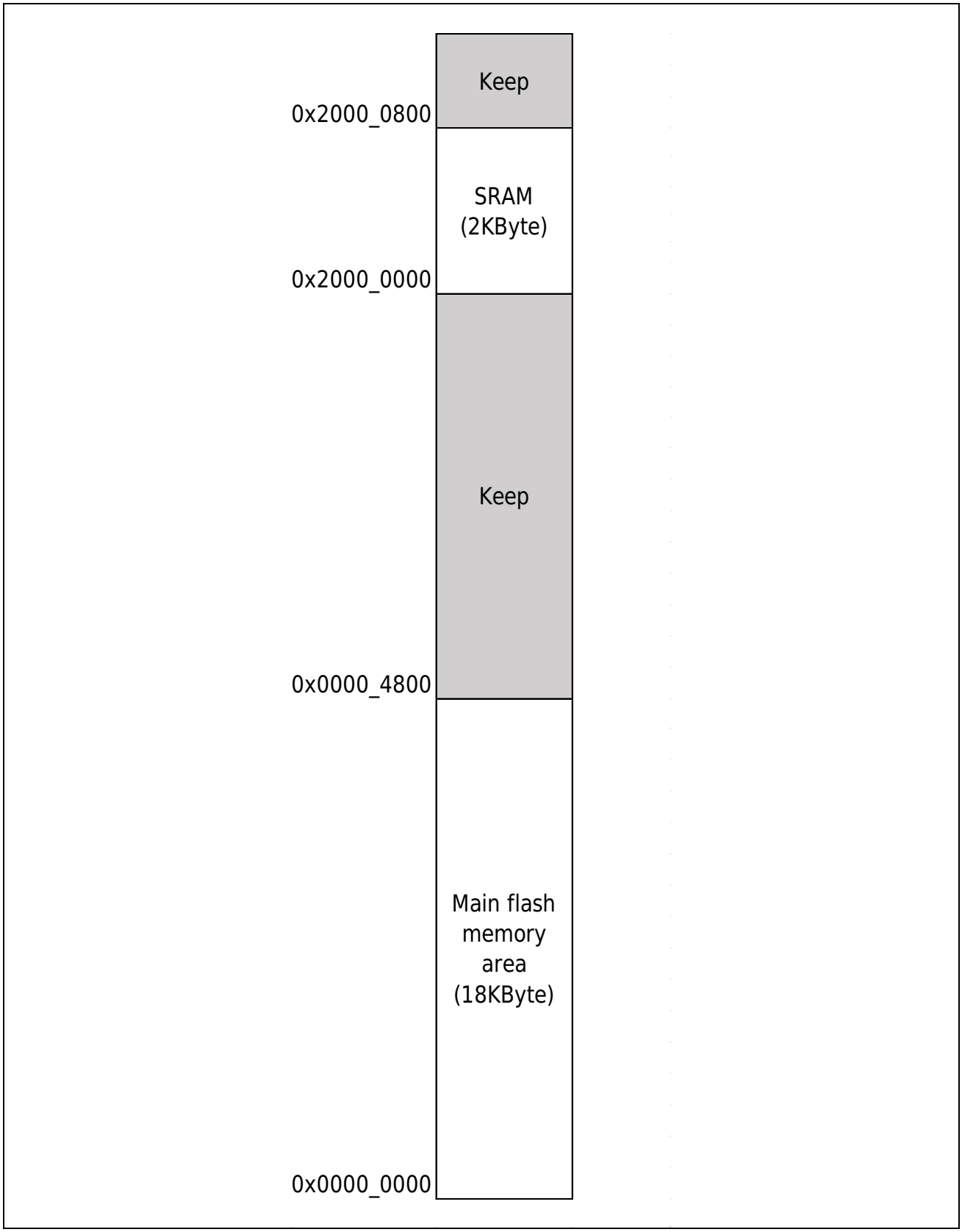
Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
ADC	ADC_AIN0~13	ADC input channel 0-13
	ADC_ExRef	ADC external reference voltage
Outsourced clock	EXTCLK	External input clock
LVD	LVD_IN0	Voltage detection input 0
	LVD_IN1	Voltage detection input 1
	LVD_IN2	Voltage detection input 2
	LVD_OUT	Voltage detection output
LPUART x=0,1	LPUARTx_TXD	LPUART data transmitter
	LPUARTx_RXD	LPUART data receiver
	LPUARTx_CTS	LPUART CTS
	LPUARTx_RTS	LPUART RTS
CTRIM	CTRIM_ETR	CTRIM external synchronization signal
	CTRIM_TOG	Toggle output signal of CTRIM
SPI	SPI_MISO	SPI module host input and slave output data signal
	SPI_MOSI	SPI module master output slave input data signal
	SPI_SCK	SPI module clock signal
	SPI_NSS	SPI chip select
I2C	I2C_SDA	I2C module data signal
	I2C_SCL	I2C module clock signal
basic timer BTIMx x = 3,4,5	BTIMx_TOGP	Toggle output signal of BTIMx
	BTIMx_TOGN	
Universal timer GTIM y=0,1,2.3	GTIM_CHy	GTIM capture input compare output
	GTIM_ETR	External count input signal of GTIM
	GTIM_TOGP GTIM_TOGN	Invert output signal of GTIM
Advanced timer ATIM3 y=0,1,2	ATIM3_CHyA	Capture input compare output A of ATIM3
	ATIM3_CHyB	Capture input compare output B of ATIM3
	ATIM3_ETR	External counting input signal of ATIM3
	ATIM3_BK	ATIM3 brake signal

Note:

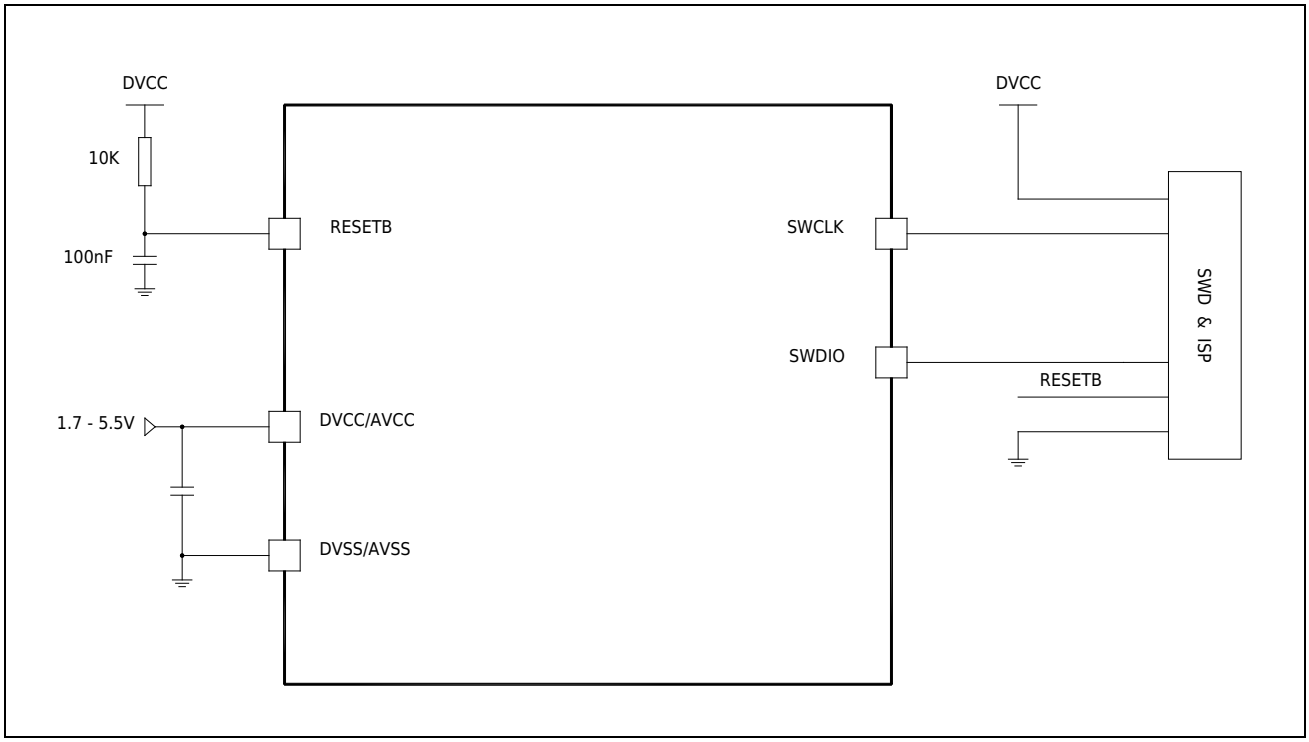
– The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.

5 Storage Area Map




Keep
0x2000_0800
SRAM
(2KByte)
0x2000_0000
Keep
0x0000_4800
Main flash
memory
area
(18KByte)
0x0000_0000

6 Typical Application Circuit Diagram



Note:

– Power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.

7 Electrical characteristics

7.1 Test Conditions

Unless otherwise specified, all voltages are based on VSS.

7.1.1 Minimum and Maximum Values

Unless otherwise specified, 100% of the products are tested on the production line under ambient temperature TA=25°C and TA=TA_{max} (TA_{max} matches the selected temperature range), and all the minimum and maximum values will be at the worst Guaranteed under the conditions of ambient temperature, supply voltage and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3Σ).

7.1.2 Typical Value

Unless otherwise specified, typical data is based on TA=25°C and VCC=3.3V. These data are only used for design guidance and not tested. The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average ± 2Σ).

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings"list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V V
V_{IN}	Input voltage on other pins(2)	VSS - 0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins		50	mV
| VSSx - VSS |	Voltage difference between different ground pins		50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.

Table 7-2 Current Characteristics

Symbol	Description	Max (1)	Unit
IVCC	The total current (supply current) through the DVCC/AVCC power cord (1)	300	mA
IVSS	The total current through the VSS ground wire (outflow current) (1)	300	mA
IIO	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
IINJ(PIN)(2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
∑IINJ(PIN) (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply system within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it is not possible to guarantee that VIN does not exceed its maximum value, ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when VIN<VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse

injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 Temperature Characteristics

Symbol	Description	Numerical value	Unit
TSTG	Storage temperature range	-60 ~ + 150	℃
TJ	Maximum junction temperature	125	℃

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	MHz
DVCC	Working voltage of digital part		1.7	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	1.7	5.5	V
PD	Power dissipation TA=105℃	TSSOP20		283	mW
	Power dissipation TA=105℃	TSSOP24		291	mW
TA	Ambient temperature	Maximum power consumption	-20	105	℃
		Low power consumption (3)	-20	125	℃
TJ	Junction temperature range		-20	125	℃

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

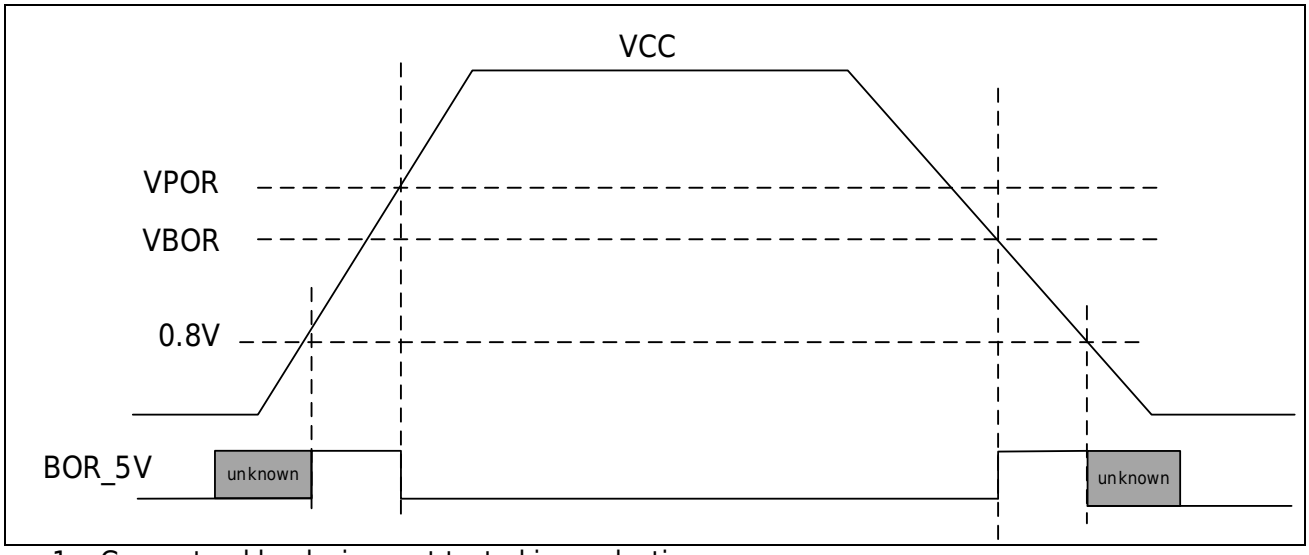
7.3.2 Working conditions at power-up and power-down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{Vcc}	VCC rising rate		0.2	20000	μs/V
t_{Vcc}	VCC falling rate		0.2	20000	μs/V

1. The data is based on the assessment results, not tested in production

7.3.3 Embedded reset and LVD module features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out Schematic Diagram

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
Vpor	POR release voltage (power-on process)			1.65	1.7	V
Vbor	BOR detection voltage (power-down process)			1.55		V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS=0001 LVD_CR.VTDS=0010 LVD_CR.VTDS=0011 LVD_CR.VTDS=0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111		1.8±3.5% 1.9±3.5% 2.0±3.5% 2.1±3.5% 2.2±3.5% 2.3±3.5% 2.4±3.5% 2.5±3.5% 2.6±3.5% 2.7±3.5% 2.8±3.5% 2.9±3.5% 3.0±3.5% 3.1±3.5% 3.2±3.5% 3.3±3.5%		V
Icomp	Power consumption			0.36		uA
Tresponse	Response time			100		μs
Tsetup	Establishment time			300		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filter time	LVD_CR.FltTime = 000 LVD_CR.FltTime = 001 LVD_CR.FltTime = 010 LVD_CR.FltTime = 011 LVD_CR.FltTime = 100 LVD_CR.FltTime = 101 LVD_CR.FltTime = 110 LVD_CR.FltTime = 111	25 75 175 375 1575 6375 25575 102375	50 100 200 400 1600 6400 25600 102400		μs

1. The data is based on the assessment results and is not tested in production.

7.3.4 Built-in reference voltage BGR

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{BGR09}	Internal 0.9V Reference Voltage	Room temperature25°C; 3.3V		0.9		V
V_{BGR09}	Internal 0.9V Reference Voltage	-20~105°C；1.7~5.5V	0.875		0.925	V
T_{Coeff}	Internal 0.9V temperature coefficient	-20~105°C		50		ppm/°C

1. The data is based on the assessment results, not tested in production.

7.3.5 Supply Current characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When turning on a peripheral: $f_{PCLK0} = f_{HCLK}$， $f_{PCLK1} = f_{HCLK}$.

Table 7-8 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
IDD (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	VCC=3.3V TA=25℃	RCH clock source	4M	505		uA
				8M	730		
				12M	955		
				22.12M	1515		
				24M	1630		
				44.24M	2755		
				48M	2980		
	All peripherals clock OFF, Run while(1) in RAM	VCC=3.3V TA=25℃	RCH clock source	4M	410		uA
				8M	545		
				12M	680		
				22.12M	1005		
				24M	1080		
				44.24M	1735		
				48M	1870		
IDD (Run mode)	All peripherals clock ON, Run while(1) in	VCC=1.7~5.5V TA=-20~105℃	RCH clock source	4M	725	870	uA
				8M	1160	1350	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
IDD (Sleep mode)	Flash			12M	1575	1820	uA
				22.12M	2545	2960	
				24M	2735	3170	
				44.24M FlashWait=1	3515	4070	
				48M FlashWait=1	3790	4380	
	All peripherals clock OFF, Run while(1) in Flash	VCC=1.7~5.5V TA=-20~105℃	RCH clock source	4M	635	770	
				8M	970	1140	
				12M	1295	1510	
				22.12M	2035	2390	
				24M	2185	2550	
				44.24M FlashWait=1	2500	2930	
				48M FlashWait=1	2685	2950	
	All peripherals clock ON	VCC=1.7~5.5V TA=-20~105℃	RCH clock source	4M	400	470	
				8M	520	610	
				12M	635	740	
				22.12M	925	1070	
				24M	990	1140	
				44.24M FlashWait=1	1570	1800	
				48M FlashWait=1	1695	1930	
	All peripherals clock OFF	VCC=1.7~5.5V TA=-20~105℃	RCH clock source	4M	305	370	
				8M	335	400	
				12M	360	430	
				22.12M	415	490	
				24M	435	520	
				44.24M FlashWait=1	550	640	
				48M FlashWait=1	585	680	
IDD (LP Run)	All peripherals clock ON, Run while(1) in Flash	VCC=1.7~5.5V	RCL32K clock source	TA=-20~25℃	7.4	14.4	uA
				TA=50℃	7.9	14.9	
				TA=85℃	9.3	16.0	
				TA=105℃	11.4	22.0	
	All peripherals clock OFF, Run while(1) in Flash	VCC=1.7~5.5V	RCL32K clock source	TA=-20~25℃	6.7	12.8	uA
				TA=50℃	7.2	13.6	
				TA=85℃	8.5	14.9	
				TA=105℃	10.6	21.0	
IDD (LP Sleep)	All peripherals clock ON	VCC=1.7~5.5V	RCL32K clock source	TA=-20~25℃	4.4	10.3	uA
				TA=50℃	4.8	10.7	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
				TA=85℃	6.1	11.2	
				TA=105℃	8.1	18.8	
	All peripherals clock OFF	VCC=1.7~5.5V	RCL32K clock source	TA=-20~25℃	3.7	7.3	uA
				TA=50℃	4.0	7.8	
				TA=85℃	5.3	10.5	
				TA=105℃	7.4	18.3	
IDD (DeepSleep mode)	WDT+LVD+ RCL32K +DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	3.2	6.9	uA
				TA=50℃	3.7	7.5	
				TA=85℃	4.9	9.2	
				TA=105℃	6.7	14.6	
	LVD+RCL32K +DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	2.6	6.2	uA
				TA=50℃	3.0	6.7	
				TA=85℃	4.0	8.7	
				TA=105℃	5.5	13	
	WDT+RCL32K +DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	3.0	6.5	uA
				TA=50℃	3.4	7.0	
				TA=85℃	4.6	8.8	
				TA=105℃	6.3	14.0	
	RCL38K + DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	3.0	6.5	uA
				TA=50℃	3.4	7.0	
				TA=85℃	4.6	8.8	
				TA=105℃	6.3	14.0	
	RCL32K + DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	3.0	6.5	uA
				TA=50℃	3.4	7.0	
				TA=85℃	4.6	8.8	
				TA=105℃	6.3	14.0	
	DeepSleep	VCC=1.7~5.5V		TA=-20~25℃	2.4	5.8	uA
				TA=50℃	2.7	6.3	
				TA=85℃	3.8	8.2	
				TA=105℃	5.2	12.5	

1. If there are no other specified conditions, the value of this Typ is measured at 25℃ & V_{CC} = 3.3V.
2. Unless otherwise specified, the Max value is the maximum value within the range of V_{CC} = 1.7-5.5V & Temperature = -20 ~ 105℃.
3. The data is based on the assessment results, not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- Deep sleep mode: The clock source is the RCH oscillator when entering deep sleep

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time			2.0		μs
	Deep sleep wake-up time	F_{HCLK} = 4 ~ 48MHz		5.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

7.3.7.1 External input high-speed clock

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{EXT}	User external clock frequency (1)		1	8	16	MHz
V_{EXTH}	Input pin high level voltage		0.7VCC		VCC	V
V_{EXTL}	Input pin low voltage		VSS		0.3VCC	V
Tr_{EXT}	Rise time (1)				20	ns
Tf_{EXT}	Falling time (1)				20	ns
Tw_{EXT}	Enter high or low time (1)		16			ns
Cin_{EXT}	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		40		60	%
IL	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

7.3.8 Internal timer characteristics

7.3.8.1 Internal RCH oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and TA conditions		0.25		%
		VCC = 1.7 ~ 5.5V T_{AMB} = -20 ~ 105°C	-3.5		+3.5	%
		VCC = 1.7 ~ 5.5V T_{AMB} = -20 ~ 50°C	-2		+2	%
F_{CLK}	Oscillation frequency		40.0		48.0	MHz
I_{CLK}	Power consumption	F_{MCLK} = 48MHz		170		μA
DC_{CLK}	Duty Cycle (1)		45	50	55	%

1. Results derived from comprehensive evaluation, not fully tested in production.

7.3.8.2 Internal RCL oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and TA conditions		0.5		%
		VCC = 1.7 ~ 5.5V T_{AMB} = -20 ~ 105°C	-5		+5	%
		VCC = 1.7 ~ 5.5V T_{AMB} = -20 ~ 50°C	-3		+3	%
F_{CLK}	Oscillation frequency			38.4 32.8		KHz
T_{CLK}	Start time			150		μs
DC_{CLK}	Duty Cycle (1)		25	50	75	%
I_{CLK}	Power consumption			1.5		μA

1. Results derived from comprehensive evaluation, not fully tested in production.

7.3.9 Memory characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
EC_{FLASH}(1)	Erase times	T_{AMB} = 25℃	20			kcycles
RET_{FLASH}(1)	Data retention period	T_{AMB} = 85℃, after 20 kcycles	20			Years
T_{b_prog}(2)	Programming time (bytes)		22		30	μs
T_{w_prog}(2)	Programming time (words)		40		52	μs
T_{p_erase}(2)	Page erase time		4		5	ms
T_{m_erase}(2)	Whole chip erase time		30		40	ms

1. Data guaranteed by audits, not tested in production.
2. Data guaranteed by design, not tested in production.

7.3.10 EFT characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class：4A
EFT to Power (IEC61000-4-4)	Class：4A

1. Data guaranteed by audit, not tested in production

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.11 ESD characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode			4		kV
$VESD_{CDM}$	ESD @ Charge Device Mode			1		kV
$VESD_{MM}$	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

1. Data guaranteed by audits, not tested in production.

7.3.12 I/O port characteristics

7.3.12.1 Output characteristics——ports

Table 7-9 Port Output Characteristics

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 4 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 8 mA, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V_{OL}	Low level output voltage Sink Current	Sinking 5 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 14 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing 8 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 18 mA, VCC = 3.3V (see Note 2)	VCC-0.6		V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 18 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V

NOTES:

1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.
3. For the package QFN20/TSSOP20, the pins PC3/PC4/PB4/PB5 are packaged together with other pins, and the driving capability is higher than other pins.

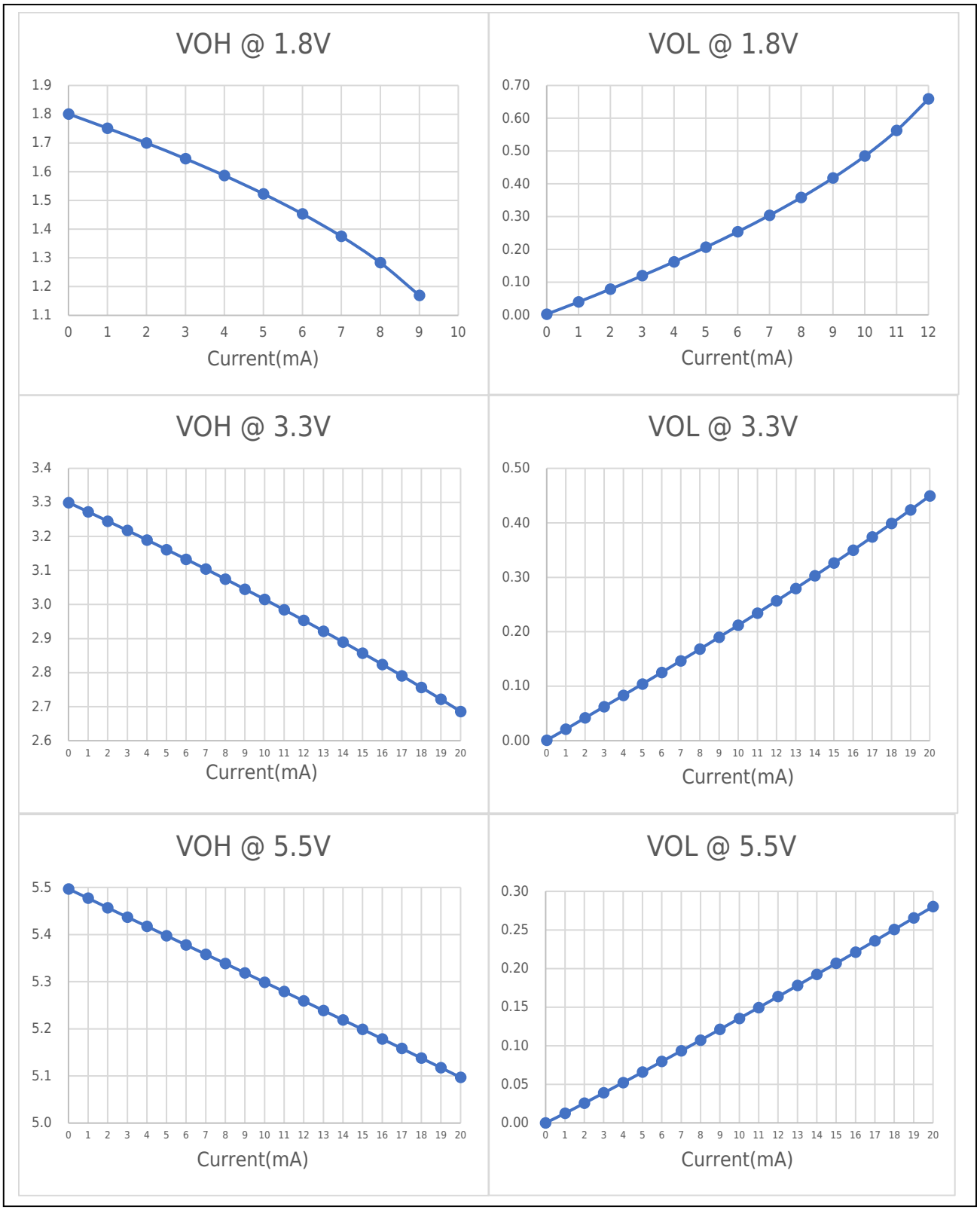


Figure 7-2 Output Port VOH/VOL Measured Curve

7.3.12.2 Input Characteristics - Ports PA, PB, PC, PD

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} - V_{IL})	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V		80		kΩ
C_{input}	Input capacitance			5		pF

1. Results derived from comprehensive evaluation, not fully tested in production.

7.3.12.3 Port external input sampling requirements - Timer Clock

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)		30		ns
t(cap)	Timer capture timing	TIMx capture pulse width Fsystem = 4MHz		0.5		μs
t(clk)	Timer clock frequency applied to pin	TIMx external clock input Fsystem = 4MHz			PCLK/2	MHz

NOTES:

1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.
2. Resulted from comprehensive evaluation, not tested in production.

7.3.12.4 Port leakage characteristics - PA, PB, PC, PD

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1,2)		±50		nA

NOTES:

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.
3. Guaranteed in production testing.

7.3.13 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

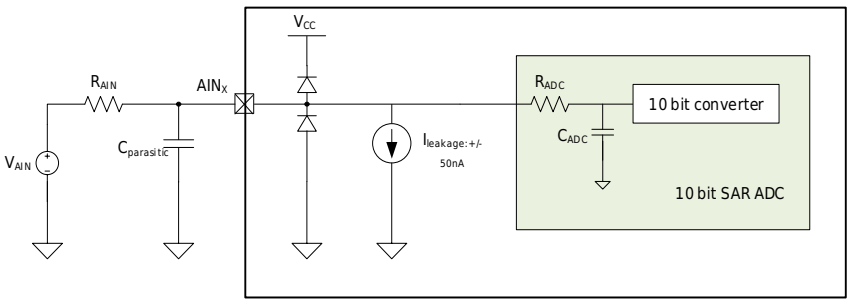
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{IL(RESETB)}$	Input low level voltage		-0.3		0.3VCC	V
$V_{IH(RESETB)}$	Input high level voltage		0.7VCC		VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$		80		kΩ
$V_{F(RESETB)}$	Input filter pulse				3	us
$V_{NF(RESETB)}$	Input unfiltered pulse		20			us

1. Guaranteed by design, not tested in production.

7.3.14 ADC characteristic

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0		AVCC	V
I_{ADC1}	Active current including reference generator and buffer	200Ksps		0.16		mA
I_{ADC2}	Active current without reference generator and buffer	1Msps		0.22		mA
C_{ADCIN}	ADC input capacitance			1.6	2	pF
R_{ADC}(1)	ADC sampling switch impedance			5		kΩ
R_{AIN}(1)	ADC external input resistor(2)				100	kΩ
F_{ADCCLK}	ADC clock Frequency				24	MHz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			5		μs
$T_{ADCCONV}$	Conversion time		19	24	25	cycles
ENOB	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.7V REF=EXREF		9.5		Bit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.7V REF=VCC		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.7V REF=EXREF		63		dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.7V REF=VCC		63		dB
DNL(1)	Differential non-linearity	500Ksps; VREF=EXREF/AVCC	-1		1	LSB
INL(1)	Integral non-linearity	500Ksps; VREF=EXREF/AVCC	-2		2	LSB
E_o(1)	Offset error		-1		1	LSB
E_g(1)	Gain error		-1		1	LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN}=\frac{M}{F_{ADC}*C_{ADC}*(N+1)*\ln(2)}-R_{ADC}$$

among themF_{ADC} It is the ADC clock frequency. Register ADC_CR0[4:2] can set its relationship with PCLK, as shown in the following table.

The following table shows the ADC clock frequencyF_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0[4:2]	**N**
000	1
001	2
010	4
011	8
……	
111	128

M is the number of sampling periods, which is set by the register ADC_CR0[13:12].

The following table shows the sampling timet_{sa}And ADC clock frequency F_{ADC}Relationship:

ADC_CR0[13:12]	**M**
00	6
01	8
10	11
11	12

The following table shows the ADC clock frequency F_{ADC}And external resistance R_{AIN}relationship (M=12, under the condition of sampling error 0.5LSB):

(KOhm)	(KHz)
10	24000
30	22000
35	18000
60	12000
120	6000
180	4000
360	2000
720	1000
1440	500
2200	350
3600	200
7200	100

For the above typical applications, you should pay attention to:

– Minimize the ADC input portAIN_Xparasitic capacitance$C_{PARACITIC}$;
– In addition to consideringR_{AIN}value, if the internal resistance of signal sourceV_{AIN}, it also needs to be considered.

7.3.15 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ATIM) Characteristics

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{res}	Timer to distinguish time	f_{TIMCLK}=48MHz	1		t_{TIMCLK}
			20.8		ns
f_{ext}	External clock frequency	f_{TIMCLK}=48MHz	0	$f_{TIMCLK/2}$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution	free count		16	Bit
				32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	f_{TIMCLK}=48MHz	1	65536	t_{TIMCLK}
			0.0208	1363	us
T_{MAX_COUNT}	Maximum possible count	f_{TIMCLK}=48MHz		16777216	t_{TIMCLK}
				349.5	ms

1. Guaranteed by design, not tested in production.

Table 7-11 General purpose timer characteristics

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{res}	Timer to distinguish time	f_{TIMCLK}=48MHz	1		t_{TIMCLK}
			20.8		ns
f_{ext}	External clock frequency	f_{TIMCLK}=48MHz	0	$f_{TIMCLK/2}$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	f_{TIMCLK}=48MHz	1	65536	t_{TIMCLK}
			0.0208	1363	us
T_{MAX_COUNT}	Maximum possible count	f_{TIMCLK}=48MHz		2147483648	t_{TIMCLK}
				44.7	s

1. Guaranteed by design, not tested in production.

Table 7-12 Low Power Timer Features

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{res}	Timer to distinguish time	f_{TIMCLK}=48MHz	1		t_{TIMCLK}
			20.8		ns
f_{ext}	External clock frequency	f_{TIMCLK}=48MHz	0	$f_{TIMCLK/2}$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	f_{TIMCLK}=48MHz	1	65536	t_{TIMCLK}
			0.0208	1363	us
T_{MAX_COUNT}	Maximum possible count	f_{TIMCLK}=48MHz		2147483648	t_{TIMCLK}
				44.7	s

1. Guaranteed by design, not tested in production.

Table 7-13 IWDT characteristics _

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=32.8KHz	0.13	64000	ms

1. Guaranteed by design, not tested in production.

Table 7-14 WWDT characteristics _

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=48MHz	0.085	699	ms

1. Guaranteed by design, not tested in production.

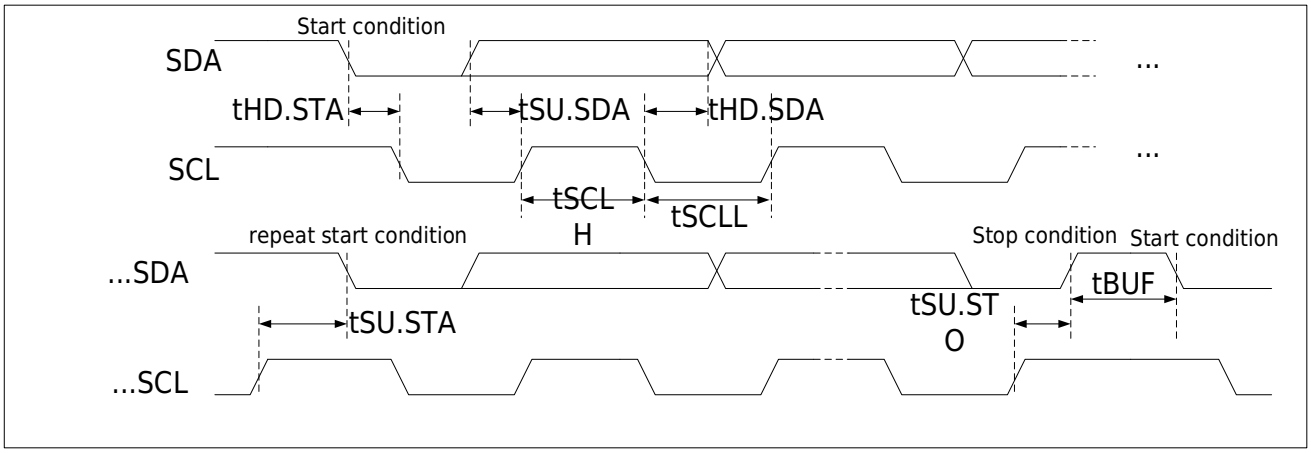
7.3.16 Communication Interface

7.3.16.1 I2C features

I2C interface characteristics are as follows:

Table 7-15 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
t_{SCLL}	SCL clock low time	5		1.25		0.5		us
t_{SCLH}	SCL clock high time	5		1.25		0.5		us
$t_{SU.SDA}$	SDA establishment time	250		100		50		ns
$t_{HD.SDA}$	SDA hold time	0		0		0		us
$t_{HD.STA}$	Start condition hold time	2.5		0.625		0.25		us
$t_{SU.STA}$	Repeated start condition establishment time	2.5		0.625		0.25		us
$t_{SU.STO}$	Stop condition establishment time	0.25		0.25		0.25		us
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		us



1. Guaranteed by design, not tested in production.

Figure 7-3 I2C Interface Timing

7.3.16.2 SPI characteristic

Table 7-16 SPI interface characteristics

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$t_{c(SCK)}$	Serial clock period	Host mode f_{PCLK} >= 32MHz	62.5		ns
		Host mode f_{PCLK} < 32MHz	$2\times t_{c(PCLK)}$		ns
		Slave mode f_{PCLK} > 16MHz	$8\times t_{c(PCLK)}$		ns
		Slave mode f_{PCLK} <= 16MHz	$4\times t_{c(PCLK)}$		ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	$0.45\times t_{c(SCK)}$	$0.55\times t_{c(SCK)}$	ns
		Slave mode	$0.5\times t_{c(SCK)}$		ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	$0.45\times t_{c(SCK)}$	$0.55\times t_{c(SCK)}$	ns
		Slave mode	$0.5\times t_{c(SCK)}$		ns
$t_{su(NSS)}$	Setup time selected by slave	Slave mode	$0.5\times t_{c(SCK)}$		ns
$t_{h(NSS)}$	Hold time selected by slave	Slave mode	$0.5\times t_{c(SCK)}$		ns
$t_{v(MO)}$	Effective time of host data output			3	ns
$t_{h(MO)}$	Hold time of host data output		-2		ns
$t_{v(SO)}$	Effective time of slave data output			$26 + 2\times t_{c(PCLK)}$	ns
$t_{h(SO)}$	Hold time of slave data output		$16 + 0.5\times t_{c(PCLK)}$		ns
$t_{su(MI)}$	Setup time of host data input		28		ns
$t_{h(MI)}$	Hold time of host data input		2		ns
$t_{su(SI)}$	Setup time of slave data input		2		ns
$t_{h(SI)}$	Hold time of slave data input		$2 + 1.5\times t_{c(PCLK)}$		ns

1. Guaranteed by design, not tested in production.

The waveform and timing parameters of the SPI interface signal are as follows:

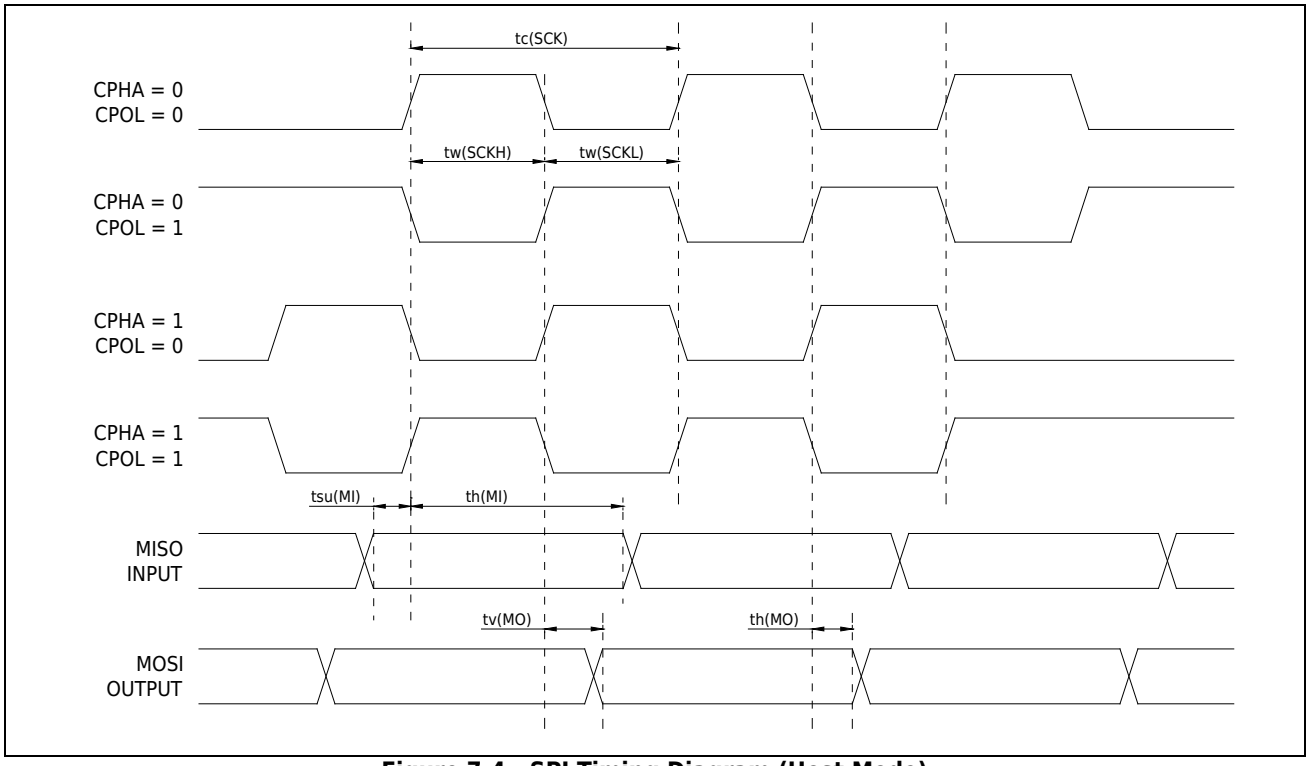


Figure 7-4 SPI Timing Diagram (Host Mode)

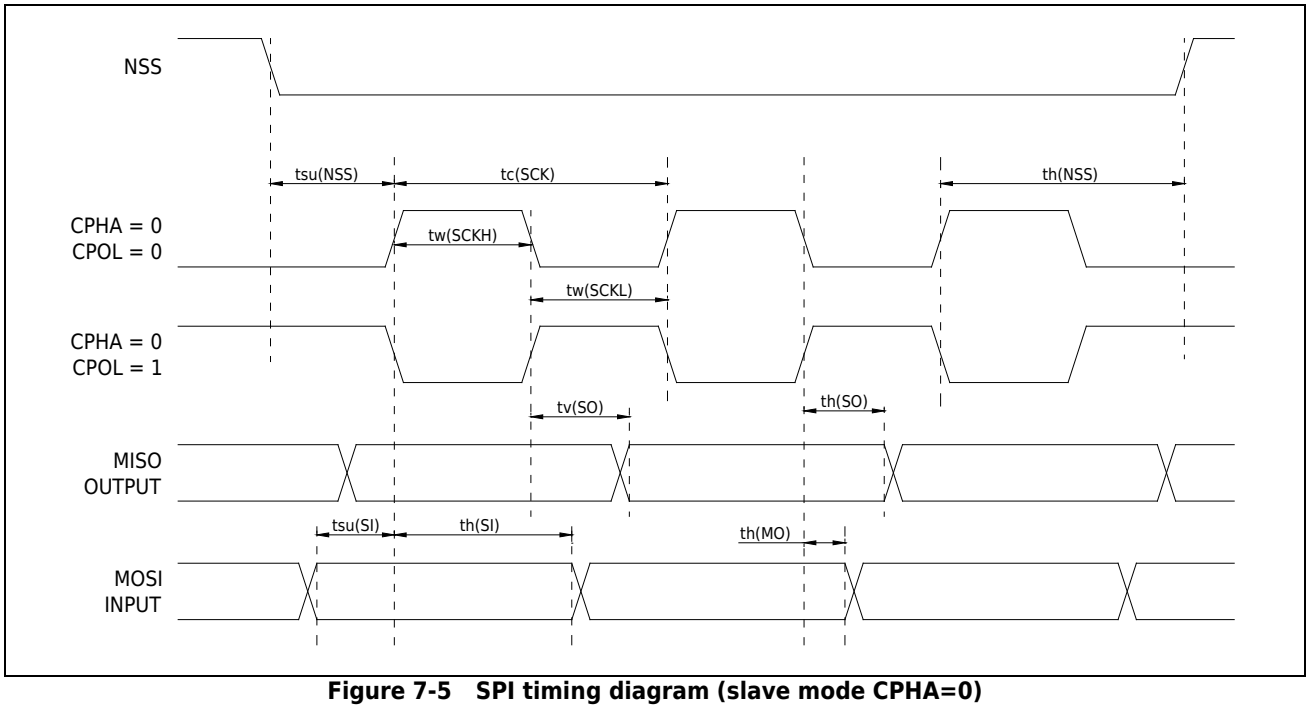


Figure 7-5 SPI timing diagram (slave mode CPHA=0)

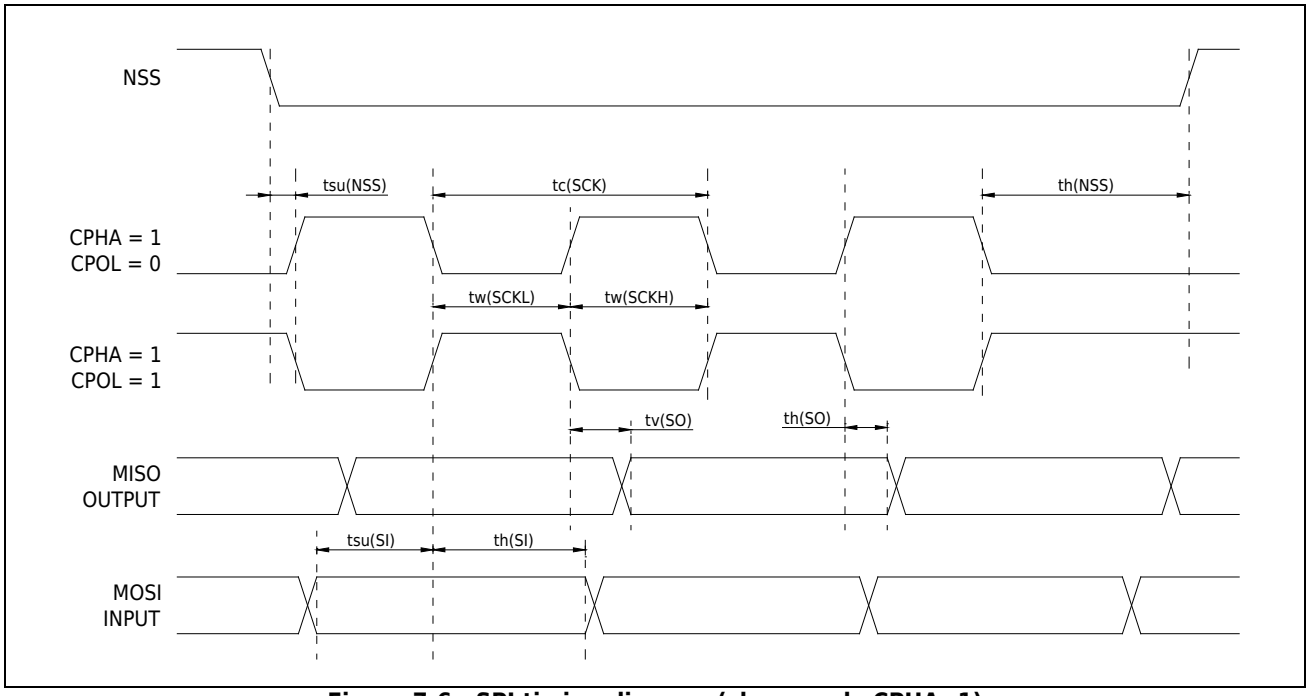
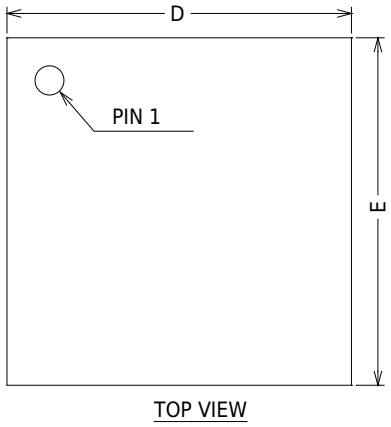


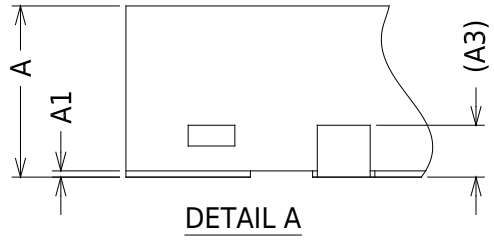
Figure 7-6 SPI timing diagram (slave mode CPHA=1)

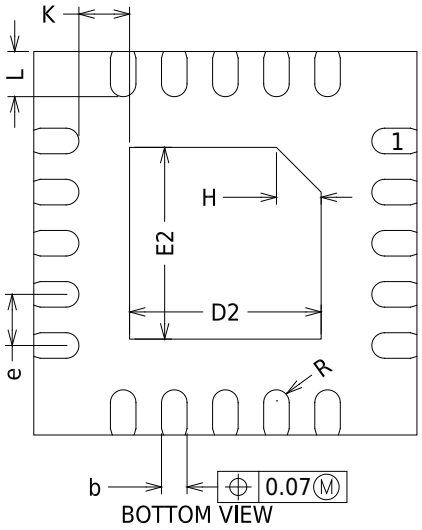
8 Package Information

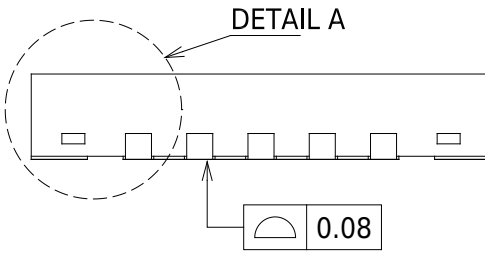
8.1 Package size

QFN20 package



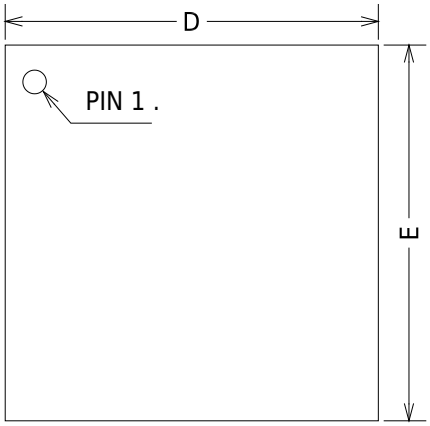




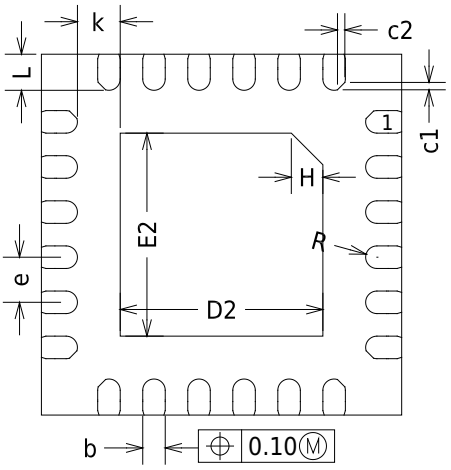


Symbol	QFN20 (3x3) millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H	0.35REF		
K	0.40REF		
L	0.25	0.35	0.45
R	0.075	-	-

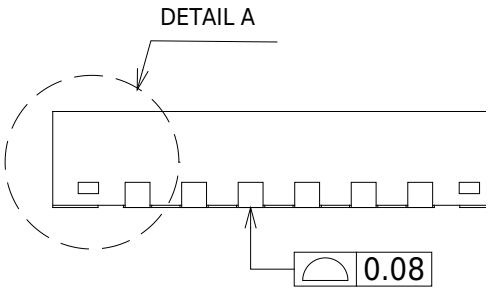
QFN24 package

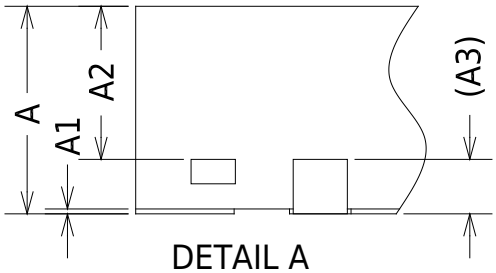


TOP VIEW



BOTTOM VIEW

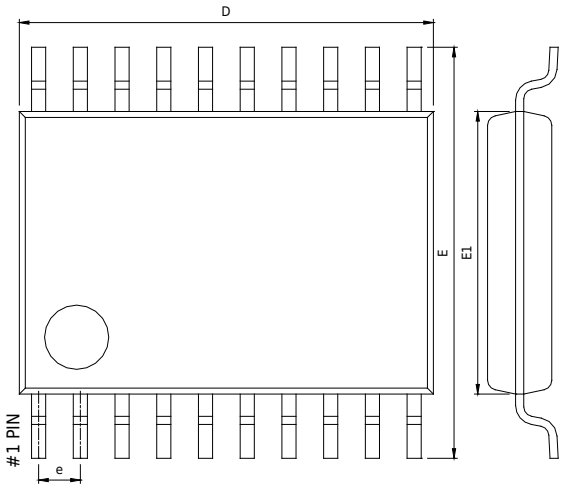


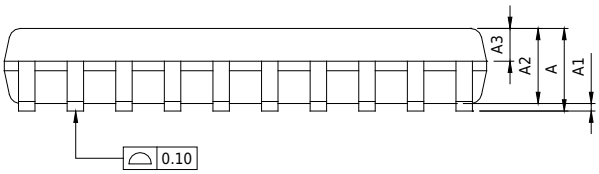


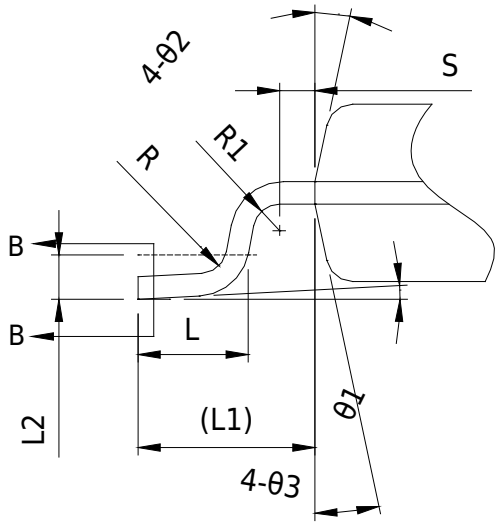
DETAIL A

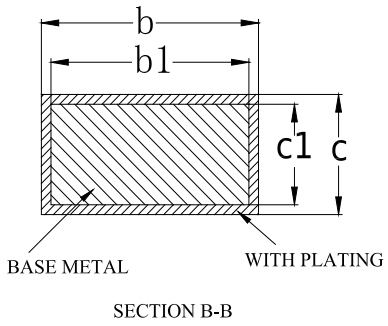
Symbol	QFN24 (4x4) millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.15	2.25	2.35
E	3.90	4.00	4.10
E2	2.15	2.25	2.35
e	0.40	0.50	0.60
L	0.35	0.40	0.45
K	0.30	--	--
H	0.35REF		
R	0.09	--	--
c1	--	0.08	--
c2	--	0.08	--

TSSOP20 package







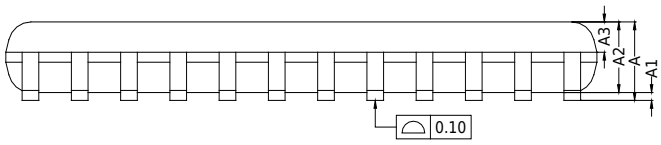


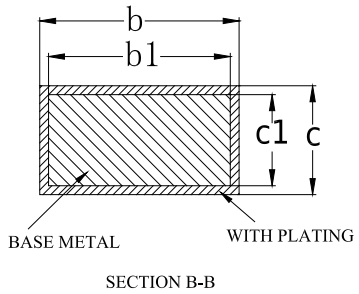
Symbol	TSSOP20 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	--	0.28
b1	0.20	0.22	0.24
c	0.10	--	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	--	--
R1	0.09	--	--
S	0.20	--	--
θ1	0°	--	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTE:

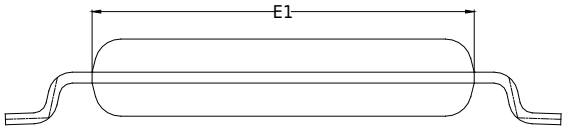
– Dimensions “D”and “E1”do not include mold flash.

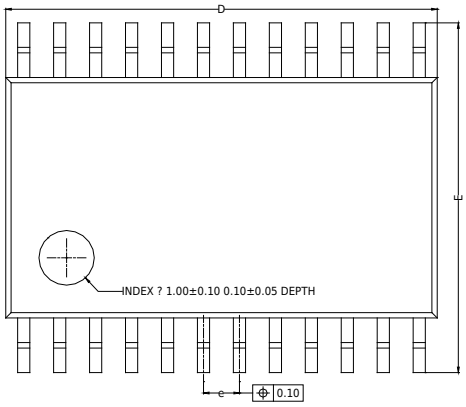
TSSOP24 package

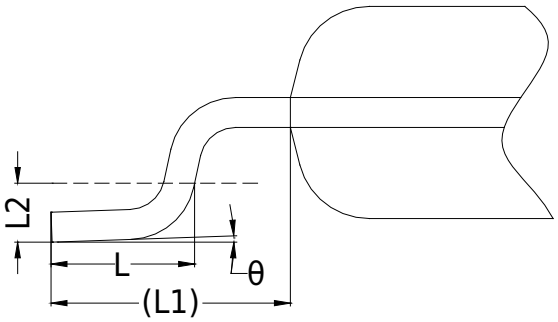




SECTION B-B







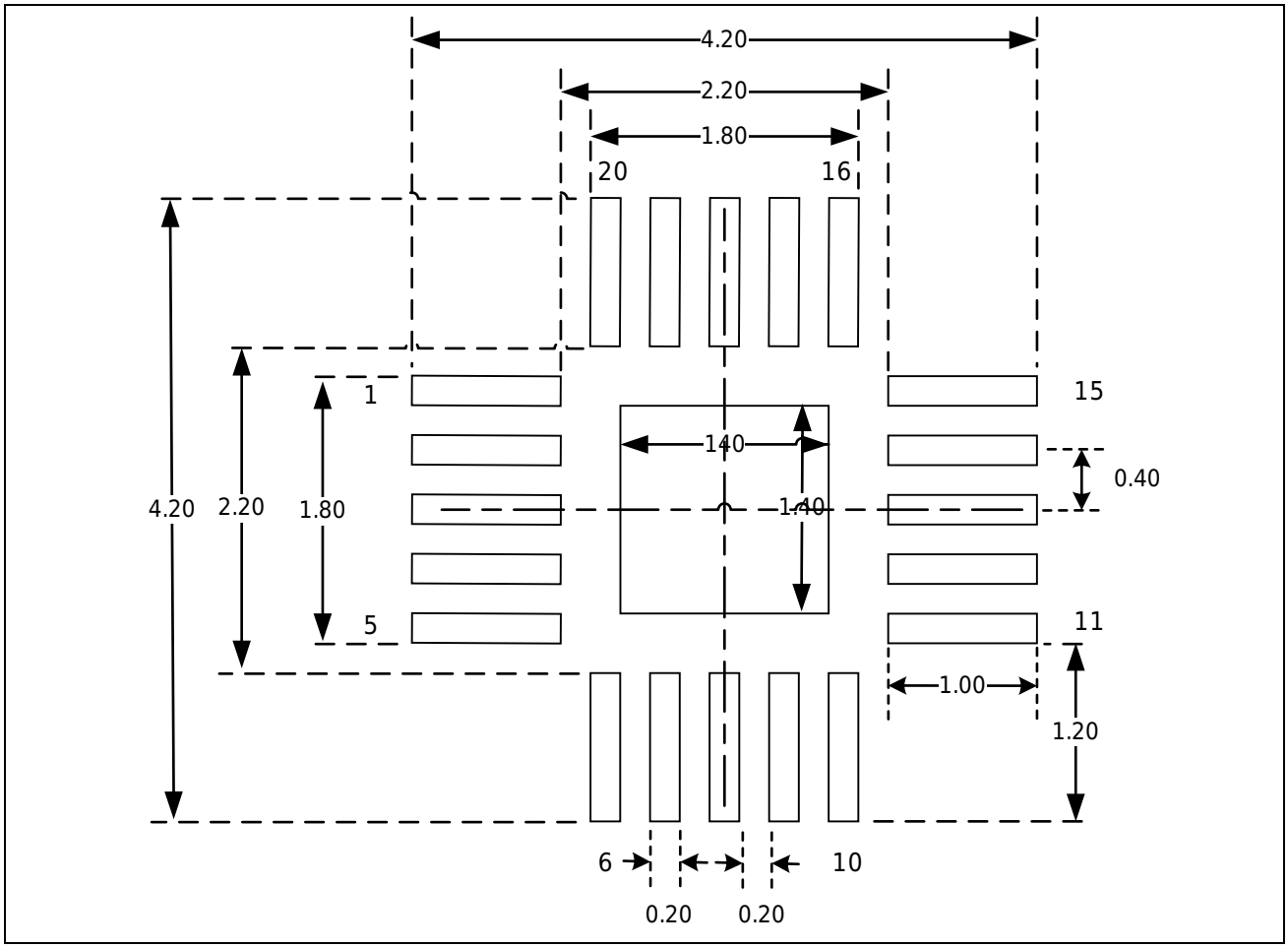
Symbol	TSSOP24 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	--	0.29
b1	0.19	0.22	0.25
c	0.10	--	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
θ	0	--	8°

NOTE:

– Dimensions “D”and “E1”do not include mold flash.

8.2 Schematic diagram of the pad

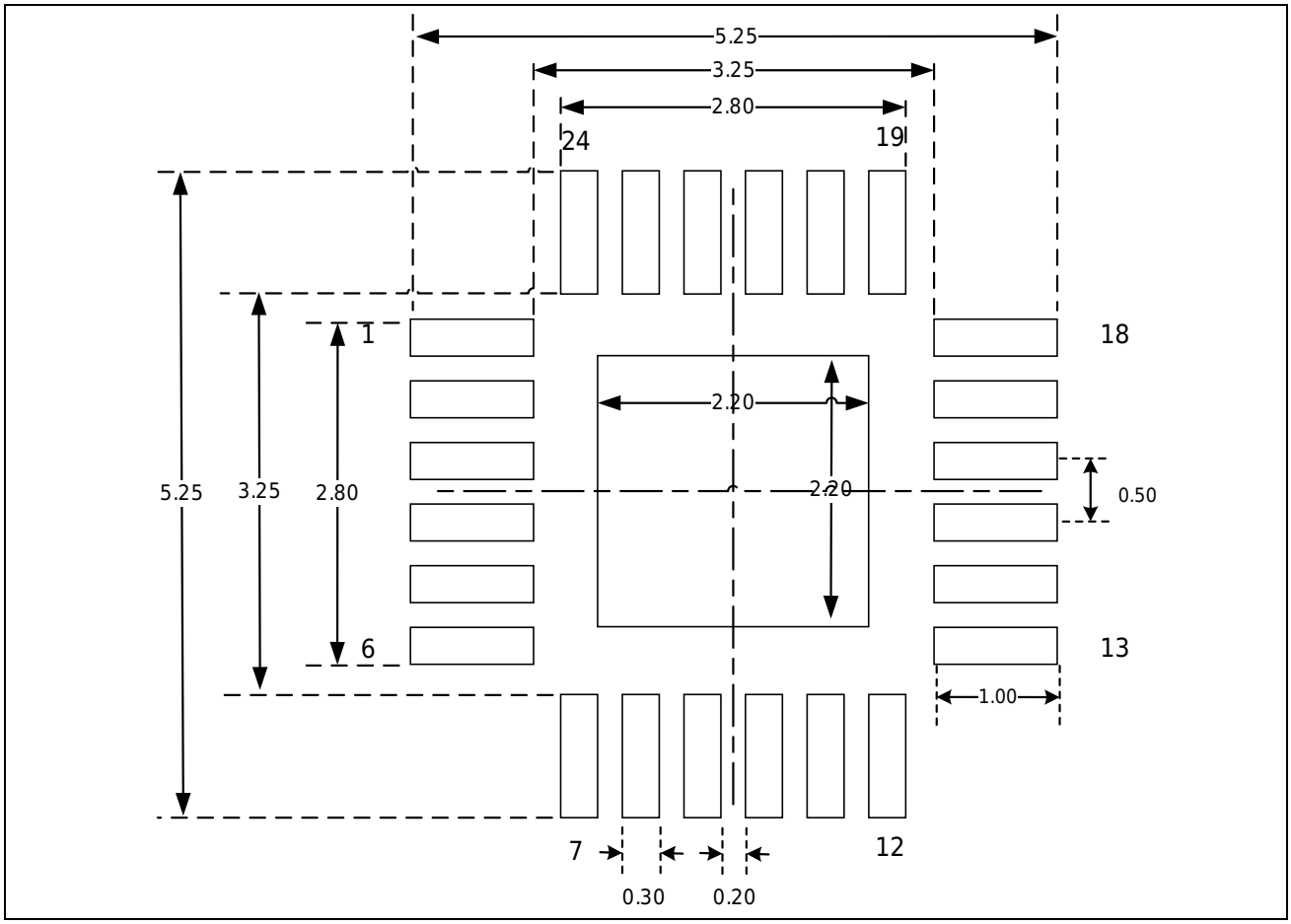
QFN20 package (3mm x 3mm)



NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

QFN24 package (4mm x 4mm)

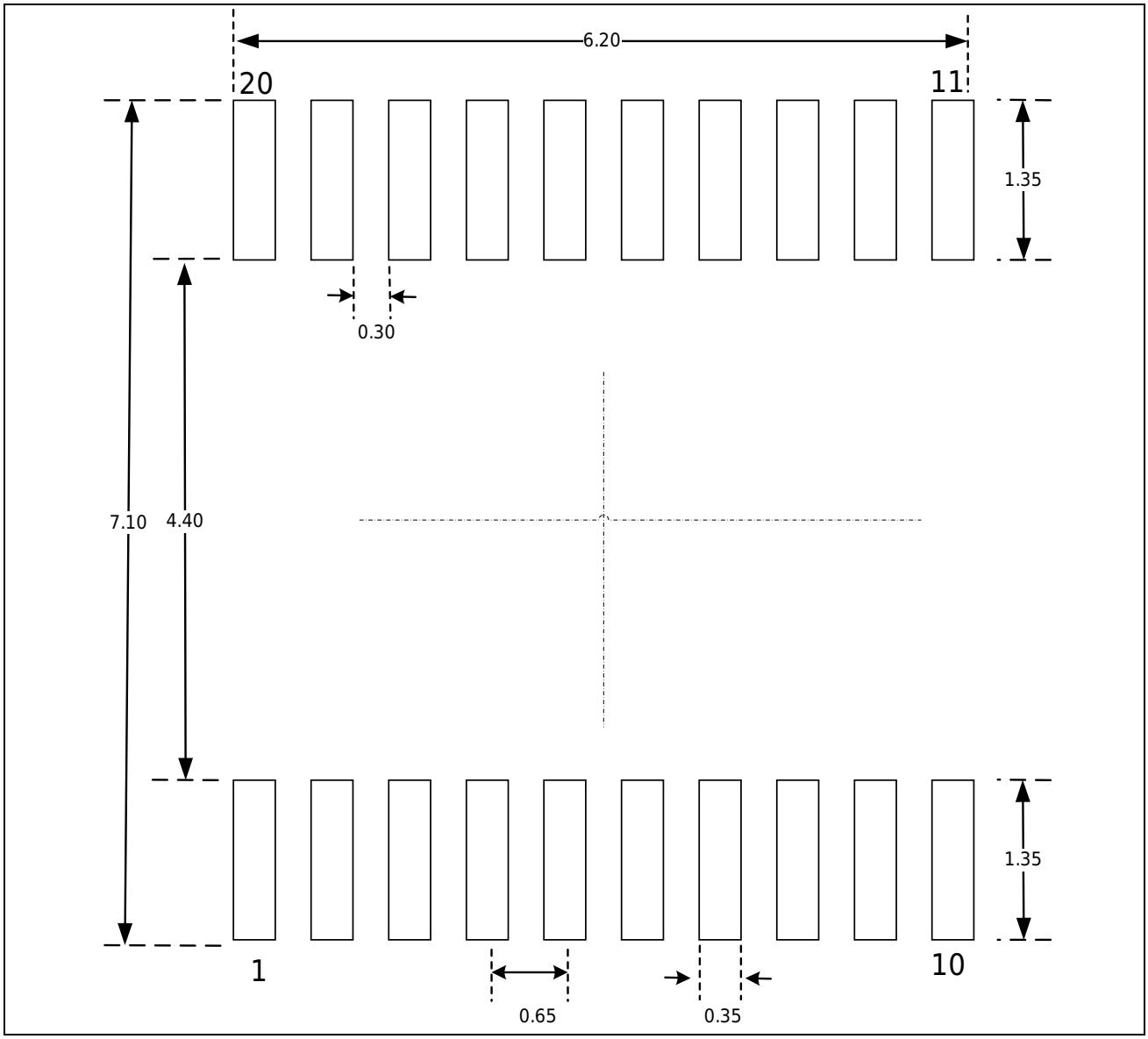


NOTE:

– Dimensions are expressed in millimeters.

– Dimensions are for reference only.

TSSOP20 package

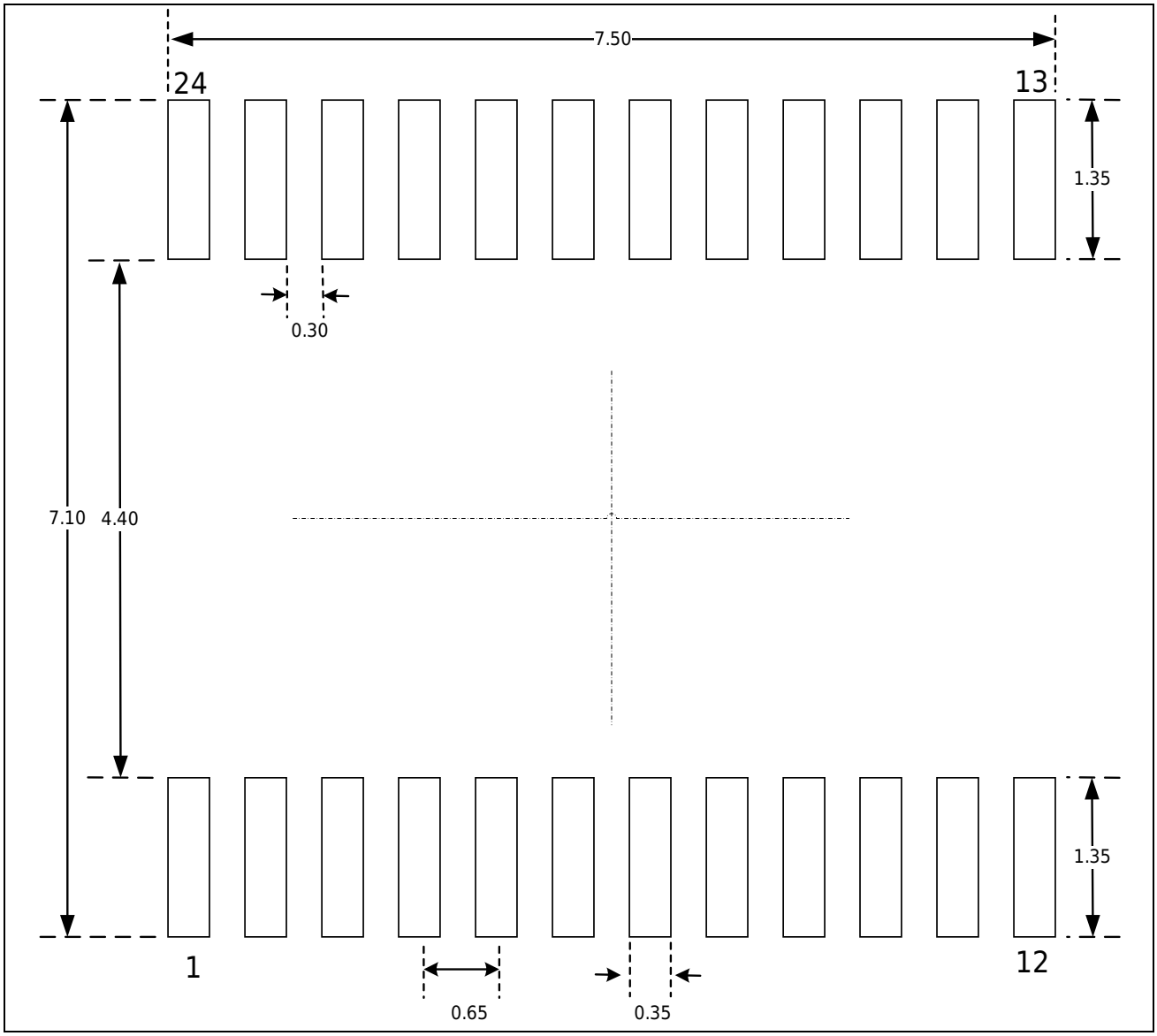


NOTE:

– Dimensions are expressed in millimeters.

– Dimensions are for reference only.

TSSOP24 package



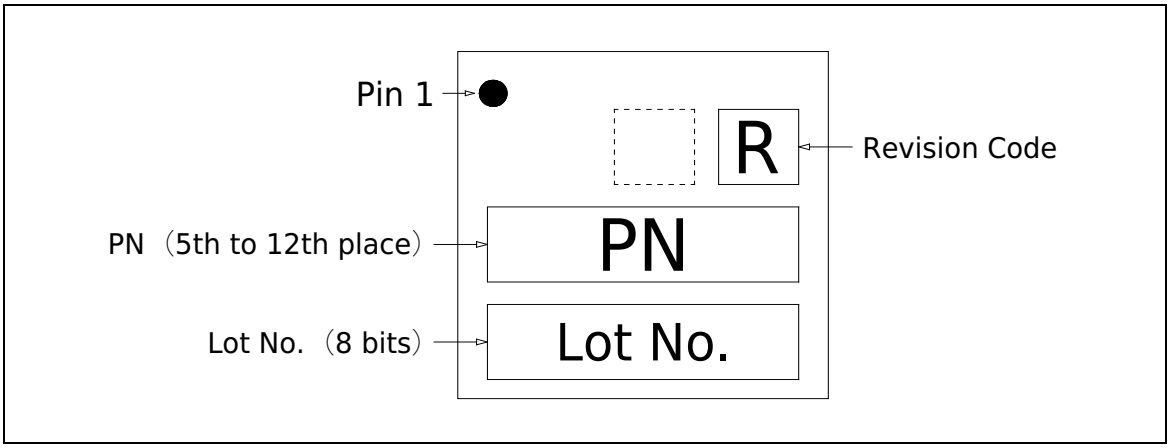
NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

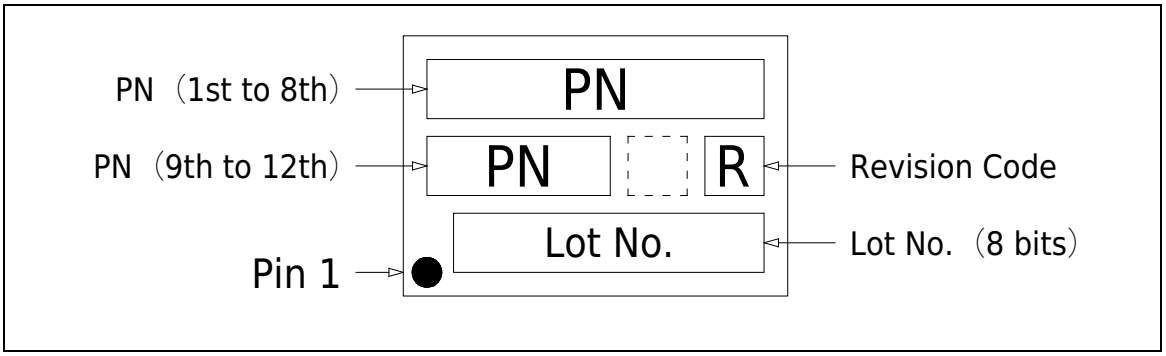
8.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

QFN20 package (3mm x 3mm) / QFN24 package (4mm x 4mm)



TSSOP20 package / TSSOP24 package



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

8.4 Package thermal resistance coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature Tj (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD}. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

The junction temperature T_j on the surface of the chip when the chip is operating at the specified operating ambient temperature must not exceed the maximum junction temperature T_J allowed by the chip.

Table 8-1 Thermal resistance coefficient of each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
QFN20 3mm x 3mm / 0.4mm pitch	70 +/- 10%	℃/W
QFN24 4mm x 4mm / 0.5mm pitch	53 +/- 10%	℃/W
TSSOP20	91 +/- 10%	℃/W
TSSOP24	80 +/- 10%	℃/W

9 Ordering Information

Part Number	HC32F002C4PZ-TSSOP20	HC32F002C4PZ-TSSOP20TR	HC32F002C4UZ-ZFN20TR	HC32F002D4PZ-TSSOP24	HC32F002D4PZ-TSSOP24TR	HC32F002D4UZ-QFN24TR
Main frequency (MHz)	48	48	48	48	48	48
Kernel	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
Flash (KB)	18	18	18	18	18	18
RAM (KB)	2	2	2	2	2	2
GPIO	17+1	17+1	17+1	21+1	21+1	21+1
Working voltage (V)	1.7 - 5.5	1.7 - 5.5	1.7 - 5.5	1.7 - 5.5	1.7 - 5.5	1.7 - 5.5
Low power timer	1	1	1	1	1	1
basic timer	3	3	3	3	3	3
Universal timer	1	1	1	1	1	1
Advanced timer	1	1	1	1	1	1
LPUART	2	2	2	2	2	2
I2C	1	1	1	1	1	1
SPI	1	1	1	1	1	1
ADC (10bit)	11ch	11ch	11ch	14ch	14ch	14ch
LVD	✓	✓	✓	✓	✓	✓
LVR	✓	✓	✓	✓	✓	✓
Working temperature (°C)	-20~105	-20~105	-20~105	-20~105	-20~105	-20~105
Encapsulation Form:	TSSOP20	TSSOP20	QFN20(3*3)	TSSOP24	TSSOP24	QFN24(4*4)
Pin number	20	20	20	24	24	24
Foot spacing	0.65mm	0.65mm	0.4mm	0.65mm	0.65mm	0.5mm
Product thickness	1.2mm	1.2mm	0.55mm	1.2mm	1.2mm	0.75mm
Packing	Tube	Tape & Reel	Tape & Reel	Tube	Tape & Reel	Tape & Reel

– Before ordering, please contact the sales window for the latest mass production information.

Version revision history

version number	Revision Date	modify the content
Rev1.0	2021/12/31	The first draft is released.
Rev1.1	2022/03/09	The company logo is updated.
Rev1.2	2022/10/14	1) Added two models: HC32F002C4PZ-TSSOP20TR, HC32F002D4PZ-TSSOP24TR; 2) In the “Pin Configuration Diagram” chapter, add the TR model, and modify the title of the corresponding diagram; 3) In the “Ordering Information” chapter, add new models, and the packaging method is Tape & Reel.
Rev1.21	2023/06/21	In the "Pin Configuration Diagram" chapter, QFN encapsulation adds GND information.