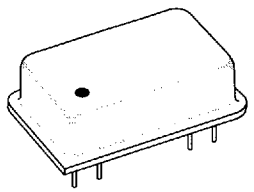
HC1199

244.01 MHz ECL Clock

- *Ideal for High-Resolution Video Display Controllers*
- *Very Low Jitter and Excellent Symmetry*
- *Rugged, Hermetic Metal DIP Case*

The HC1199 pixel or "dot" clock is designed for the graphics controller of 2048 × 1536 pixel non-interlaced video displays with 60 Hz vertical scan rates. The 244.01 MHz fundamental oscillation mode, made possible by surface acoustic wave (SAW) technology, provides compact size, and low jitter and power consumption. The MC100E ECLinPS™ differential output is fully compatible with 100K ECL loads.



DIP14S-8 Case (pin-out A)

ABSOLUTE MAXIMUM RATINGS

Rating		Value	Units
Power Supply Voltage (V_{EE}) Pin 1 to Case Ground		-8 to 0	VDC
Output Current (CLOCK, Pin 7 or $\overline{CLOCK}$, Pin 8)		50	mA
Case Temperature	Powered	0 to +70	°C
	Storage	-40 to +85	

ELECTRICAL CHARACTERISTICS

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Output Frequency	Absolute Frequency	F_O	1	243.949	—	244.071	MHz
	Relative to 244.010 MHz	ΔF_O		—	—	±250	ppm
Output	Output HIGH Voltage	V_{OH}	2	-1.035	-0.955	-0.880	V
	Output LOW Voltage	V_{OL}		-1.810	-1.705	-1.610	V
	Rise or Fall Time (20-80%)	t_r or t_f		—	655	—	ps
	Symmetry		3	45	50	55	%
	Period or Delay Jitter (rms)		4	—	1	—	ps
DC Power Supply	Operating Voltage	V_{EE}	1, 2	-4.800	-4.5	-4.200	VDC
	Operating Current	I_{EE}		—	60	85	mA
Operating Ambient Temperature		T_A	1	0	—	+70	°C

Lid Symbolization (YY = year, WW = week number)	RFM HC1199 244.01 MHz YYWW

Notes:

1. Unless noted otherwise, all specifications apply with CLOCK and $\overline{CLOCK}$ terminated in 50 Ω to -2.0 VDC per the specified test fixture for any combination of V_{EE} and T_A within the specified operating ranges.
2. Input/output voltage limits apply only for V_{EE} = -4.50 ±0.01 VDC. Additional V_{EE} variation (within specification) must be added to these limits.
3. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of CLOCK and $\overline{CLOCK}$.
4. Applies to delay jitter between CLOCK and $\overline{CLOCK}$ after 20 cycles and to period jitter of CLOCK or $\overline{CLOCK}$. Measurements are made with the Tektronix CSA803 communications signal analyzer with at least 1000 samples. Jitter induced by electrical noise on the V_{EE} input or mechanical vibration is not included. Dedicated external voltage regulation and careful PCB layout are recommended for minimum jitter.
5. The design, manufacturing process, and specifications of this device are subject to change without notice.
6. One or more of the following U. S. patents apply: 4,616,197, 4,670,681, and 4,760,352.
7. ECLinPS™ is a trademark of Motorola, Inc. RFM® is a registered trademark of RF Monolithics, Inc.
8. CAUTION: ELECTROSTATIC SENSITIVE DEVICE. Observe precautions for handling.