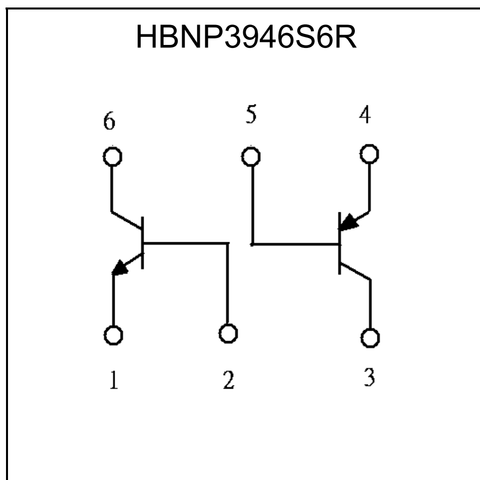
General Purpose NPN / PNP Epitaxial Planar Transistors (dual transistors)

HBNP3946S6R

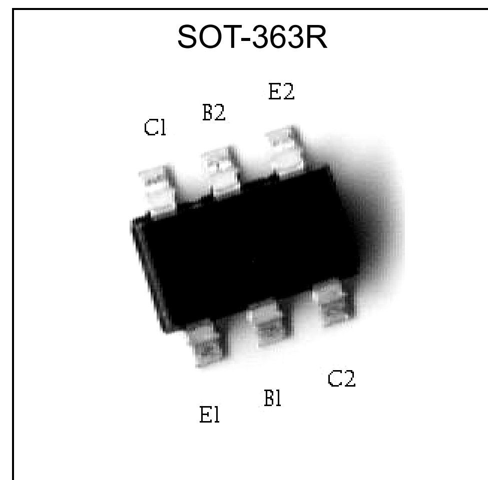
Features

- Includes a 2N3904 chip and 2N3906 chip in a SOT-363R package.
- Mounting possible with SOT-323 automatic mounting machines.
- Transistor elements are independent, eliminating interference.
- Mounting cost and area can be cut in half.

Equivalent Circuit

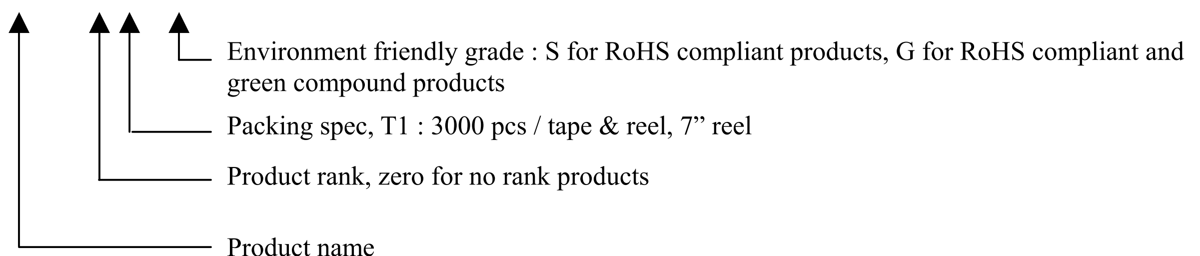


Outline



Ordering Information

Device	Package	Shipping
HBNP3946S6R-0-T1-G	SOT-363 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		TR1 (NPN)	TR2 (PNP)	
Collector-Base Voltage	V_{CBO}	60	-40	V
Collector-Emitter Voltage	V_{CEO}	40	-40	V
Emitter-Base Voltage	V_{EBO}	6	-5	V
Collector Current	I_C	200	-200	mA
Power Dissipation	Pd	300(total) *1		mW
Junction Temperature	Tj	150		°C
Storage Temperature	Tstg	-55~+150		°C

Note: *1 200mW per element must not be exceeded.

Characteristics (Ta=25°C)

• **TR1 (NPN)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	60	-	-	V	I_C=10μA
BV_{CEO}	40	-	-	V	I_C=1mA
BV_{EBO}	6	-	-	V	I_E=10μA
I_{CBO}	-	-	100	nA	V_{CB}=50V
I_{CEX}	-	-	50	nA	V_{CE}=30V, V_{EB}=3V
I_{EBO}	-	-	100	nA	V_{EB}=5V
$V_{CE(sat)}$	-	-	0.2	V	I_C=10mA, I_B=1mA
*$V_{CE(sat)}$	-	-	0.3	V	I_C=50mA, I_B=5mA
$V_{BE(sat)}$	0.65	-	0.85	V	I_C=10mA, I_B=1mA
*$V_{BE(sat)}$	-	-	0.95	V	I_C=50mA, I_B=5mA
h_{FE}	40	-	-	-	V_{CE}=1V, I_C=100μA
h_{FE}	70	-		-	V_{CE}=1V, I_C=1mA
h_{FE}	100	-	300	-	V_{CE}=1V, I_C=10mA
h_{FE}	60	-	-	-	V_{CE}=1V, I_C=50mA
*h_{FE}	30	-	-	-	V_{CE}=1V, I_C=100mA

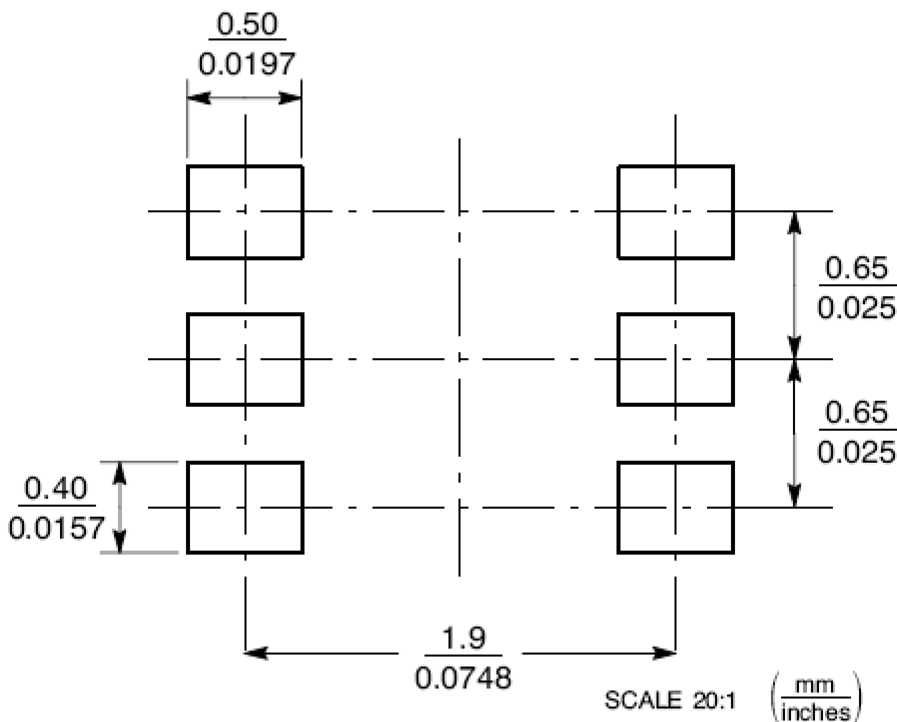
*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

• **TR2 (PNP)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-40	-	-	V	I_C=-10μA
BV_{CEO}	-40	-	-	V	I_C=-1mA
BV_{EBO}	-5	-	-	V	I_E=-10μA
I_{CBO}	-	-	-100	nA	V_{CB}=-40V
I_{CEX}	-	-	-50	nA	V_{CE}=-30V,V_{EB}=-3V
I_{EBO}	-	-	-100	nA	V_{EB}=-4V
$V_{CE(sat)}$	-	-	-0.25	V	I_C=-10mA, I_B=-1mA
$V_{CE(sat)}$	-	-	-0.4	V	I_C=-50mA, I_B=-5mA
$V_{BE(sat)}$	-0.65	-	-0.85	V	I_C=-10mA, I_B=-1mA
$V_{BE(sat)}$	-	-	-0.95	V	I_C=-50mA, I_B=-5mA
h_{FE}	60	-	-	-	V_{CE}=-1V, I_C=-100μA
h_{FE}	80	-	-	-	V_{CE}=-1V, I_C=-1mA
h_{FE}	100	-	300	-	V_{CE}=-1V, I_C=-10mA
h_{FE}	60	-	-	-	V_{CE}=-1V, I_C=-50mA
*h_{FE}	30	-	-	-	V_{CE}=-1V, I_C=-100mA

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Recommended Soldering Footprint



Typical Characteristics

- **TR1 (NPN)**

$T_J = 25°C$
$T_J = 125°C$

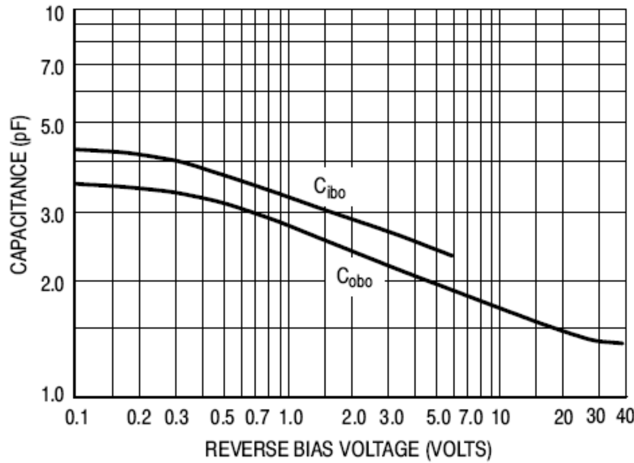


Figure 1. Capacitance

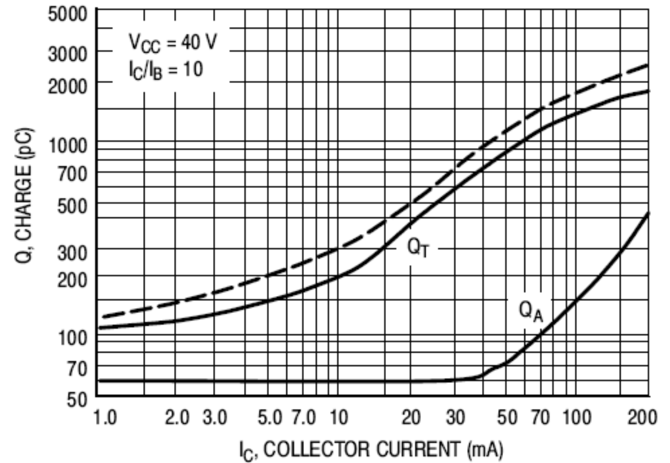


Figure 2. Charge Data

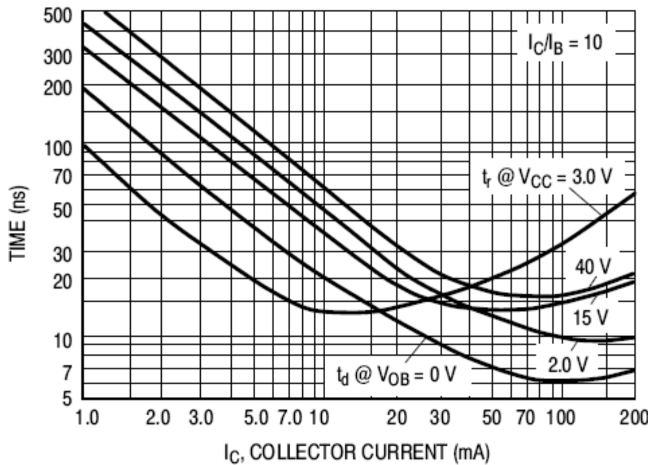


Figure 3. Turn−On Time

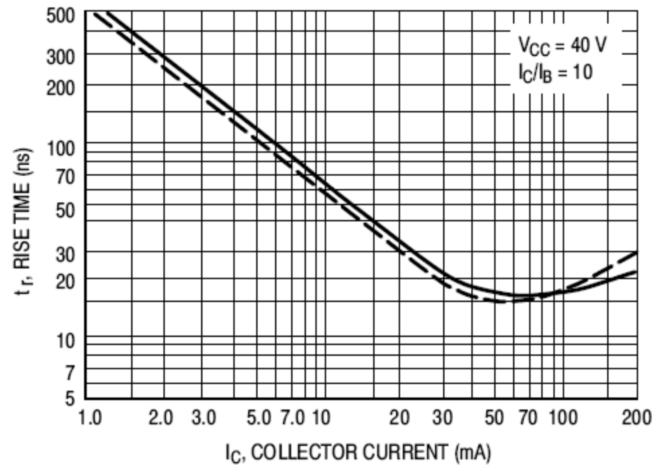


Figure 4. Rise Time

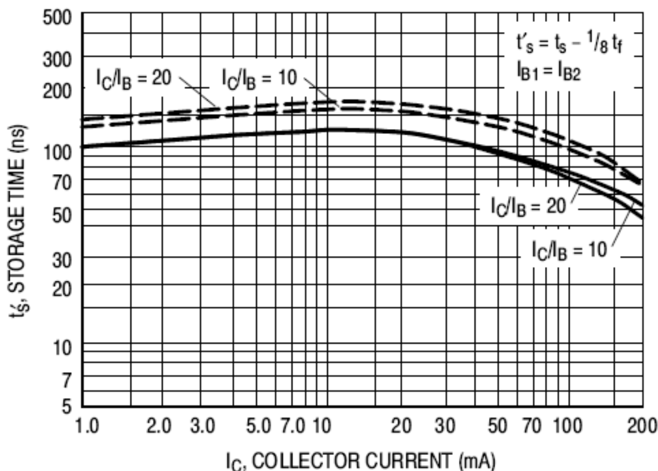


Figure 5. Storage Time

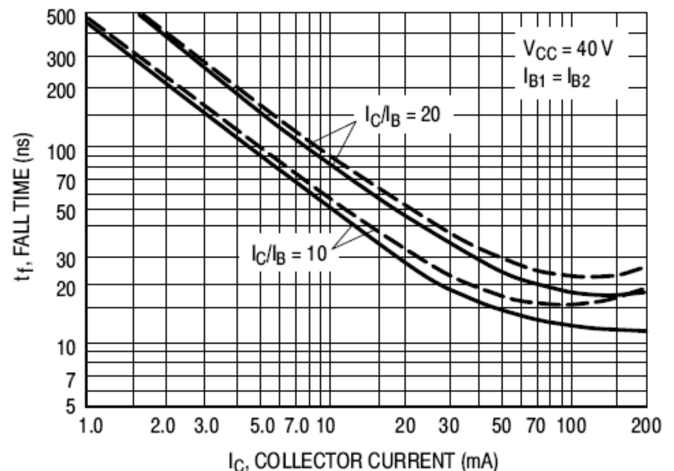


Figure 6. Fall Time

NOISE FIGURE VARIATIONS

(V_{CE} = 5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

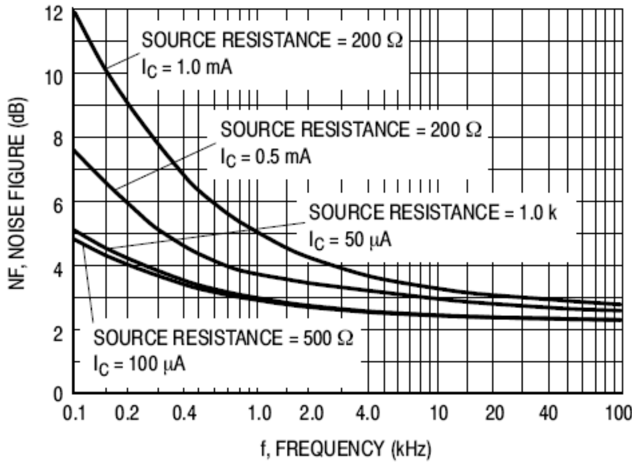


Figure 7.

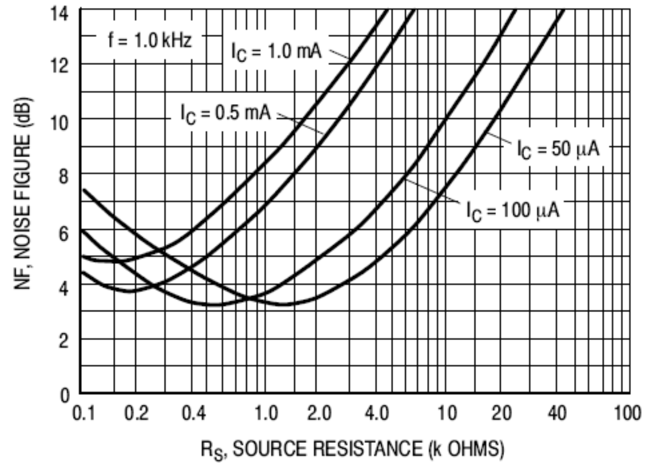


Figure 8.

h PARAMETERS

(V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C)

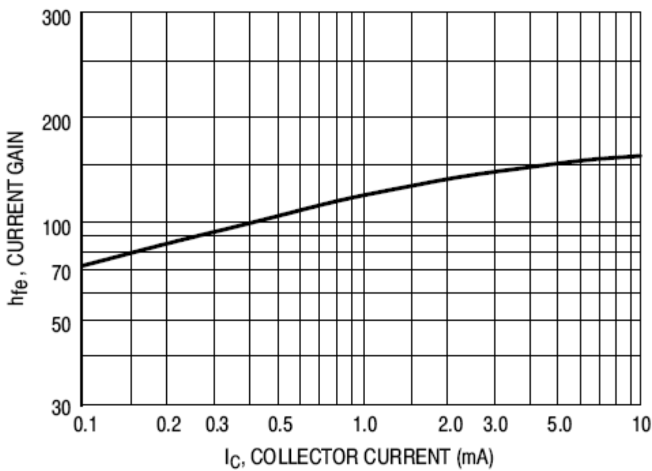


Figure 9. Current Gain

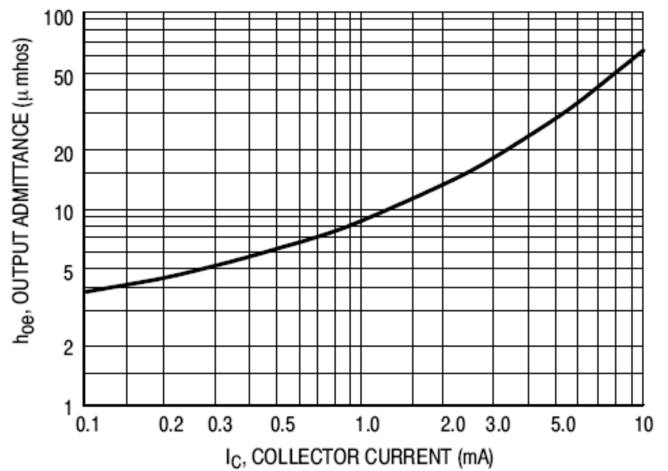


Figure 10. Output Admittance

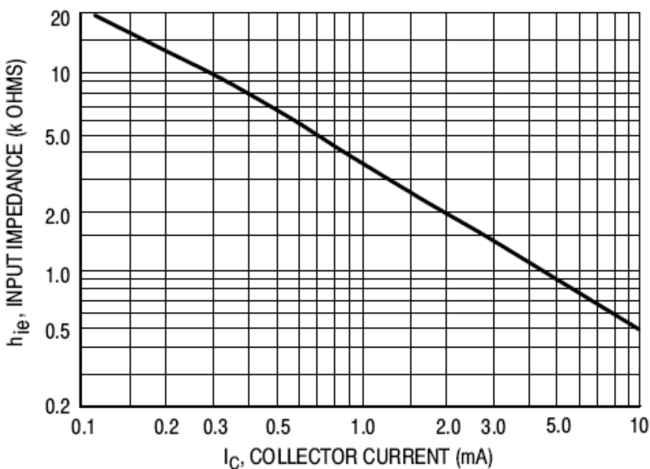


Figure 11. Input Impedance

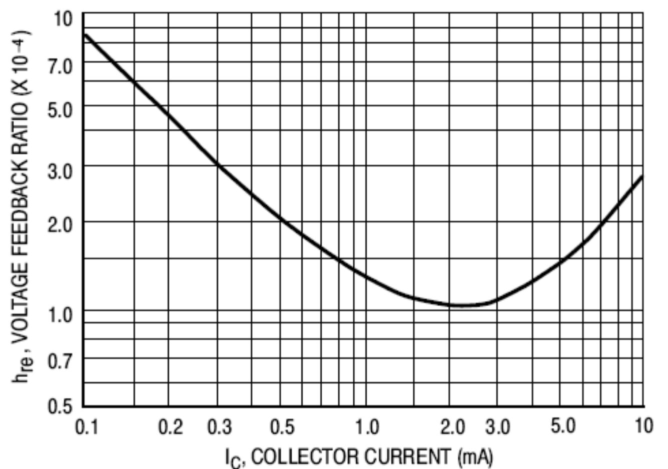


Figure 12. Voltage Feedback Ratio

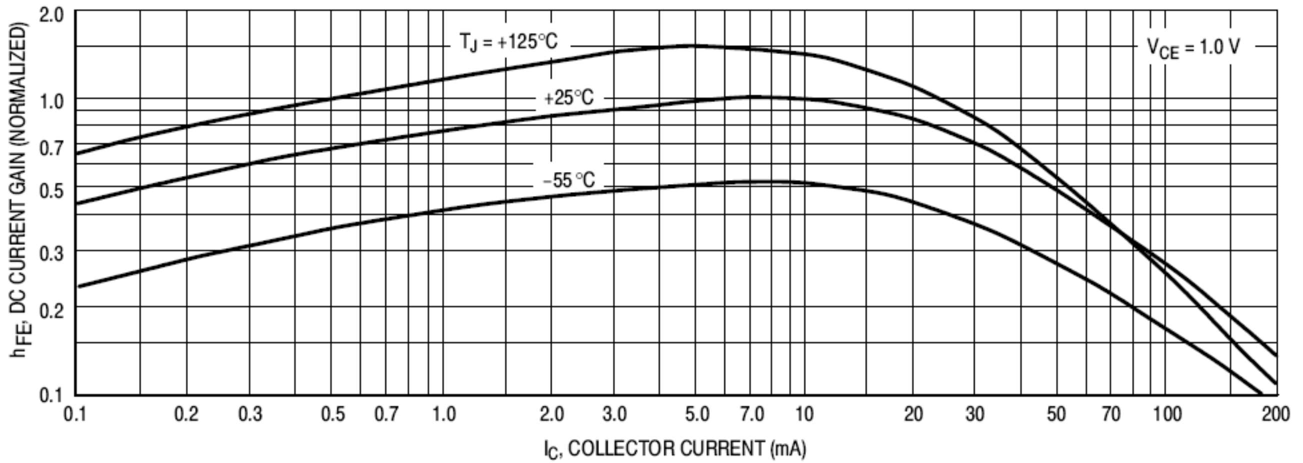


Figure 13. DC Current Gain

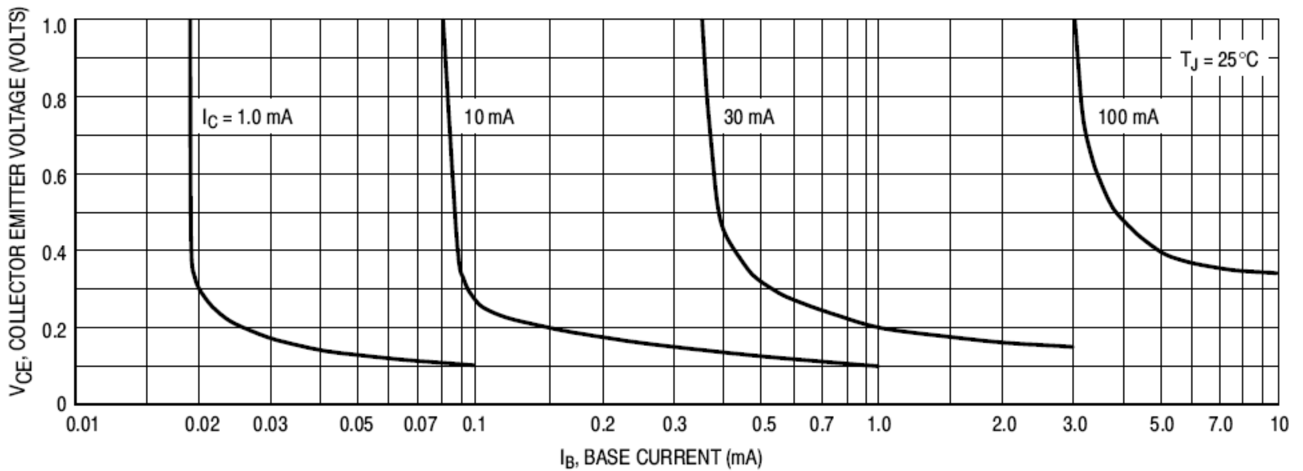


Figure 14. Collector Saturation Region

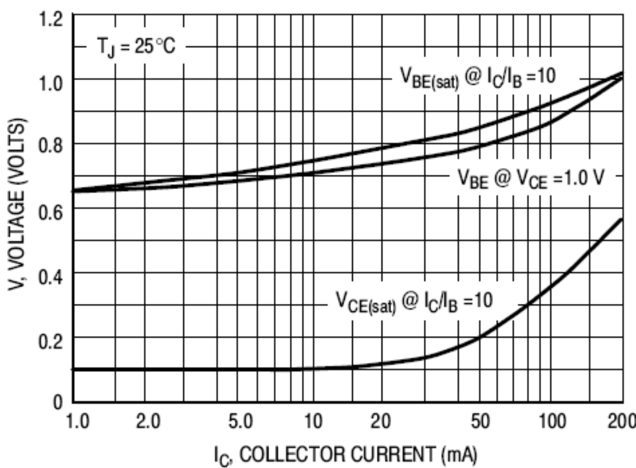


Figure 15. "ON" Voltages

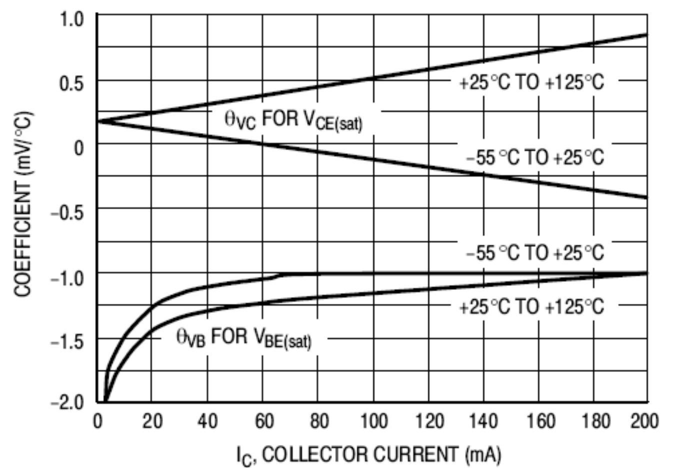


Figure 16. Temperature Coefficients

• **TR2 (PNP)**

— T_J = 25°C
- - T_J = 125°C

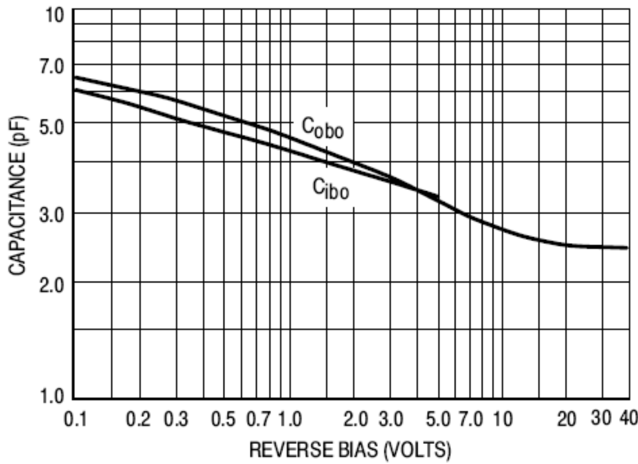


Figure 1. Capacitance

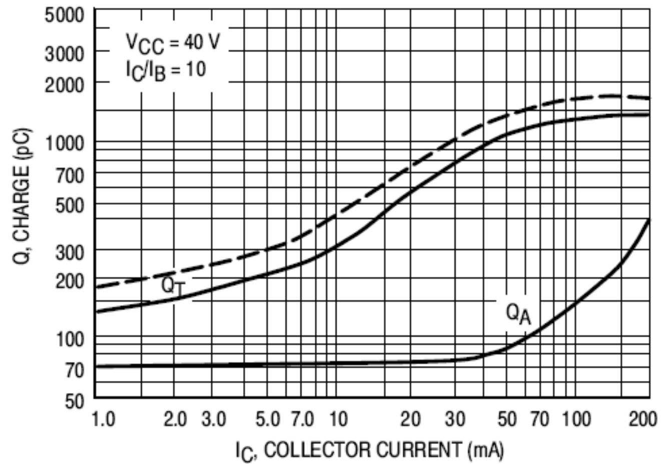


Figure 2. Charge Data

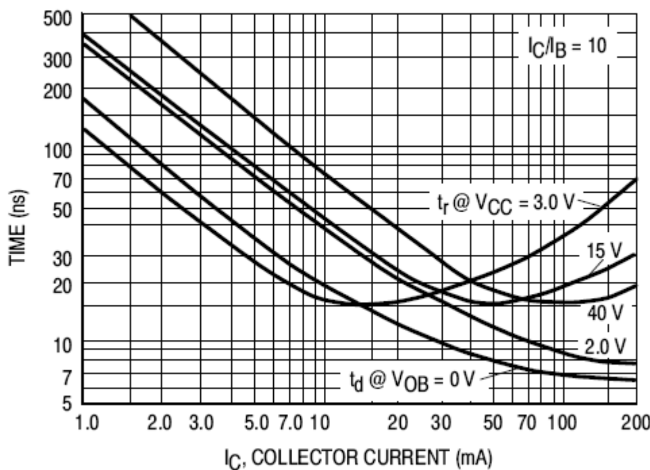


Figure 3. Turn–On Time

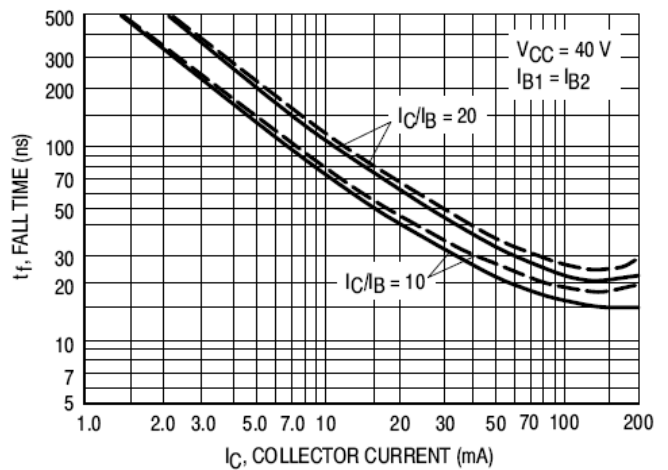


Figure 4. Fall Time

NOISE FIGURE VARIATIONS

(V_{CE} = –5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

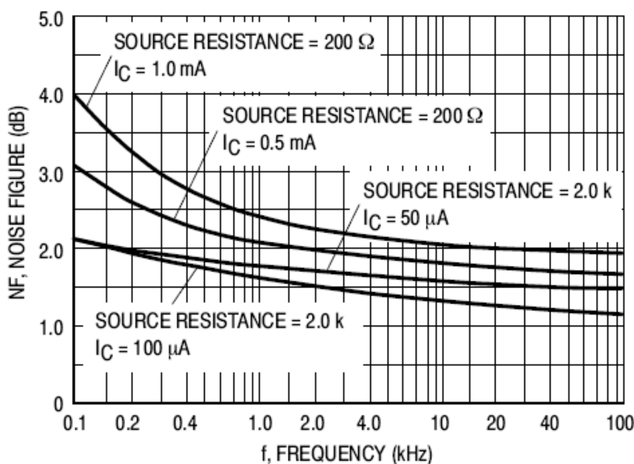


Figure 5.

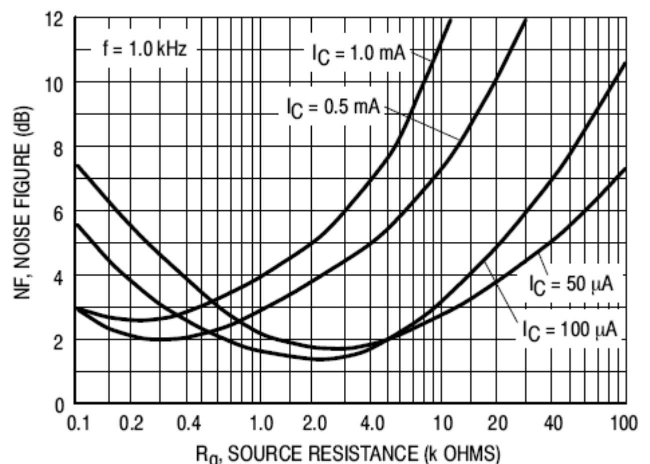


Figure 6.

h PARAMETERS

(V_{CE} = –10 Vdc, f = 1.0 kHz, T_A = 25°C)

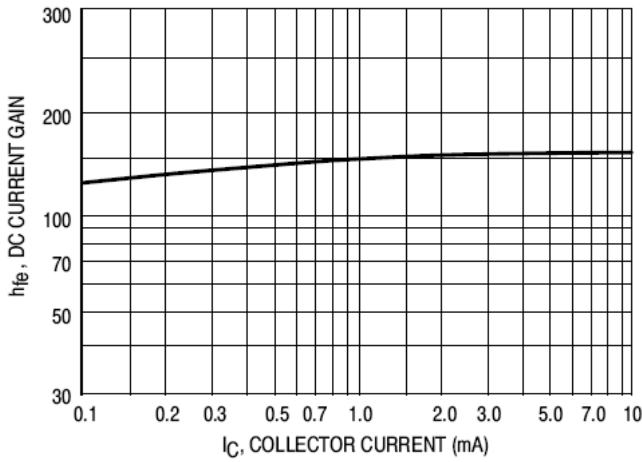


Figure 7. Current Gain

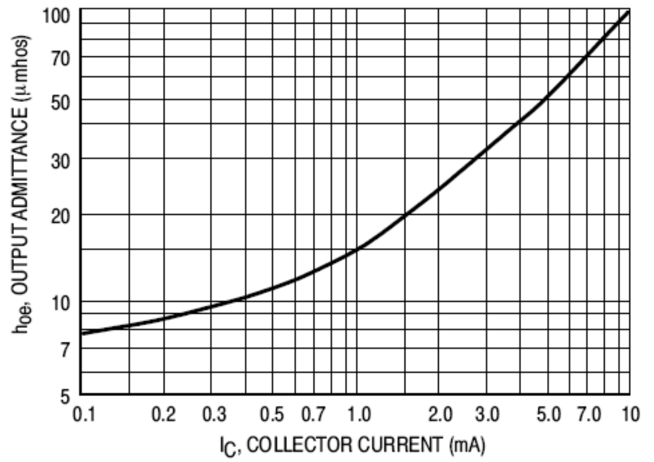


Figure 8. Output Admittance

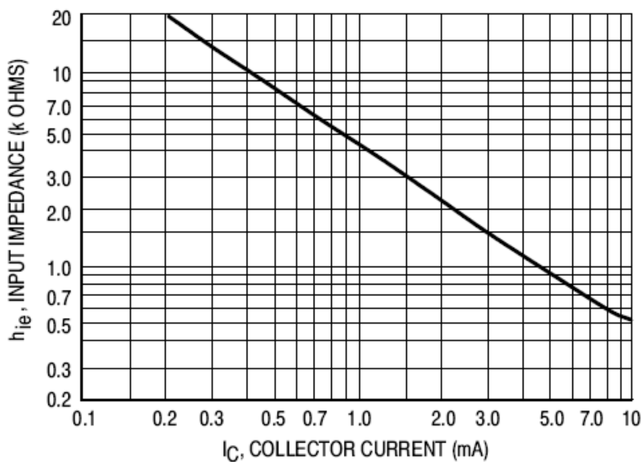


Figure 9. Input Impedance

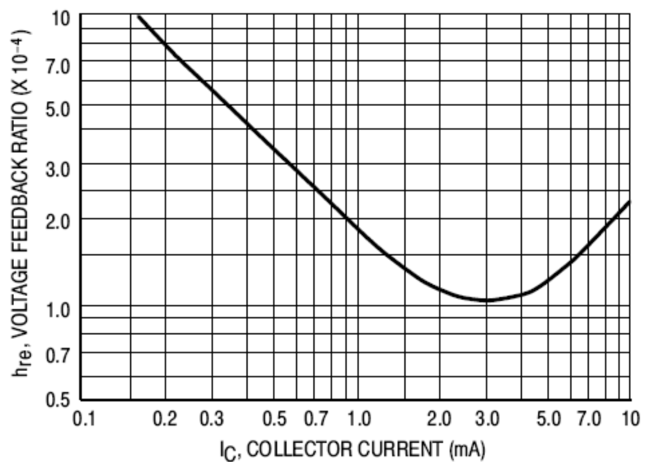


Figure 10. Voltage Feedback Ratio

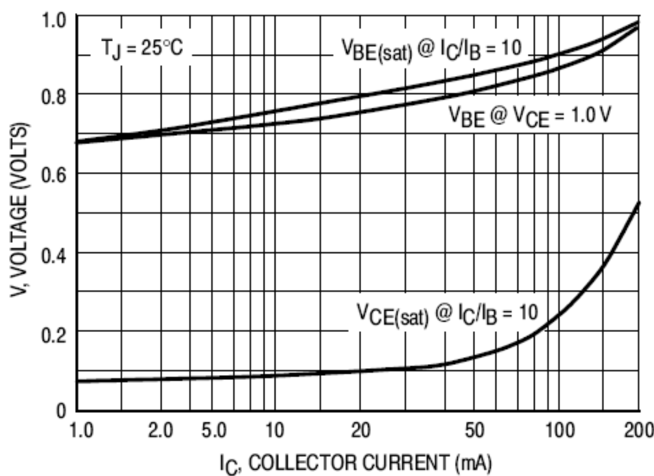


Figure 11. “ON” Voltages

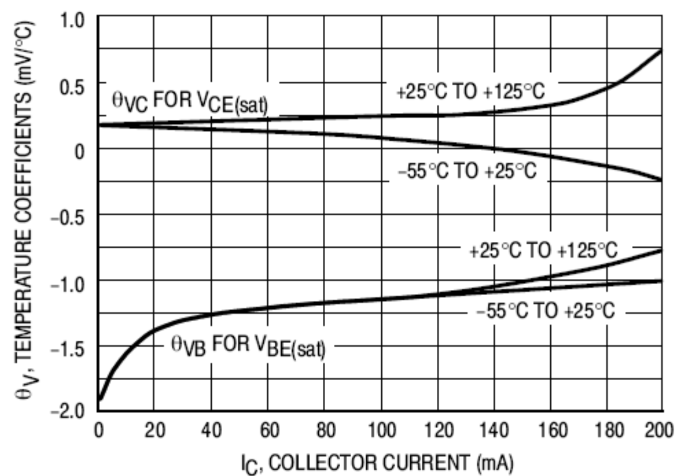


Figure 12. Temperature Coefficients

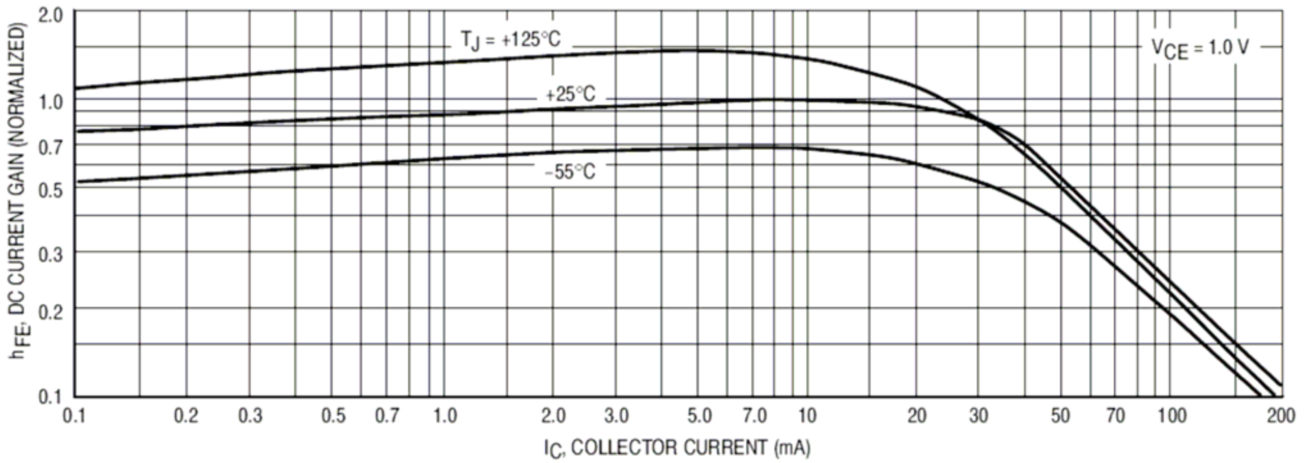


Figure 13. DC Current Gain

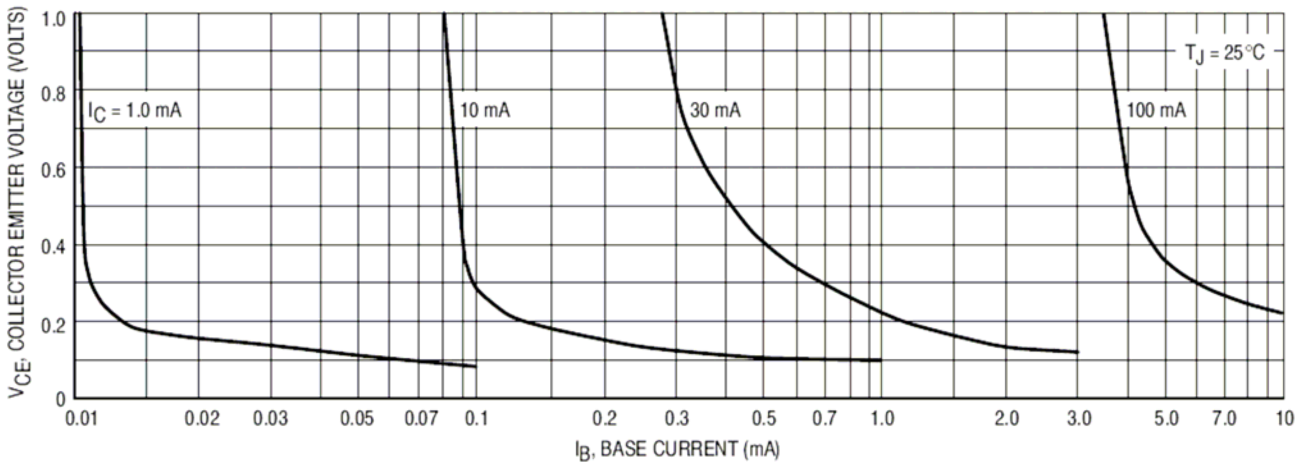
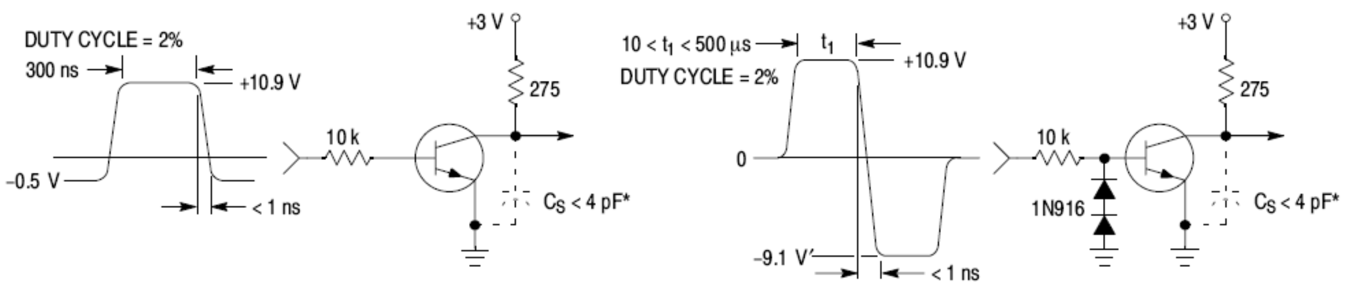


Figure 14. Collector Saturation Region

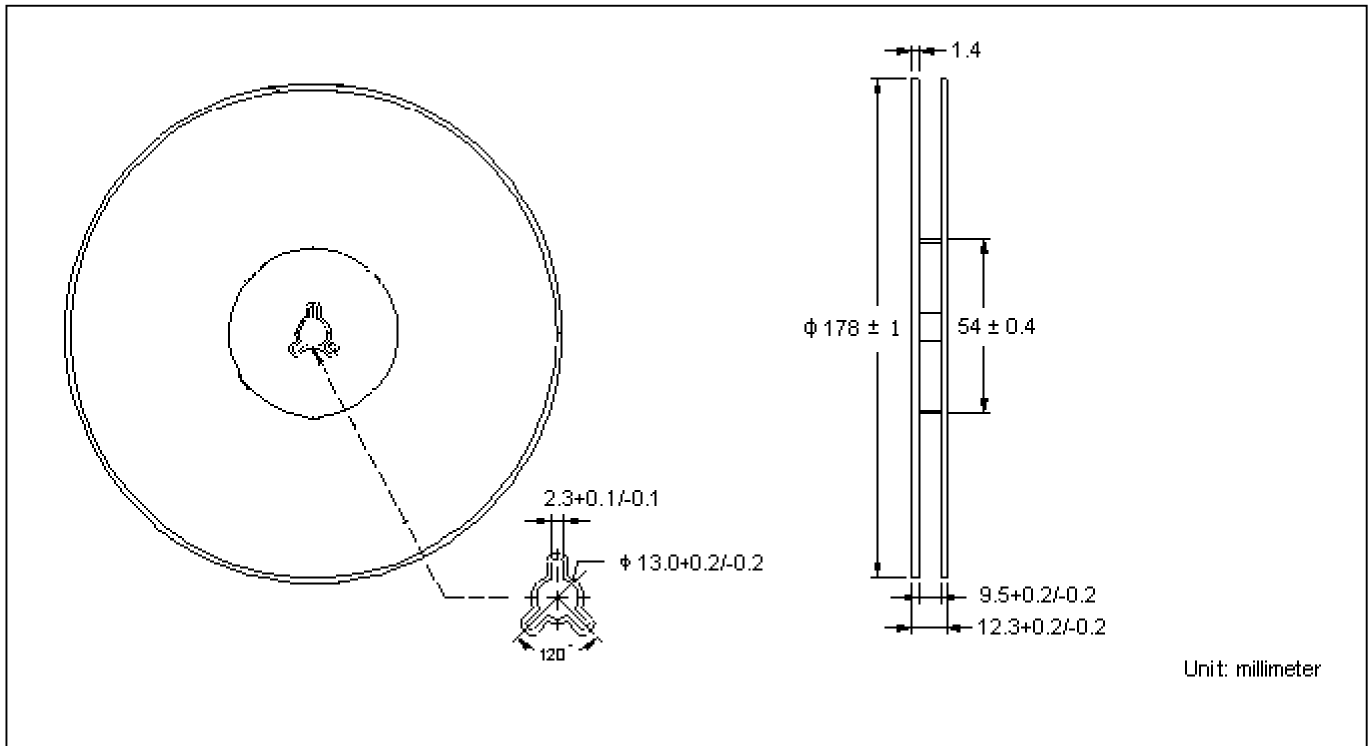


* Total shunt capacitance of test jig and connectors

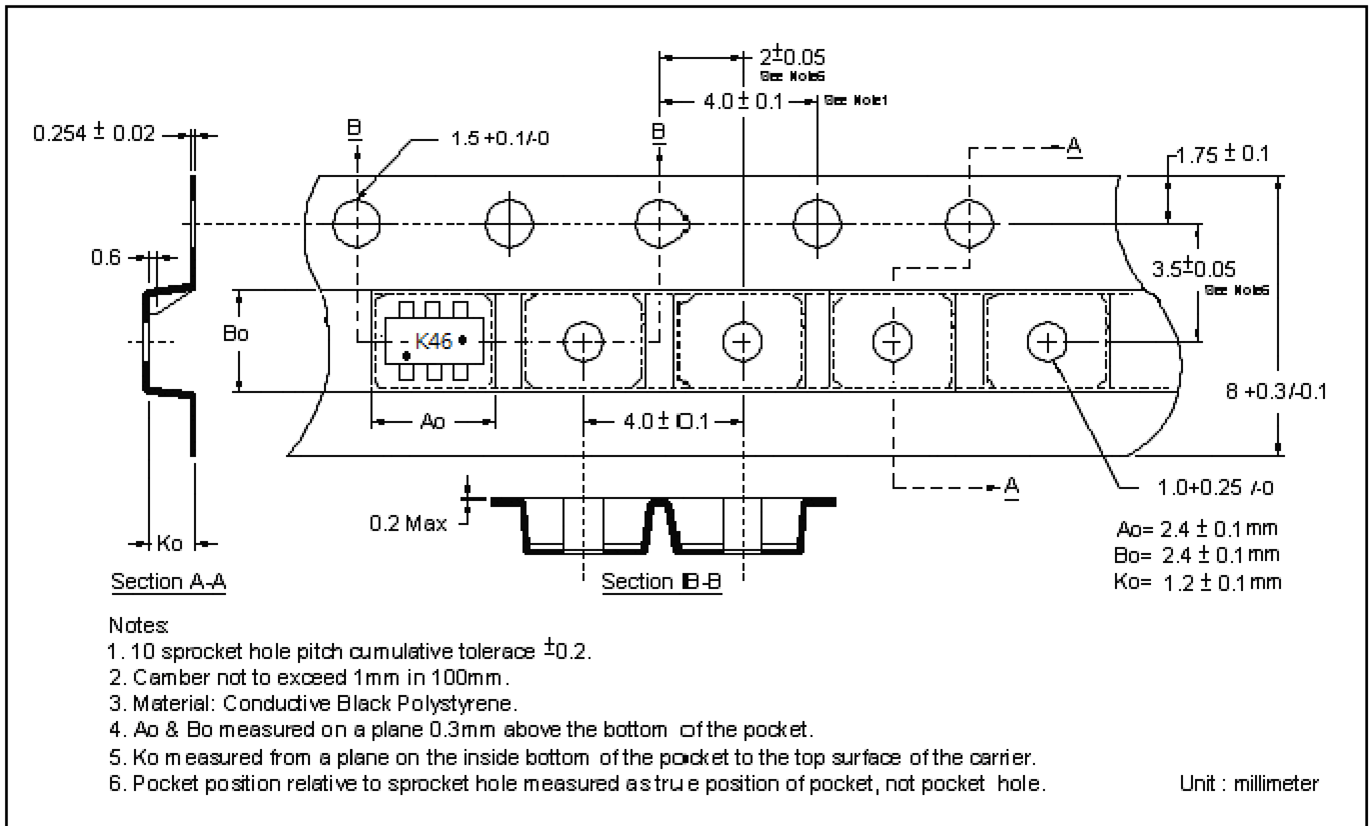
Delay and Rise Time Equivalent Test Circuit

Storage and Fall Time Equivalent Test Circuit

Reel Dimension



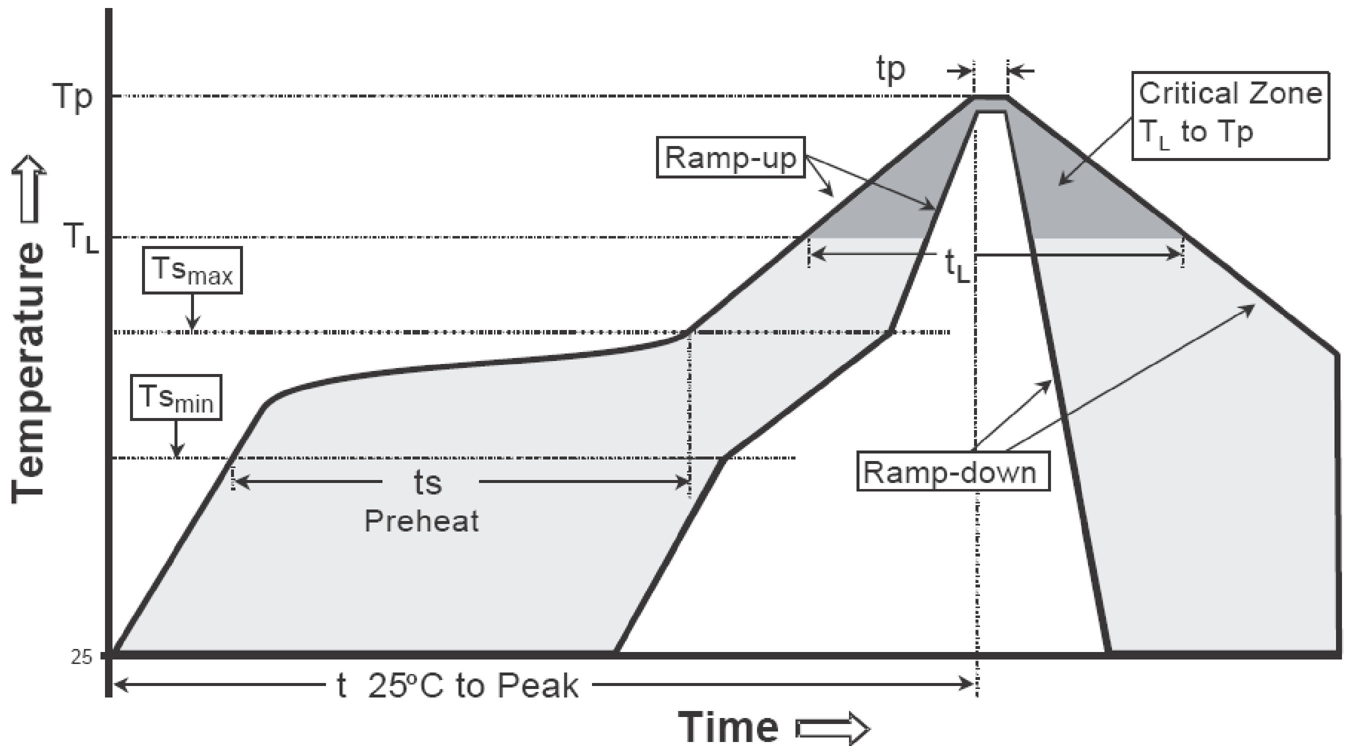
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

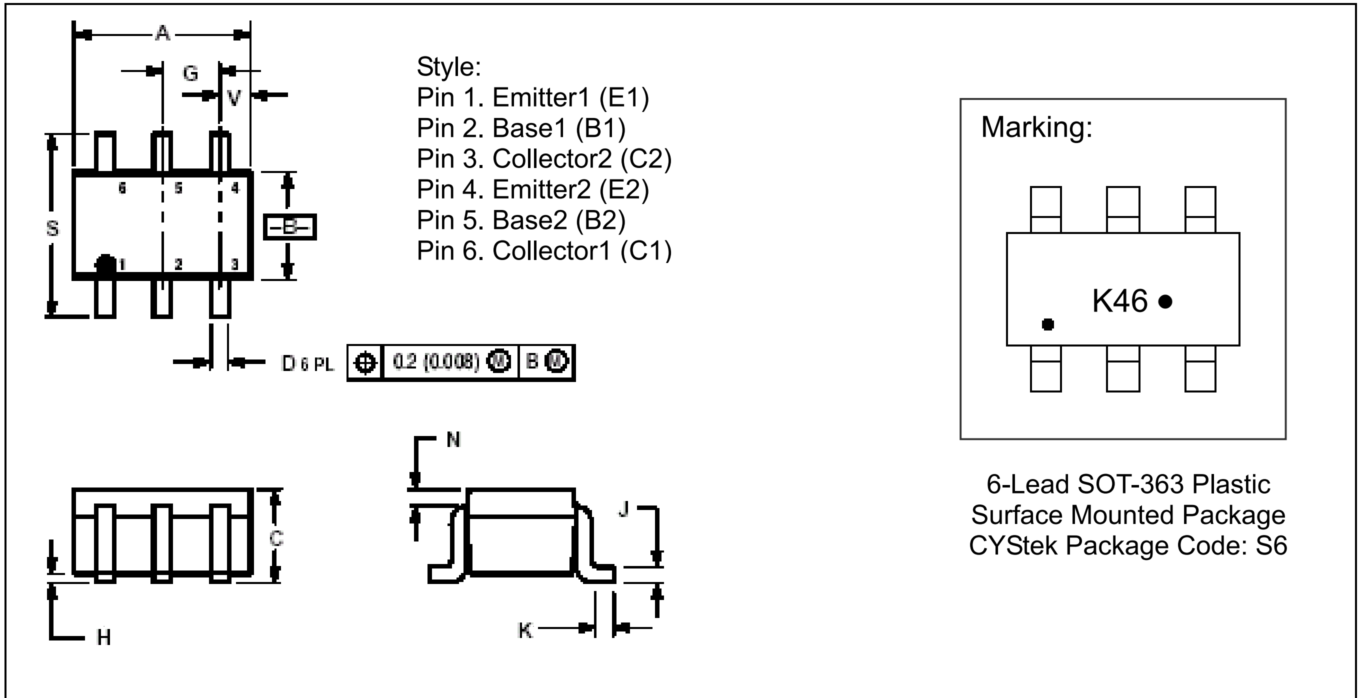
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



6-Lead SOT-363 Plastic Surface Mounted Package
CYStek Package Code: S6

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.071	0.087	1.8	2.2	J	0.004	0.010	0.1	0.25
B	0.045	0.053	1.15	1.35	K	0.004	0.012	0.1	0.30
C	0.031	0.043	0.8	1.1	N	0.008 REF		0.20 REF	
D	0.004	0.012	0.1	0.3	S	0.079	0.087	2.00	2.40
G	0.026BSC		0.65BSC		Y	0.012	0.016	0.30	0.40
H	-	0.004	-	0.1					

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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