Dual PNP Digital Transistors

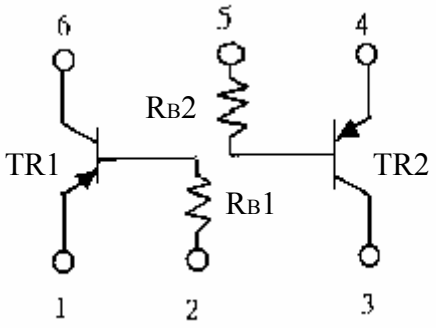
HBA143TS6R

Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Two DTA143T chips in a SOT-363 package.
- Mounting by SOT-323 automatic mounting machines is possible.
- Mounting cost and area can be cut in half.
- Transistor elements are independent, eliminating interference.
- Complements the HBC143TS6R.
- Pb-free package.

Equivalent Circuit

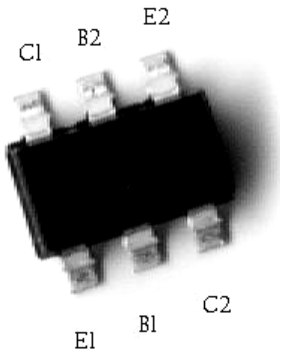
HBA143TS6R



RB1=4.7kΩ , RB2=4.7 kΩ

Outline

SOT-363R



Absolute Maximum Ratings (Each Transistor,Ta=25℃)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-50	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-100	mA
Power Dissipation	Pd	200 (Note)	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note: 150mW per element must not be exceeded.

Characteristics (Each Transistor, Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Collector-Base Breakdown Voltage	V_{CBO}	-50	-	-	V	I_C=-50μA
Collector-Emitter Breakdown Voltage	V_{CEO}	-50	-	-	V	I_C=-1mA
Emitter-Base Breakdown Voltage	V_{EBO}	-5	-	-	V	I_E=-50μA
Collector-Base Cutoff Current	I_{CBO}	-	-	-0.5	μA	V_{CB}=-50V
Emitter-Base Cutoff Current	I_{EBO}	-	-	-0.5	μA	V_{EB}=-4V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	0.1	-0.3	V	I_C=-5mA, I_B=-0.25mA
DC Current Gain	h_{FE}	100	-	600	-	V_{CE}=-5V, I_C=-1mA
Input Resistance	R	3.29	4.7	6.11	kΩ	-
Transition Frequency	f_T	-	250	-	MHz	V_{CE}=-10V, I_C=-5mA, f =100MHz *

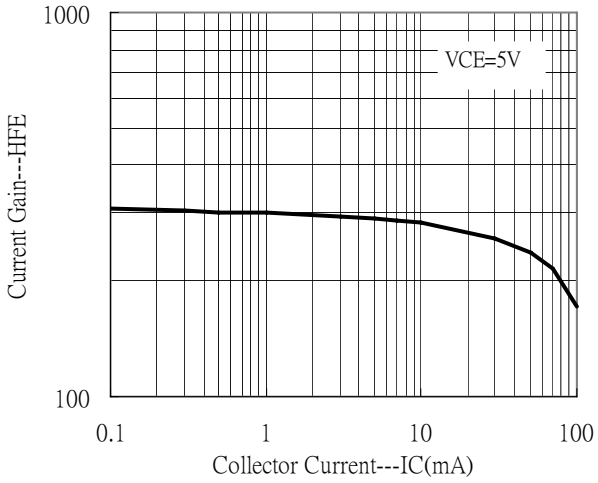
* Transition frequency of the device

Ordering Information

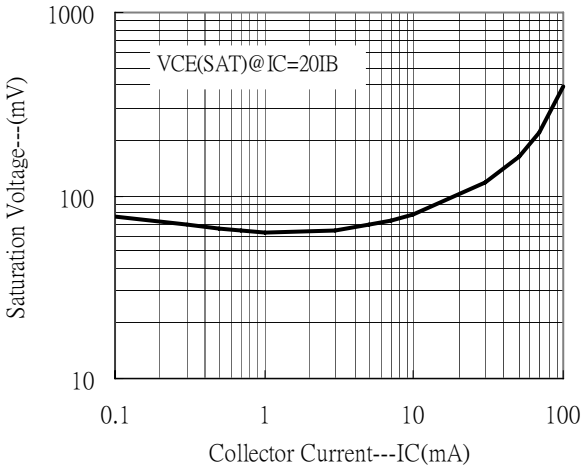
Device	Package	Shipping	Marking
HBA143TS6R	SOT-363 (Pb-free)	3000 pcs / Tape & Reel	0F

Characteristic Curves

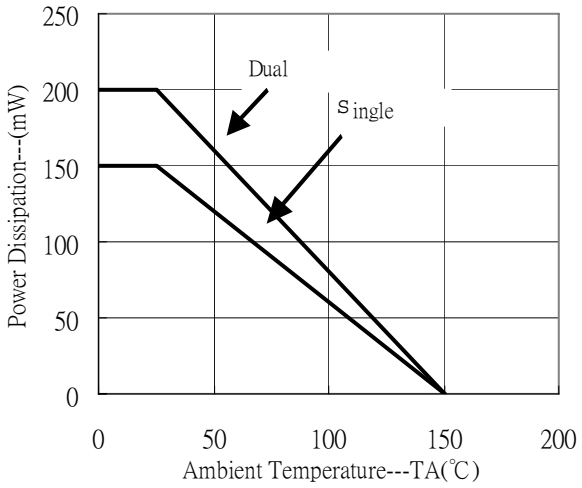
Current Gain vs Collector Current



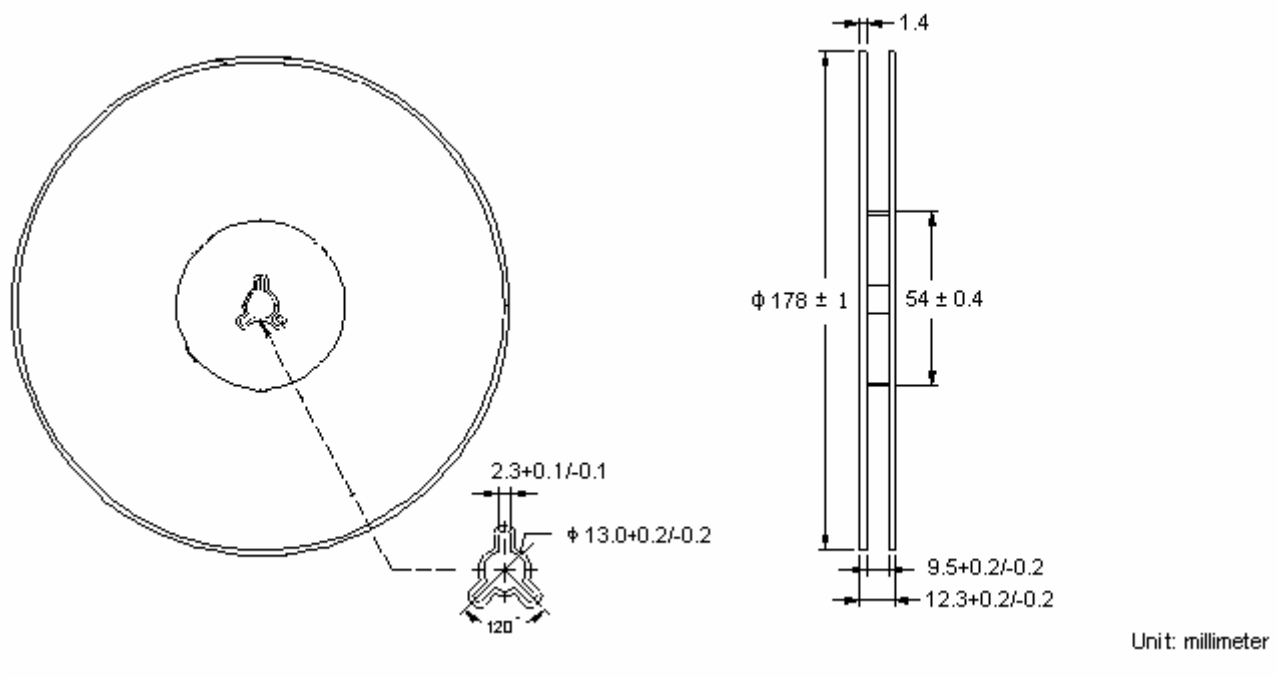
Saturation Voltage vs Collector Current



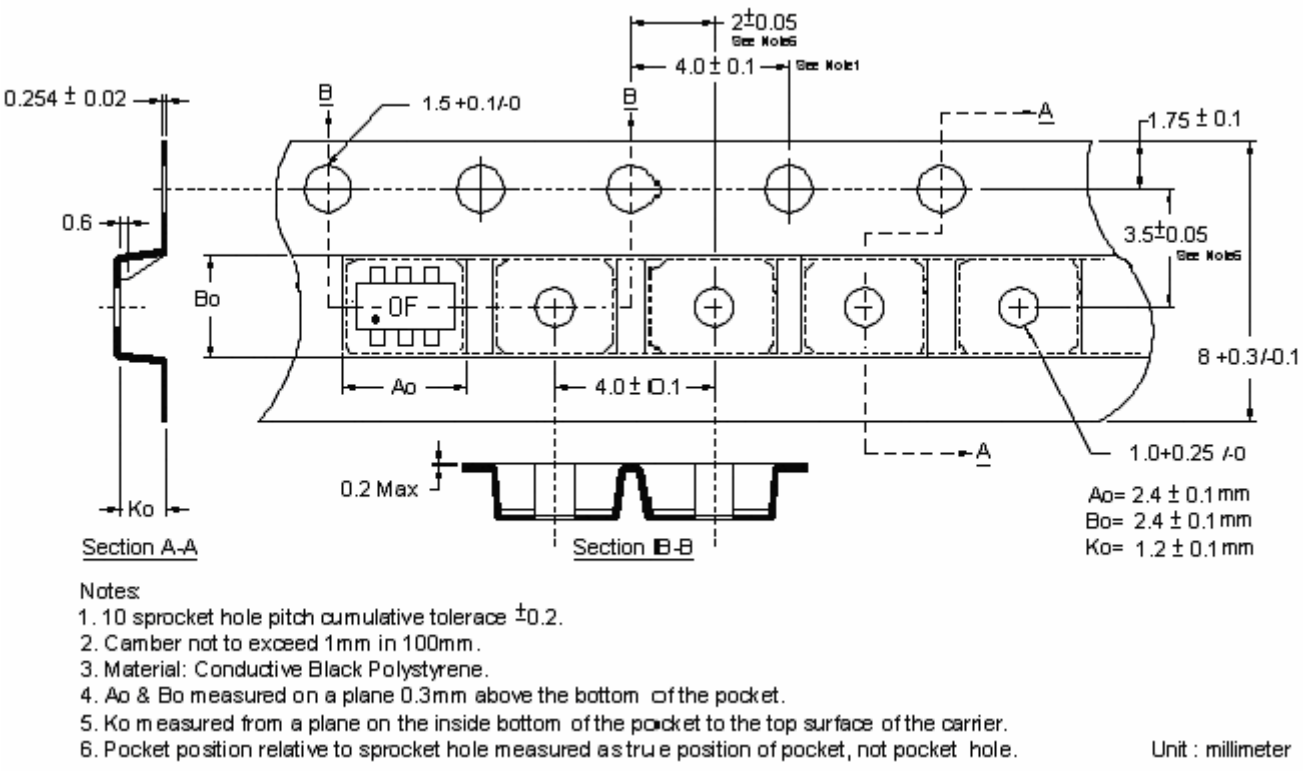
Power Derating Curves



Reel Dimension



Carrier Tape Dimension



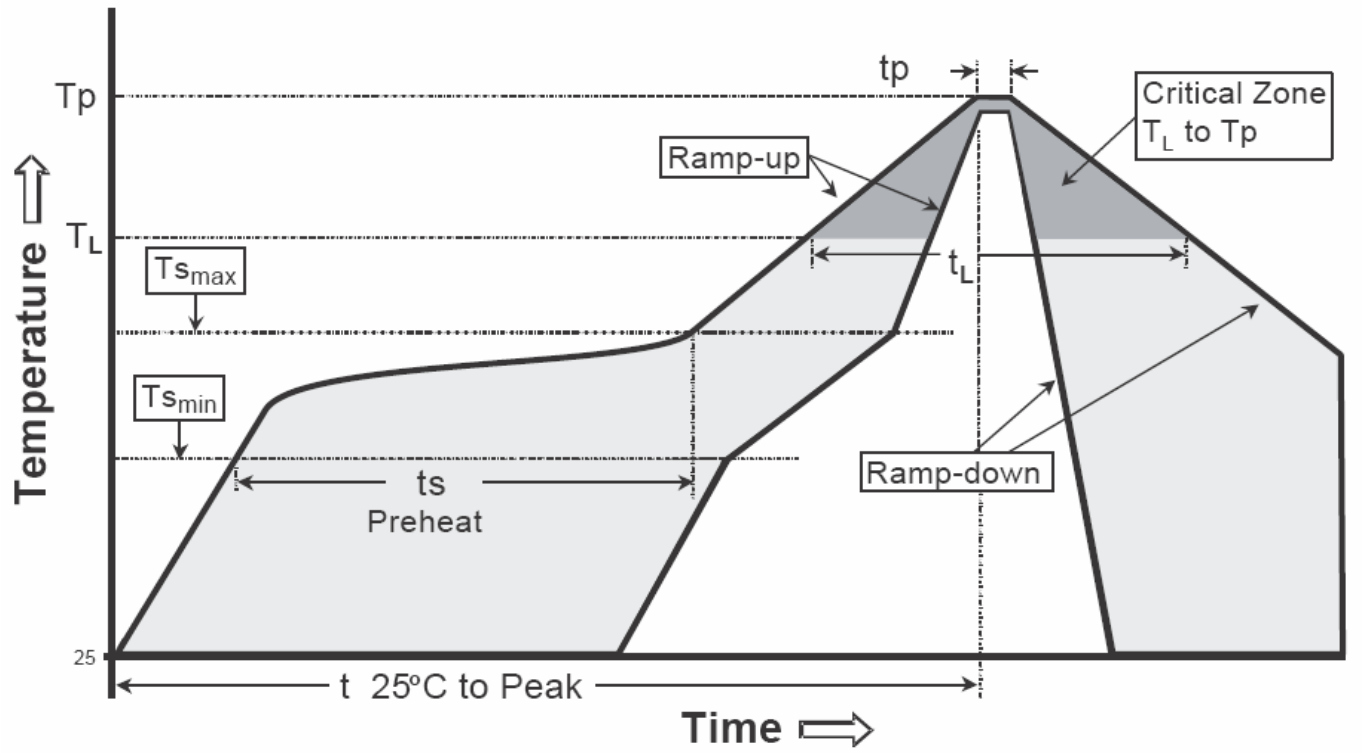
Notes:
1. 10 sprocket hole pitch cumulative tolerace ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

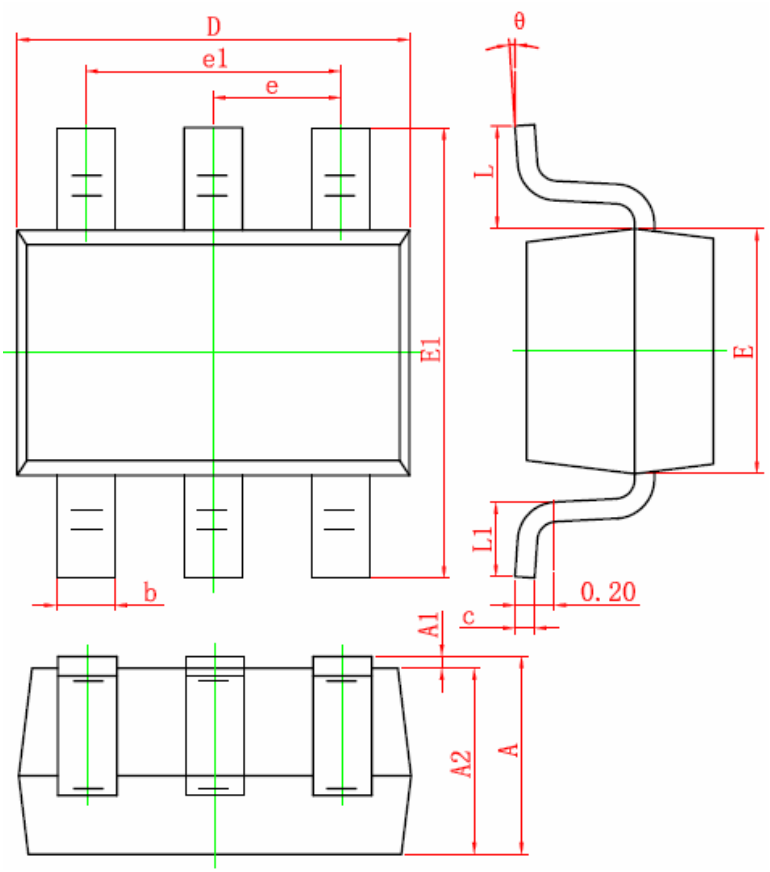
Recommended temperature profile for IR reflow



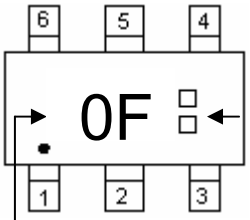
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



Marking:



Date Code:
Year + Month
Year : 6→2006, 7→2007,…, etc
Month : 1→Jan 2→Feb, …, 9→Sep, A→Oct, B→Nov, C→Dec

Device Code

6-Lead SOT-363R Plastic Surface Mounted Package
CYStek Package Code: S6R

Style:
Pin 1. Emitter1 (E1)
Pin 2. Base1 (B1)
Pin 3. Collector2 (C2)
Pin 4. Emitter2 (E2)
Pin 5. Base2 (B2)
Pin 6. Collector1 (C1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650 TYP		0.026 TYP	
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525 REF		0.021 REF	
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.