HAF2021(L), HAF2021(S)

Silicon N Channel MOS FET Series
Power Switching

REJ03G0179-0200Z
(Previous ADE-208-1459A(Z))
Rev.2.00
Mar.05.2004

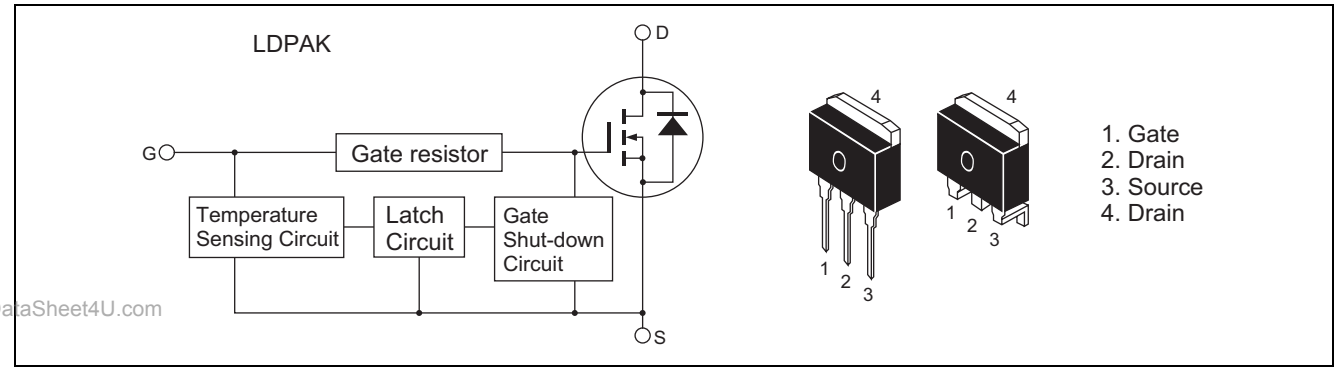
Description

This FET has the over temperature shut–down capability sensing to the junction temperature. This FET has the built–in over temperature shut–down circuit in the gate area. And this circuit operation to shut–down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

Features

- Logic level operation (6 V Gate drive)
- High endurance capability against to the short circuit
- Built–in the over temperature shut–down circuit
- Latch type shut–down operation (Need 0 voltage recovery)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
Gate to source voltage	V_{GSS}	–2.5	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ Note1	100	A
Body-drain diode reverse drain current	I_{DR}	50	A
Channel dissipation	Pch Note2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current	I_{IH1}	—	—	100	µA	Vi = 6 V, V_{DS} = 0
(Gate non shut down)	I_{IH2}	—	—	50	µA	Vi = 3.5 V, V_{DS} = 0
	I_{IL}	—	—	1	µA	Vi = 1.2 V, V_{DS} = 0
Input current	$I_{IH(sd)1}$	—	0.6	—	mA	Vi = 6 V, V_{DS} = 0
(Gate shut down)	$I_{IH(sd)2}$	—	0.35	—	mA	Vi = 3.5 V, V_{DS} = 0
Shut down temperature	T_{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V_{OP}	3.5	—	12	V	

Electrical Characteristics

(Ta = 25°C)

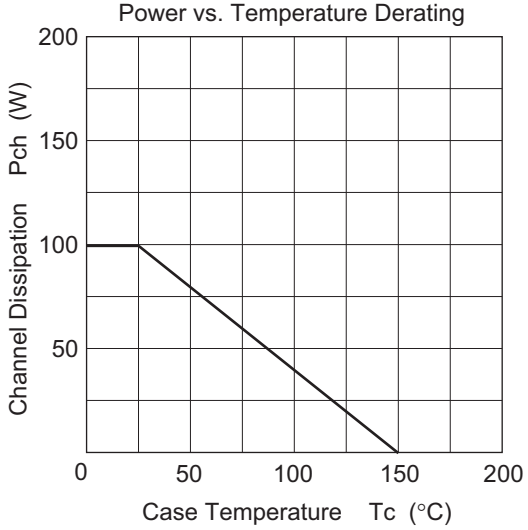
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	90	—	—	A	V_{GS} = 6 V, V_{DS} = 10 V
Drain current	I_{D2}	—	—	10	mA	V_{GS} = 1.2 V, V_{DS} = 10 V
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	I_G = 300 µA, V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–2.5	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS1}	—	—	100	µA	V_{GS} = 6 V, V_{DS} = 0
	I_{GSS2}	—	—	50	µA	V_{GS} = 3.5 V, V_{DS} = 0
	I_{GSS3}	—	—	1	µA	V_{GS} = 1.2 V, V_{DS} = 0
	I_{GSS4}	—	—	–100	µA	V_{GS} = –2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS(op)1}$	—	0.6	—	mA	V_{GS} = 6 V, V_{DS} = 0
	$I_{GS(op)2}$	—	0.35	—	mA	V_{GS} = 3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.2	—	3.4	V	I_D = 1 mA, V_{DS} = 10 V
Forward transfer admittance	$\|y_{fs}\|$	15	50	—	S	I_D = 25 A, V_{DS} = 10 V [Note3]
Static drain to source on state resistance	$R_{DS(on)}$	—	8	12	mΩ	I_D = 25 A, V_{GS} = 10 V [Note3]
Static drain to source on state resistance	$R_{DS(on)}$	—	9.5	15	mΩ	I_D = 25 A, V_{GS} = 6 V [Note3]
Output capacitance	Coss	—	1450	—	pF	V_{DS} = 10 V , V_{GS} = 0, f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	µs	I_D = 25 A, V_{GS} = 10 V
Rise time	t_r	—	75	—	µs	R_L = 1.2 Ω
Turn-off delay time	$t_{d(off)}$	—	3	—	µs	
Fall time	t_f	—	2.6	—	µs	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	110	—	ns	I_F = 50 A, V_{GS} = 0 diF/ dt =50 A/µs
Over load shut down operation time [Note4]	t_{os}	—	0.8	—	ms	V_{GS} = 6 V, V_{DD} = 16 V

Notes: 3. Pulse test

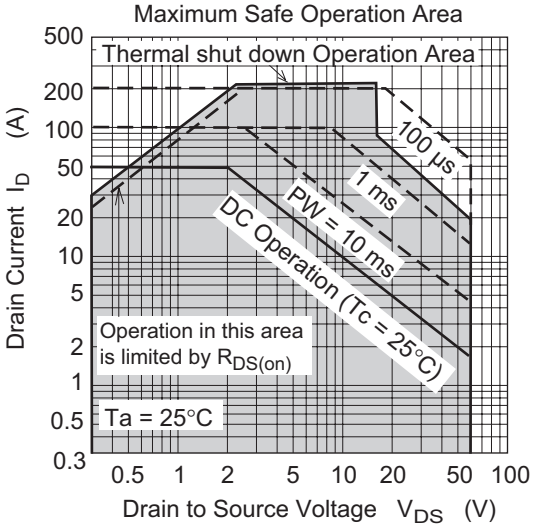
4. Including the junction temperature rise of the over loaded condition.

Main Characteristics

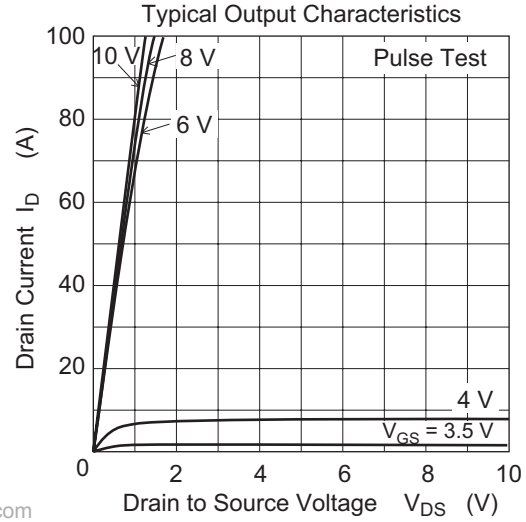
Power vs. Temperature Derating



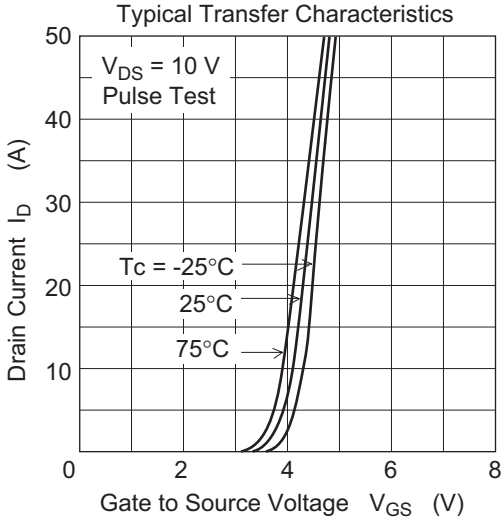
Maximum Safe Operation Area



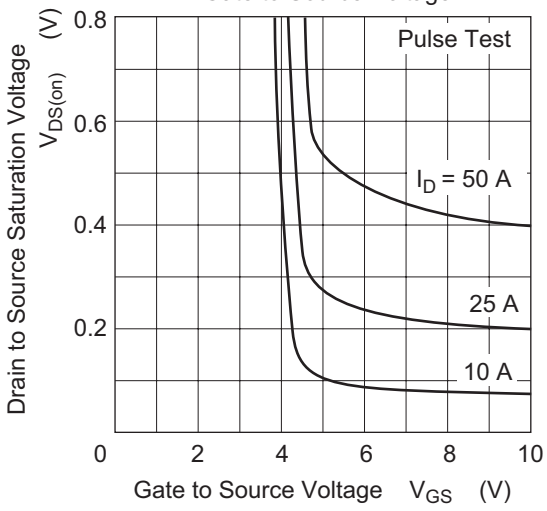
Typical Output Characteristics



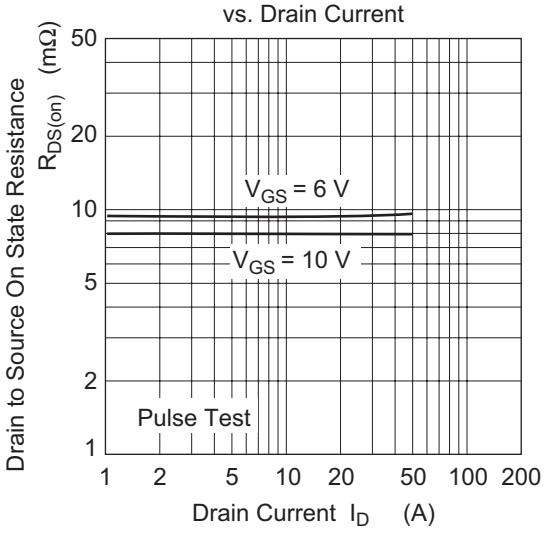
Typical Transfer Characteristics



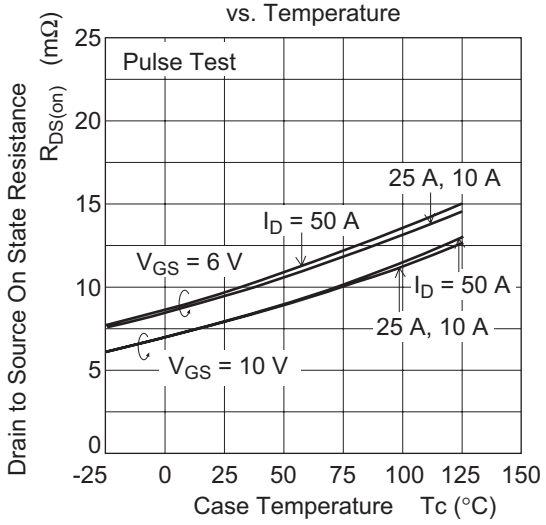
Drain to Source Saturation Voltage vs. Gate to Source Voltage



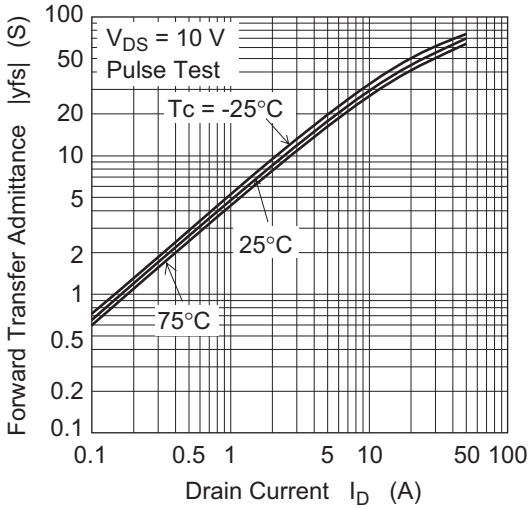
Static Drain to Source State Resistance vs. Drain Current



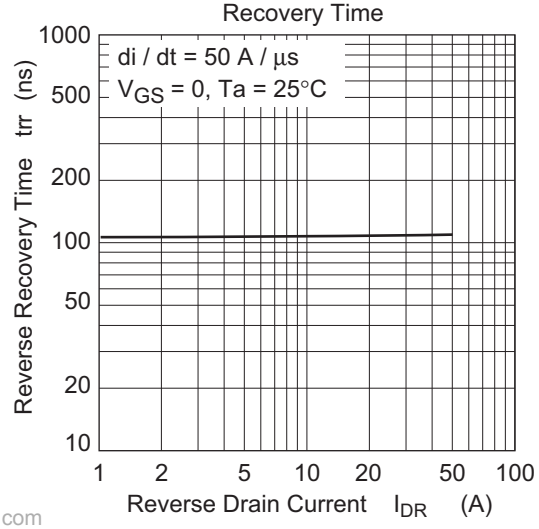
Static Drain to Source State Resistance vs. Temperature



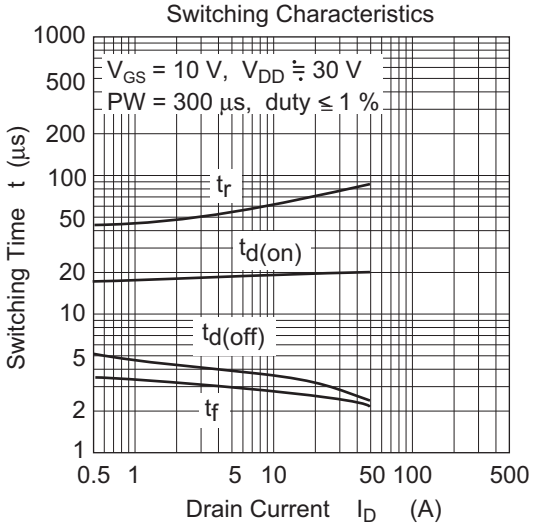
Forward Transfer Admittance vs. Drain Current



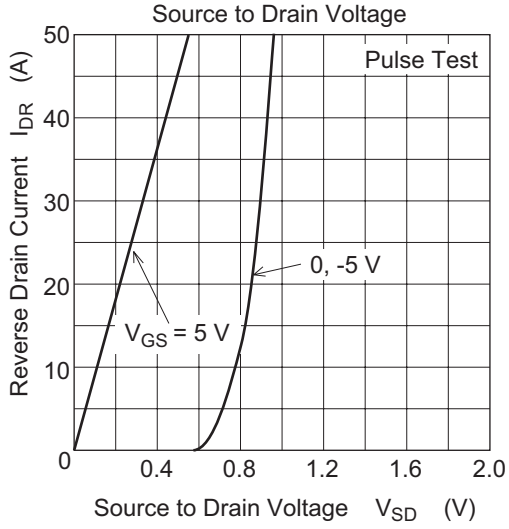
Body to Drain Diode Reverse Recovery Time



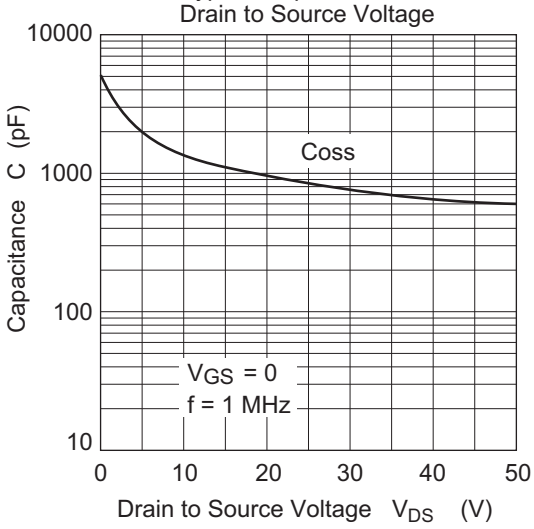
Switching Characteristics



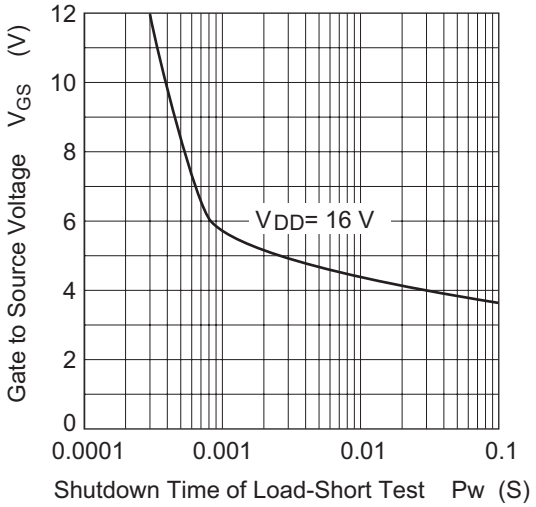
Reverse Drain Current vs. Source to Drain Voltage



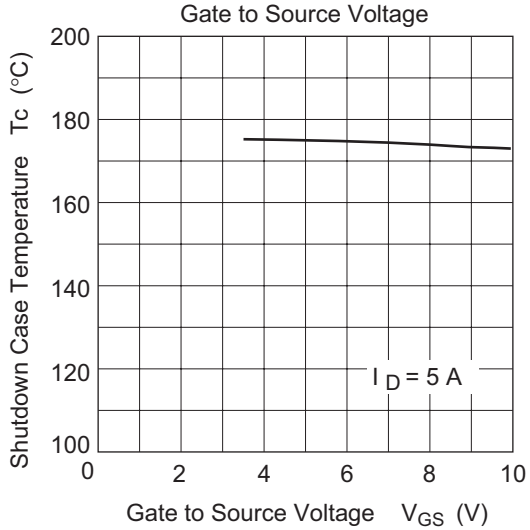
Typical Capacitance vs. Drain to Source Voltage



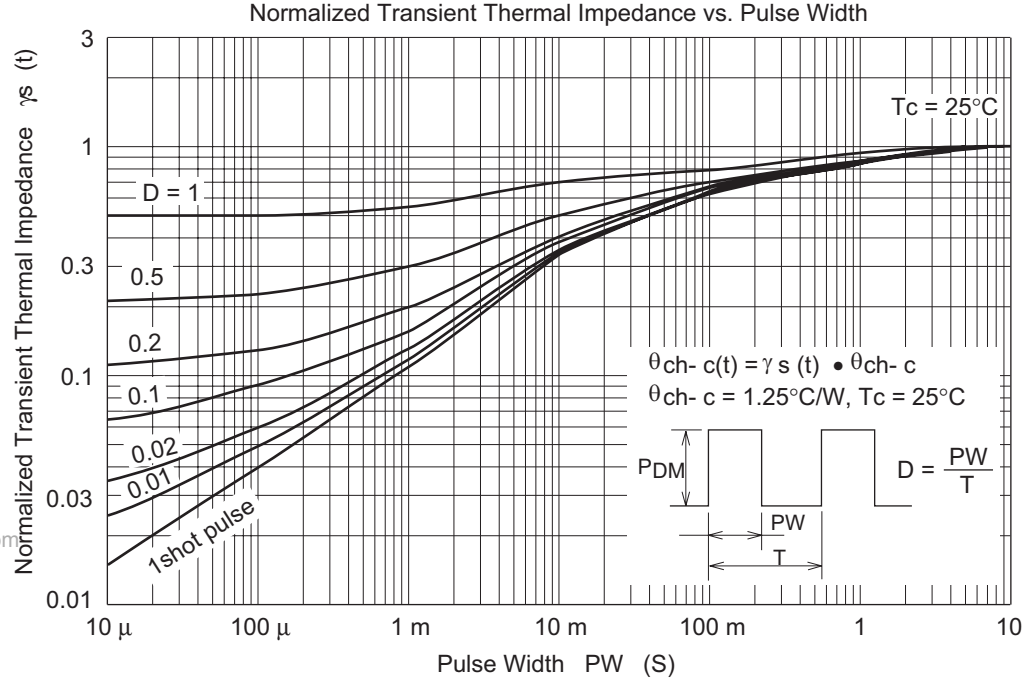
Gate to Source Voltage vs.
Shutdown Time of Load-Short Test



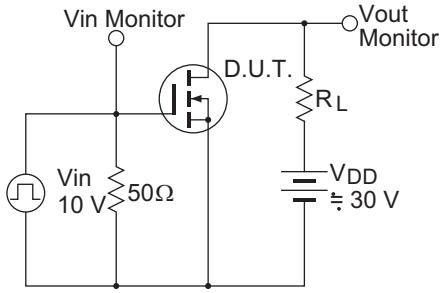
Shutdown Case Temperature vs.
Gate to Source Voltage



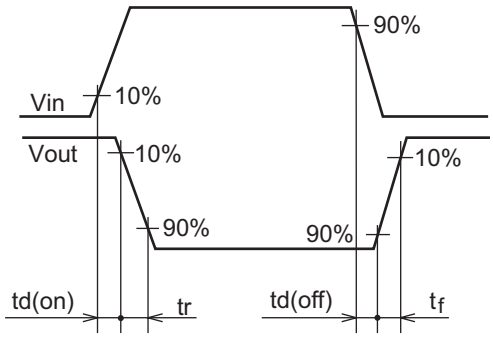
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

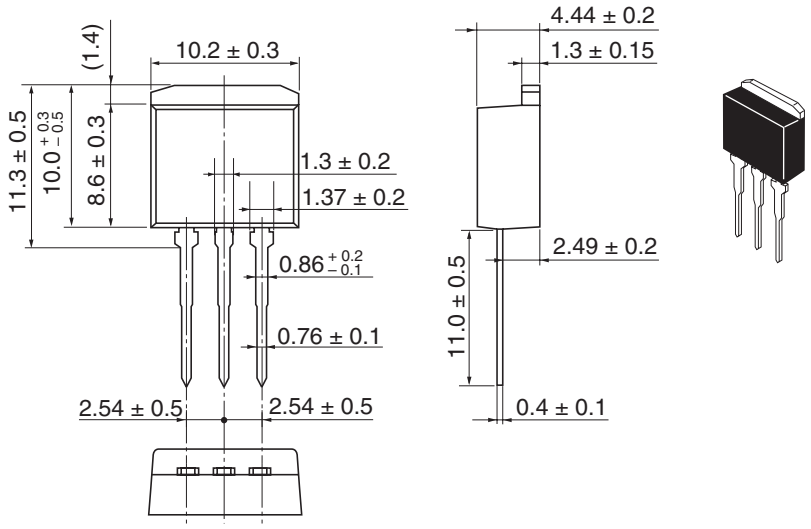


Waveform



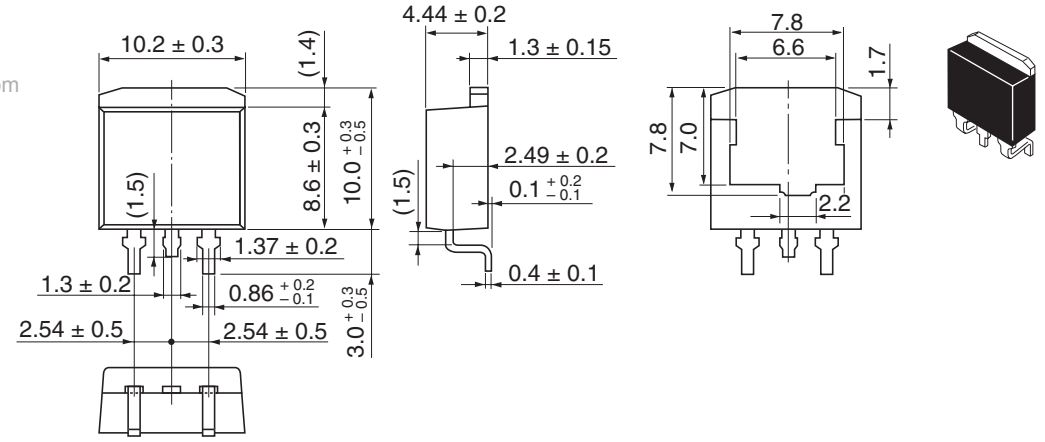
Package Dimensions

As of January, 2003
Unit: mm



Package Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.40 g

As of January, 2003
Unit: mm



Package Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

Ordering Information

Part Name	Quantity	Shipping Container
HAF2021-90L	Max:50pcs/sack	sack
HAF2021-90S	Max:50pcs/sack	sack
HAF2021-90STL	1000pcs/Reel	Embossed tape
HAF2021-90STR	1000pcs/Reel	Embossed tape

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .1.0