HA12188AF

Pre-Amplifier and Servo IC for Quadruple-Speed CD-ROM

HITACHI

ADE-207-183(Z)

1st. Edition
October 1995

Description

The typical values of built-in capacitances in this IC are reduced 10% compared with those in IC HA12188F. The values of Electrical Characteristics of this IC are same as those of IC HA12188F.

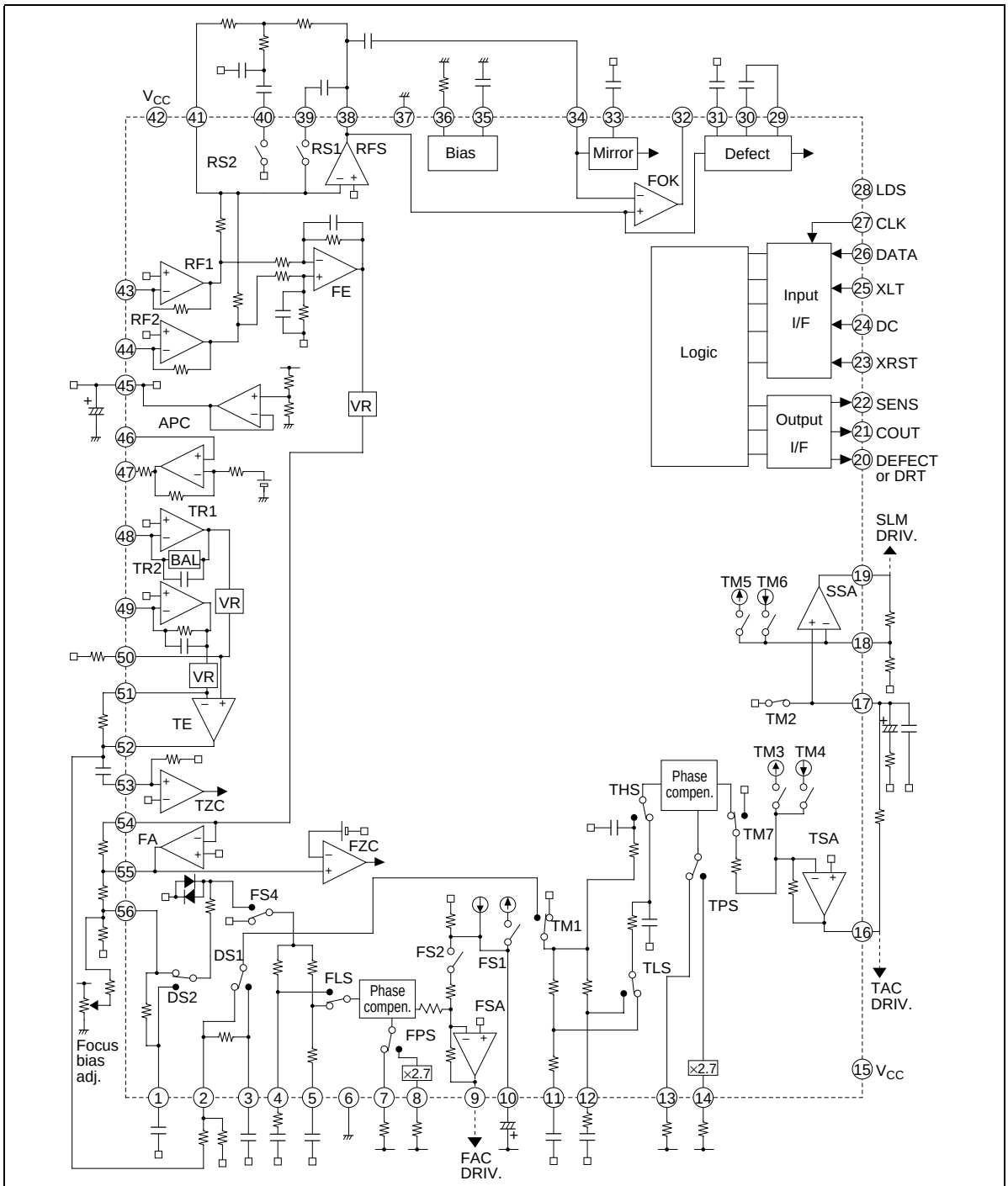
Functions

- RF amplifier
- Focus error amplifier
- Tracking error amplifier
- FOK detector
- Mirror detector
- Defect detector
- APC amplifier
- Focus, tracking, and sled servo control
- Inner/outer direction detector

Features

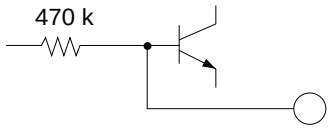
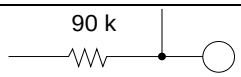
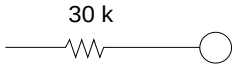
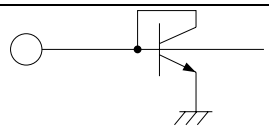
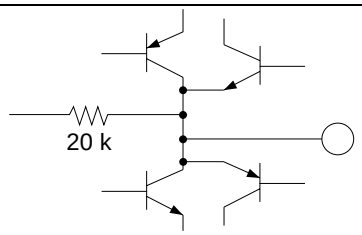
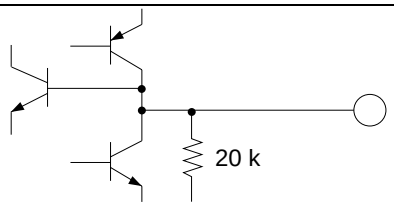
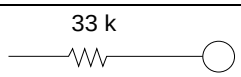
- Built-in variable resistors for adjusting tracking error EF balance, tracking gain, and focus gain
- Single power supply
- Supports double and quadruple speeds
- Few external components
- FP-56 package

Block Diagram

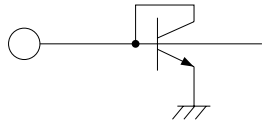
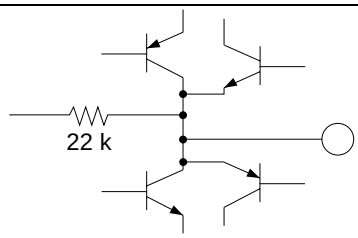
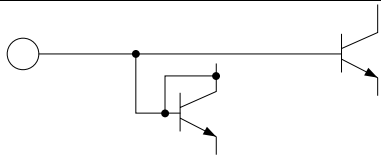
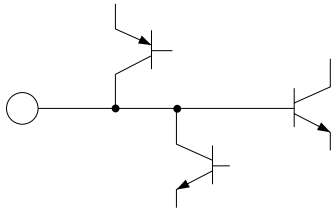
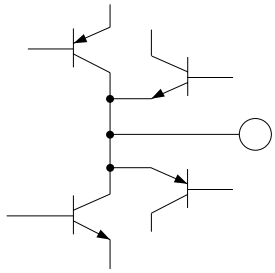


- The states of the IC's internal switches at XRST = "L" are shown at block diagram.
- The black dot symbol of transfer switch shows on state.
- The symbols " ⊤ " mean connecting to V_{CC}.
- The symbols " ⊓ " mean connecting to pin 45.

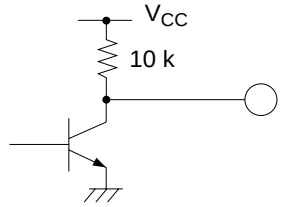
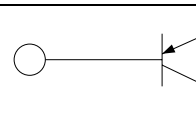
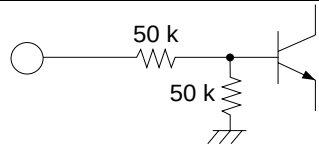
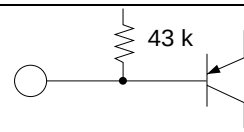
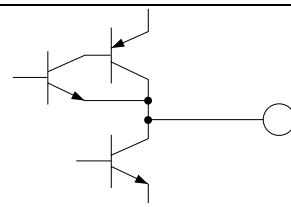
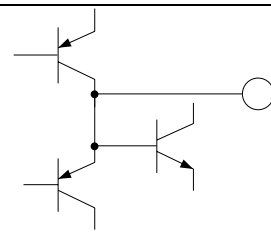
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Function
1	FH		Focus error hold signal output
3	TH		Tracking error hold signal output
2	TSI		Tracking servo input
56	FSI		Focus servo input
4	FLS		Focus-servo low-frequency filter resistor & capacitor connection (FLS on)
5	$\overline{\text{FLS}}$		Focus-servo low-frequency filter capacitor connection (FLS off)
6	SGND	—	Servo ground
7	$\overline{\text{FPS}}$		Resistor connection for programming focus-servo phase compensation (FPS off)
8	FPS		Resistor connection for programming focus-servo phase compensation (FPS on)
9	FSA		Focus servo output
10	FS1		FS1 voltage output
11	$\overline{\text{TLS}}$		Tracking servo low-frequency filter capacitor connection (TLS off)

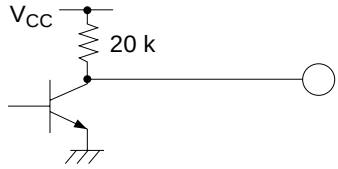
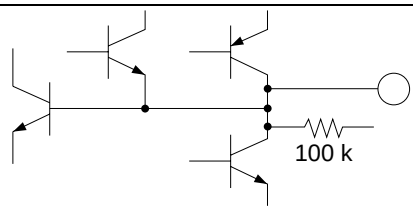
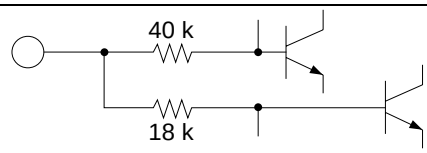
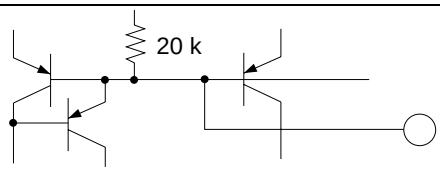
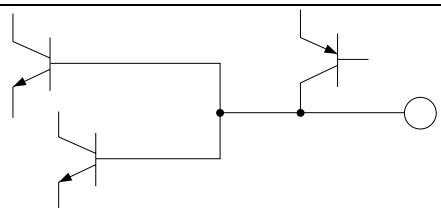
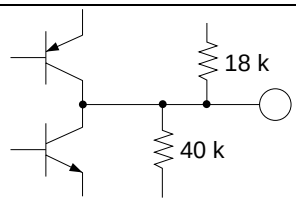
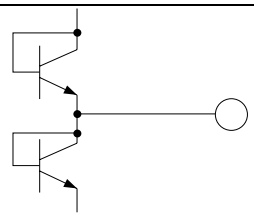
Pin Descriptions and Equivalent Circuits (cont)

Pin No.	Symbol	Equivalent Circuit	Function
12	TLS		Tracking servo low-frequency filter resistor & capacitor connection (TLS on)
13	$\overline{\text{TPS}}$		Resistor connection for programming tracking servo phase compensation (TPS off)
14	TPS		Resistor connection for programming tracking servo phase compensation (TPS on)
15	SV_{CC}	—	Servo power supply
16	TSA		Tracking servo output
17	TM2		Sled servo input
18	SSM		SSA amplifier inverting input
19	SSA		Sled servo output

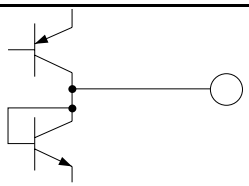
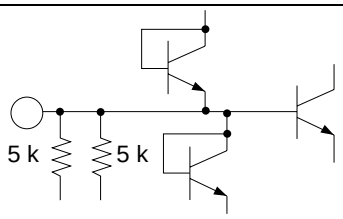
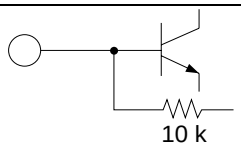
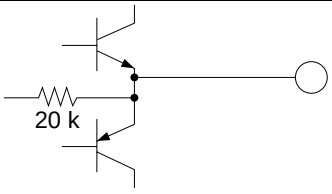
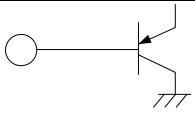
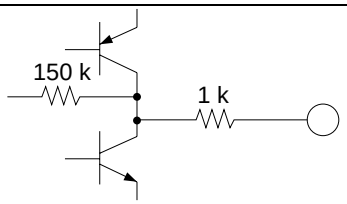
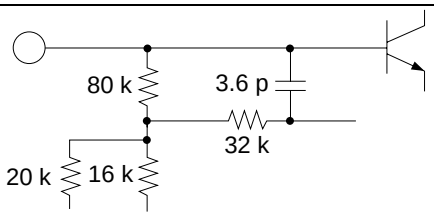
Pin Descriptions and Equivalent Circuits (cont)

Pin No.	Symbol	Equivalent Circuit	Function
20	DRT		Defect signal output or inner/outer direction signal output
21	COUT		COUT output
22	SENS		SENS output
23	XRST		Reset input
24	DC		DC input
25	XLT		XLT input
26	DATA		Data input
27	CLK		Clock input
28	LDS		Laser switch input
29	DFIN		Defect comparator input
30	DFO		Defect envelope signal output
31	DFH		Defect hold signal output

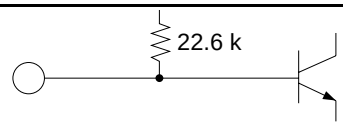
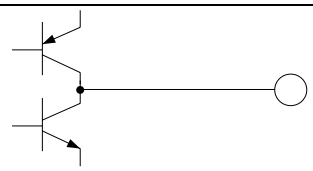
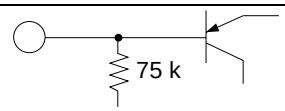
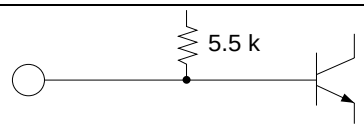
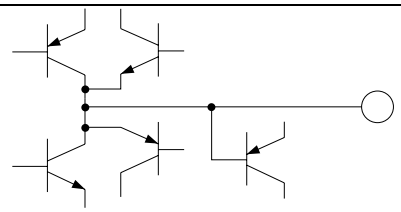
Pin Descriptions and Equivalent Circuits (cont)

Pin No.	Symbol	Equivalent Circuit	Function
32	FOK		FOK comparator output
33	MIRH		Mirror hold signal output
34	RFA		RF signal AC input
35	BYPS		Capacitor connection for ripple filter
36	ISET		Resistor connection for programming reference current
37	PGND	—	Pre-amplifier ground
38	RFO		RF signal output
39	RS1		RS1 switch

Pin Descriptions and Equivalent Circuits (cont)

Pin No.	Symbol	Equivalent Circuit	Function
40	RS2		RS2 switch
41	RFM		RFS amplifier inverting input
42	PV_{CC}	—	Pre-amplifier power supply
43	RF1		RF1 amplifier input
44	RF2		RF2 amplifier input
45	V_C		Voltage reference output
46	MD		APC amplifier input
47	LD		APC amplifier output
48	TR1		TR1 amplifier input
49	TR2		TR2 amplifier input

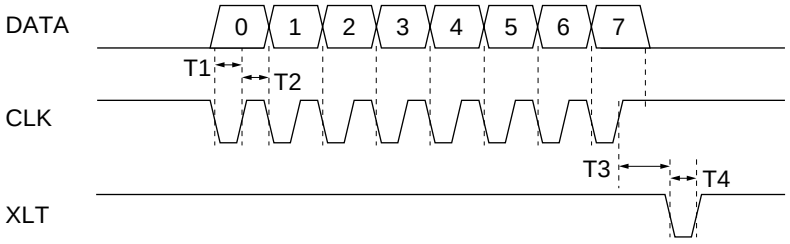
Pin Descriptions and Equivalent Circuits (cont)

Pin No.	Symbol	Equivalent Circuit	Function
50	TEP		TE amplifier non-inverting input
51	TEM		TE amplifier inverting input
52	TEO		TE amplifier output
53	TZC		TZC comparator input
54	FAM		FA amplifier inverting input
55	FAO		FA amplifier output

Operation

1. Microprocessor Control

The IC's internal switches can be operated by sending control data from a microprocessor. The signal timing is shown in figure 1, and the control commands are listed in table 1.



Item	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{CLK}	—	—	520	kHz
Clock pulse width	T1, T2	0.96	—	—	µs
Delay time	T3	1	—	—	µs
Latch pulse width	T4	2	—	—	µs

Figure 1 Timing Diagram for Microprocessor Control

Signals from the microprocessor are input at pins 23 to 27. A low input at the XRST pin resets the IC. Normally this pin should be kept high. (See figure 2.)

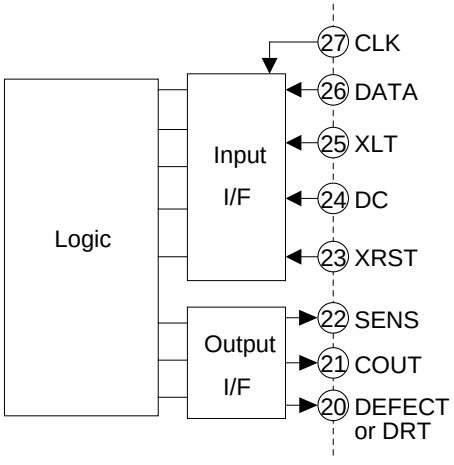


Figure 2 Microprocessor Interface

Table 1 Microprocessor Control Commands

	DATA *1								SENS
	D7	D6	D5	D4	D3	D2	D1	D0	
Focus mode	0	0	0	0	(FS4)	DEFECT OFF *2	(FS2)	(FS1)	FZC
Tracking mode and FS1 DRT setting	0	0	0	1	DRT *3 0: Defect 1: Direction	(TM7) *4	FS1 current *5	(THS)	H
Access control mode	0	0	1	0	See table 2				TZC
Pulse setting mode	0	0	1	1	TM3, TM4 current *6 D3 D2 Current value 0 0 32µA 0 1 16µA 1 0 24µA 1 1 8µA		TM5, TM6 current *6 D1 D0 Current value 0 0 32µA 0 1 16µA 1 0 24µA 1 1 8µA		H
Speed setting mode	0	1	0	0	Mirror *7 D3 D2 Mode 0 0 Normal 0 1 Double 1 1 Quadruple		Focus tracking (FLS) (FPS) (TLS) (TPS)	RF (RS1) (RS2)	H
EF balance adjustment	0	1	0	1	(BAL3)	(BAL2)	(BAL1)	(BAL0)	H
Tracking gain and focus gain adjustment	0	1	1	0	0 ; Focus gain	(GF2)	($\overline{GF1}$)	(GF0)	H
					1 ; Tracking gain	(GT2)	($\overline{GT1}$)	(GT0)	H

Notes:
1. The switch name surrounded by circle means that the switch turns on when the corresponding bit is “1”. The switch name with bar surrounded by circle means that the switch turns on when the corresponding bit is “0”.
2. “DEFECT OFF” means that switches DS1 and DS2 don’t turn on when the corresponding bit is “1”. Though the “DEFECT OFF” bit is set, the output at pin 20 is defect signal (in defect signal output mode).
3. DRT (pin 20) outputs defect signal when the corresponding bit is “0”, and outputs direction signal when the corresponding bit is “1”.
4. TM7 can turn on only when COUT is high.
5. The value of two current sources over switch FS1 are 18 µA(source) 36 µA(sink) when the corresponding bit is “1”, and are 9 µA(source) 18 µA(sink) when the corresponding bit is “0”.
6. The current values through switches TM3, TM4, TM5 and TM6 can be selected in four steps.
7. The speed of Mirror circuit can be selected in three steps. Don’t use D3 = “1”, D2 = “0” mode.

Table 2 Access Control Mode

	DATA				ST1						ST2						ST3					
	D3	D2	D1	D0	TM6	TM5	TM4	TM3	TM2	TM1	TM6	TM5	TM4	TM3	TM2	TM1	TM6	TM5	TM4	TM3	TM2	TM1
$20	0	0	0	0					○				○		○							○
$21	0	0	0	1									○									○
$22	0	0	1	0		○			○			○	○		○		○				○	○
$23	0	0	1	1	○				○		○		○		○		○				○	○
$24	0	1	0	0					○	○				○	○							○
$25	0	1	0	1						○				○								○
$26	0	1	1	0		○			○	○		○		○	○		○				○	○
$27	0	1	1	1	○				○	○	○			○	○		○				○	○
$28	1	0	0	0				○	○				○		○							○
$29	1	0	0	1				○					○									○
$2A	1	0	1	0		○		○	○			○	○		○		○				○	○
$2B	1	0	1	1	○			○	○		○		○		○		○				○	○
$2C	1	1	0	0			○		○					○	○							○
$2D	1	1	0	1			○							○								○
$2E	1	1	1	0		○	○		○			○		○	○		○				○	○
$2F	1	1	1	1	○		○		○		○			○	○		○				○	○

A circle means that the switch is ON.

Note: After the microprocessor sends serial data, TM1 to TM6 can be switched among the states listed under ST1 to ST3 by input at the DC pin. First, if the microprocessor sends serial data when DC is high, TM1 to TM6 are placed in the state listed under ST1. When DC is brought low, the states change to the states listed under ST2. Then if DC is brought high again, the states change to the states listed under ST3.

Table 2-A Access Control Mode Appendix

1) Tracking servo

DATA		Tracking servo movement
D3	D2	at DC = H (ST1)
0	0	Servo loop off
0	1	Servo loop on
1	0	Servo loop off jump to outside track
1	1	Servo loop off jump to inside track

2) Sled servo

DATA		Sled servo movement
D1	D0	at DC = H (ST1)
0	0	Servo loop off
0	1	Servo loop on
1	0	Servo loop off move to outside track
1	1	Servo loop off move to inside track

2. RF and Focus Error Pre-Amplifiers

The main beam output signals from the photodiode IC are led in through resistors at pins 43 and 44. The outputs of amplifiers RF1 and RF2 are summed by amplifier RFS to generate the EFM RF signal. (*1)

External resintances of pins 43 and 44 and amplifier RFS should be set according to the pick-up so that the RF signal at pin 38 is about 1.5 V_{OP} (the difference between the peak level of 11T signal component and the voltage at no signal).

Switches RS1 and RS2 operate together under microprocessor control. For example they are on for normal or double speed, and off for quadruple speed. ON resistance of RS1 is 1.1kΩ typ and on resistance of RS2 is 530Ω typ.

Figure 3-A shows the frequency characteristic at pin 38 in the condition of figure 3.(Input resistances of pins 43 and 44 are 10kΩ.)

External resistances and capacitances should be fitted according to the pick-up. Stray capacitances of board print patterns have influence on this frequency characteristic. Therefore external resistances and capacitances should be set considering stray capacitances.

Amplifier FE subtracts the output of amplifier RF2 from the output of amplifier RF1 to generate the focus error signal. The gain is 0dB. The focus error signal is output as the output of amplifier FA at pin 55, with a gain set by variable resistor VR and the external resistance values. With the external resistors in figure 3, the gain of amplifier FA is 8.7dB (initial value after reset).

Variable resistor VR is controlled by 3-bit data. The gain can be varied from –5dB to +7dB with respect to the reset value.

The focus error signal is binarized by comparator FZC, with a Vth equal to V_C + 0.38V.

A reference voltage of 1/2 V_{CC} is output at pin 45. The IC's internal reference voltage is connected internally.

The feedback resistance of amplifier FA should be set according to the pick-up so that the focus S-curve at pin 55 is about 3V peak-to-peak.

Note: 1 The sink current of amplifier RFS is about 1mA. When load capacitance of pin 38 is big because of wiring with CD DSP LSI etc, please use buffer amplifier. (for example emitter follower transistor)

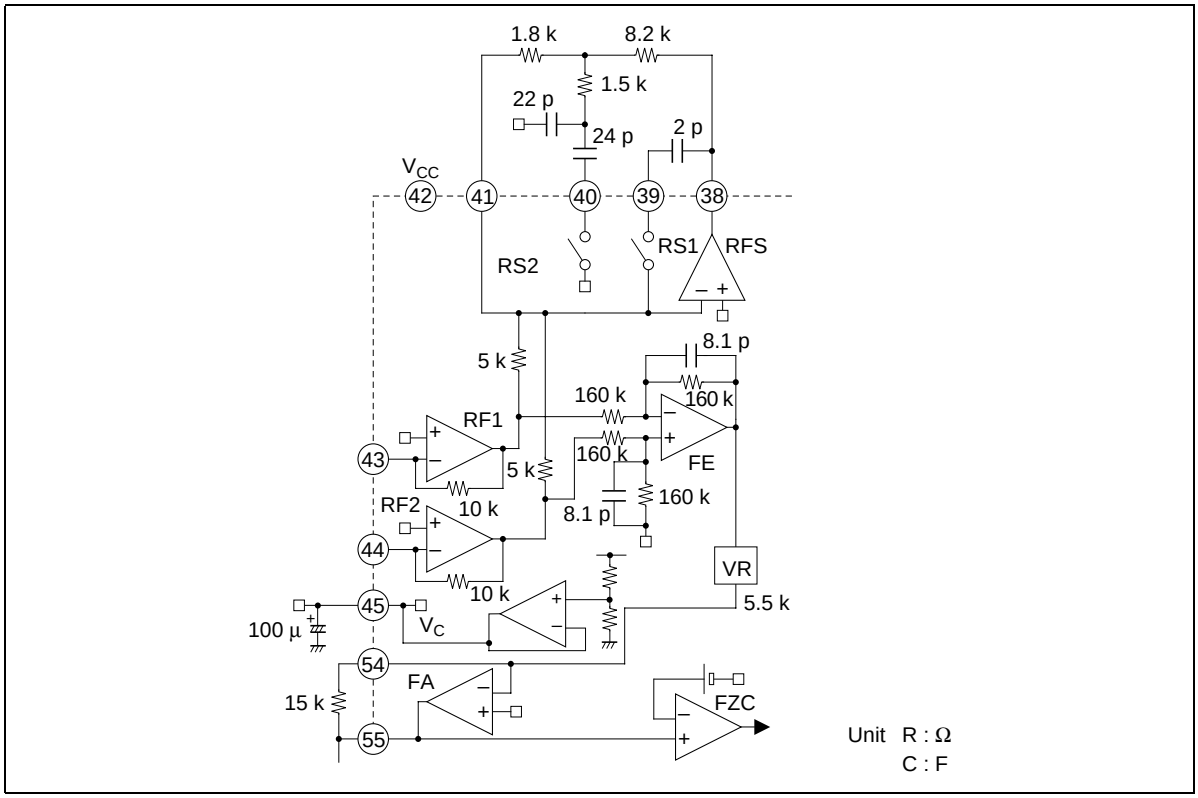


Figure 3 RF and Focus Error Pre-Amplifiers

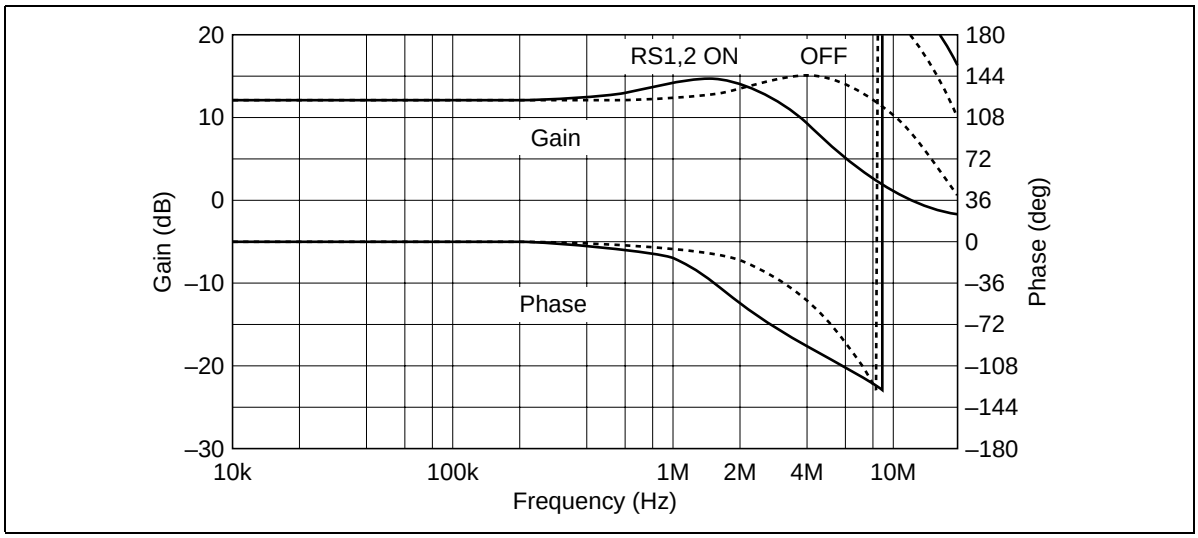


Figure 3-A Frequency characteristic example of RF preamplifiers

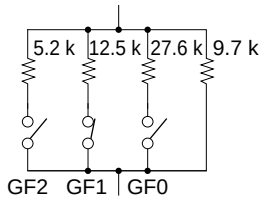


Figure 4 Focus VR

Table 3 Focus VR and Gain

D2	D1	D0	VR	Gain
0	1	0	9.7k	–4.8dB
0	1	1	7.2k	–2.2dB
0	0	0	5.5k	±0dB
0	0	1	4.6k	+1.6dB
1	1	0	3.4k	+3.8dB
1	1	1	3k	+4.9dB
1	0	0	2.7k	+6.0dB
1	0	1	2.4k	+6.8dB

3. Tracking Pre-Amplifiers

The sub-beam outputs from the photodiode IC are led in through resistors at pins 48 and 49.

External resistances of pins 48 and 49 and amplifier TE should be set according to the pick-up so that the traverse signal at pin 52 is about 2 V_{PP}.

After a reset, the initial value of the feedback resistance BAL from amplifier TR1 to pin 48 is 400kΩ, the same as the feedback resistance from amplifier TR2 to pin 49.

BAL has a variable resistance value that is controlled by 4-bit data. The variable range is from –32% to +28% of the reset value. This resistance can be varied to adjust the EF balance of the tracking error.

Amplifier TE generates the tracking error signal. Its input signals are received from the preceding stage through variable resistors VR. With the external resistor values in figure 5, after a reset, the initial value of the gain is 8.8dB.

The variable VR resistance is controlled by 3-bit data. The gain can be varied from –5dB to +7dB with respect to the reset value.

The tracking error signal is coupled through a capacitor to input pin 53 and binarized by comparator TZC, with a Vth equal to V_C. (*1)

Note: 1 At normal speed the output of amplifier TE contains much EFM signal components. Therefore the output of amplifier TE had better be led in through LPF for reduction of EFM signal components at pin 53.

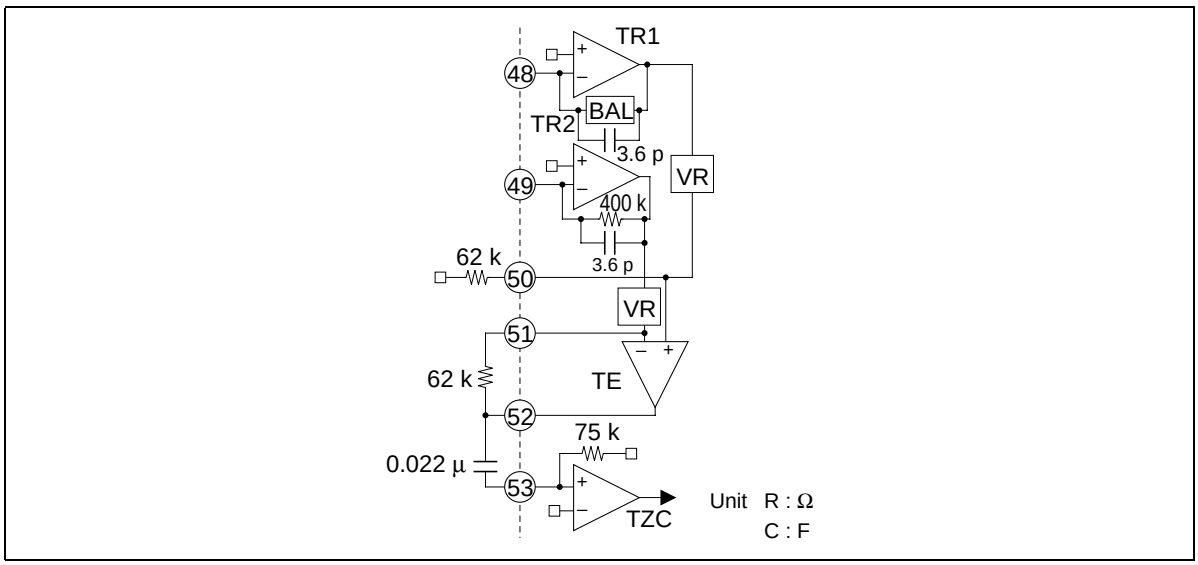


Figure 5 Tracking Pre-Amplifiers

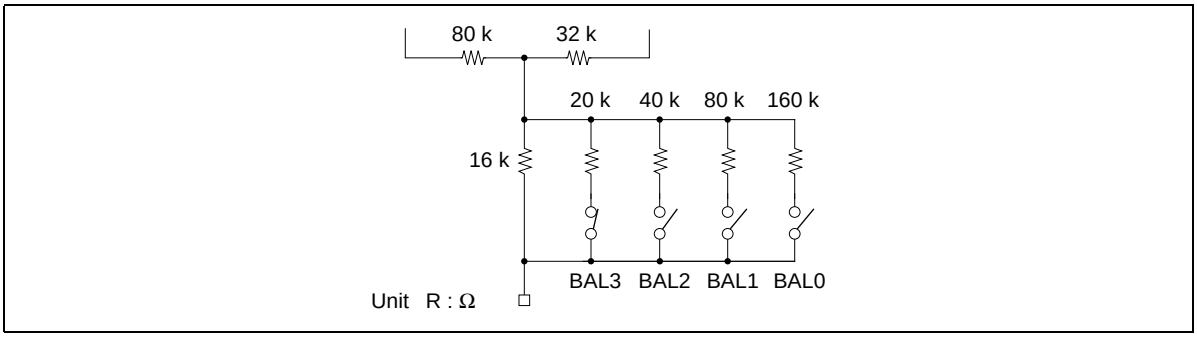


Figure 6 BAL

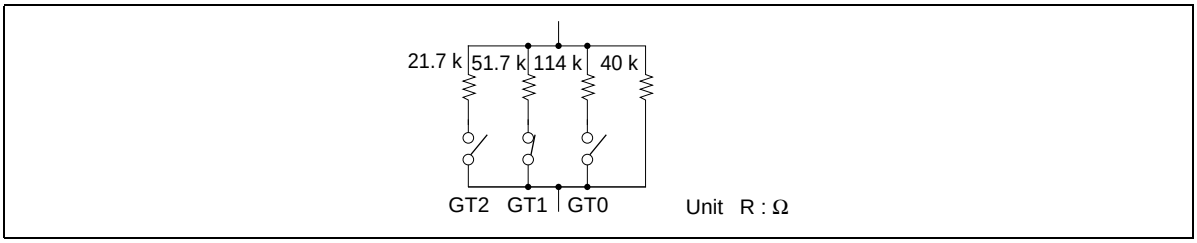


Figure 7 Tracking VR

Table 4 Tracking VR Values and Gain

D2	D1	D0	VR	Gain
0	1	0	40k	–4.9dB
0	1	1	29.6k	–2.3dB
0	0	0	22.6k	±0dB
0	0	1	18.8k	+1.6dB
1	1	0	14.1k	+3.9dB
1	1	1	12.5k	+4.9dB
1	0	0	11.1k	+6.1dB
1	0	1	10.1k	+6.9dB

Table 5 BAL Values

D3	D2	D1	D0	BAL	Ratio
1	0	0	0	272k	–32%
1	0	0	1	288k	–28%
1	0	1	0	304k	–24%
1	0	1	1	320k	–20%
1	1	0	0	336k	–16%
1	1	0	1	352k	–12%
1	1	1	0	368k	–8%
1	1	1	1	384k	–4%
0	0	0	0	400k	±0%
0	0	0	1	416k	+4%
0	0	1	0	432k	+8%
0	0	1	1	448k	+12%
0	1	0	0	464k	+16%
0	1	0	1	480k	+20%
0	1	1	0	496k	+24%
0	1	1	1	512k	+28%

4. FOK Detector

This detector is a comparator that generates the FOK signal. FOK is one of the signals that determines when to activate the focus servo. When the voltage at pin 38 exceeds the voltage at pin 34 by approximately 0.4V, pin 32 goes high.

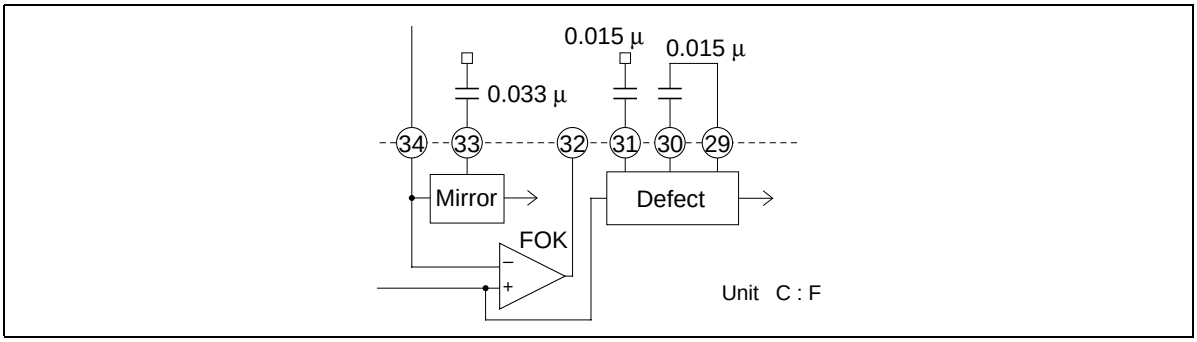


Figure 8 Mirror, FOK, and Defect Detectors

5. Defect Detector

When a scratched disc is played, the EFM RF signal has the shape shown in figure 9 (a). The defect detector detects the drop-out area of this signal. Scratches with dimensions of about 100µm or greater are detected.

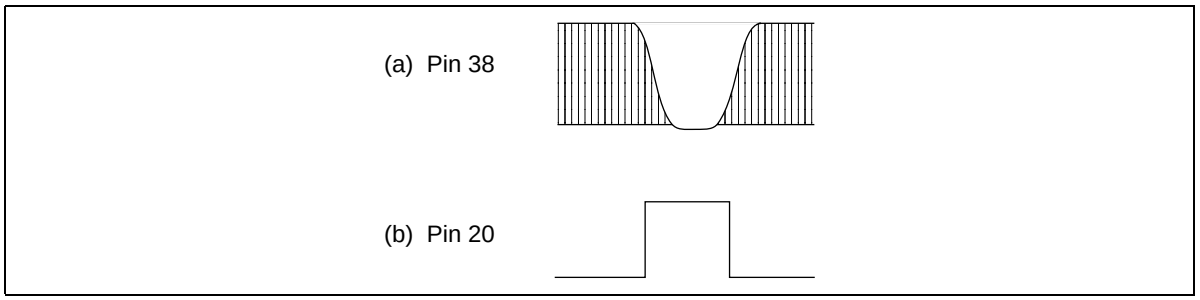


Figure 9 Defect Detector Waveforms

6. Mirror Detector

As the pick-up travels across tracks, the EFM RF signal varies as in figure 10 (a). At pin 34, the signal varies as in figure 10 (b). The mirror detector detects the mirror areas. The external capacitor on pin 33 integrates the track-crossing frequency component.

The internal time constant of the mirror detector can be set for normal, double, or quadruple speed by microprocessor commands, to raise the trackable range of track-crossing frequencies.

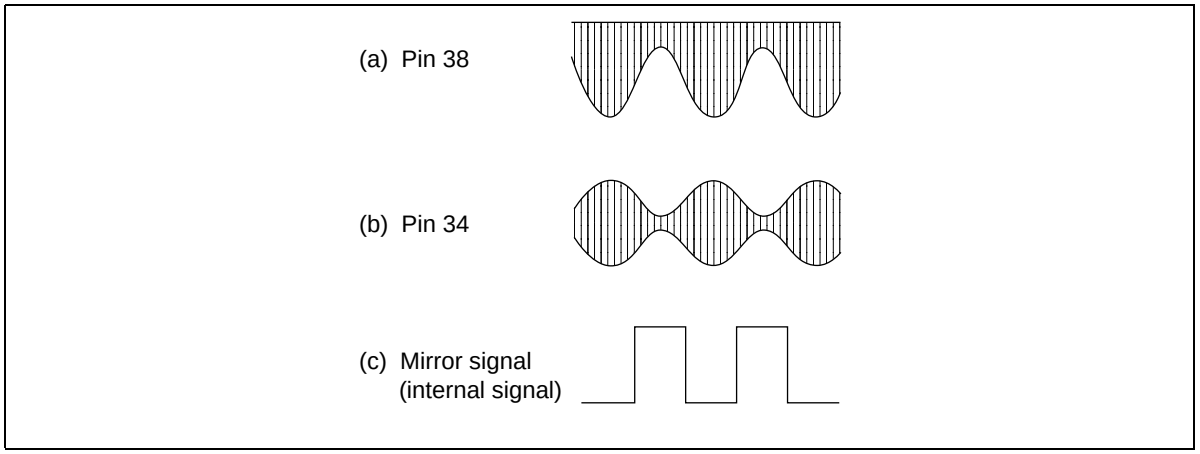


Figure 10 Mirror Detector Waveforms

7. Bias

The 12-kΩ external resistor on pin 36 sets the reference value of the IC's internal bias current. Use only this resistance value. The IC will not operate correctly with other resistance values.

Pin 35 is for a bypass capacitor to eliminate noise from the IC's internal bias circuits.

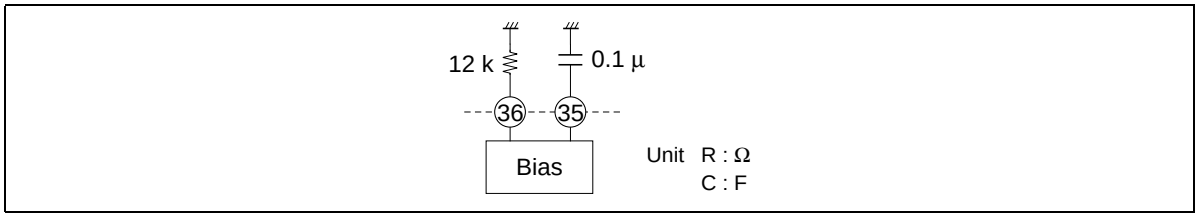


Figure 11 Bias

8. APC

This circuit is for the Psub laser diode. The APC circuit is switched off when pin 28 is high.

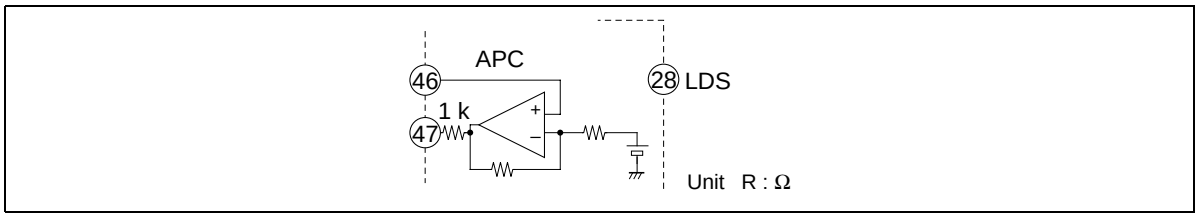


Figure 12 APC

9. Focus Servo System

The focus error signal is led in through a gain-control resistor to pin 56. Focus bias is adjusted at pin 56.

When a defect is detected, switch DS2 propagates the focus error signal, which is integrated by an internal resistor and external capacitor. Switch DS2 also inverts the phase of the propagated signal.

Switch FS4 is the focus servo loop switch.

Switch FLS switches low frequency filter, thereby switching the AC gain of the servo.

Switch FPS switches the peak phase-compensation frequency. This switch is linked with switch FLS and tracking servo switches TLS and TPS. For example this switch is off at normal, double speed and is on at quadruple speed.

The DC gain from input at pin 56 to output at pin 9 is 19dB. Figure 14 shows the frequency characteristic when pin 4, 5 are open.

Switch FS1 switches a current source to generate the focus search voltage. When switch FS2 is switched on, focus is acquired by switching switch FS1 on and off.

The current through switch FS1 can be switched in two stages: 36µA sink/18µA source, and 18µA sink/9µA source.

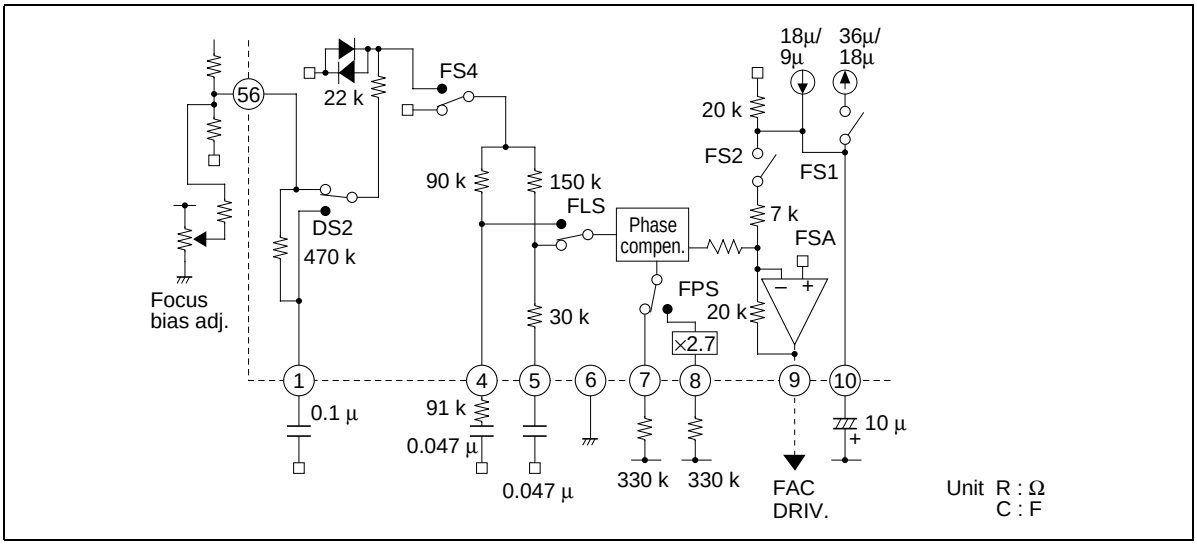
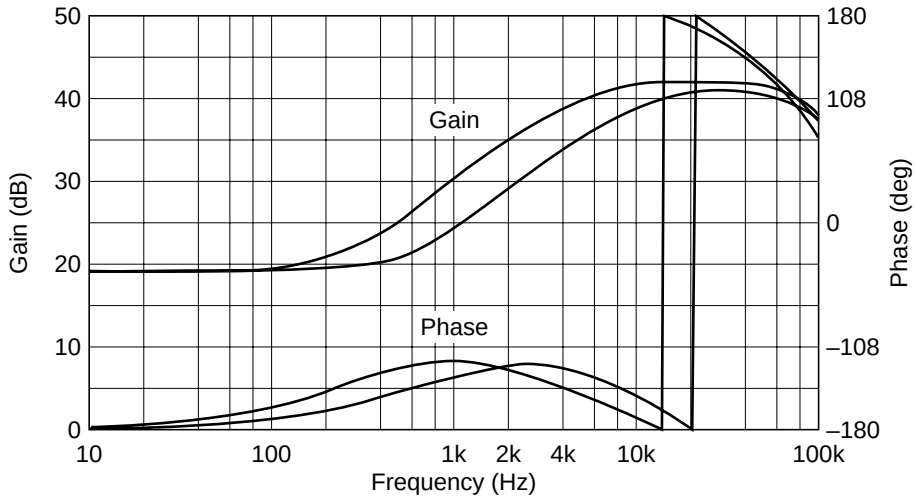


Figure 13 Focus Servo



Note: Peak frequency of phase compensation is inversely proportional to external resistance value (330kΩ at this figure) of pin 7, 8.(dot line : $40 mode, solid line : $42 mode)

Figure 14 Focus Servo Frequency Characteristic (pin 4, 5 are open)

The transform function of phase compen block at figure 13 is as follows.

$$\frac{VOUT}{VIN} \approx \frac{8.95}{1+j\omega\,(2.7\times10^{-6})} \cdot \frac{1+j\omega\left(\frac{7.9\times10^{-9}}{I}\right)}{1+j\omega\left(\frac{5.6\times10^{-10}}{I}\right)}$$

$$\phi \approx \tan^{-1}\omega\left(\frac{7.9\times10^{-9}}{I}\right) - \tan^{-1}\omega\left(\frac{5.6\times10^{-10}}{I}\right) - \tan^{-1}\omega\,(2.7\times10^{-6})$$

at FPS OFF $I = I_7$ at FPS ON $I = 2.7\ I_8$

$$I_7 \text{ or } I_8 \approx \frac{V_{CC} - 0.71V}{\text{External resistance value of pin 7 or 8}}$$

10. Tracking Servo System

The tracking error signal is led in through a gain-control resistor to pin 2.
When a defect is detected, switch DS1 propagates the tracking error signal, which is integrated by an internal resistor and external capacitor. Switch DS1 also inverts the phase of the propagated signal.
Switch TM1 is the tracking servo loop switch.
Switch TLS switches low frequency filter, thereby switching the AC gain of the servo.
The purpose of switch THS is to raise the high-frequency gain.
Switch TPS switches the peak phase-compensation frequency. This switch is linked with switch TLS and focus servo switches FLS and FPS. For example this switch is off at normal, double speed and is on at quadruple speed.
Switch TM7 is turned on by taking the logical AND of COUT and microprocessor data, to improve the performance of the pick-up. COUT is a signal generated by latching Mirror with both edges of TZC.

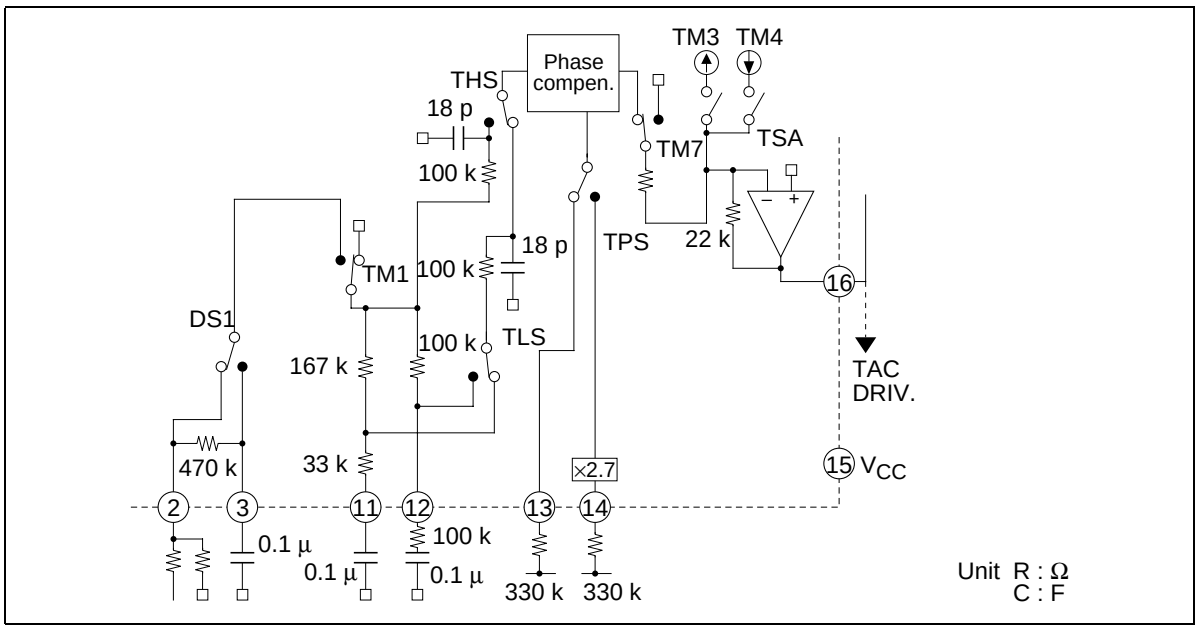
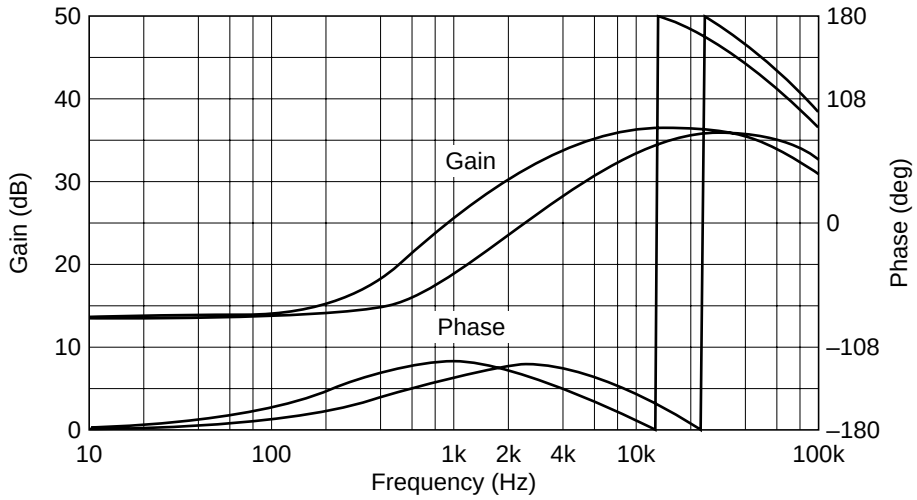


Figure 15 Tracking Servo



Note: Peak frequency of phase compensation is inversely proportional to external resistance value (330kΩ at this figure) of pin 13, 14. (dot line : $40 mode, solid line : $42 mode)

Figure 16 Tracking Servo Frequency Characteristic (pin 11, 12 are open)

The transform function of phase compen block at figure 15 is as follows.

$$\frac{VOUT}{VIN} \approx 4.47 \quad \frac{1+j\omega\left(\frac{7.9\times10^{-9}}{I}\right)}{1+j\omega\left(\frac{5.6\times10^{-10}}{I}\right)}$$

$$\phi \approx \tan^{-1}\omega\left(\frac{7.9\times10^{-9}}{I}\right) - \tan^{-1}\omega\left(\frac{5.6\times10^{-10}}{I}\right)$$

at TPS OFF $I = I_{13}$ at TPS ON $I = 2.7\ I_{14}$

$$I_{13} \text{ or } I_{14} \approx \frac{V_{CC} - 0.71V}{\text{External resistance value of pin 13 or 14}}$$

Figure 17 shows the phase relationships of Mirror, the tracking error, TZC, and COUT. TM7 operates to prevent the moving direction component of the tracking error signal from reaching the actuator.

The purpose of switches TM3 and TM4 is to generate the track jump voltage. A positive voltage appears at pin 16 when TM3 is switched on. A negative voltage appears at pin 16 when TM4 is switched on.

The current values through switches TM3 and TM4 can be selected in four steps: 8μA, 16μA, 24μA, and 32μA. The DC gain from input at pin 2 to output at pin 16 is 13dB. Figure 16 shows the frequency characteristic when pin 11, 12 are open.

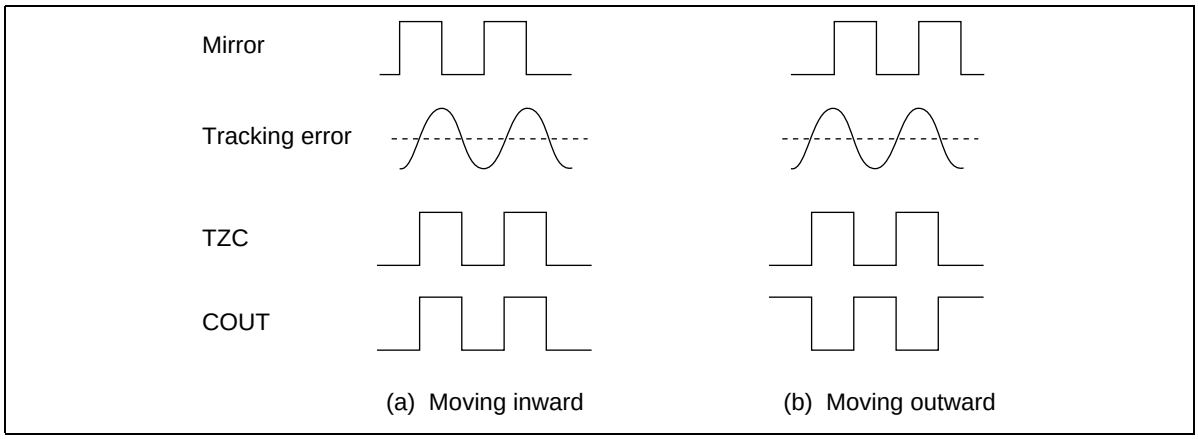


Figure 17 Phase Relationships of Mirror and Other Signals

11. DRT

DRT is an output signal that indicates the inward or outward direction. In the example in figure 18, DRT is low during motion from outer toward inner tracks, and high for motion in the reverse direction. This signal is output from pin 20 on command from the microprocessor.

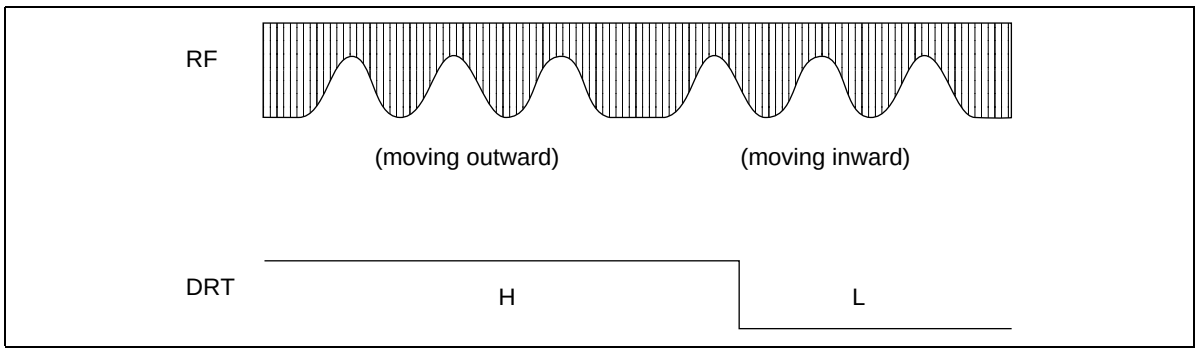


Figure 18 DRT

12. Sled Servo

The signal output at pin 16 is passed through a low-pass filter and input at pin 17. TM2 is the loop switch of the sled servo.

TM5 and TM6 are current switches that generate voltages for large movements of the sled. A positive voltage appears at pin 19 when TM5 is switched on. A negative voltage appears at pin 19 when TM6 is switched on.

The current values through switches TM5 and TM6 can be selected in four steps: 8µA, 16µA, 24µA, and 32µA.

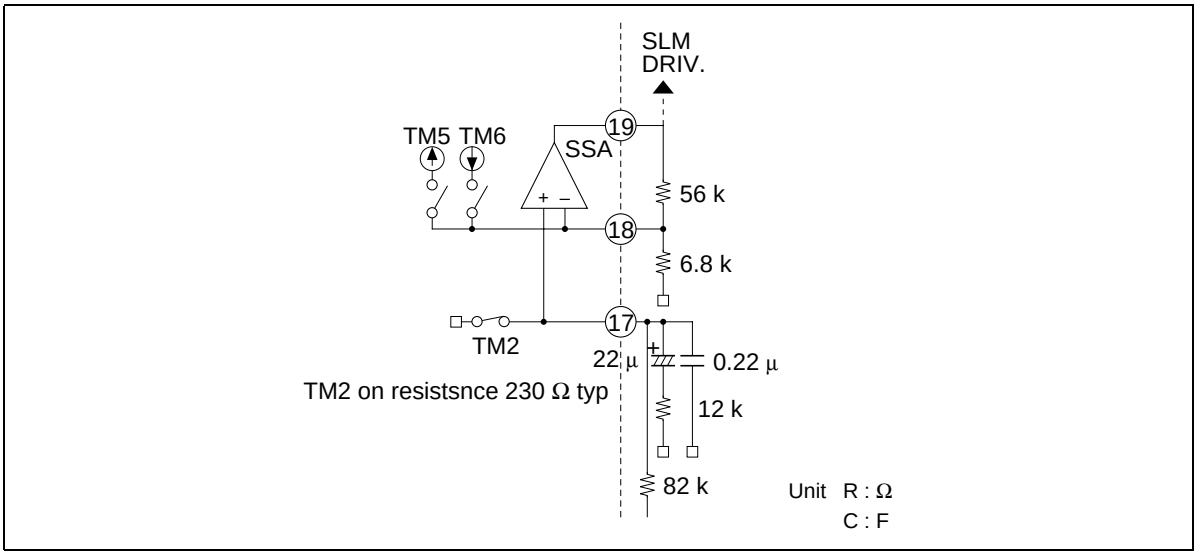


Figure 19 Sled Servo

13. Direct Control

The switches in the tracking control and sled servo control blocks can be switched on and off by microprocessor commands. TM1 to TM6 can also be controlled directly by the DC pin after input of serial data from the microprocessor.

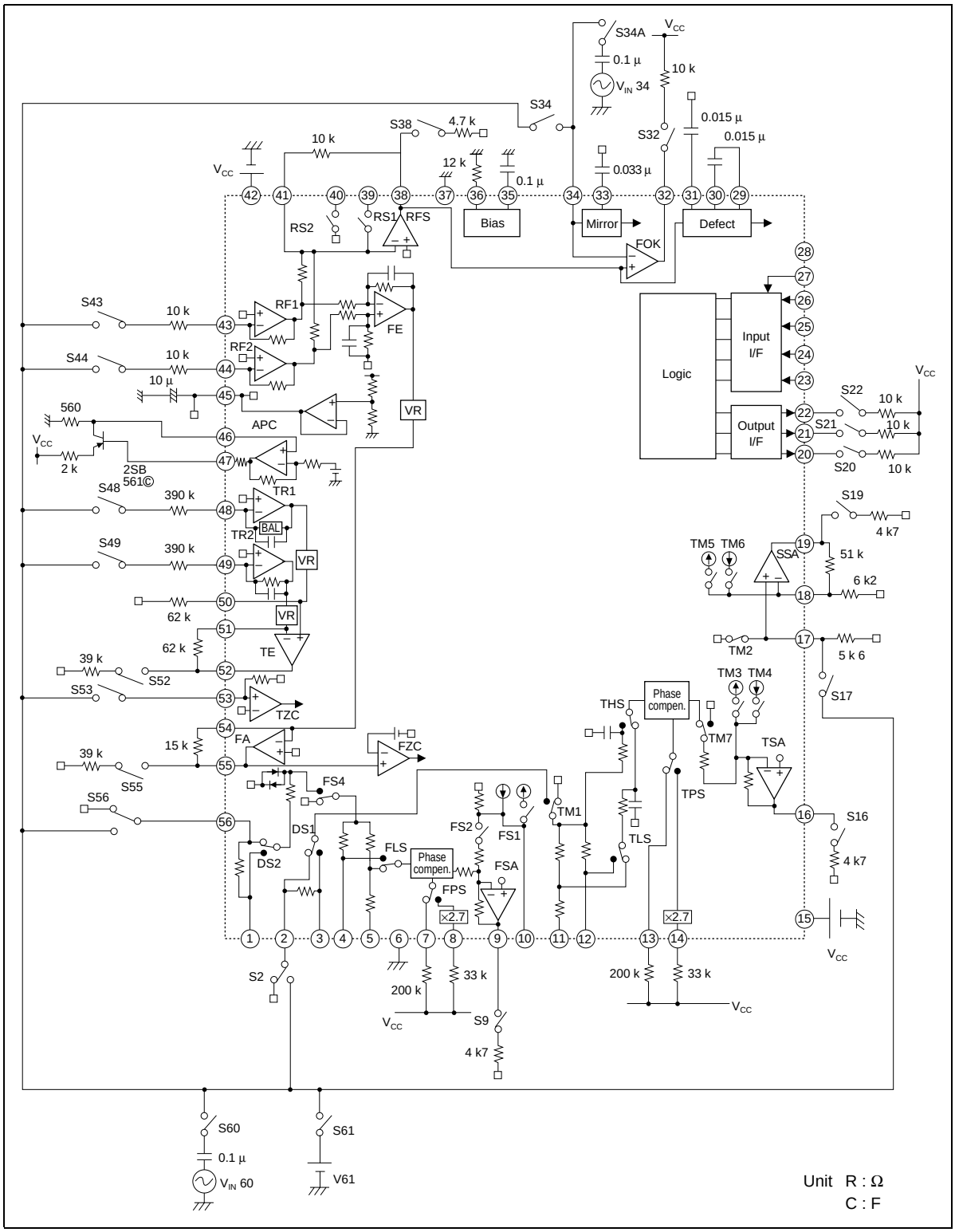
When the microprocessor sends a command from $20 to $2F as serial data with DC high, TM1 to TM6 are placed in the states indicated under ST1 in table 2. Next, when DC is driven low, the states change to ST2. When DC is brought high again, the states change to ST3.

Example of using the DC terminal for 1 track jump is as follows.

For inside track jump, after sending the $2C at DC = “H”, when the TZC’s rising edge is detected set DC = “L” and set DC = “H” after a setting time.

For outside track jump, after sending the $28 at DC = “H”, when the TZC’s falling edge is detected, set DC = “L” and set DC = “H” after a setting time.

Test Circuit Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	7	V
Power dissipation	P_T	550	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Note: Recommended operating power supply voltage range: 5 ±0.5V.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins
1.Current dissipation		I_{CC}	—	36	52	mA	No signal	15, 42
2.Reference voltage		V_C	2.3	2.5	2.7	V	I45 = ±5mA	45
RF amp.	3.Offset voltage	V_{RF}	–65	0	65	mV		38
	4.Max. output level H	V_{RFH}	4.2	—	—	V	S38,S43,S44,S61 V61 = 4.0V	38
	5.Max. output level L	V_{RFL}	—	—	2.1	V	S38,S43,S44,S61 V61 = 1.0V	38
	6.Voltage gain	G_{VRF}	10.0	12.0	14.0	dB	S43, S44, S60 V38/V_{IN} 60	38
Focus error amp.	7.Offset voltage	V_{FA}	–65	0	65	mV		55
	8.Max. output level H	V_{FAH}	4.0	4.5	—	V	S44, S55, S61 V61 = 4.0V	55
	9.Max. output level L	V_{FAL}	—	0.5	1.0	V	S43, S55, S61 V61 = 4.0V	55
	10.Voltage gain 1	G_{VFAI}	6.7	8.7	10.7	dB	S43, S60 V55/V_{IN} 60	55
	11.Voltage gain 2	G_{VFA2}	6.7	8.7	10.7	dB	S44, S60 V55/V_{IN} 60	55
Tracking error amp.	12.Offset voltage	V_{TE}	–50	0	50	mV		52
	13.Max. output level H	V_{TEH}	4.0	4.5	—	V	S49, S52, S61 V61 = 4.0V	52
	14.Max. output level L	V_{TEL}	—	0.5	1.0	V	S48, S52, S61 V61 = 4.0V	52
	15.Voltage gain 1	G_{VTE1}	7.0	9.0	11.0	dB	S49, S60 V52/V_{IN} 60	52
	16.Voltage gain 2	G_{VTE2}	7.0	9.0	11.0	dB	S48, S60 V52/V_{IN} 60	52
FOK	17.FOK Vth	V_{FOK}	0.25	0.38	0.50	V	S34, S61 when V32 ≥ 4V Min (V38 – V34)	32
	18.“H” output voltage	V_{FKH}	4.7	—	—	V	S34, S61	32
	19.“L” output voltage	V_{FKL}	—	—	0.4	V	S32, S34, S61	32
Defect	20.Max operation frequency	F_{DH}	2	—	—	kHz	S43, S44, S60	20
	21.Min operation frequency	F_{DL}	—	—	1	kHz	S43, S44, S60	20
	22.“H” output voltage	V_{DFH}	4.7	—	—	V		20
	23.“L” output voltage	V_{DFL}	—	—	0.4	V	S20	20

Note: All offset voltages are values referring to V_C (pin 45)at XRST = “L”.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins
Defect	24.Operation min input level	V_{DF1}	0.75	—	—	VPP	S43, S44, S60	20
	25.operation max input level	V_{DF2}	—	—	2.5	VPP	S43, S44, S60	20
COUT	26.Max operation frequency	F_{CO}	100	—	—	kHz	S34A, S53, S60 *[1] Mirror Qudruple mode	21
	27.“H” output voltage	V_{COH}	4.7	—	—	V		21
	28.“L” output voltage	V_{COL}	—	—	0.4	V	S21	21
CLK, DATA, XLT, DC, XRST	29.“H” input level	V_{MH}	4.0	—	—	V		23 to 27
	30.“L” input level	V_{ML}	—	—	1.0	V		23 to 27
APC	31.APC voltage	V_{APC}	0.09	0.16	0.23	V		46
32.TZC Vth		V_{TZC}	–40	0	40	mV	S53, S61 Refer to V53	53
33.FZC Vth		V_{FZC}	0.25	0.38	0.50	V	S43, S61	55
Focus servo amp.	34.Offset voltage	V_{FO}	–100	0	100	mV		9
	35.Max output level H	V_{FOH}	4.0	4.5	—	V	S9, S56, S61 FS4 on, V61 = 1.0V	9
	36.Max output level L	V_{FOL}	—	0.8	1.0	V	S9, S56, S61 FS4 on, V61 = 4.0V	9
	37.Voltage gain	G_{VFO}	16.9	18.9	20.9	dB	S56, S60 $V9/V_{IN}$ 60 FS4, FLS, FPS on	9
	38.Search voltage 1	V_{S1}	–0.70	–0.51	–0.32	V	FS2 on $V9 – V_{FO} – V_C$	9
	39.Search voltage 2	V_{S2}	0.32	0.51	0.70	V	FS2, FS1 on $V9 – V_{FO} – V_C$	9
Tracking servo amp.	40.Offset voltage	V_{TO}	–120	0	120	mV		16
	41.Max output level H	V_{TOH}	4.0	4.5	—	V	S2, S16, S61 TM1 on, V61 = 1.0V	16
	42.Max output level L	V_{TOL}	—	0.8	1.0	V	S2, S16, S61 TM1 on, V61 = 4.0V	16

Note: 90deg phase differnce between V_{IN} 34 and V_{IN} 60.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins
Tracking servo amp.	43.Voltage gain	G_{VTO}	11.4	13.4	15.4	dB	S2, S60 TLS, TPS, TM1 on V16/V_{IN} 60	16
	44.TM3 voltage	V_{TM3}	0.51	0.71	0.89	V	TM3 on V16 – V_{TO} – V_C	16
	45.TM4 voltage	V_{TM4}	–0.89	–0.71	–0.51	V	TM4 on V16 – V_{TO} – V_C	16
Sled servo amp.	46.Offset voltage	V_{SO}	–66	0	66	mV		19
	47.Max output level H	V_{SOH}	4.0	4.5	—	V	S17, S19, S61 TM2 on V61 = 4.0V	19
	48.Max output level L	V_{SOL}	—	0.8	1.0	V	S17, S19, S61 TM2 on, V61 = 1.0V	19
	49.Voltage gain	G_{VS}	17.3	19.3	21.3	dB	S17, S60 TM2 on, V19/V_{IN} 60	19
	50.TM5 voltage	V_{TM5}	0.55	0.85	1.10	V	16µA mode TM5 on V19 – V_{SO} – V_C	19
	51.TM6 voltage	V_{TM6}	–1.10	–0.85	–0.55	V	16µA mode TM6 on V19 – V_{SO} – V_C	19
SENS	52.“H” output voltage	V_{SEH}	4.7	—	—	V		22
	53.“L” output voltage	V_{SEL}	—	—	0.4	V	S22	22
LDS	54.“H” input voltage	V_{LDH}	3.5	—	—	V		28
	55.“L” input voltage	V_{LDL}	—	—	0.5	V		28
Focus VR	56.VR gain 1	G_{FVR1}	–5.8	–4.8	–3.8	dB	S43, S60 V55 / V_{IN}60 – G_{VFA1}	55
	57.VR gain 2	G_{FVR2}	–3.2	–2.2	–1.2	dB	S43, S60 V55 / V_{IN}60 – G_{VFA1}	55
	58.VR gain 3	G_{FVR3}	2.8	3.8	4.8	dB	S43, S60 V55 / V_{IN}60 – G_{VFA1}	55
	59.VR gain 4	G_{FVR4}	5.8	6.8	7.8	dB	S43, S60 V55 / V_{IN}60 – G_{VFA1}	55
Tracking VR	60.VR gain 1	G_{TVR1}	–5.9	–4.9	–3.9	dB	S48, S60 V52 / V_{IN}60 – G_{VTE2}	52
	61.VR gain 2	G_{TVR2}	–3.3	–2.3	–1.3	dB	S48, S60 V52 / V_{IN}60 – G_{VTE2}	52
	62.VR gain 3	G_{TVR3}	2.9	3.9	4.9	dB	S48, S60 V52 / V_{IN}60 – G_{VTE2}	52
	63.VR gain 4	G_{TVR4}	5.9	6.9	7.9	dB	S48, S60 V52 / V_{IN}60 – G_{VTE2}	52

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins
BAL	64.BAL gain 1	G_{BA1}	–4.2	–3.2	–2.2	dB	S48, S60 $V52/V_{IN}60 – G_{VTE2}$	52
	65.BAL gain 2	G_{BA2}	–3.7	–2.7	–1.7	dB	S48, S60 $V52/V_{IN}60 – G_{VTE2}$	52
	66.BAL gain 3	G_{BA3}	–3.2	–2.2	–1.2	dB	S48, S60 $V52/V_{IN}60 – G_{VTE2}$	52
	67.BAL gain 4	G_{BA4}	–2.4	–1.4	–0.4	dB	S48, S60 $V52/V_{IN}60 – G_{VTE2}$	52
	68.BAL gain 5	G_{BA5}	1.1	2.1	3.1	dB	S48, S60 $V52/V_{IN}60 – G_{VTE2}$	52
Mirror	69.Operation min input level	V_{MI1}	0.25	—	—	V_{PP}	S34A, S53, S60 Quadraple mode	21
	70.Operation max input level	V_{MI2}	—	—	2.5	V_{PP}	S34A, S53, S60 Quadraple mode	21

Test Method Notes

Item No.	Notes
1	I15 (I15 means “current at pin 15”. Following expressions are same as this expression.)+ I42
2	V45 (V45 means “voltage at pin 45”. Following expressions are same as this expression. These symbols mean DC voltage at DC measuring and AC voltage at AC measuring.)
3	$V38 – V_C$
4, 5	V38
6	$20\log (V38 / V_{IN}60)$ $V_{IN}60$ = 500kHz, 0.2 V_{PP}
7	$V55 – V_C$
8, 9	V55
10, 11	$20\log (V55 / V_{IN}60)$ $V_{IN}60$ = 4kHz, 0.5 V_{PP}
12	$V52 – V_C$
13, 14	V52
15, 16	$20\log (V52 / V_{IN}60)$ $V_{IN}60$ = 4kHz, 0.5 V_{PP}
17	(V38 – V34) at the point that V32 exceeds 4V when V61 is lowered from 2.5V.
18, 19	V32
20	The maximum frequency for VIN60 such that the pin 20 signal is still a square wave. $V_{IN}60 = 0.25 V_{PP} + V_C + 95mV_{DC}$
21	The minimum frequency for VIN60 such that the pin 20 signal is still a square wave. $V_{IN}60 = 0.25 V_{PP} + V_C + 95mV_{DC}$
22, 23	V20

Test Method Notes (cont)

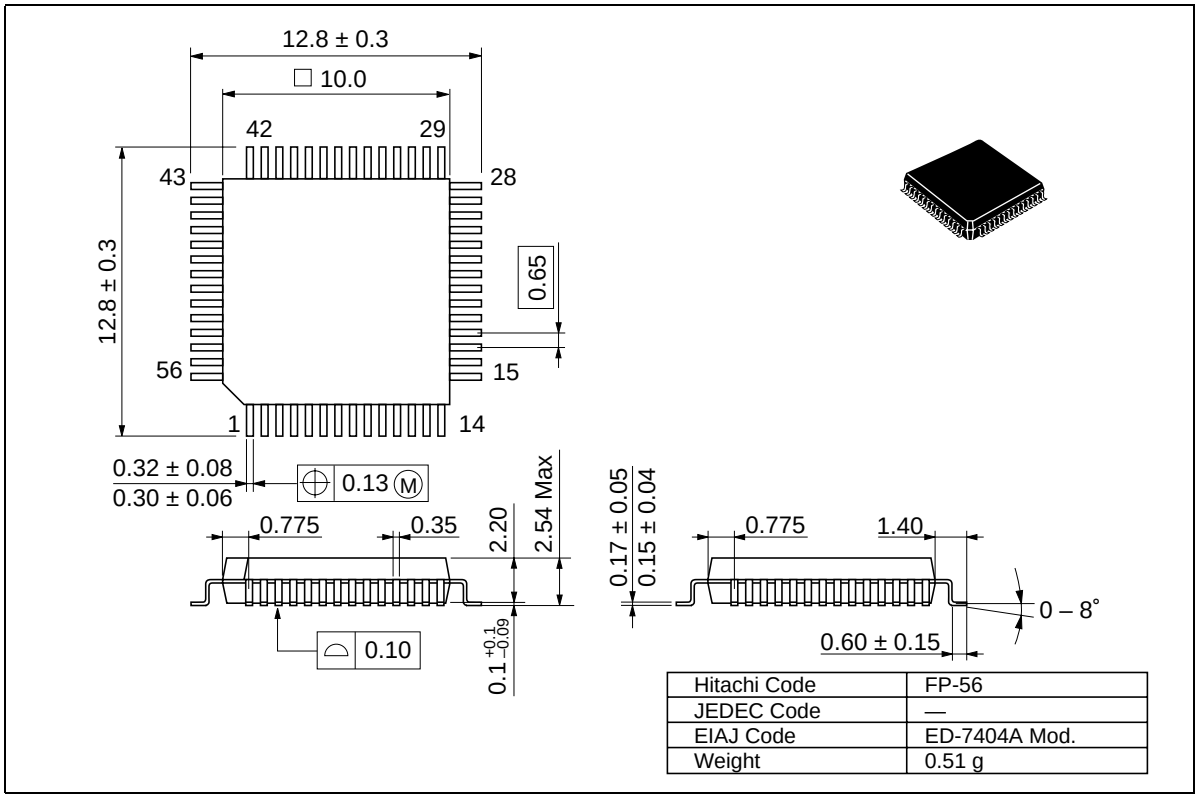
Item No.	Notes
24	The minimum voltage for V38 such that the pin 20 signal is still a square wave. $V_{IN}60$ = 1kHz + V_C + 95mV_{DC}
25	The maximum voltage for V38 such that the pin 20 signal is still a square wave. $V_{IN}60$ = 1kHz + V_C + 95 mV_{DC}
26	$V_{IN}60$, $V_{IN}34$ 90deg phase difference input signal $V_{IN}60 = V_{IN}34 = 1\ V_{PP}$ The maximum frequency for $V_{IN}60$ ($V_{IN}34$) such that the pin 21 signal is still a square wave.
27, 28	V21
29	H input voltage of pin 23 to 27
30	L input voltage of pin 23 to 27
31	V46
32	(V61 – V53) such that V22 exceeds 4V when V61 is upped from 2.4V. (SENS = TZC mode)
33	(V55 – V_C) such that V22 exceeds 4V when V61 is upped from 2.5V. (SENS = FZC mode)
34	V9 – V_C
35, 36	V9
37	20log (V9 / $V_{IN}60$) $V_{IN}60$ = 1kHz, 0.15 V_{PP}
38, 39	V9 – VFO – V_C
40	V16 – V_C
41, 42	V16
43	20log (V16 / $V_{IN}60$) $V_{IN}60$ = 1kHz, 0.3 V_{PP}
44, 45	V9 – VTO – V_C
46	V19 – V_C
47, 48	V19
49	20log (V19 / $V_{IN}60$) $V_{IN}60$ = 4kHz, 0.15 V_{PP}
50, 51	V19 – VSO – V_C
52, 53	V22
54	Input voltage of pin 28 such that APC is off.
55	Input voltage of pin 28 such that APC is on.
56	GF2 = 0, $\overline{GF}1$ = 1, GF0 = 0 20log (V55 / $V_{IN}60$) – G_{VFA1} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
57	GF2 = 0, $\overline{GF}1$ = 1, GF0 = 1 20log (V55 / $V_{IN}60$) – G_{VFA1} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
58	GF2 = 1, $\overline{GF}1$ = 1, GF0 = 0 20log (V55 / $V_{IN}60$) – G_{VFA1} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
59	GF2 = 1, $\overline{GF}1$ = 0, GF0 = 1 20log (V55 / $V_{IN}60$) – G_{VFA1} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
60	GT2 = 0, $\overline{GT}1$ = 1, GT0 = 0 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
61	GT2 = 0, $\overline{GT}1$ = 1, GT0 = 1 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
62	GT2 = 1, $\overline{GT}1$ = 1, GT0 = 0 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5 V_{PP}
63	GT2 = 1, $\overline{GT}1$ = 0, GT0 = 1 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5 V_{PP}

Test Method Notes (cont)

Item No.	Notes
64	$\overline{BAL}3$ = 1, BAL2 = 0, BAL1 = 0, BAL0 = 0 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5V_{PP}
65	$\overline{BAL}3$ = 1, BAL2 = 0, BAL1 = 0, BAL0 = 1 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5V_{PP}
66	$\overline{BAL}3$ = 1, BAL2 = 0, BAL1 = 1, BAL0 = 0 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5V_{PP}
67	$\overline{BAL}3$ = 1, BAL2 = 1, BAL1 = 0, BAL0 = 0 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5V_{PP}
68	$\overline{BAL}3$ = 0, BAL2 = 1, BAL1 = 1, BAL0 = 1 20log (V52 / $V_{IN}60$) – G_{VTE2} $V_{IN}60$ = 4kHz, 0.5V_{PP}
69	The minimum input voltage for VIN34 such that the pin 21 signal is still a square wave. $V_{IN}60$ = 1MHz, 1 V_{PP} $V_{IN}34$ = 100kHz
70	The maximum input voltage for VIN34 such that the pin 21 signal is still a square wave. $V_{IN}60$ = 1MHz, 1 V_{PP} $V_{IN}34$ = 100kHz

Package Dimensions

Unit: mm



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EIAJ Code	ED-7404A Mod.
Weight	0.51 g

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