HA12187FP

Bus Interface Driver/Receiver IC

HITACHI

ADE-207-174A (Z)

2nd Edition
Jun. 1999

Description

The HA12187FP was developed to be used as a bus interface driver/receiver IC in automotive audio equipment controllers. It implements a two-wire serial bus.

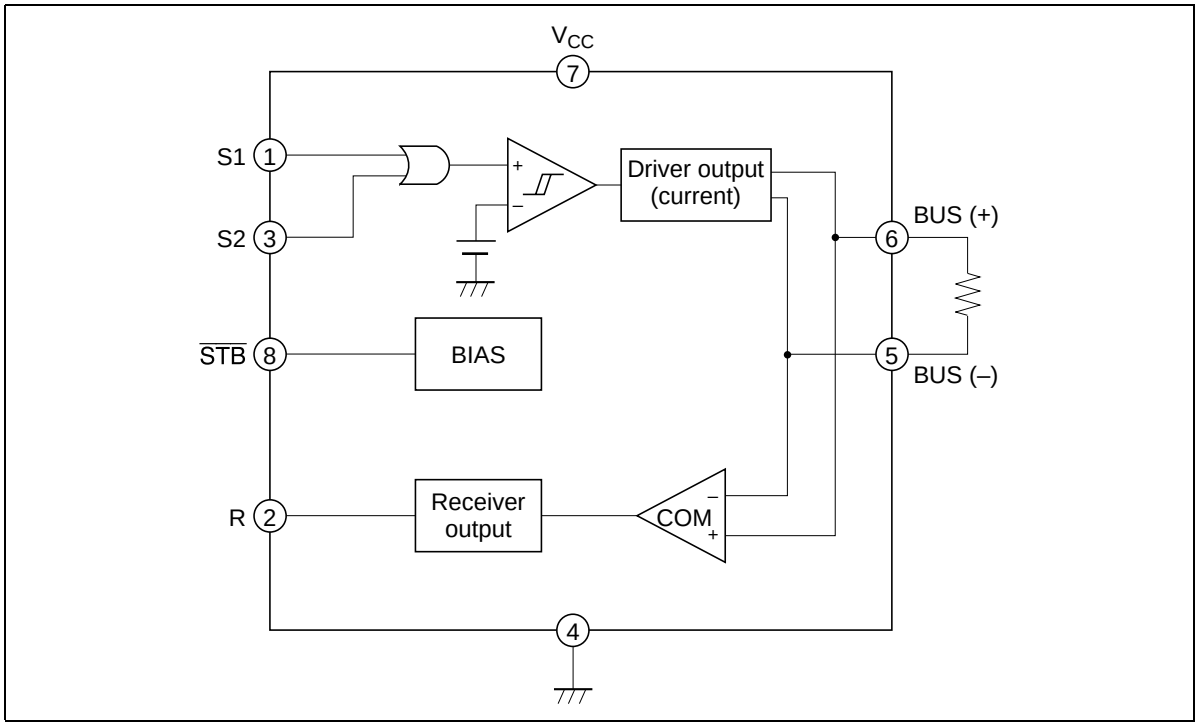
Functions

- Two-input OR circuit
- Input comparator circuit
- Current output driver circuit
- Receiver input comparator circuit
- Receiver output circuit
- Standby circuit

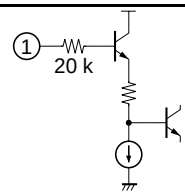
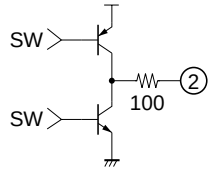
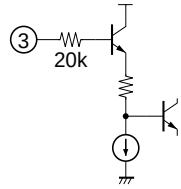
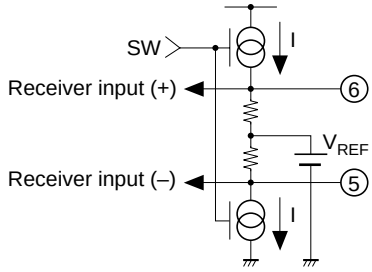
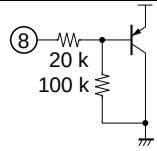
Features

- Supports two data inputs (Pins 1 and 3 are the input pins)
- Comparators with hysteresis characteristics were adopted for the inputs
- Current drive output drivers adopted (Output current: 3.8 mA typical)
- Comparators with hysteresis characteristics were adopted for the receivers
- Wide receiver common-mode input operating range (Common-mode input operating range: 0 to 5 V typical)
- The driver output and the receiver input can withstand high voltages (Maximum rating: 18 V)
- Standby function (The IC enters standby mode when pin 8 goes low)
- Operating power-supply voltage range: 5 V ±0.5 V

Block Diagram



Pin Functions

Pin No.	Symbol	Function	Equivalent Circuit
1	S1	Data input	
2	R out	Receiver output	
3	S2	Data input	
4	GND	GND	
5	BUS (–)	Bus output (–) Receiver input (–)	
6	BUS (+)	Bus output (+) Receiver input (+)	
7	V_{CC}	Power supply	
8	$\overline{STB}$	Standby control input	

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Power-supply voltage	V_{cc}	7	V	
Allowable power dissipation	Pd	400	mW	Ta ≤ 85°C
Operating temperature	Topr	–40 to 85	°C	
Storage temperature	Tstg	–55 to 125	°C	
Input voltage	Vin	–1.0 to 6.7	V	
Bus input voltage	Bus	18	V	

Note: Recommended operating power supply voltage range: 5 V ±0.5 V

Electrical Characteristics (V_{CC} = 5.0 V, Ta = 25°C)

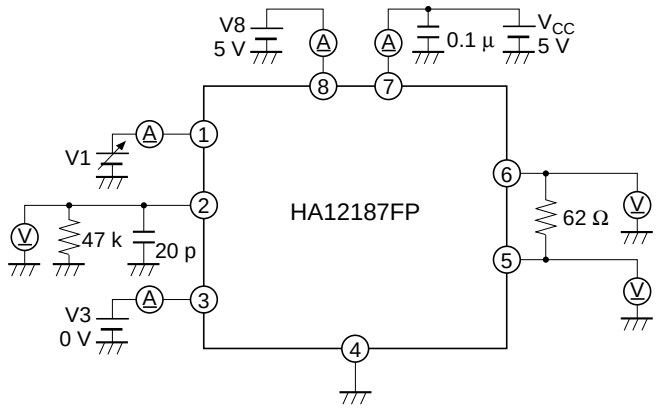
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Test Circuit
S1	High-level input voltage	V_{IHS1}	3.5	—	—	V	V1 = 0 V → 5 V, V3 = 0 V With the potential difference between pin 5 and pin 6 120 mV or more	1	Figure 1
	Low-level input voltage	V_{ILS1}	—	—	1.5	V	V1 = 5 V → 0 V, V3 = 0 V With the potential difference between pin5 and pin 6 20 mV or less	1	
	High-level input current	I_{IHS1}	—	—	1	µA	V1 = 5 V, V3 = 0 V	1	
	Low-level input current	I_{ILS1}	—	—	1	µA	V1 = 0 V, V3 = 0 V	1	
S2	High-level input voltage	V_{IHS2}	3.5	—	—	V	V3 = 0 V → 5 V, V1 = 0 V With the potential difference between pin 5 and pin 6 120 mV or more	3	Figure 1
	Low-level input voltage	V_{ILS2}	—	—	1.5	V	V3 = 5 V → 0 V, V1 = 0 V With the potential difference between 5 and pin 6 20 mV or less	3	
	High-level input current	I_{IHS2}	—	—	1	µA	V1 = 0 V, V3 = 5 V	3	
	Low-level input current	I_{ILS2}	—	—	1	µA	V1 = 0 V, V3 = 0 V	3	
Driver	High-level output current	I_{OH}	3.0	3.8	4.8	mA	$I_{OH} = \| V_{OHD+} - V_{OHD-} \| / 62\ \Omega$	5, 6	Figure 1
	Low-level output leakage current	I_{OL}	—	—	1	µA	Pin 5 voltage = V_{OP-} $I_{OL} = \| V_{OP+} - V_{OP-} \| / RI$	5, 6	
	Reference operating voltage (+)	V_{OP+}	2.3	2.5	2.7	V	V1 = 0 V, V3 = 0 V	6	
	Reference operating voltage (–)	V_{OP-}	2.3	2.5	2.7	V	V1 = 0 V, V3 = 0 V	5	
Current drain 1		$I_{CC}H$	5.5	7.3	9.5	mA	V1 = 5 V, V3 = 0 V	7	Figure 1
Current drain 2		$I_{CC}L$	1.7	2.2	2.7	mA	V1 = 0 V, V3 = 0 V	7	Figure 1

Electrical Characteristics (V_{CC} = 5.0 V, Ta = 25°C) (cont)

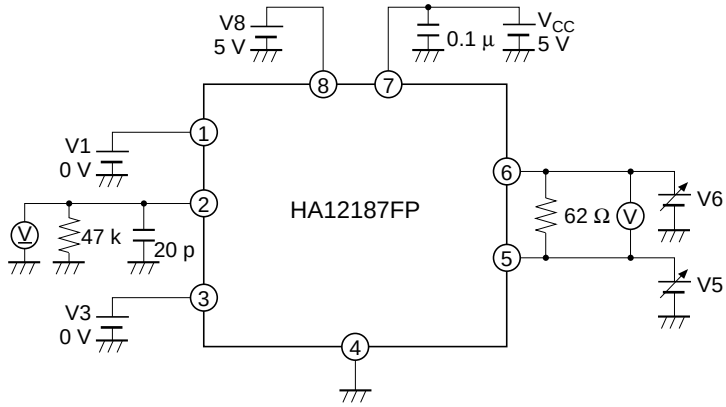
Item		Symbol	Min	Typ	Max	Unit	Test Condition	Test Pin	Test Circuit
Receiver	High-level input voltage (1)	V_{IH1}	—	80	120	mV	V6 = 0 → 5 V, pin 2 = 4 V or more, V1 = 0V, V3 = 0V, V5 = V_{OP-}, V_{IH1} = V6 – V5	2	Figure 2
	Low-level input voltage (1)	V_{IL1}	20	45	—	mV	V6 = 5 → 0 V, pin 2 = 1 V or less, V1 = 0 V, V3 = 0 V, V5 = V_{OP-}, V_{IL1} = V6 – V5	2	Figure 2
	Input hysteresis voltage (1)	V_{IHYS1}	10	35	60	mV	V_{IHYS1} = V_{IH1} – V_{IL1}		
	High-level common-mode input voltage	V_{IHCOM}	4.5	—	—	V	V5 = 0 → 5 V, pin 2 = 4 V or more, V1 = 0 V, V3 = 0 V, V6 – V5 = 120 mV	5	Figure 2
	Low-level common-mode input voltage	V_{ILCOM}	5	—	—	V	V5 = 0 → 5 V, pin 2 = 1 V or less, V1 = 0 V, V3 = 0 V, V6 – V5 = 20 mV	5	Figure 2
	Receiver input resistance*[1]	RI	25	35	45	kΩ	V1 = 0 V, $RI = \frac{0.6\,V}{I1-I2}$	5, 6	Figure 3
	High-level output voltage	V_{OH}	4.5	—	—	V	V1 = 5 V, V3 = 0 V	2	Figure 1
	Low-level output voltage	V_{OL}	—	—	1.0	V	V1 = 0 V, V3 = 0 V	2	Figure 1
Power supply off output leakage current		I_{OLEAK}	—	—	1	µA	V_{CC} off, V8 = 0 V, V6 = 5 V, V1 = 0 V, V3 = 0 V, SW1 on	5, 6	Figure 4
STB on voltage		VSTBon	—	—	1.5	V	V8 = 5 → 0 V, V1 = 5 V, V8 when I_{CC} ≤ 20 µA	7	Figure 4
STB off voltage		VSTBoff	3.5	—	—	V	V8 = 0 → 5 V, V1 = 5 V, V8 when I_{CC} ≥ 4.5 mA	7	Figure 4
Standby mode current drain		I_{CCstb}	—	10	20	µA	V1 = 5 V, V3 = 0 V, V8 = 0 V	7	Figure 4
Standby mode leakage current		Istb-Leak	—	—	1	µA	V1 = 5 V, V3 = 0 V, V8 = 0 V, V6 = 5 V, SW1 on	5, 6	Figure 4
Delay time (L → H)		DLY1	—	600	800	nS	See the operating waveform figure	2	Figure 5
Delay time (H → L)		DLY2	—	450	800	nS	See the operating waveform figure	2	Figure 5

Note: 1. I1 is the measured current when V6 = (V_{OP+}) + 0.3 V, and I2 is the measured current when V6 = (V_{OP+}) – 0.3 V.

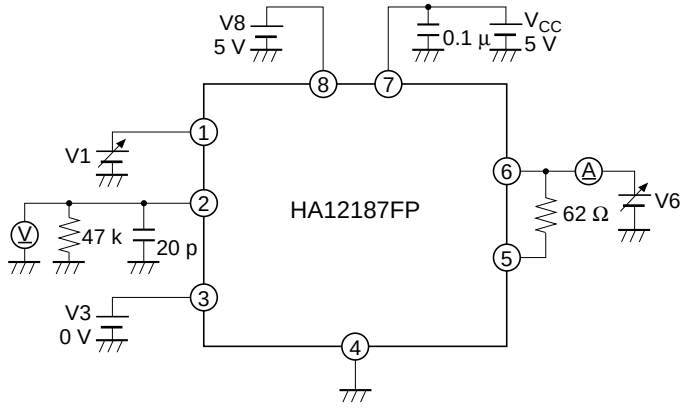
Test Circuits



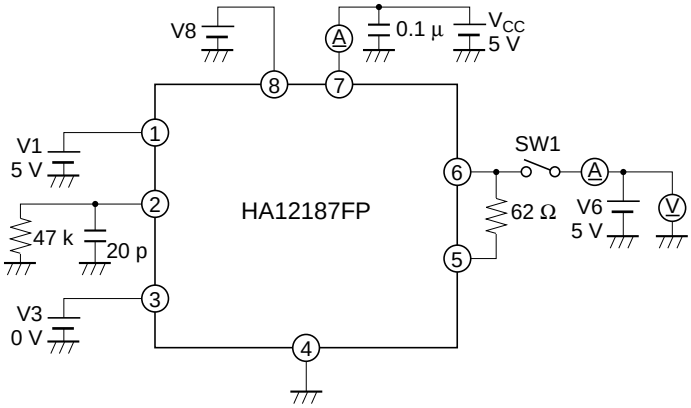
Test Circuit 1



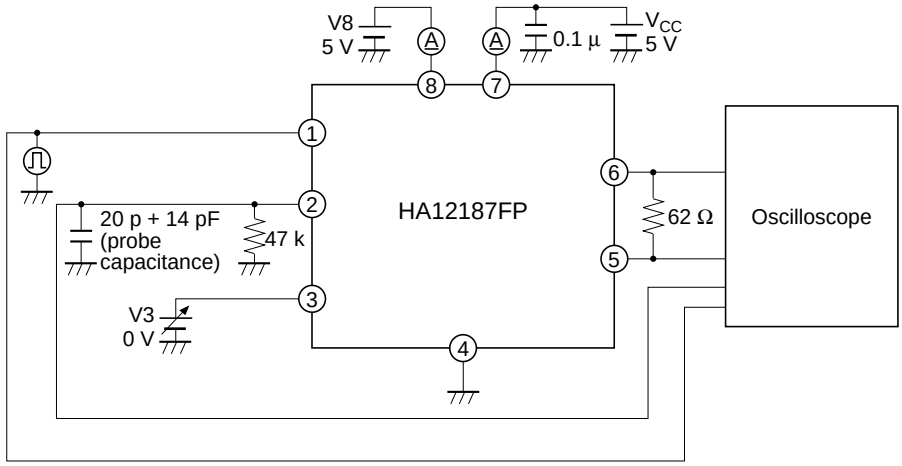
Test Circuit 2



Test Circuit 3

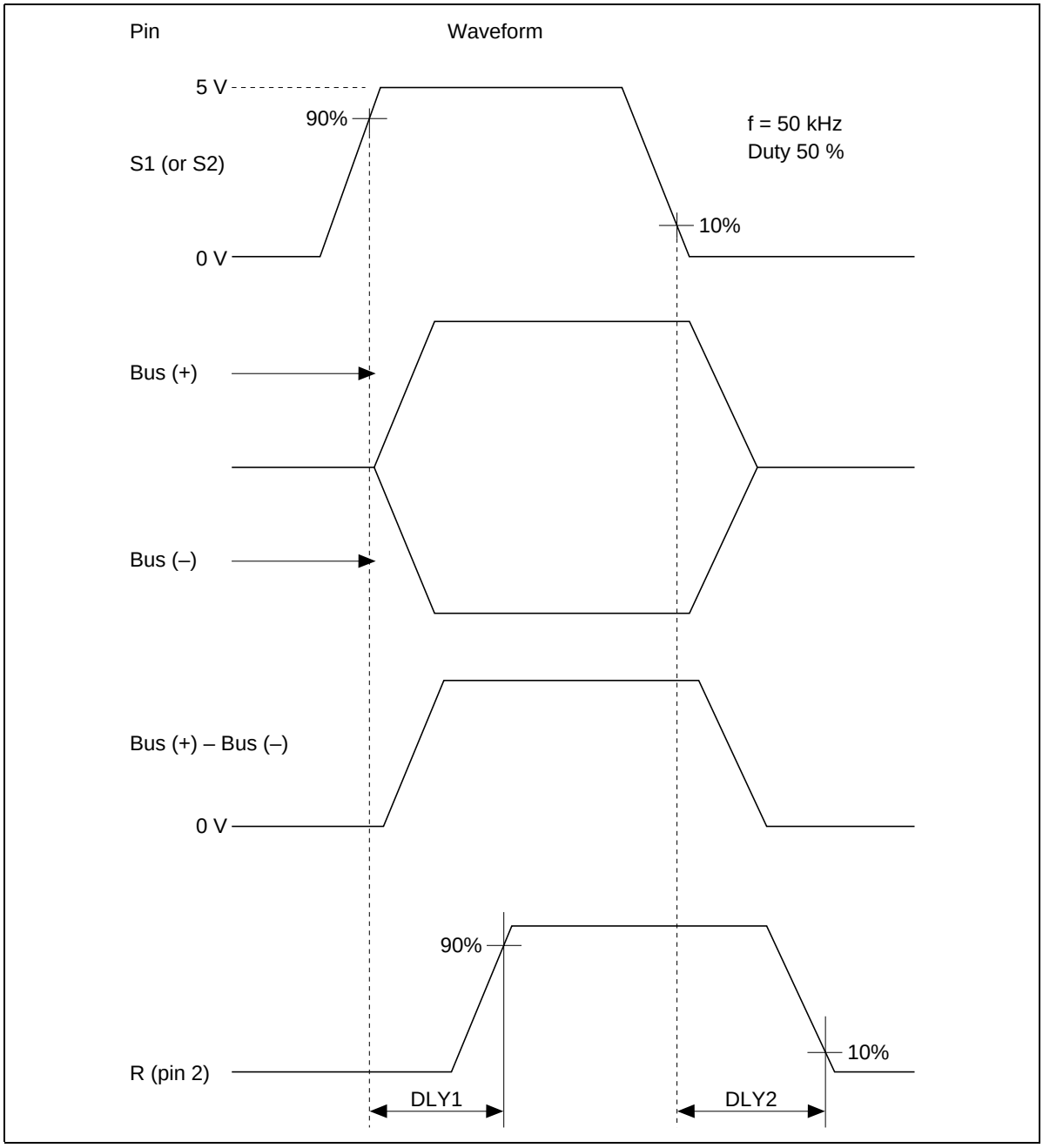


Test Circuit 4

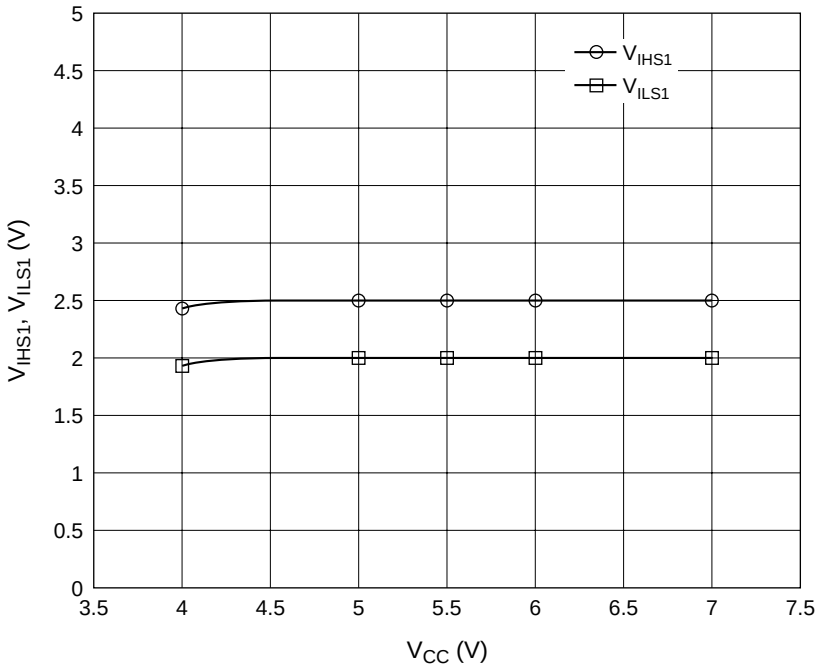


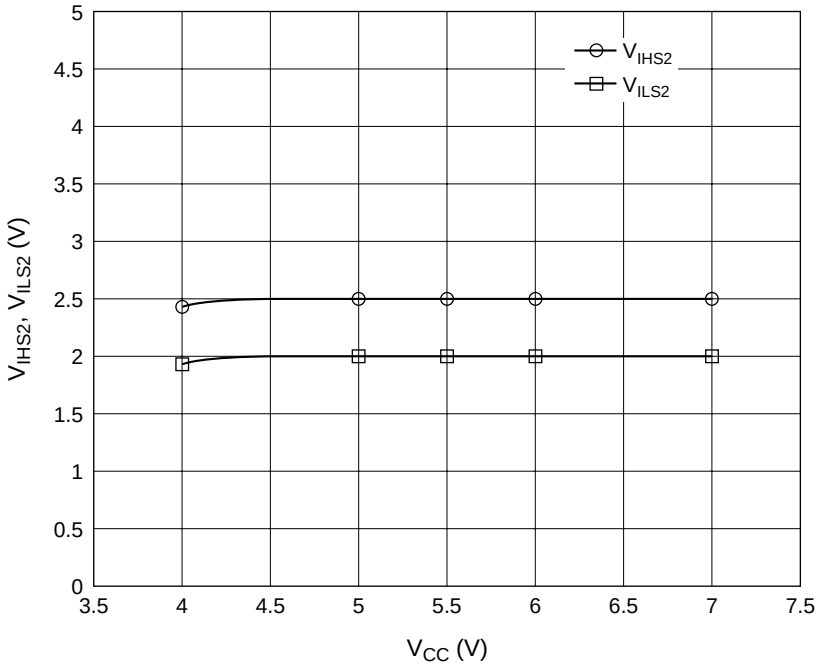
Test Circuit 5

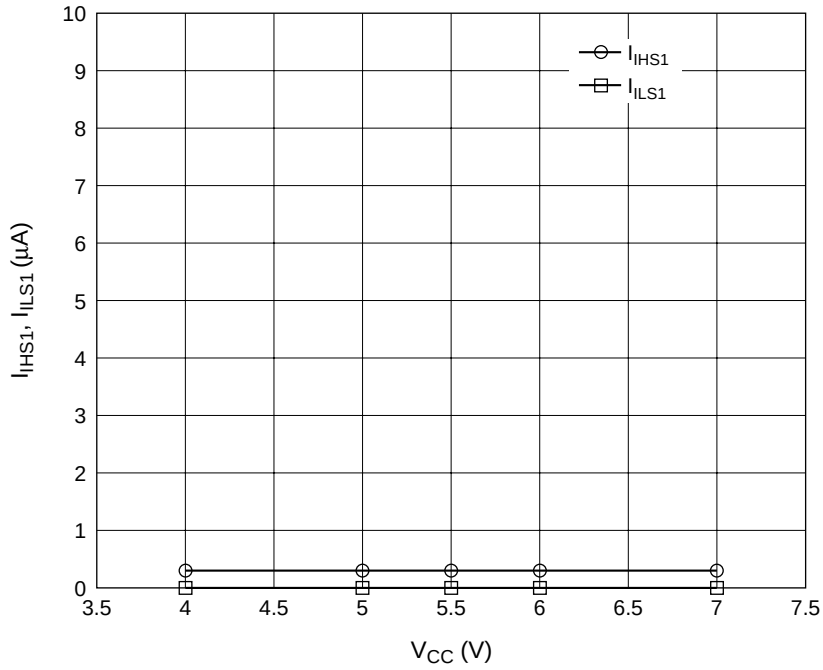
Operating Waveforms



Main Characteristics



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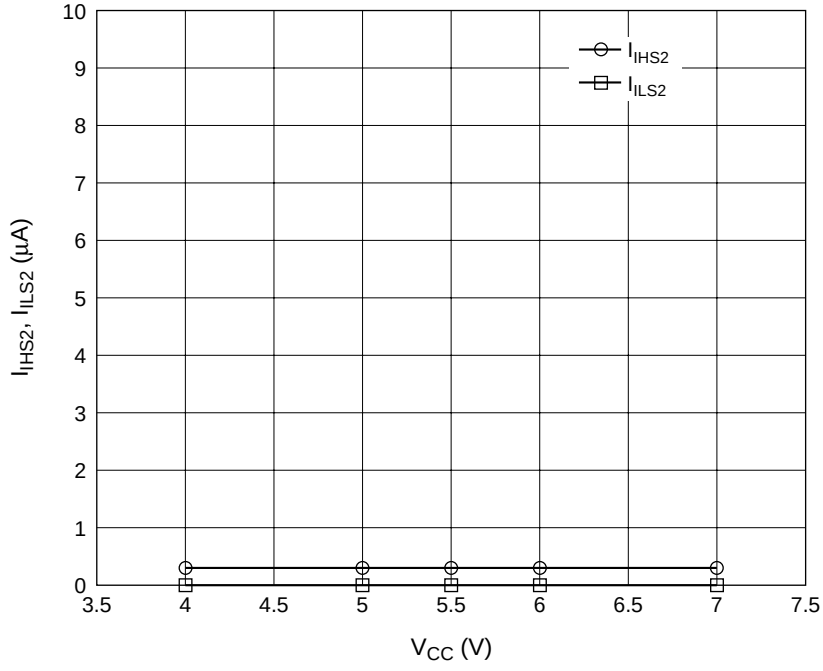
7.5
I_{IHS1}
I_{ILS1}
I_{IHS1}, I_{ILS1} (µA)
V_{CC} (V)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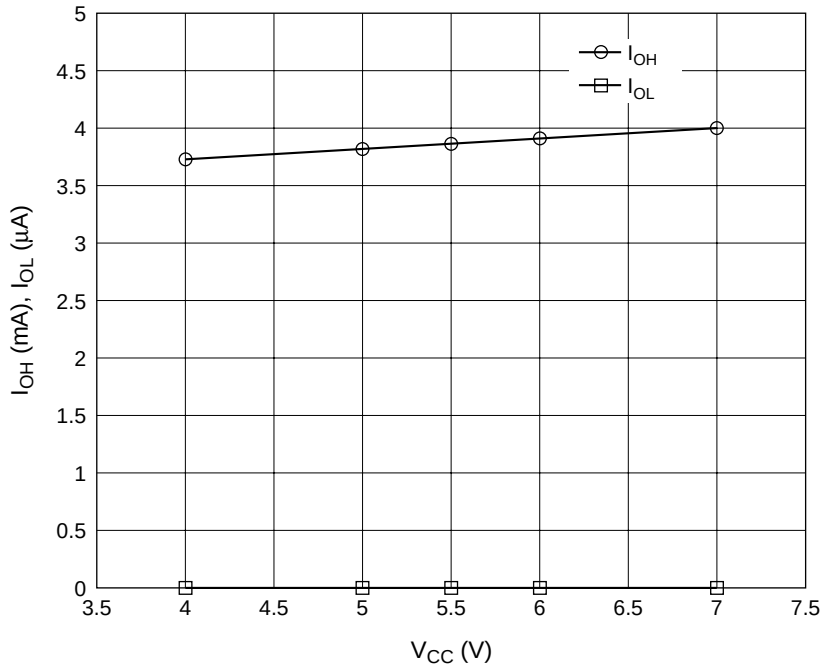
I_{IHS2}
I_{ILS2}
I_{IHS2}, I_{ILS2} (µA)
V_{CC} (V)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6.5
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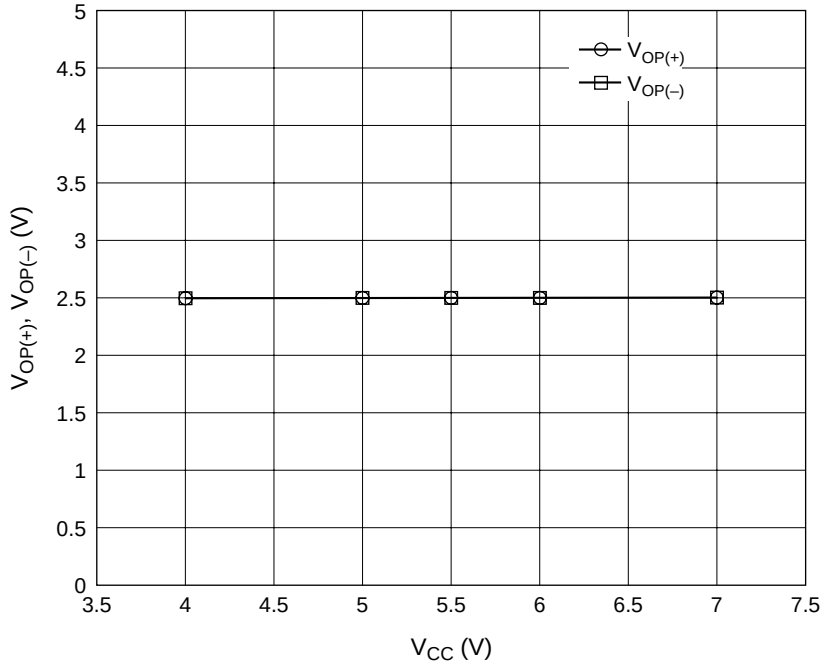
7.5
I_{OH}
I_{OL}
I_{OH} (mA), I_{OL} (µA)
V_{CC} (V)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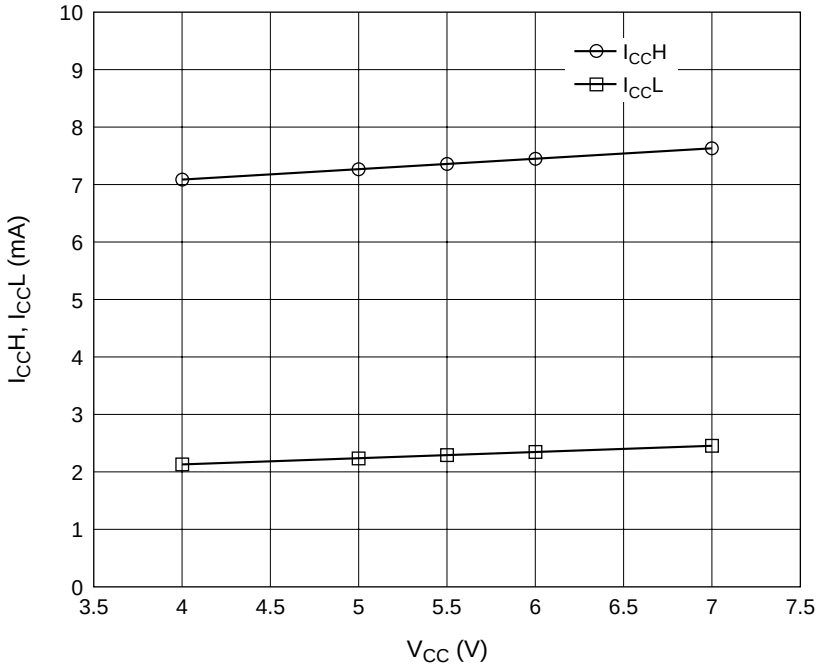
7.5
$V_{OP(+)}$
$V_{OP(-)}$
$V_{OP(+)}$, $V_{OP(-)}$ (V)
V_{CC} (V)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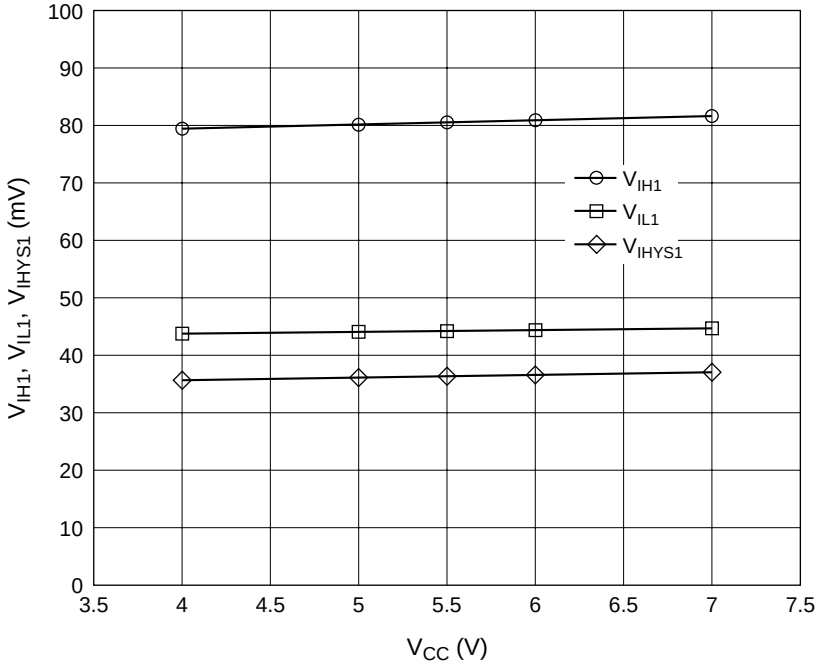
$I_{CC}H$
$I_{CC}L$
$I_{CC}H$, $I_{CC}L$ (mA)
V_{CC} (V)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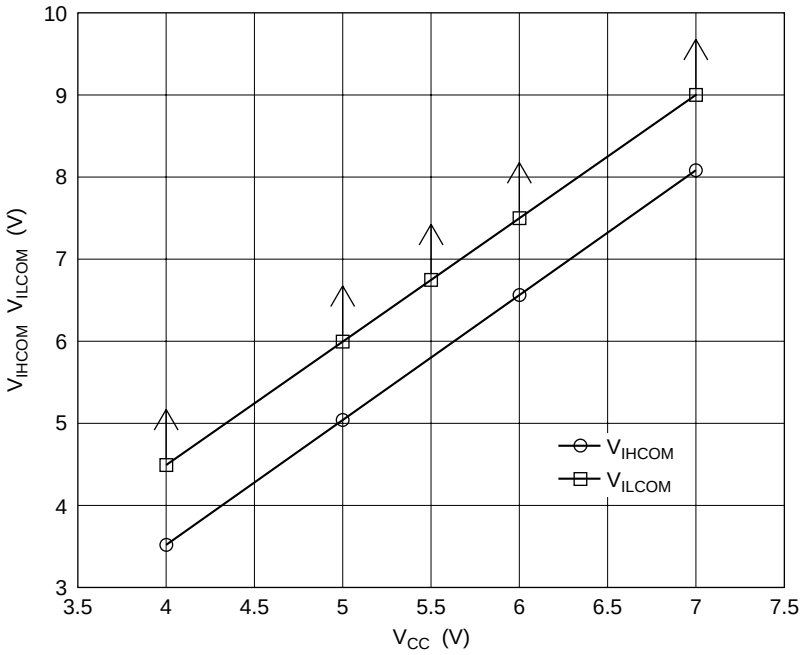
7.5
V_{IH1}
V_{IL1}
V_{IHYS1}
V_{IH1}, V_{IL1}, V_{IHYS1} (mV)
V_{CC} (V)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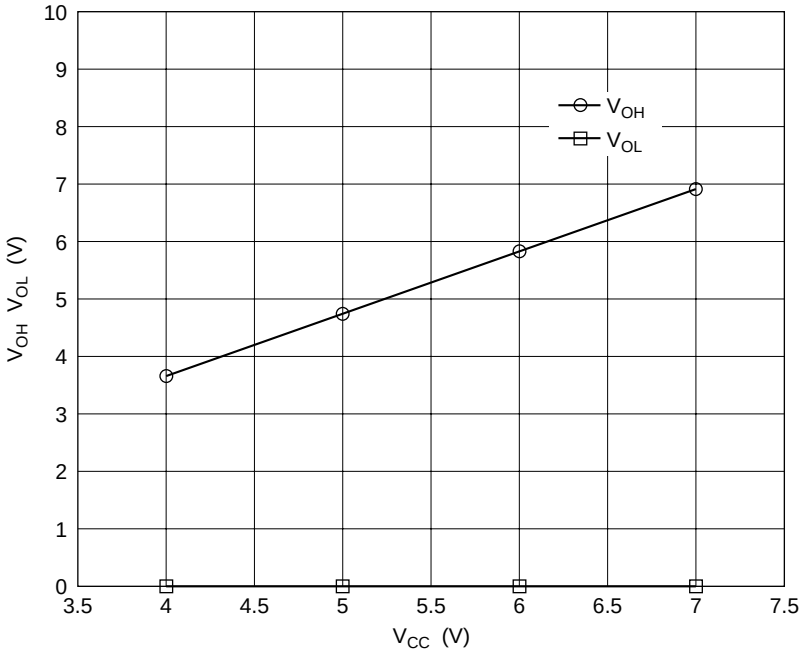
7.5
V_{IHCOM} V_{ILCOM} (V)
V_{CC} (V)
V_{IHCOM}
V_{ILCOM}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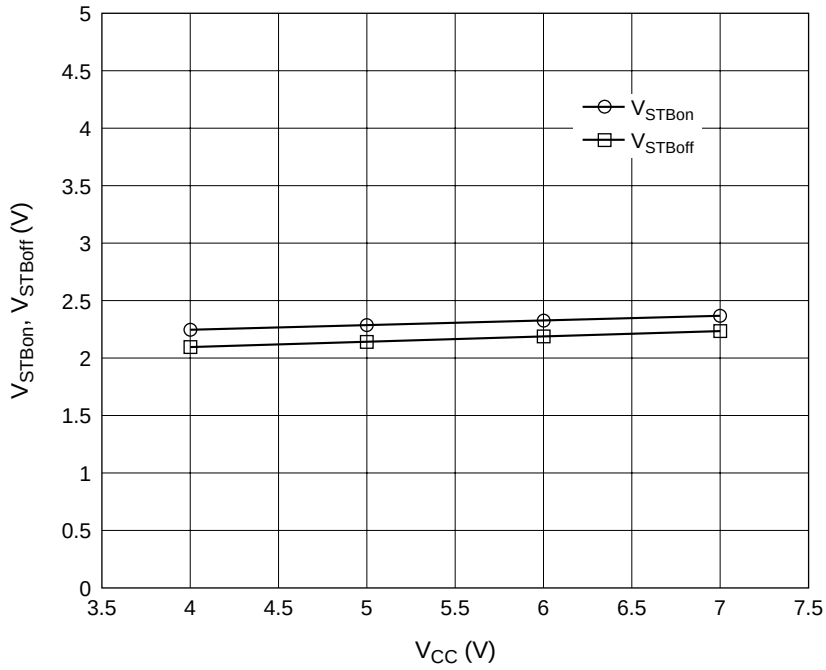
7.5
V_{OH} V_{OL} (V)
V_{CC} (V)
V_{OH}
V_{OL}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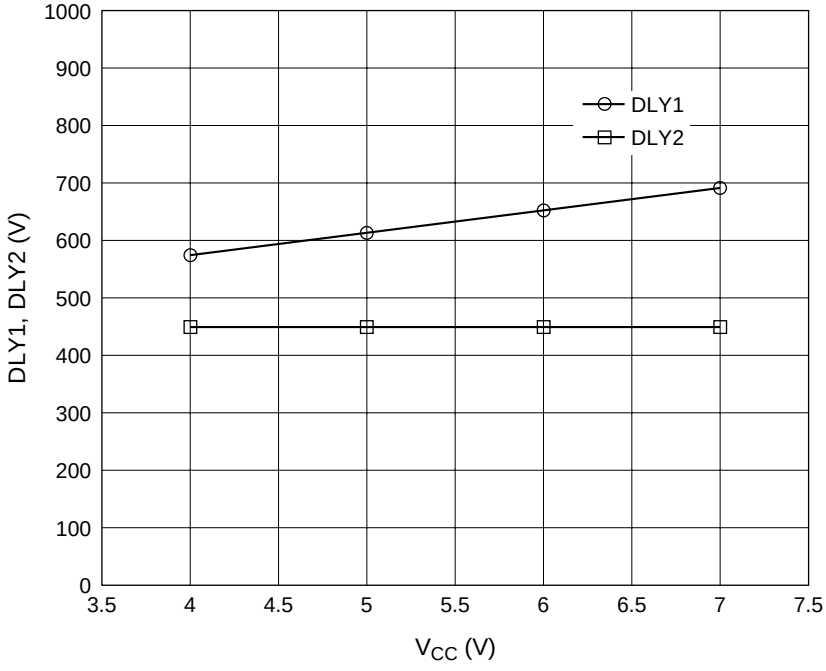
7.5
V_{STBon}
V_{STBoff}
V_{STBon}, V_{STBoff} (V)
V_{CC} (V)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500
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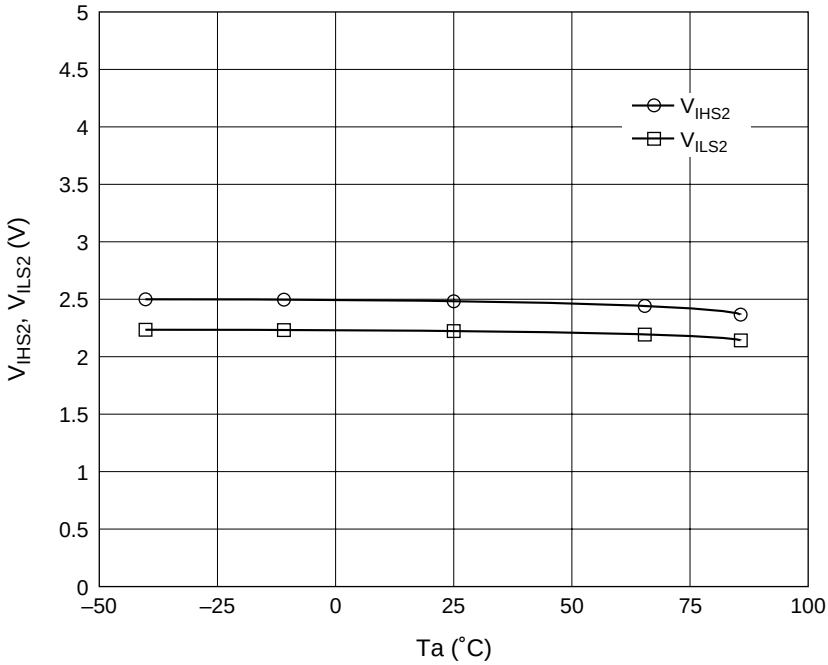
DLY1
DLY2
DLY1, DLY2 (V)
V_{CC} (V)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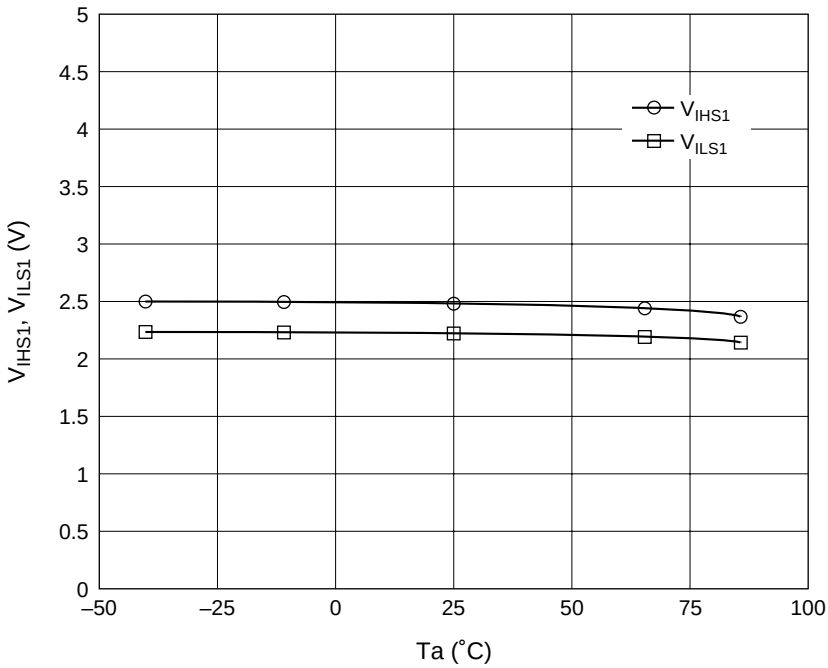
100
Ta (˚C)
V_{IHS2}, V_{ILS2} (V)
V_{IHS2}
V_{ILS2}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–25
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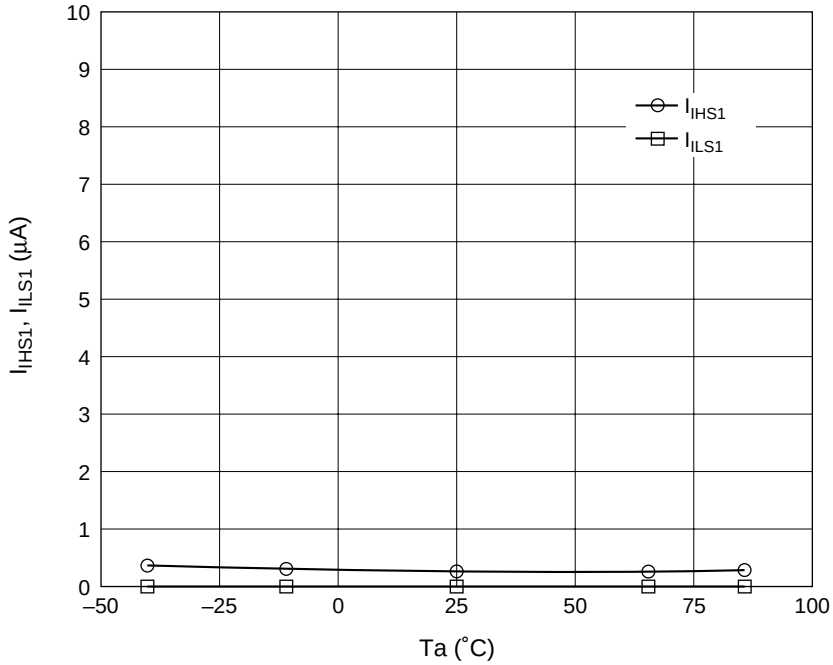
50
75
100
Ta (˚C)
V_{IHS1}, V_{ILS1} (V)
V_{IHS1}
V_{ILS1}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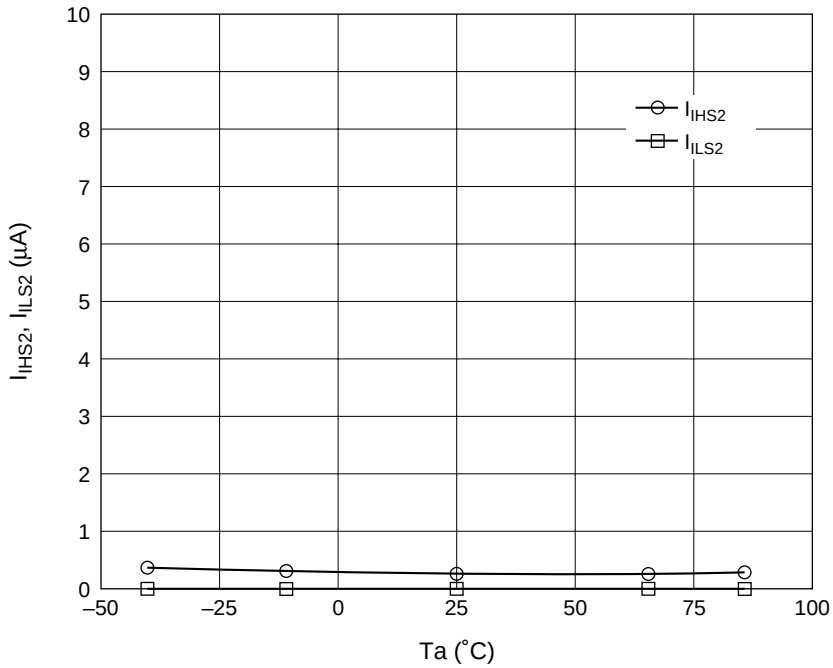
Ta (˚C)
I_{IHS1}, I_{ILS1} (µA)
I_{IHS1}
I_{ILS1}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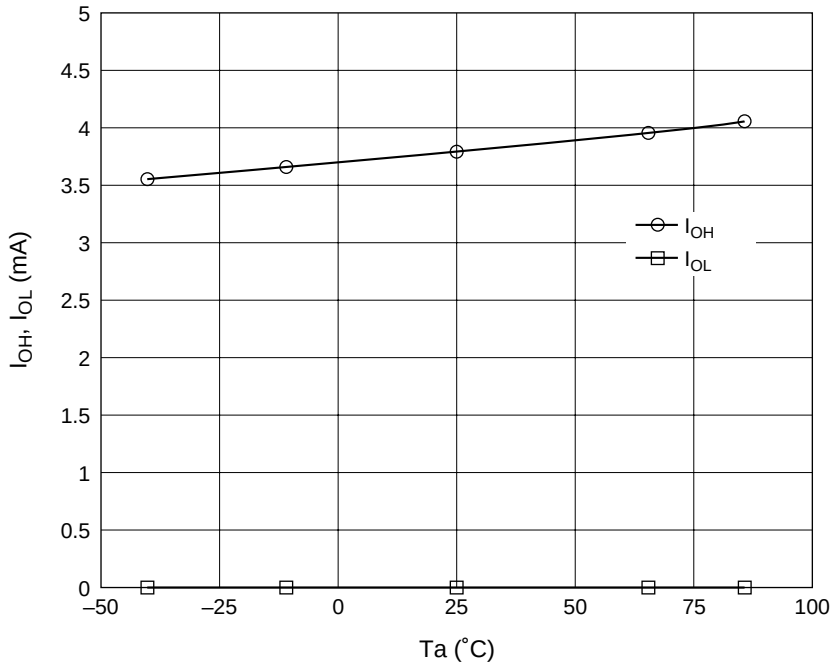
100
Ta (˚C)
I_{IHS2}, I_{ILS2} (µA)
I_{IHS2}
I_{ILS2}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1.5
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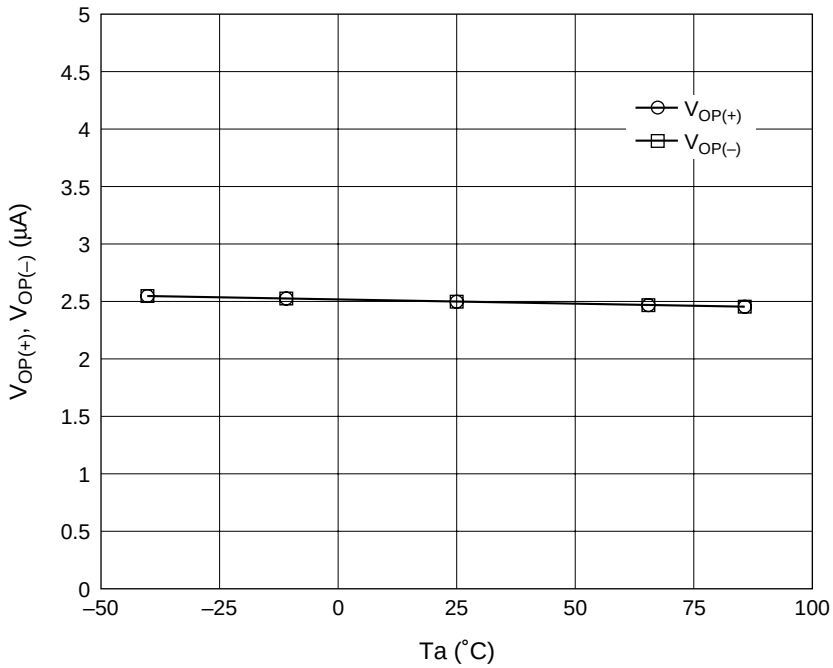
25
50
75
100
I_{OH}, I_{OL} (mA)
Ta (˚C)
I_{OH}
I_{OL}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–50
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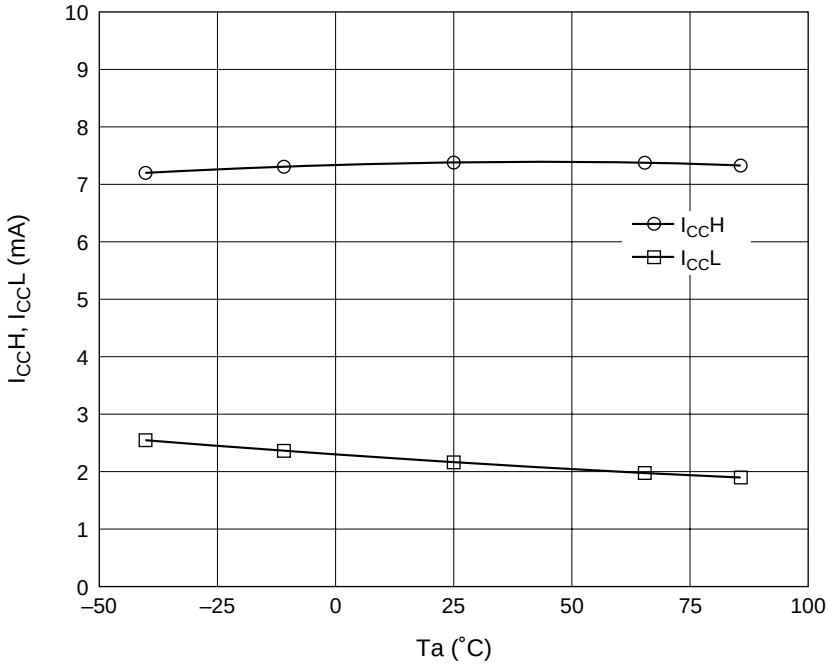
25
50
75
100
$V_{OP(+)}$, $V_{OP(–)}$ (µA)
Ta (˚C)
$V_{OP(+)}$
$V_{OP(–)}$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4
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2
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–25
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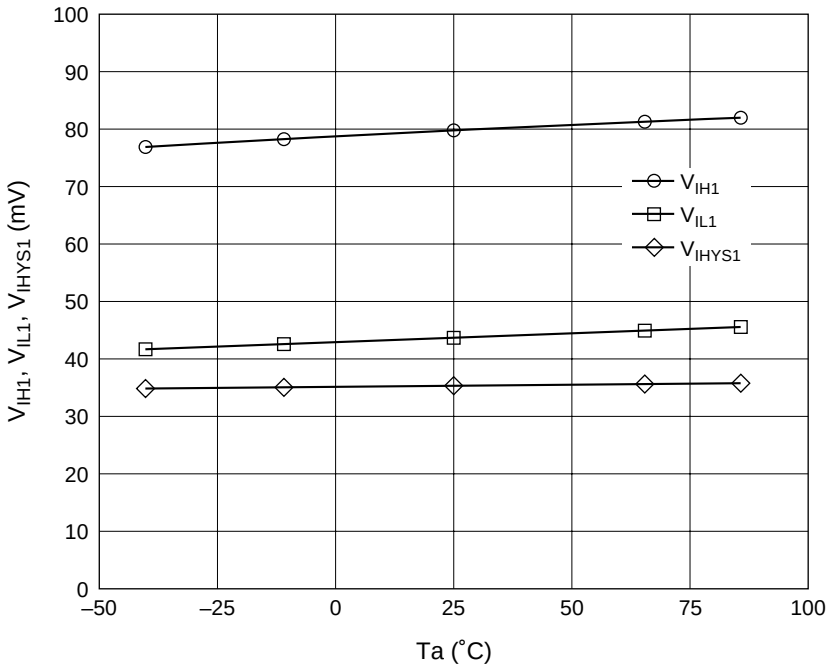
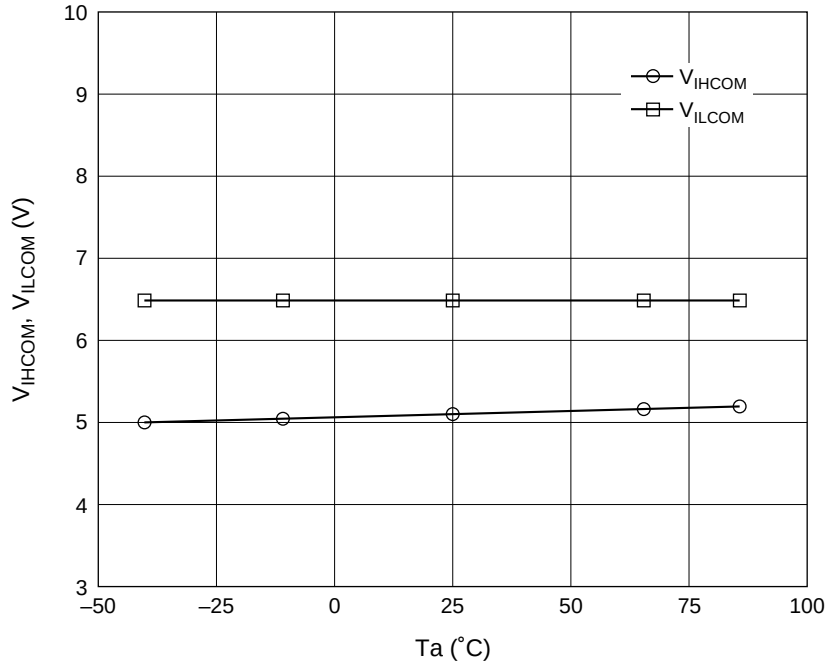
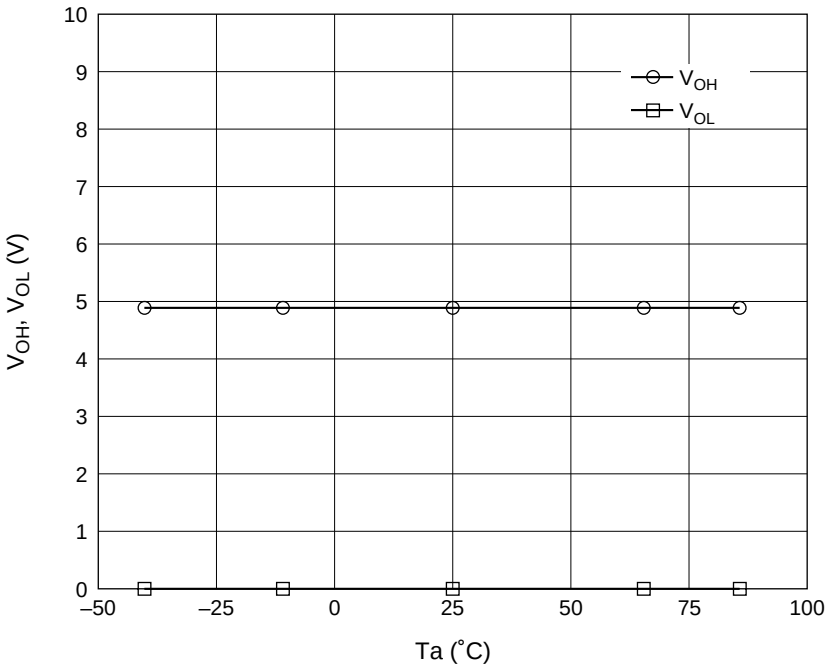
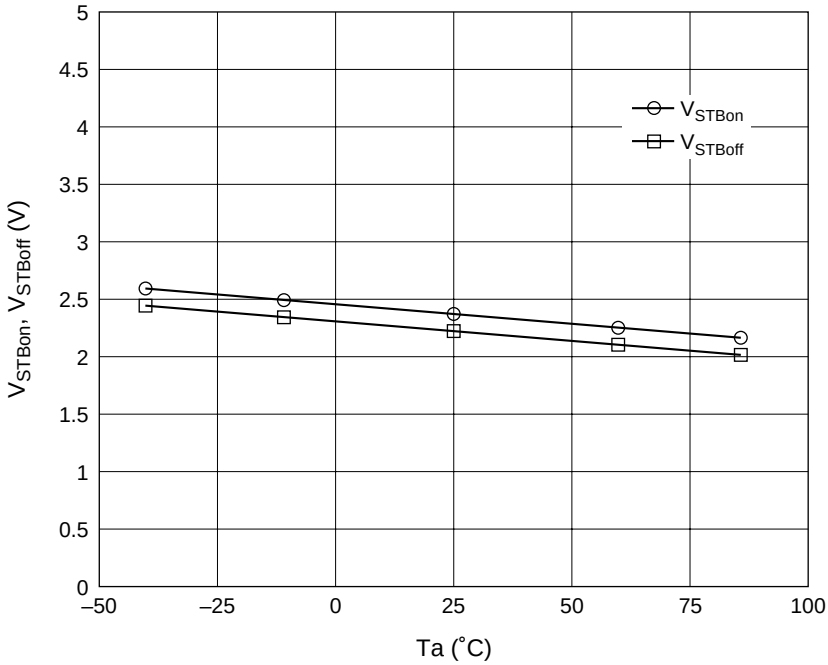
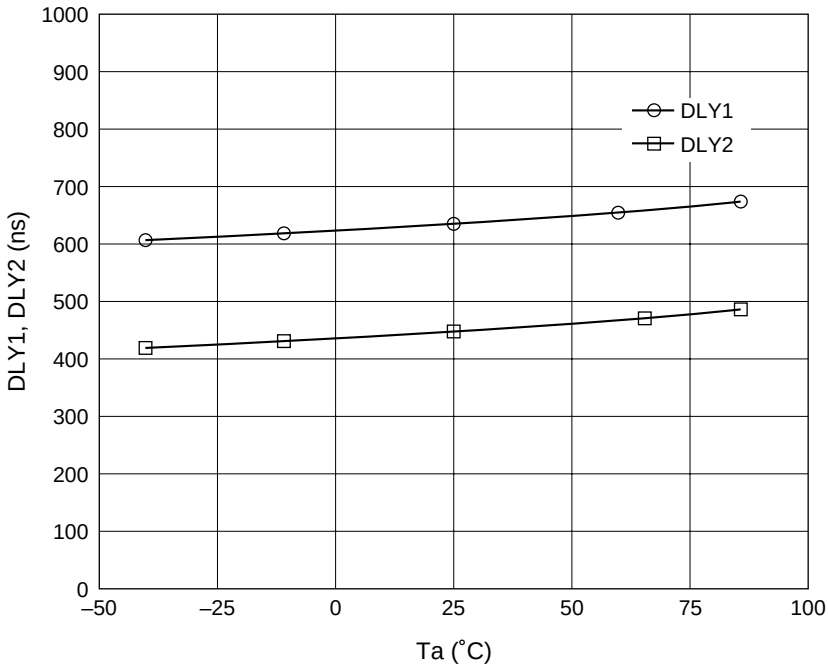
25
50
75
100
Ta (˚C)
$I_{CC}H$, $I_{CC}L$ (mA)
$I_{CC}H$
$I_{CC}L$


100
90
80
70
60
50
40
30
20
10
0
–50
–25
0
25
50
75
100
Ta (˚C)
V_{IH1}, V_{IL1}, V_{IHYS1} (mV)
V_{IH1}
V_{IL1}
V_{IHYS1}


10
9
8
7
6
5
4
3
–50
–25
0
25
50
75
100
V_{IHCOM}
V_{ILCOM}
V_{IHCOM}, V_{ILCOM} (V)
Ta (˚C)

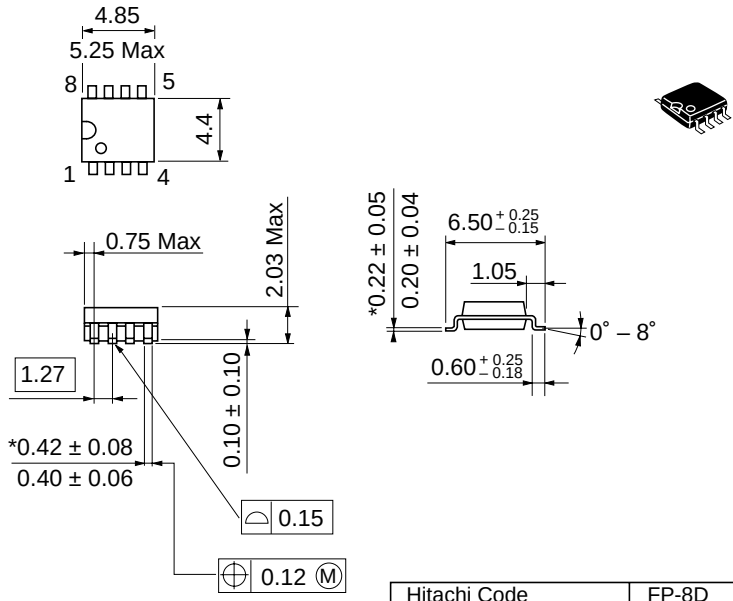

10
9
8
7
6
5
4
3
2
1
0
–50
–25
0
25
50
75
100
V_{OH}
V_{OL}
V_{OH}, V_{OL} (V)
Ta (˚C)


5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
–50
–25
0
25
50
75
100
V_{STBon}
V_{STBoff}
V_{STBon}, V_{STBoff} (V)
Ta (˚C)


1000
900
800
700
600
500
400
300
200
100
0
–50
–25
0
25
50
75
100
DLY1
DLY2
DLY1, DLY2 (ns)
Ta (˚C)

Package Dimensions

Unit: mm



Hitachi Code	FP-8D
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.10 g

*Dimension including the plating thickness
Base material dimension

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