MCP Specification

4Gb (256Mb x16) NAND Flash
+ 4Gb (64Mb x32 2/CS 2CKE) mobile DDR

Document Title

MCP
4Gb (256Mb x16) NAND Flash / 4Gb (2*64Mb x32 2CS 2CKE) DDR

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft - 4Gb NAND Flash D-Die - 4Gb mobile DDR (2 x 2Gb Mobile DDDR A-Die)	Oct. 2010	Preliminary
1.0	First version	Nov. 2010	
1.1	Editorial Change	Mar. 2011	

FEATURES

[MCP]

- Operation Temperature
  - -30°C ~ 85°C
- Packcage
  - 137-ball FBGA - 10.5x13.0mm^2, 1.2t, 0.8mm pitch
  - Lead & Halogen Free

[NAND Flash]

- Multiplane Architecture
- Supply Voltage
  - Vcc = 1.7 - 1.95 V
- Memory Cell Array
  - (1K + 32) words x 64 pages x 4096 blocks
- Page Size
  - (1K+ 32 spare) Words
- Block Size
  - (64K + 2K spare) Words
- Page Read / Program
  - Random access : 25us (max.)
  - Sequential access : 45ns (min.)
  - Page program time : 250us (typ.)
  - Multi-page program time (2 pages) : 250us (typ.)
- COPY BACK PROGRAM
  - Automatic block download without latency time
- FAST BLOCK ERASE
  - Block erase time: 3.5ms (typ.)
  - Multi-block erase time (2 blocks) : 3.5ms (typ.)
- CACHE READ
  - Internal (2048 + 64) Byte buffer to improve the read throughtput.
- STATUS REGISTER
  - Normal Status Register (Read/Program/Erase)
  - Extended Status Register (EDC)
- BLOCK PROTECTION
  - To Protect Block against Write/Erase
- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions.
- DATA RETENTION
  - 100,000 Program / Erase cycles (with 1bit /528Byte ECC)
  - 10 Year Data retention

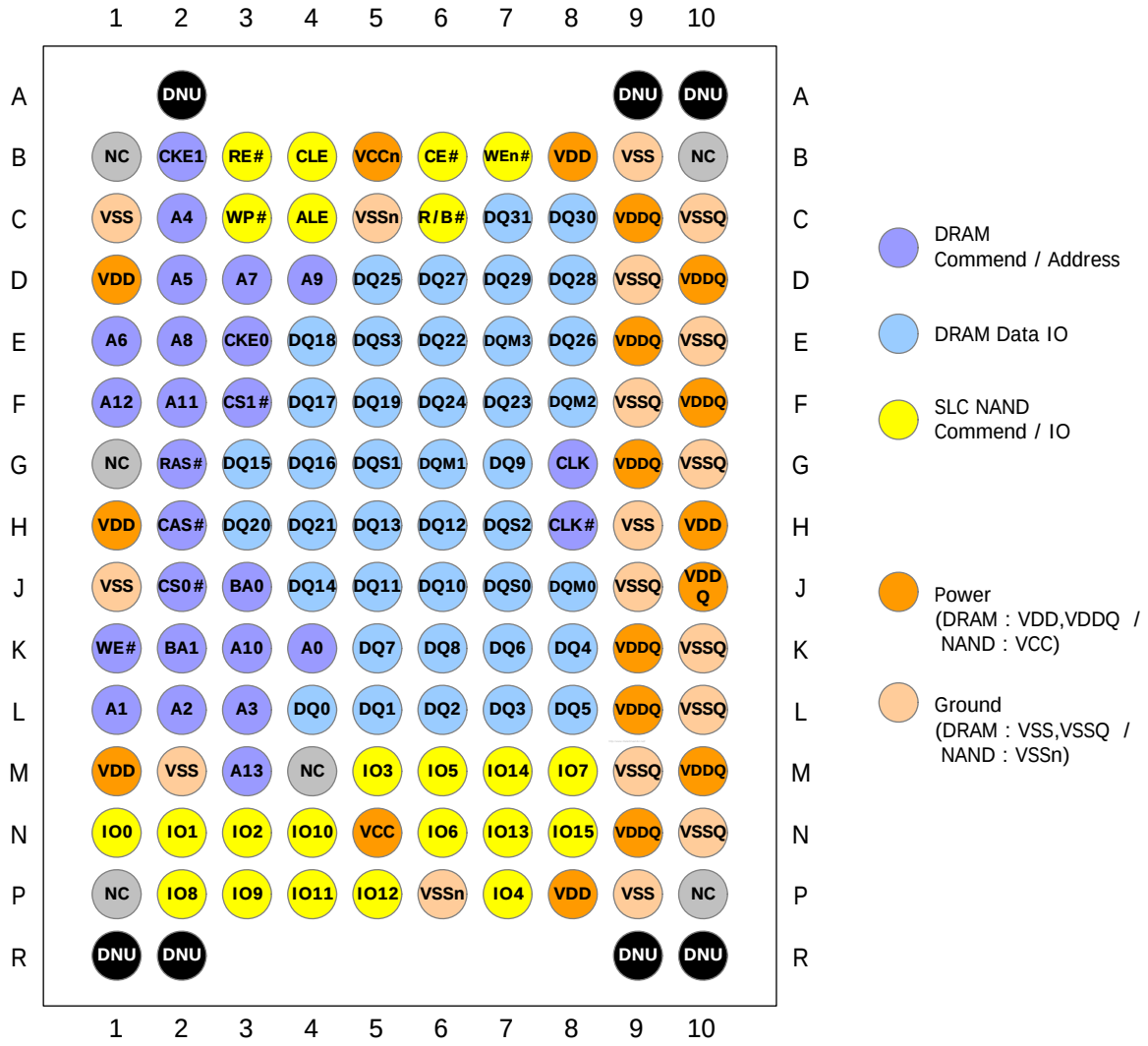
[DDR SDRAM]

- Double Data Rate architecture
  - two data transfer per clock cycle
- x32 bus width
- Supply Voltage
  - VDD / VDDQ = 1.7 - 1.95 V
- Memory Cell Array
  - 16Mb x 4Bank x 32 I/O x 2 Die
- Bidirectional data strobe (DQS)
- Input data mask signal (DQM)
- Input Clock
  - Differential Clock Inputs (CK, /CK)
- MRS, EMRS
  - JEDEC Standard guaranteed
- CAS Latency
  - Programmable CAS latency 2 or 3 supported
- Burst Length
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H9DA4GH4JJAMCRR-46M	NAND Flash mobile DDR	1.8V 1.8V	4Gb (256Mb x16) 4Gb (64Mb x32 x 2dies)	45ns DDR 333	137Ball FBGA (Lead & Halogen Free)
H9DA4GH4JJAMCR-4QM	NAND Flash mobile DDR	1.8V 1.8V	4Gb (256Mb x16) 4Gb (64Mb x32 x 2dies)	45ns DDR 370	137Ball FBGA (Lead & Halogen Free)
H9DA4GH4JJAMCR-4EM	NAND Flash mobile DDR	1.8V 1.8V	4Gb (256Mb x16) 4Gb (64Mb x32 x 2dies)	45ns DDR 400	137Ball FBGA (Lead & Halogen Free)

Ball Assignment



Top View

137ball 10.5x13 MCP (x16 SLC NAND + x32 LPDDR)

Pin Description

SYMBOL	DESCRIPTION

< 4Gb (256Mb x16) NAND Flash >

I/O0 ~ I/O15	Data Input / Output
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy Out
VCC	Supply Voltage
VSS	Ground

< 4Gb (2*64Mb x32 2CS 2CKE) mobile DDR >

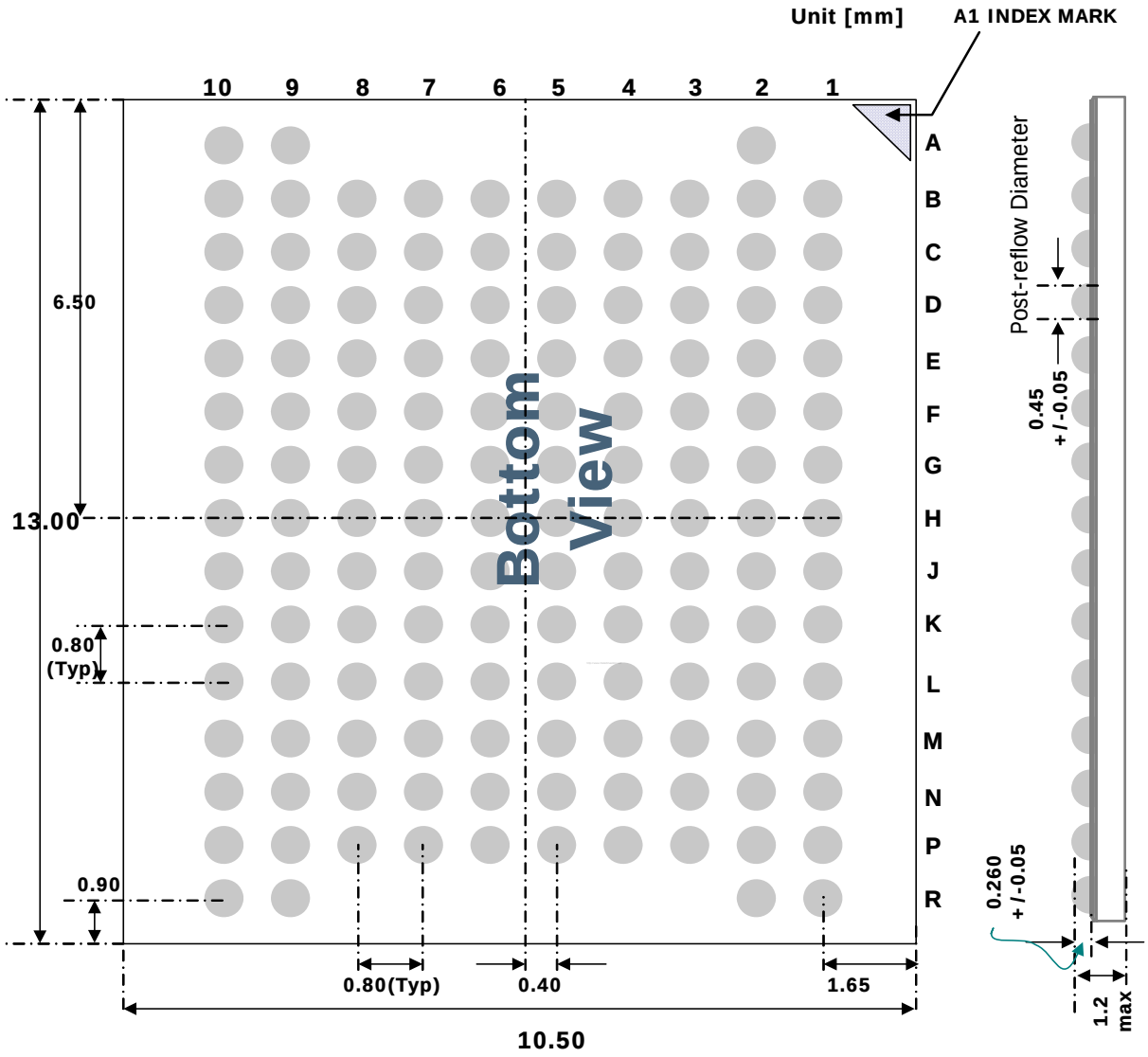
CK, $\overline{CK}$	Differential Clock Inputs
CKE0, CKE1	Clock Enable
$\overline{CS0}$, $\overline{CS1}$	Chip Select
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Command Inputs
BA0, BA1	Bank Address Inputs
A0 ~ A13	Address Inputs
DQ0 ~ DQ31	Data Bus
DQM0~DQM3	Input Data Mask
DQS0~DQS3	Data Strobe
VDD	Power Supply
VSS	Ground
VDDQ	I/O Power Supply
VSSQ	I/O Ground

< Common >

DNU	Do Not Use
NC	No Connection

PACKAGE INFORMATION

137 Ball 0.8mm pitch 10.5mm x 13.0mm (t=1.2mm) FBGA



4Gb (256Mb x16) NAND FLASH D-Die

1 Summary Description

The Hynix NAND Flash has a 256Mx16bit with spare 16Mx8 bit capacity.
The device is offered in 1.8 Vcc Power Supply, and with x16 I/O interface
Its NAND cell provides the most cost-effective solution for the solid state mass storage market.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 4096 blocks, composed by 64 pages.
Memory array is split into 2 planes, each of them consisting of 2048 blocks.
Like all other 2KB - page NAND Flash devices, a program operation allows to write the 2112-byte page in typical 250us and an erase operation can be performed in typical 3.5ms on a 128K-byte block.
In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane). As a consequence, multi-plane architecture allows program time to be reduced by 40% and erase time to be reduction by 50%. In case of multi-plane operation, there is small degradation at 1.8V application in terms of program/erase time.

The multiplane operations are supported both with traditional and ONFI 1.0 protocols.
Data in the page can be read out at and 45nsec cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

A WP# pin is available to provide hardware protection against program and erase operations.
The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal.
Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of Nand Flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.
In addition, device supports ONFI 1.0 specification.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation:1 bit error out of every 264-word (x16) can be detected. With this feature it is no longer necessary to use an external to detect copy back operation errors.
Multiplane copy back is also supported, both with traditional and ONFI 1.0 protocols. Data read out after copy back read (both for single and multiplane cases) is allowed.
In addition, Cache program and multi cache program operations improve the programing throughput by programing data using the cache register.

The devices provide two innovative features: page re-program and multiplane page re-program. The page re-program allows to re-program one page. Normally, this operation is performed after a previously failed page program operation. Similarly, the multiplane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multiplane page re-program operation is performed after a previously failed multiplane page program operation. The page re-program and multi-plane

page re-program guarantee imporve performance, since data insertion can be omitted during re-program operations, and save ram buffer at the host in the case of program failure.

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permantely.
- Serial number (unique identifier), which allows the devices to be nuniquely indentified.
- Read ID2 extention
- Non-volatile protection to lock sensible data permanently.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, no described in the data-sheet. For more details about them, contact your nearest Hynix sales office.

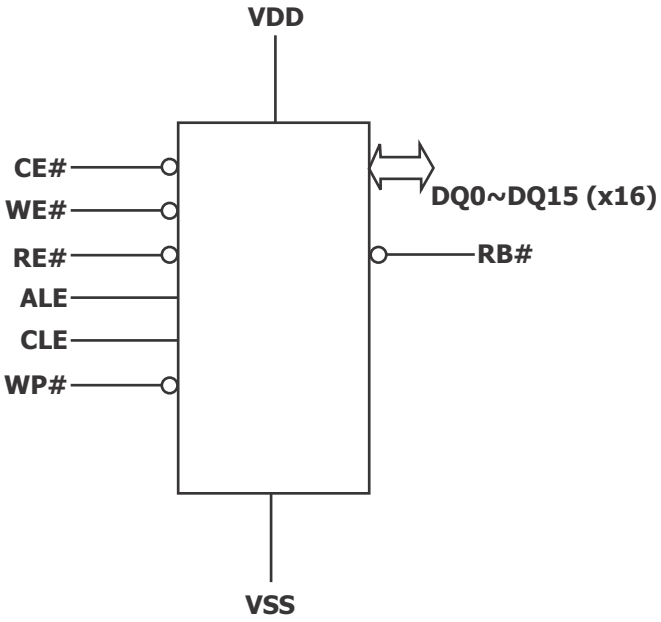


Figure 1: Logic Diagram

DQ15 - DQ0	Data Input / Outputs (x16)
CLE	Command latch enable
ALE	Address latch enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
RB#	Ready/ Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connected internally

Table 2: Signal Names

1.2 PIN DESCRIPTION

Pin Name	Description
DQ0 - DQ15	**DATA INPUTS/OUTPUTS** The DQ pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE#). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
CE#	**CHIP ENABLE** This input controls the selection of the device. When the device is busy CE# low does not deselect the memory.
WE#	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**WRITE PROTECT** The WP# pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
RB#	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	**SUPPLY VOLTAGE FOR IO BUFFER** The V_{CC} supplies the power for all the operations (Read, Write, Erase). An internal lock circuit prevent the insertion of Commands when V_{CC} is less than V_{LKO}
V_{SS}	**GROUND**
NC / DNU	**NO CONNECTED / DON'T USE**

Table 3: Pin Description

NOTE:

1. A 0.1uF capacitor should be connected between the V_{CC} Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

2. an internal voltage detector disables all functions whenever V_{CC} is below 1.1V (1.8V) version to protect the device from any involuntary program/erase during power transitions.

1.3 Functional block diagram

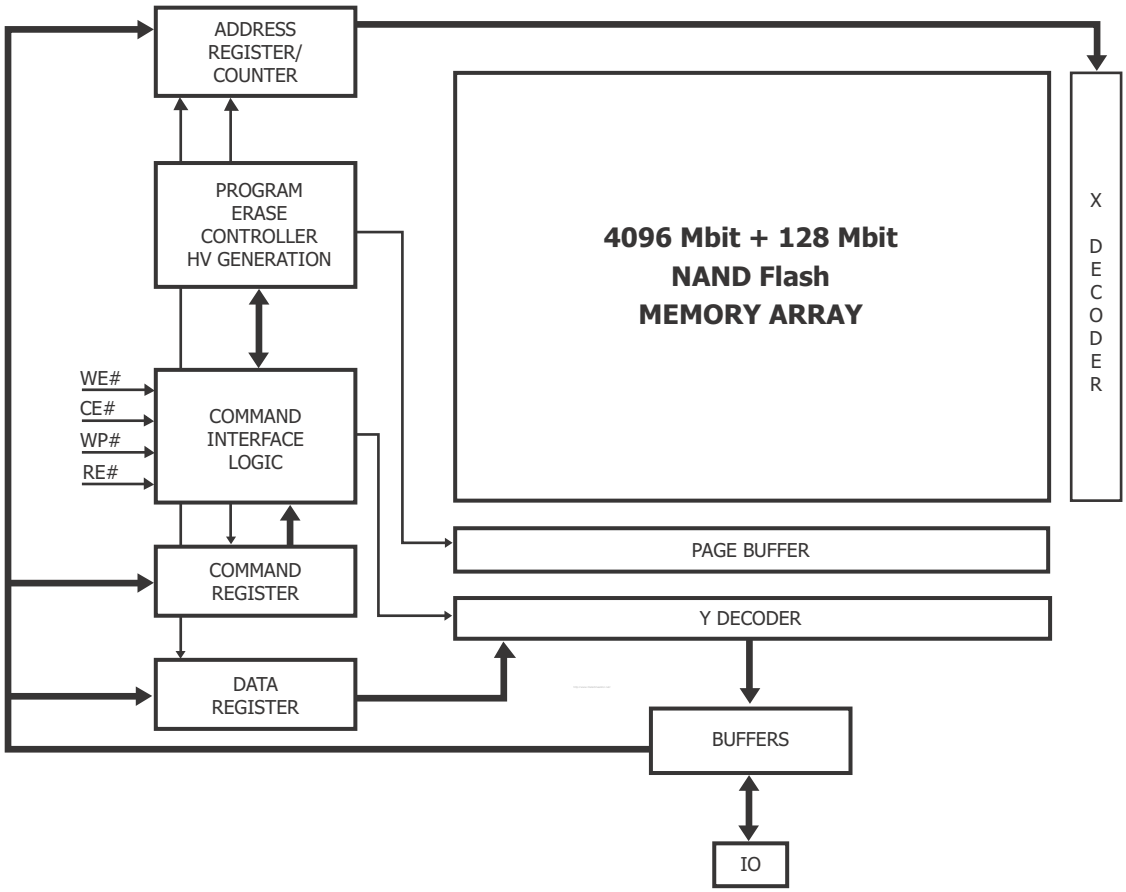


Figure 3: block description

1.4 Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	0	0	0	0	0
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th Cycle (*)	A27	A28	A29	A30	0	0	0	0

Table 5: Address Cycle Map (x16)

(*): A29 for 8Gbit DDP(1CE). A29:A30 for 16Gbit QDP(1CE)

As far as the address bits are concerned, the following rules apply:

A0 - A10 : column address in the page
A11 - A16 : page address in the block
A17 : plane address (for multi-plane operations) / block address (for normal operations)
A18 - A30 : block address

1.5 Command Set

Command(1)	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h			
READ FOR COPY-BACK	00h	35h			
SPECIAL READ FOR COPY BACK	00h	36h			
READ ID	90h				
READ ID2	30h-65h-00h	30h			
RESET	FFh				Yes(2)
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
CACHE PGM (Start) / (continue)	80h	15h			
PAGE REPROGRAM / Nth PAGE CACHE REPROGRAM (end)	8Bh	10h			
Nth PAGE CACHE REPROGRAM (continue)	8Bh	15h			
N-1th PAGE CACHE REPROGRAM (continue)	8Ah	15h			
COPY BACK PGM (start)	85h	10h			
(Traditional) MULTI PLANE PROGRAM(3)	80h	11h	81h	10h	
ONFI MULTIPLANE PROGRAM	**80h**	**11h**	**80h**	**10h**	
MULTIPLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	
(Traditional) MULTIPLANE CACHE PGM (start/cont)	80h	11h	81h	15h	
ONFI MULTIPLANE CACHE PGM (start/cont)	**80h**	**11h**	**80h**	**15h**	
(Traditional) MULTIPLANE CACHE PGM (end)(3)	80h	11h	81h	10h	
ONFI MULTIPLANE CACHE PGM (end)	**80h**	**11h**	**80h**	**10h**	
Nth PAGES MULTIPLANE CACHE RE-PROGRAM (cont)	8Bh	11h	8Bh	15h	
Nth PAGES MULTIPLANE CACHE RE-PROGRAM (end)	8Bh	11h	8Bh	10h	
N-1th PAGES MULTIPLANE CACHE RE-PROGRAM (cont)	8Ah	11h	8Ah	15h	
(Traditional) MULTI PLANE COPY BACK PROGRAM(3)	85h	11h	81h	10h	
ONFI MULTIPLANE COPYBACK PGM	**85h**	**11h**	**85h**	**10h**	
BLOCK ERASE	60h	D0h			
(Traditional) MULTI PLANE BLOCK ERASE(3)	60h	60h	D0h		
ONFI MULTIPLANE BLOCK ERASE	**60h**	**D1h**	**60h**	**D0h**	
READ STATUS REGISTER	70h				Yes
READ STATUS ENHANCED	**78h**				**Yes**
RANDOM DATA INPUT	85h				
RANDOM DATA OUTPUT	05h	E0h			
CACHE READ(SEQUENTIAL)	**31h**				
CACHE READ ENHANCED (RANDOM)	**00h**	**31h**			
CACHE READ END	**3Fh**				
READ PARAMETER PAGE	**Ech**				
EDC STATUS READ	7Bh				
EXTENDED READ STATUS	F2h/F3h/F4h/F5h				Yes

Table 6: Public Command Set

NOTE:

1. Commands listed in BOLD are referring to ONFI 1.0 Specification.
2. Only during cache ready busy.
3.Command maintained for backward compatibility

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Data Output (on going)	
X	X	L(1)	H	H	X	Data Output (suspended)(2)	
L	L	L	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / V_{CC}	Stand By	

Table7: Mode Selection

NOTES:

1. As 4Gbit SLC F41 is CE# don't care device, CE# high during latency time does not stop the read operation.

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. (see **Figure 1** and **Table 6**)
Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.Table 28

2.1. Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See **Figure 5** and **Table 28** for details of the timings requirements. Command codes are always applied on IO7:0 regardless of the bus configuration. (X16)

2.2. Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See **Figure 5** and **Table 28** for details of the timings requirements. Addresses are always applied on IO7:0 regardless of the bus configuration. (X16). Refer to **Table 4** and **Table 5** for more detailed information.

2.3. Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See **Figure 7** and **Table 28** for details of the timings requirements.

2.4. Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See **Figure 8** to **Figure 11** and **Table 28** for details of the timings requirements.

2.5. Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6. Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 1056 (x16) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45nsec (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.
Check Figure 12, Figure 13, Figure 14 as references.

3.2 Data handling retirctions during program sequences

Applications which use the error detection code in copy back must respect some restrictions related to data handling during program sequence.
The error dection code check is used during copy back program and multiplane copy back program operations to detect single bit errors pccurred in the source page (for details about EDC)

Note: The restrictions described below are not valid if the application uses the copy back program or multiplane copy back program without EDC check.

When data handling is performed, the page program, multiplane page program, page re-program, multiplane page re-program, cache ptrgram and multiplane cache program operations, must respect the following restrictions:
1. Program operations must be performed on the whole page, or on the whple EDC unit at a time.
2. For each program operation, random data input can be executed only once for each EDC unit.

Copy back program or multiplane copy back program opeations must respect the following restrictions:
1. If rando, data input is applied in a given EDC unit, the data of the whole EDC unit must be inserted. In ohter words, the EDC check is possible only if the whole EDC unit is modified during a copy back program sequence.
2. For each program operation, rando, data input can be executed only once for each EDC unit.

3.3 Page Program

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automat-

ically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 and Figure 15 detail the sequence.
The device is programmed basically by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 1056 (x16) in a single page program cycle.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 31. In addition, pages must be sequentially programmed within a block.
Users which use "EDC check" in copy back must comply with some limitations related to data handling during one page program sequence. Please refer to Section 3.10 for details.

3.4. Multiple plane program

Device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1^{st} page. Address for this page must be in the 1^{st} plane (A<18>=0). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1^{st} page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2^{nd} page address (5 cycles) and its serial data input. Address for this page must be in the 2^{nd} plane (A<18>=1). Program Confirm command (10h) makes parallel programming of both pages to start. **Figure 20** and **Figure 21** describe the sequences.

User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (t_{DBSY}).
In case of fail in any of 1^{st} and 2^{nd} page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to **section 3.11** for further info.

The number of consecutive **partial page programming operations** (NOP) within the same page must not exceed the number indicated in **Table 27.** In addition, it is recommended to program pages sequentially within a block.

3.5. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A29 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify.
Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 19 details the sequence.

3.6. Multiple plane Block Erase

Multiple plane erase, allows parallel erase of two blocks in parallel, one per each memory plane.
Two different command sequences are allowed in these case, traditional and ONFI 1.0.

In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start.

In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.
See **Figure 25** for details.

As an alternative, the ONFI 1.0 multiplane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multiplane confirm). Between the two block-related sequences, a short busy time t_{IEBSY} will occur. See **Table 27** and **Figure 26** for details.
Address limitation required for multiple plane program applies also to multiple plane erase. Also operation progress can be checked like in the multiple plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced.

As for multiplane page program, the address of the first second page must be within the first plane (A17=0 for x16 devices) and second plane (A18 = 1 for devices, A17=1 for x16 devices), respectively.

3.7. Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read (without mandatory serial access) and copy back -program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE# (see **Figure 17**), or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation.
Source and Destination page in the copy back program sequence must belong to the same device plane (x16 : same A17)
Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in **Figure 18.**
This device includes automatic Error Detection Code check during copy back operation, to detect single bit errors in EDC units occurred in the source page.
More details on EDC operation, and limitation related to data input handling during one copy back program sequence are available in **section 3.10**

3.8. Multiple plane copy back Program

As for page program, device supports Multi-plane copy back program with exactly same sequence and limitations. Multi plane copy back program must be preceded by 2 single page read for copy back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
EDC check is available also for multi-plane copy back program.
Users which use "EDC check" in copy back must comply with some limitations related to data handling during one multi-plane copy back program sequence. Please refer to **Section 3.10** for details.

Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in **Figure 22**, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in **Figure 23** and **Figure 24**.

3.9. Special read for copy back

The device feature the "special read for copy back".
If copy back read (described in **sections 3.7** and **3.8**) is triggered with confirm command "36h" instead "35h", copy back read from target page(s) will be executed with an increased internal (Vpass) voltage.
This special feature is used in order to try to recover incorrigible ECC read errors due to over-program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy back" sequences..

Excluding the copy-back read confirm command, all other features described in **sections 3.7** and **3.8** for standard copy back remain valid (including the figures referred to in those sections).

3.10. EDC operation

Error Detection Code check is a feature which be used during copy back program operation (both single and multi-plane) to detect single bit errors occurred in the source page (s).

- In the x16 version EDC allows detection of up to 1 single bit error every 264 words, where each 264 word group is composed by 256 words of main array and 8 words of spare area (see **Table 10** and **Table 11**). The described 264 word area is called "EDC unit".

EDC result can be checked through specific Read EDC register command, available only during copy back program and only for the device version supporting ECC=1. EDC register can be queried during the copy back program busy time t_{PROG}

For "EDC check" feature to operate correctly specific conditions on data input handling apply for page program and copy back program (single, cached, multi-plane):

For the case of page program

1) In section 3.2 it was explained that a number of consecutive partial program operations (NOP) is allowed within the same page. In case this feature is used, the number of partial program operations occurring in the same EDC unit must not exceed "one" (1). In other words, page program operations must be performed on the whole page, or on whole EDC unit at a time.

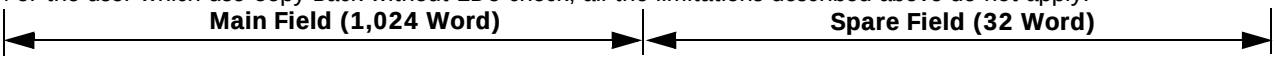
2) "random data input" in a given EDC unit can be executed several times during one page program sequence, but data insertion in each column address of each EDC unit must not exceed "one" (1).

For the case of copy back program

1) If random data input is applied in a given EDC unit, the data of the whole EDC unit must be inserted. In other words, the EDC check is possible only if the whole EDC unit is modified during one copy back program sequence

2) "random data input" in a given EDC unit can be executed several times during one copy back sequence , but data insertion in each column address of the EDC unit must not exceed "one" (1)

For the user which use Copy Back without EDC check, all the limitations described above do not apply.



"A"area (1st sector)	"B"area (2nd sector)	"C"area (3rd sector)	"D"area (4th sector)	"E"area (1st sector)	"F"area (2nd sector)	"G"area (3rd sector)	"H"area (4th sector)
256 words	256 words	256 words	256 words	8 words	8 words	8 words	8 words

Table 10: page organization in EDC units (x16)

Sector	Main Field (Column 0~1023)		Spare Field (Column 1024~1055)	
	Area Name	Column Address	Area Name	Column Address
1st 264-word Sector	"A"	0~255	"E"	1024~1031
2nd 264-word Sector	"B"	256~511	"F"	1032~1039
3rd 264-word Sector	"C"	512~767	"G"	1040~1047
4th 264-word Sector	"D"	768~1023	"H"	1048~1055

Table 11: page organization in EDC units (x16)

3.10 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to **Table 13** for specific Status Register definition, and to **Figure 9** and **Figure 36** for timings. The command register remains in Status Read mode until further commands are issued. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.11 Read Status Register.

The device contains a Status Register to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. Refer to **Table 12** for specific Status Register definition, and to **Figure 10** and **Figure 38** for timings.

If Read Status register command is issued during multi-plane operations Read Status Register polling shall return the combined status value related to the outcome of the operation in the two planes according to this table:

Status Register bit	Composite status value
Bit 0, Pass/Fail	OR
Bit 1, Cache Pass/Fail	OR

Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

The command register remains in Status Read mode until further commands are issued. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Note:
Read Status Register command shall not be used for concurrent operations in of multi-dice stack configurations (single CE#). For this case, either "Read Status Enhanced" (**Section 3.12**) shall be used instead.

3.12 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases:

- on a specific die of a multi-dice stack configurations (single CE#), in case of concurrent operations

When 4Gbit dice are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single CE#), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.)

- on a specific plane in case of multi-plane operations in the same die.

Figure 39 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.

Refer to **Table 12** for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

3.13 Read Status Register field definition

Table 12 below lists the meaning of each bit of Read Status Register and Read Status Enhanced

IO	Page Program / Page Reprogram	Block Erase	Read	Cache Read	Cache Program / Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail	N Page Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass / Fail	N - Page Pass: '0' Fail: '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Active: '0' Idle: '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data cache Read/Busy Busy: '0' Ready: '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 12: Status Register Coding

3.14 Read EDC status register

This operation is available only in copy back program and it allows the detection of errors occurred during read for copy back. In case of multiple plane copy back, it is not possible to know which of the two read operation caused the error. After writing Read EDC status register command (7Bh) to the command register, a read cycle outputs the content of the EDC Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last.
Operation is same as read status register command. Refer to **Table 13** for specific EDC Register definitions:

IO	Copy back program	CODING
0	Pass / Fail	Pass: '0' Fail: '1'
1	EDC status	No error: '0' Error: '1'
2	EDC validity	Invalid: '0' Valid: '1'
3	NA	-
4	NA	-
5	Ready / Busy	Busy: '0' Ready: '1'
6	Ready / Busy	Busy: '0' Ready: '1'
7	Write Protect	Protected: '0' Not Protected: '1'

Table 13: EDC register coding

3.15 Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to **table 16** for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written. Refer to **Figure 28** for further details.

3.16 Cache Read

Cache Read can be used to increase the read operation speed, as defined in **Section 3.1**, which is available only within a block. As soon as the user starts to read one page, the device automatically lpads the next page into the cache register. Serial data output may be executed while data in the memory is read into cache register, Cache Read is initiated by the page read sequence (00-30h) on a page M.
After random access to the first page is complete (R/B# returned to high, or read status register IO<6> switches to high), two command sequences can be used to continue read cache:

- sequential read cache continue (command "31h" only): once the command is latched into the command register (see **Figure 30**), device does busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register At the end of this phase cache register data can be output by toggling RE# while the "next "page (page address M+1) is read from the memory array into data register.

- random read cache continue (sequence "00h" <page N address> "31"): once the command is latched into the command register (**see Figure 31**), device does busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register At the end of this phase cache register data can be output by toggling RE# while page N is read from the memory array into data register.

Subsequent pages are read by issuing additional "sequential" or "random" read cache continue command sequences.
If serial data output time of one page exceeds random access time (t_R), the random access time of the next page is hidden by data downloading of the previous page.
On the other hand, if 31h is issued prior to complete the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.
To terminate cache read, 3Fh command should be issued (see **Figure 32**). This command transfer data from data register
to the cache register without issuing next page read.
During the Cache Read Operation, device doesn't allow any other command except for 31h, 3Fh, Read SR or reset (FFh).
To carry out other operations Cache read must be ended either by 3Fh command or device must be reset by issuing FFh.

Read Status command (70h) may be issued to check the status of the different registers, and the busy/ready status of the cached read operations. More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to output new data.
b) the status bit I/O<5> can be used to determine when the cell reading of the current data register contents is complete.

Note:
31h and 3Fh commands reset the column counter thus when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random data output command can be used to switch column address.

3.17 Cache Program

Cache Program is used to improve the program throughput by programing data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transffered to the page buffer is programmed into the memory array.
Cache program is available only within a block

After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is conse quently processed through a pipeline model.
In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCBSYW).
Read Status commands (70h or 78h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete.
c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while program ming page N. The latter can be polled upon I/O<5> status bit changing to "1".

I/O<1> may be read together with I/O<0>.
If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

See **Table 12** and **Figure 40** for more details.

3.18 Multi-plane Cache Program

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.
The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows:
a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1^{st} page. Ad dress for this page must be within 1^{st} plane (A<20>=0). The data of 1^{st} page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b) The Dummy Page Program Confirm command (11h) stops 1^{st} page data input and the device becomes busy for a short time (t_{DBSY}).
c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2^{nd} page address (5 cycles) and its serial data input. Address for this page must be within 2^{nd} plane (A<20>=1). The data of 2^{nd} page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the

data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command se quence.

The sequence 80h-...- 11h...-...81h...-...15h (or the corresponding ONFI 80h-...- 11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

The sequence to end multi-plane cache program is 80h-...- 11h...-...81h...-...10h (or 80h-...- 11h...-...80h...-...10h for the ONFI 1.0 case).
Figure 50 and Figure 51 show the command sequence for the multi plane cache program operation for the two protocols. Multi-plane Cache program is available only within two paired blocks belonging to the two planes..

User can check operation status by R/B# pin or read status register commands (70h or 78h)
If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:
a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

See **Table 12** for more details

If the system monitor rs the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the sta tus bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.
Refer to **section 3.11** for further information.

3.19 Page Re-Program.

The device support an innovative page re-program operation that allows to re-program a page, after a previously failed page program operation. Compared to a standard page progra, operation, the re-program feature imporves performance, since data insertion can be omitted during re-program operations, an daves rambuffer at the host.

This command allows the re-programming of the same pattern of the last (failed) page into another memory location of the same plane as the failed page
The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle (as described in **Figure 43**). On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm"10h"(as described in **Figure44**)
The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The "program confirm" command (10h) initiates the re-programming process.
The internal write state controller automatically executes the algorithms and controls timings necessary for program and-verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Users which use "EDC check" in copy back must comply with some limitations related to data handling during one page reprogram sequence . Please refer to **Section 3.10** for details.

3.20 Multi-plane Page Re-Program.

Device supports multiple plane re-program: in other words, it is possible to re-program on different device locations 2 pages in parallel, one per each plane, (one of or both of) which had previously failed multi-plane program.

A multiple plane re-program cycle consists of re-program setup command (8Bh), followed by the five cycle address inputs. Address for this page must be in the 1st plane.
Serial data for the 1st page is allowed (as indicated in **Figure 45**) if the pattern bound for the target page is different from that of the previous page, otherwise it can be omitted (as indicated in **Figure 46**). If data insertion in the page is performed, random data input command (85h) can be executed multiple times.
The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, another reprogram command "8Bh" must be issued, followed by 2nd page address (5 cycles). Address for this page must be in the 2nd plane .
Again, serial data for the 2nd page can be input if the pattern bound for the target page is different from that of the previous page, otherwise it can be omitted. If data insertion in the page is performed, random data input command (85h) can be executed multiple times.
Program Confirm command (10h) makes parallel programming of both pages to start. **Figure 20** and **Figure 21** describe the sequences.

User can check operation status by monitoring RB# pin or reading status register command, as if it were a normal page program: read status register command is also available during Dummy Busy time (t_{DBSY}).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued. Refer to **section 3.11** for further info.

Page reprogram cannot cross plane boundaries (A18): in other words if reprogram of one page belonging to the first plane is executed, the data of the latter can be programmed only on other page of the same memory plane.

Users which use "EDC check" in copy back must comply with some limitations related to data handling during one multi-plane page program sequence. Please refer to **Section 3.10** for details.

The multiplane page re-program operation can not go byeyond plane boundaries. For example, if a re-program operation of a page bleonging to th first plane (A17=0 for x16 devices) is executed, the data already inserted can be programmed only on another page of the dame memory plane (A17=0 for x16 devices)

3.21 Cached Re-Program

In **section 3.17** the feature of cache program was explained. In that section, it was also highlighted that cache program may result in a fail either in the last cached page (N^{th}), or in the previous one ($N-1^{th}$), both of which can be detected by reading the Status Register.
In this event, the 4Gbit F41 SLC implements the innovative (optional) feature of "page re-program".
This allows the re-programming of the same pattern of either the (failed) N^{th} page or of the $N-1^{th}$ page into another memory location of the same plane as the failed pages.

1) for the case of the N^{th} page re-program, the command sequence consists of re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, either the "cache program confirm" (15h) or "program confirm" command (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before either the "cache program confirm" (15h) or "program confirm" command (10h) For the case of the N^{th} page re-program, the device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
Figure 47 and **Figure 48** show two scenarios related to N^{th} page cache re-program.

2) for the case of the $N-1^{th}$ page re-program, the command sequence consists of re-program setup(8Ah), followed by the five cycle address inputs of the target page, and the the "cache program confirm" (15h)
In this case, data in is not allowed. In addition, if cache re-program sequence is issued for page $N-1^{th}$, cache re-program for page N^{th} must be inserted too.
Figure 49 and **Figure 50** show two scenarios related to N^{th} page cache re-program.

Either the "cache program confirm" (15h) or "program confirm" command (10h) can be issued to trigger the re-programming process.

The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. the "cache program confirm" (15h) or "program confirm" command (10h) are issued, the Read Status Register 70h or Read Status enhanced 78h commands may be inserted to monitor the outcome of the process.
The role and meaning of the Status register bits is explained in **Table 12** and in **section 3.17**. Alternatively, the system controller can detect the completion of a program cycle by monitoring the RB# output.

NOTES:
1) Cache reprogram is an optional feature which is activated with appropriate cam configuration.
2) Users which use "EDC check" in copy back must comply with some limitations related to data handling during cache program sequence. Please refer to **Section 3.10** for details.

3.22 Multi-plane Cached Re-Program

The multi-plane cached re-program is an extension of cached reprogram described in **Section 3.21**
This allows the re-programming of the same pattern of either the latest (failed) N^{th} pages or of the $N-1^{th}$ pages of the multi-plane cache sequence into other memory locations.

1) for the case of the N^{th} page re-program, the command sequence consists of re-program setup (8Bh), followed by the five cycle address inputs. Address for this page must be in the 1^{st} plane.
Serial data for the 1^{st} page is allowed if the pattern bound for the target page is different from that of the previous page, otherwise it can be omitted. If data insertion in the page is performed, random data input command (85h) can be executed multiple times.

The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, another reprogram command "8Bh" must be issued, followed by 2nd page address (5 cycles). Address for this page must be in the 2nd plane.

Again, serial data for the 2nd page can be input if the pattern bound for the target page is different from that of the previous page, otherwise it can be omitted. At the end of this phase, either the "cache program confirm" (15h) or "program confirm" command (10h) can be issued.

If data insertion in the page is performed, random data input command (85h) can be executed multiple times.

Figure 51 to **Figure 52** show two scenarios related to Nth pages multi-plane cache re-program.

2) for the case of the N-1th pages re-program, the command sequence consists of re-program setup (8Ah), followed by the five cycle address inputs. Address for this page must be in the 1st plane.
Serial data for the 1st page is not allowed.
The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, another reprogram command "8Ah" must be issued, followed by 2nd page address (5 cycles). Address for this page must be in the 2nd plane.
At the end of this phase, either the "cache program confirm" (15h) must be issued.
In addition, if cache re-program sequence is issued for pages N-1th, cache re-program for pages Nth must be inserted too.

Figure 53 and **Figure 54** show two scenarios related to N-1th page cache re-program.

Either the "cache program confirm" (15h) or "program confirm" command (10h) can be issued to trigger the re-programming process.

The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. the "cache program confirm" (15h) or "program confirm" command (10h) are issued, the Read Status Register 70h or Read Status enhanced 78h commands may be inserted to monitor the outcome of the process .
The role and meaning of the Status register bits is explained in Table 13 and in section 3.21. Alternatively, the system controller can detect the completion of a program cycle by monitoring the RB# output.

Page reprogram cannot cross plane boundaries (A18): in other words if reprogram of one page belonging to the first plane is executed, the data of the latter can be programmed only on other page of the same memory plane.

The multiplane page re-program operation can not go byeyond plane boundaries. For example, if a re-program operation of a page bleonging to th first plane (A17=0 for x16 devices) is executed, the data already inserted can be programmed only on another page of the dame memory plane (A17=0 for x16 devices)

note:
1) Multi-plane Cached reprogram is an optional feature which is activated with appropriate cam configuration.

2) Users which use "EDC check" in copy back must comply with some limitations related to data handling during multi-plane program sequence. Please refer to **Section 3.10** for details.

3.23 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Two different Read ID configuration are supported: the "legacy" 5-byte, and the "advanced" 6-byte versions.
The device operating mode (5-byte or 6 byte) is selected through cam setting.

3.23.1 Legacy Read ID

Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. **Figure 27** shows the operation sequence, while **Table 14** to **Table 18** explain the byte meaning. Complete read id code table is as follows.

DENSITY	ORG	VCC	1st	2nd	3rd	4th (1)	5th
4 Gbit	X16	1.8V	ADh	BCh	90h	55h	54h
8 Gbit DDP	X16	1.8V	ADh	B3h	D1h	55h	58h
16 Gbit QDP	X16	1.8V	ADh	B5h	D2h	55h	5Ch

Table 14: Legacy " Read ID for supported configurations

NOTE: for 1.8V version, IO<7,3>=00 would mean "50nsec", while device serial cycle time is 45nsec

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 15: "Legacy" Read ID bytes meaning

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

Table 16: Legacy Read ID 3rd byte description

4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Redundant Area Size (byte/512byte)	8 16					0 1	
Organization	X16		1				
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

Table 17: Legacy Read ID 4th byte description

5th ID Data

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1	I/O0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Reserved		0			0	0

Table 18: Legacy Read ID 5th byte description

3.24 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. **Figure 28** shows the operation sequence

3.25 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. **Figure 37** defines the Read Parameter Page behavior.
This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at leat five times.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

3.26 Parameter Page Data Structure Definition

Table21 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 **section 5.4.1**

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache ntegrit 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page

111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0,
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	ntegrita CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Table 21: Parameter page data

NOTE: "O" stands for Optional, "M" for Mandatory

4. OTHER FEATURES

4.1 Data Protection and Power on / off sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.8V (3V version), or 1.1V (1.8V version).

The power-up and power-down sequence is shown in **Figure 33** in this case V_{CC} and V_{CCQ} on the one hand (and VSS and V_{SSQ} on the other hand) are shorted together at all times

The Ready/Busy signal shall be valid within 100us since the power supplies have reached the minimum values (as specified on), and shall return to one within 5msec (max).
During this busy time, the device executes the initialization process (cam reading), and dissipates a current ICC0 (30mA max) in addition, it disregards all command excluding Read Status Register (70h).
At the end of this busy time, the device deaults into "read setup", thus if user decides to issue page read command, the 00h command may be skipped.

WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 100usec is required before internal circuit gets ready for any command sequences as shown in **Figure 33**. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copyback, random read completion. The RB# pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more RB# outputs to be Or-tied. Because pull-up resistor value is related to tr(RB#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (**refer to Figure 34**). Its value can be determined by the following guidance.

4.3 Write protect (#WP) handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec.
Switching WP# low during this time is equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.
The R/B# pin will stay low for t_{RST} (similarly to **Figure 29**). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value.
Refer to **Table 12** for more information on device status.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the set-up commands (80h or 60h).

The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in F**igure 35** and **Figure 36**.

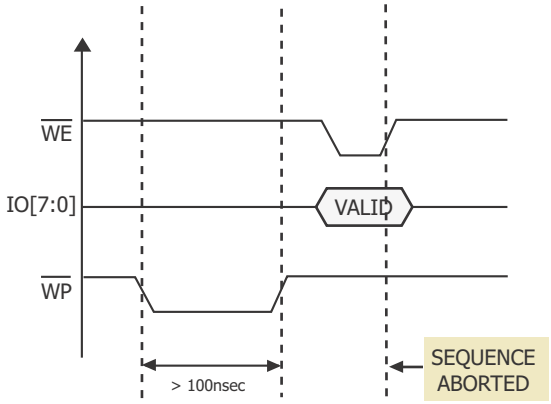


Figure 4: WP# low timing requirements during program/erase command sequence

5. Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Numbe, 4Gb	N_{VB}	4016	-	4096	Blocks

Table 22: Valid Blocks Number

(*) Each 4Gb has maximum 80 bad blocks
NOTE: The 1st block is quranteed to be a valid blick at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature(Mobile Temperature Range)	-30 to 85	°C
T_{BIAS}	Temperature Under Bias	-50 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{IO}(2)	Input or Output Voltage	-0.6 to 2.7	V
V_{CC}	Supply Voltage	-0.6 to 2.7	V

Table 23: Absolute maximum ratings

NOTES:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Expo sure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMi croelectronics SURE Program and other relevant quality documents.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

Parameter		Symbol	Test Conditions	1.8Volt			Unit
				Min	Typ	Max	
Power on current		I_{CC0}	Power up Current (Refer to 4.41)	-	15	30	mA
Operating Current	Sequential Read	I_{CC1}	t_{RC} = **see table 28** CE#=v_{IL}, I_{out}=0MA	-	10	20	mA
	Program	I_{CC2}	Norma	-	-	20	mA
			Cache	-	-	30	mA
	Erase	I_{CC3}	-	-	10	20	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/Vcc	-	-	1	mA
Stand-By Current (CMOS)		I_{CC5}	CE#=Vcc-0.2, WP#=0/Vcc	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	uA
Input High Voltage		V_{IH}	-	Vcc *0.8	-	Vcc +0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	Vcc- *0.2	V
Output High Voltage Level		V_{OH}	I_{OH}= -100uA	Vcc- 0.1	-	-	V
			I_{OH}= -400uA	-	-	-	V
Output Low Voltage Level		V_{OL}	I_{OH}= -100uA	-	-	0.1	V
			I_{OL}= 2.1mA	-	-	-	V
Output Low Current (RB#)		I_{OL}(RB#)	V_{OL}= 0.1V	3	-	4	mA
			V_{OL}= 0.4V	-	-	-	mA

Table 24: DC and Operating Characteristics

NOTES:

1) all V_{CCQ} and VCC pins, and VSS and VSSQ pins respectively are shorted together
2) Values listed in this table refer to the complete voltage range for V_{CC} and V_{CCQ} and to a single device in case of device stacking
3) All current measurement are performed with a 0.1uF capacitor connected between the Vcc Supply Voltage pin and the Vss Ground pin.
4) Standby current measurement can be performed after the device has completed the initialization process at power up. Refer to **Section 4.1**for more details

Parameter	Value
	1.8Volt
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc / 2
Output Load (1.7V - 1.95Volt)	1 TTL GATE and CL=30(1.8V)

Table 25: AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	V_{IL}= 0V	-	10	pF
Input Capacitance (1)	C_{IN}	V_{IN}= 0V	-	10	pF

Table 26: Pin Capacitance (TA = 25C, f=1.0MHz)

NOTE: For the stacked devices version the Input Capacitance is **10pF x (number of stacked chips)** and the I/O ca pacitance is **10pF x (number of stacked chips)**

Parameter		Symbol	Min	Typ	Max	Unit
Program Time/ Multi-plane program Time (1.8V)		t_{PROG}	-	250	700	us
Dummy Busy Time for Two Plane Program		t_{DBSY}	-	0.5	1	us
Cache program short busy time		t_{CBSYW}	-	5	t_{PROG}	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	4	Cycle
Block Erase Time/ Multi-plane Block Erase Time (1.8V)		t_{BERS}	-	3.5	10	ms
Read Cache busy time		tCBSYR	-	3	tR	us
Multi-plane erase short busy time (ONFI protocol only)		t_{IEBSY}	-	0.5	1	us

Table 27: Program / Erase Characteristics

NOTE: Typical program time is defined as the time within which more than 50% of the whole pages are programmed (Vcc=1.8V, and 25*C)

Parameter	Symbol	1.8 Volt		Unit
		Min	Max	
CLE Setup time	t_{CLS}	25		ns
CLE Hold time	t_{CLH}	10		ns
CE# Setup time	t_{CS}	35		ns
CE# Hold time	t_{CH}	10		ns
WE# Pulse width	t_{WP}	25		ns
ALE Setup time	t_{ALS}	25		ns
ALE Hold time	t_{ALH}	10		ns
Data Setup time	t_{DS}	20		ns
Data Hold time	t_{DH}	10		ns
Write Cycle time	t_{WC}	45		ns
WE# High Hold time	t_{WH}	15		ns
Address to Data Loading time	t_{ADL}	100		ns
Data Transfer from Cell to Register	t_{R}		25	us
ALE to RE# Delay	t_{AR}	10		ns
CLE to RE# Delay	t_{CLR}	10		ns
Ready to RE# Low	t_{RR}	20		ns
RE# Pulse Width	t_{RP}	25		ns
WE# High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	45		ns
RE# Access Time	t_{REA}		30	ns
CE# Low to RE# Low	t_{CR}	10		ns
RE# High to Output Hi-Z	t_{RHZ}		100	ns
CE# High to Output Hi-Z	t_{CHZ}		30	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10		ns
RE# High to Output Hold	t_{RHOH}	15		ns
RE# Low to Output Hold	t_{RLOH}	-		ns
CE# High to Output Hold	t_{COH}	15		ns
RE# High Hold Time	t_{REH}	15		ns
Output Hi-Z to RE# Low	t_{IR}	0		ns
RE# High to WE# Low	t_{RHW}	100		ns
WE# High to RE# Low	t_{WHR}	60		ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(2)	ns
Write protection time	t_{WW}	100		ns

Table 28: AC Timing Characteristics

NOTES: 1. The time to Ready depends on the value of the pull-up resistor tied to RB# pin

6. Timing Diagrams

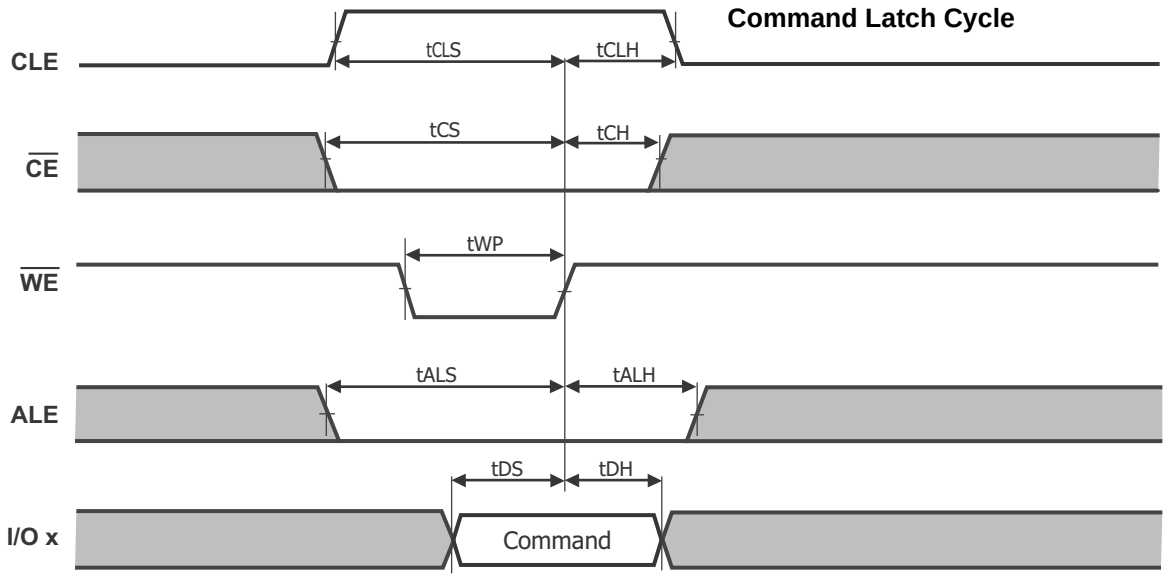
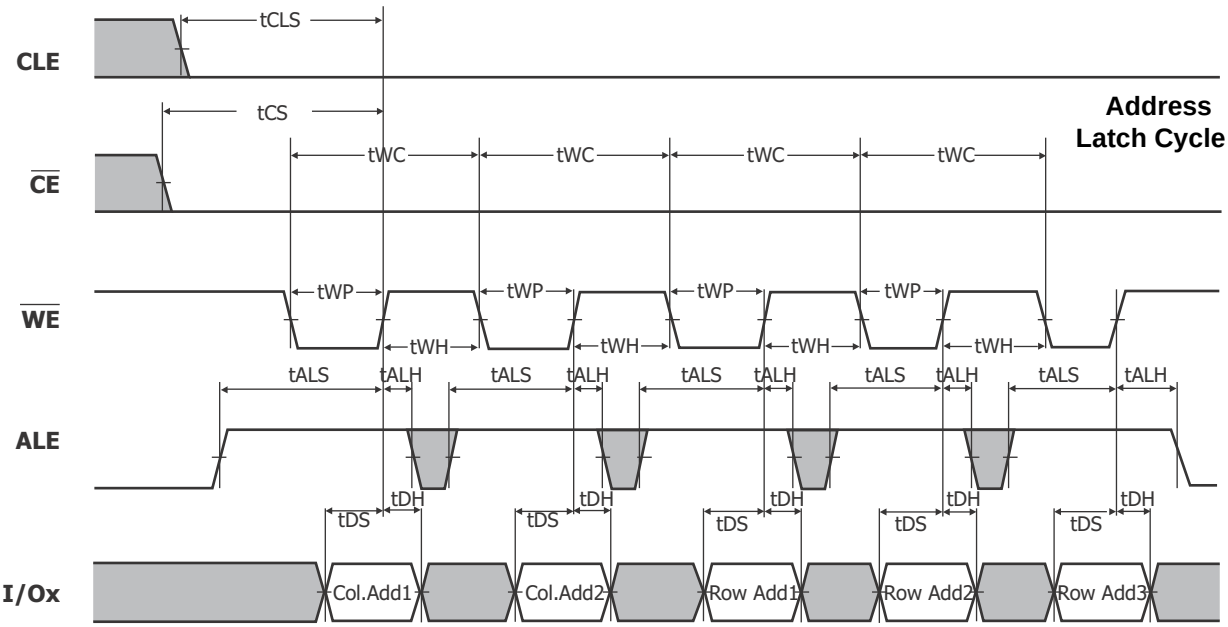


Figure 5: Command Latch Cycle



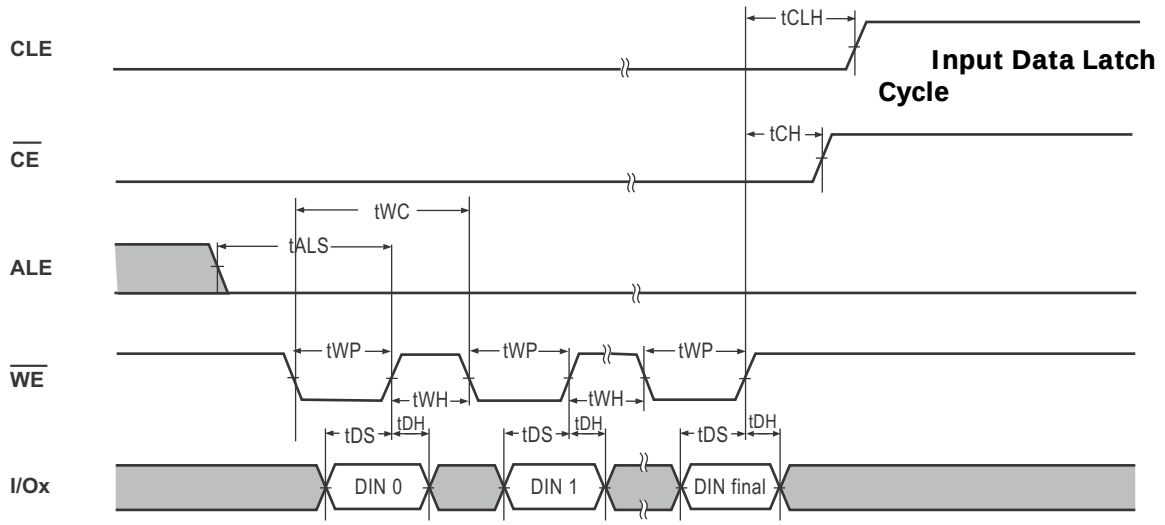
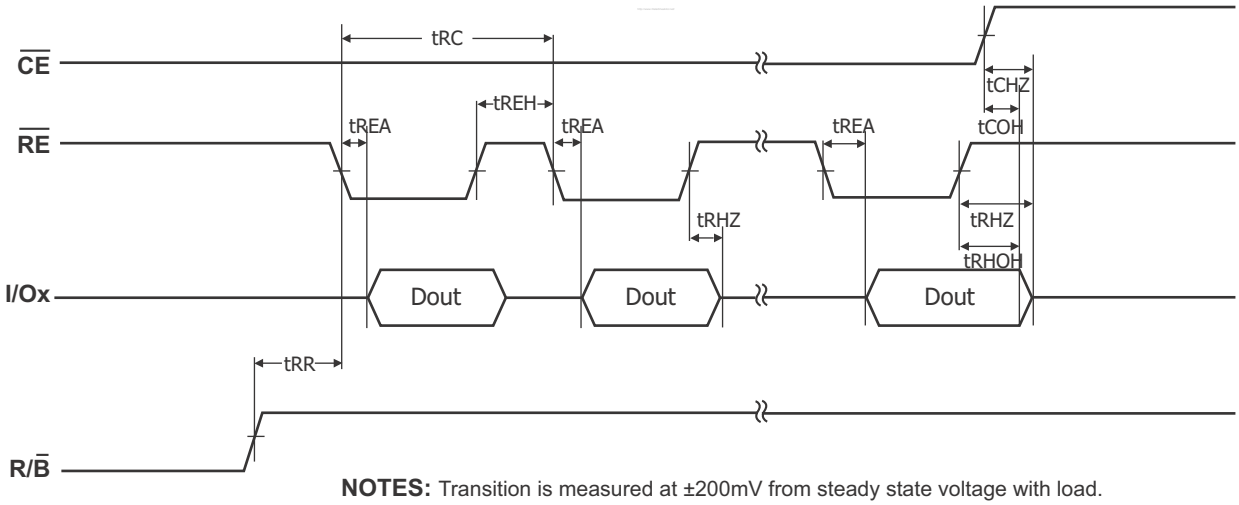


Figure 7: Input Data Latch Cycle

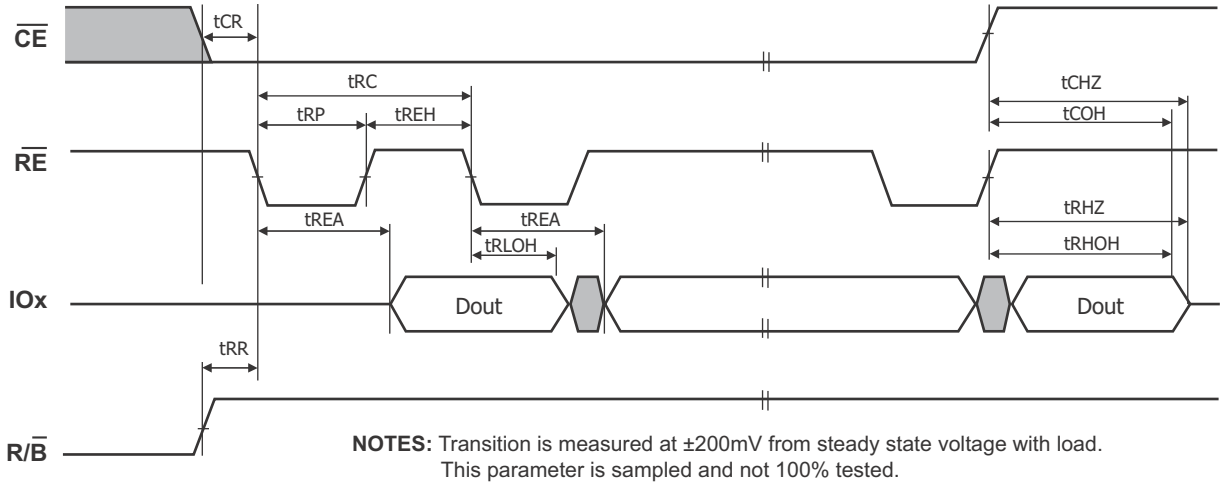
* Serial Access Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



NOTES: Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read

Serial Access Cycle after Read (EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)



NOTES: Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read

Status Read Cycle & EDC Status Read Cycle

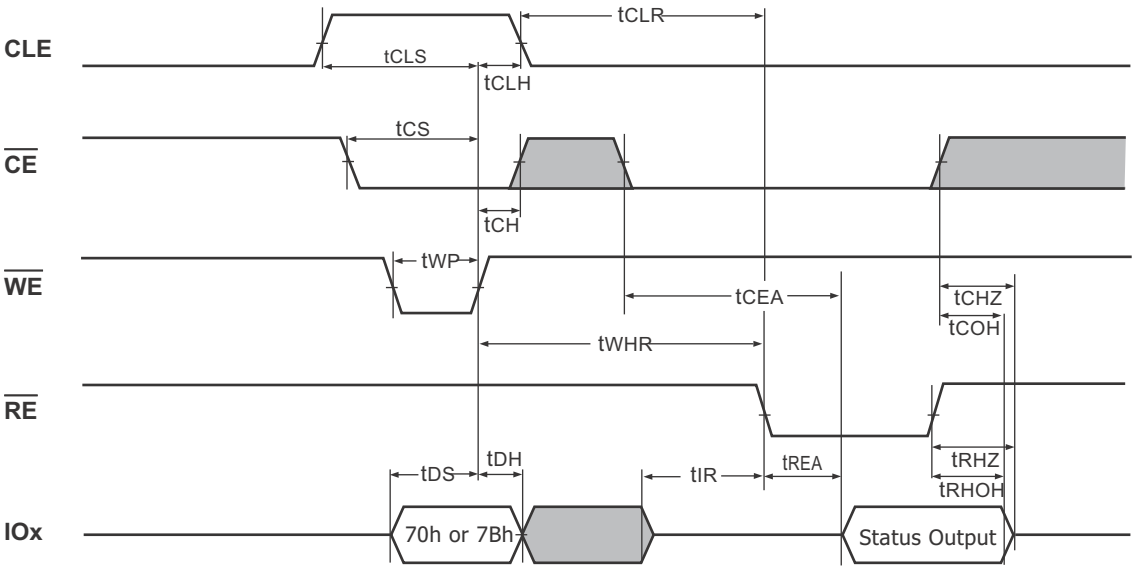


Figure 10: Status / EDC Read Cycle

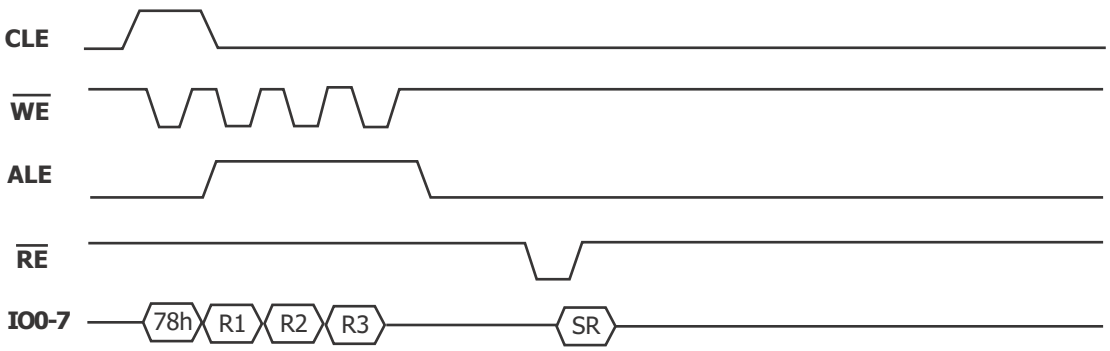
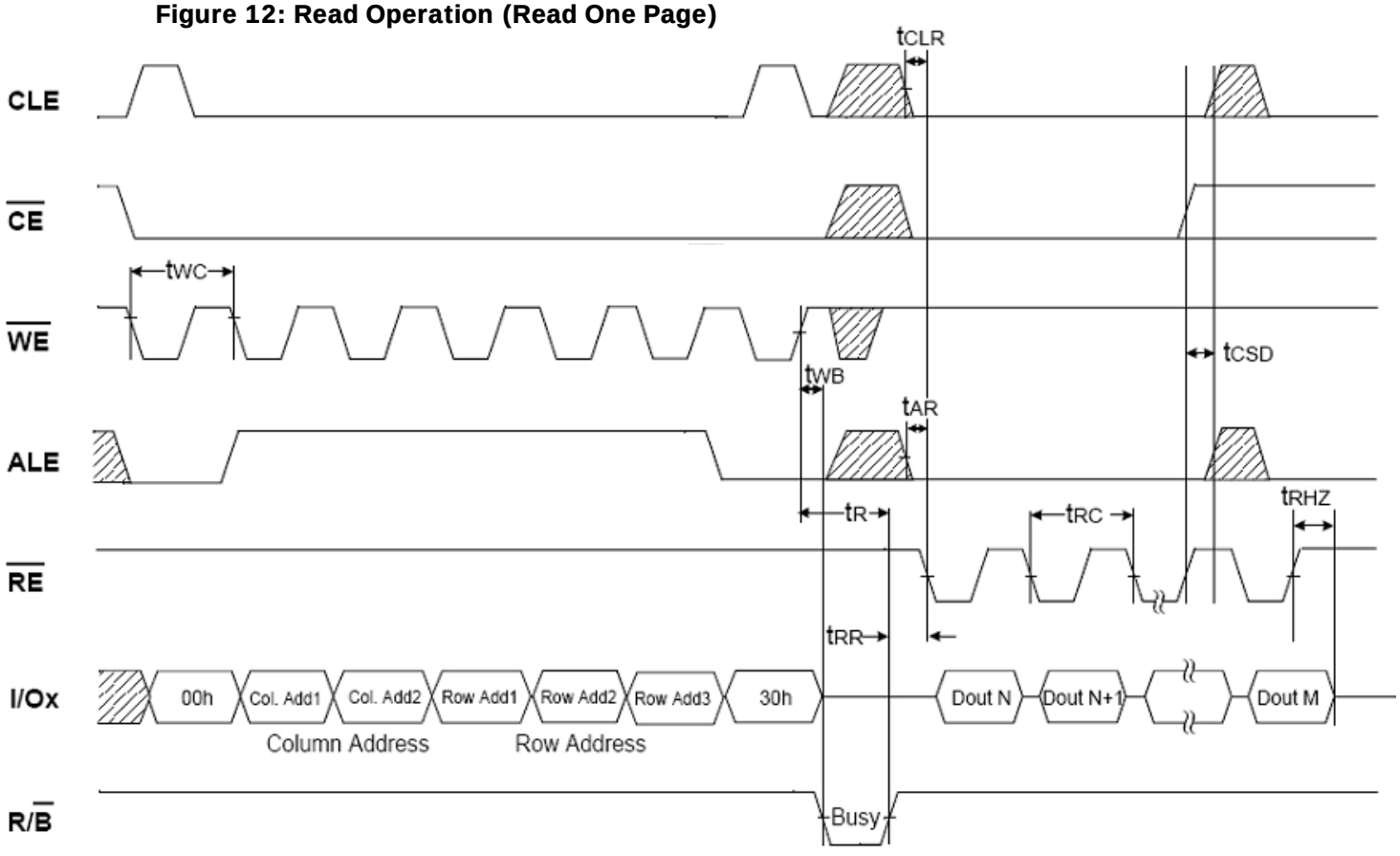


Figure 11: Read Status Enhanced cycle

Read Operation

Figure 12: Read Operation (Read One Page)



Read Operation (Intercepted by $\overline{CE}$)

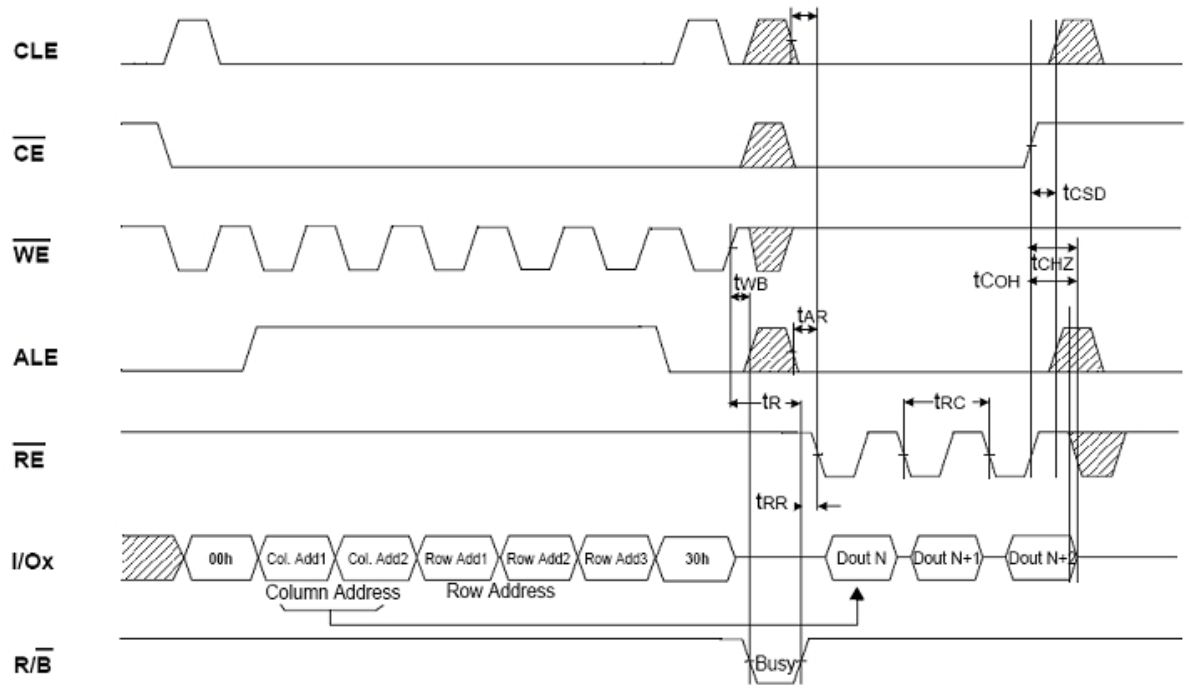


Figure 13: Read Operation intercepted by CE#

Random Data Output In a Page

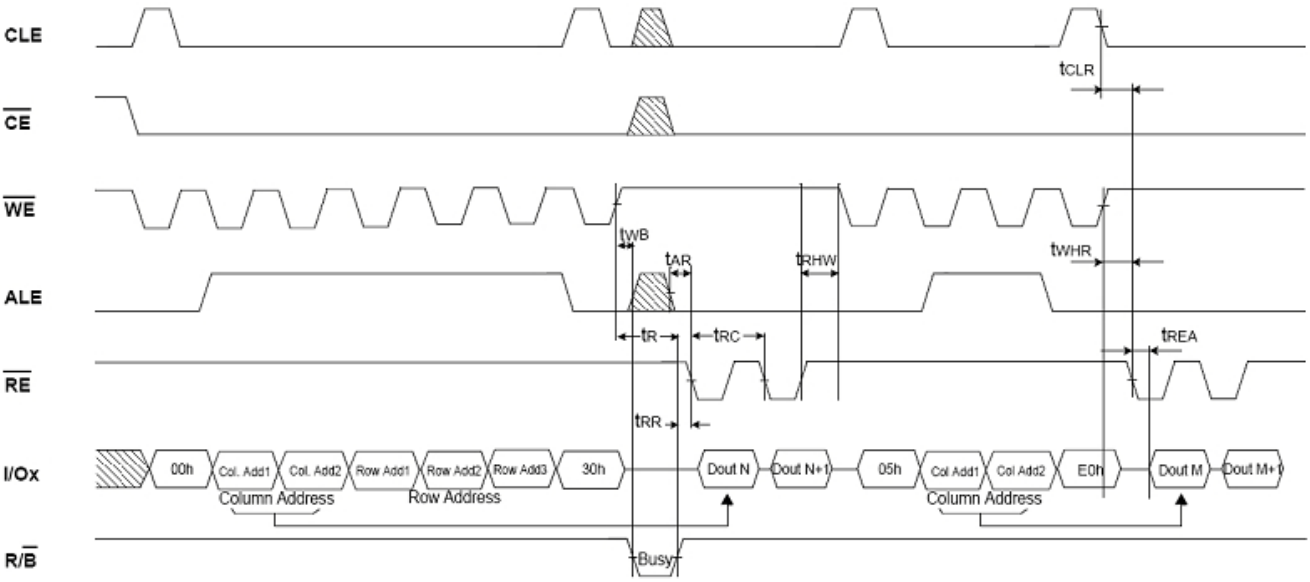
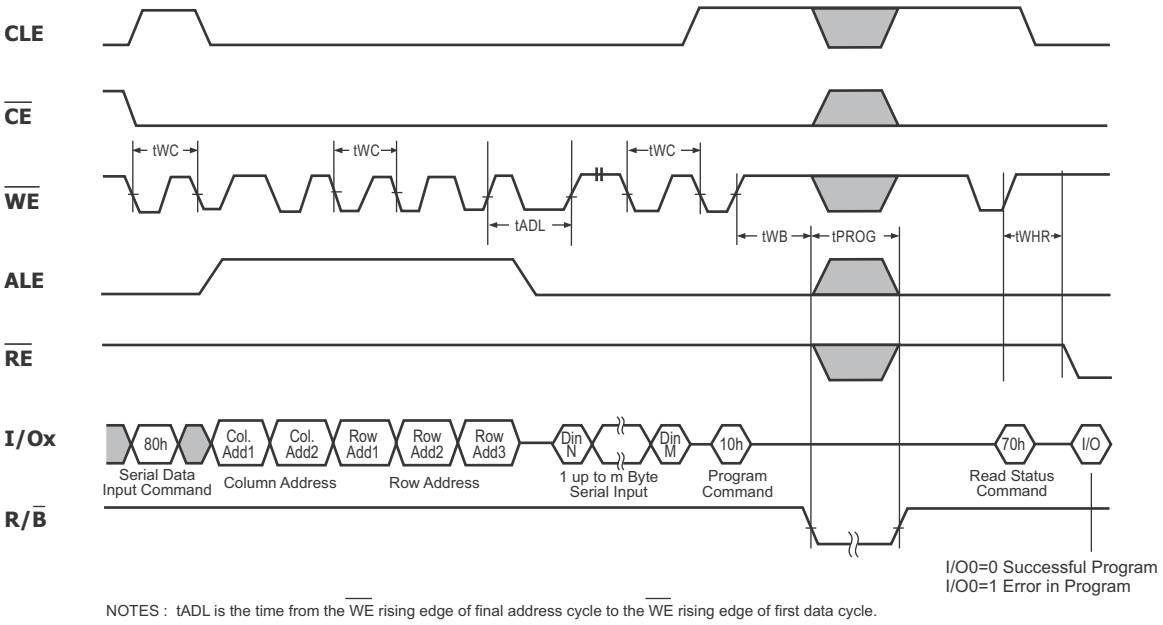


Figure 14: Random Data Output

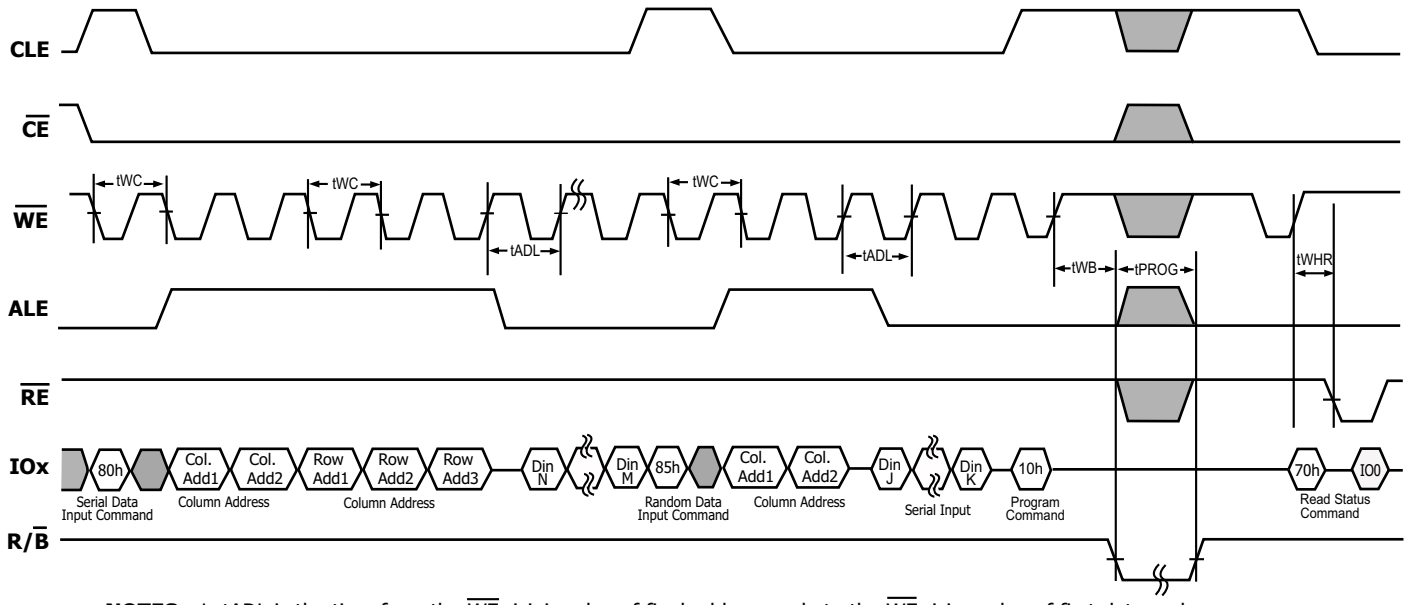
Page Program Operation



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 15: Page Program Operation

Page Program Operation with Random Data Input



NOTES : 1. tADL is the time from the WE risinig edge of final address cycle to the WE rising edge of first data cycle.
2. For EDC operation. only one time random data input is possible at same address.

Figure 16: Random Data In

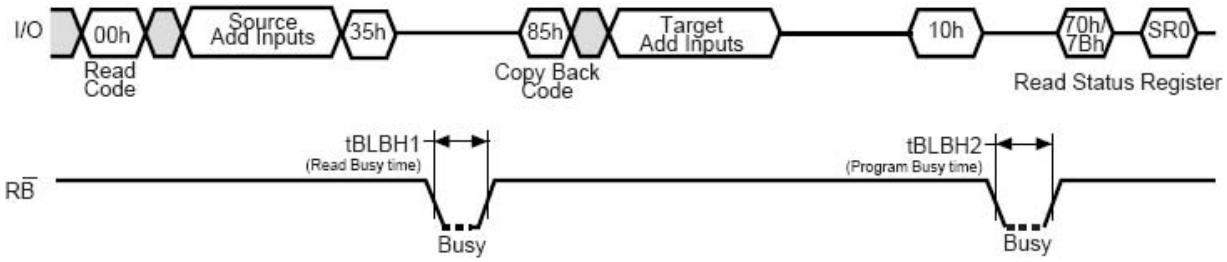


Figure 17: Copy back read with optional data readout

Copy- Back Program Operation With Random Data Input

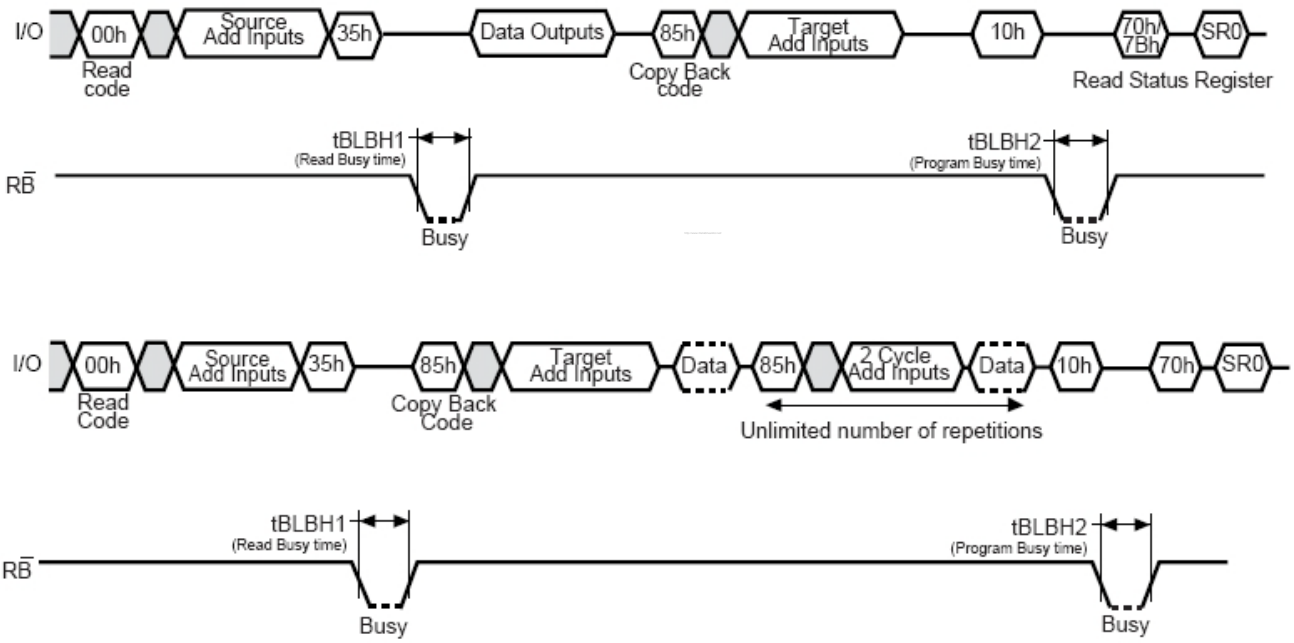


Figure 18: Copy Back Program with Random Data Input

Block Erase Operation

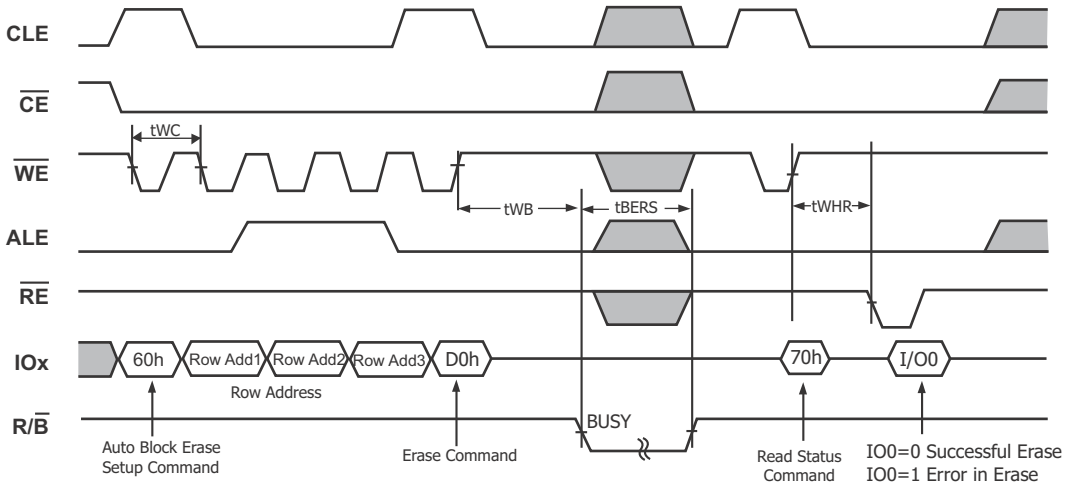
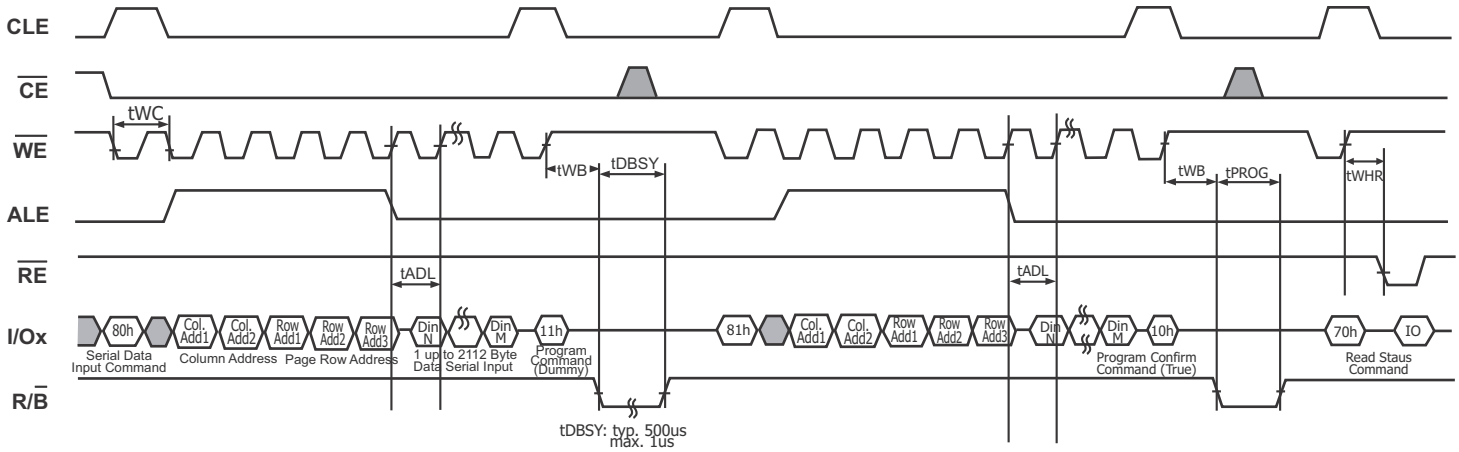
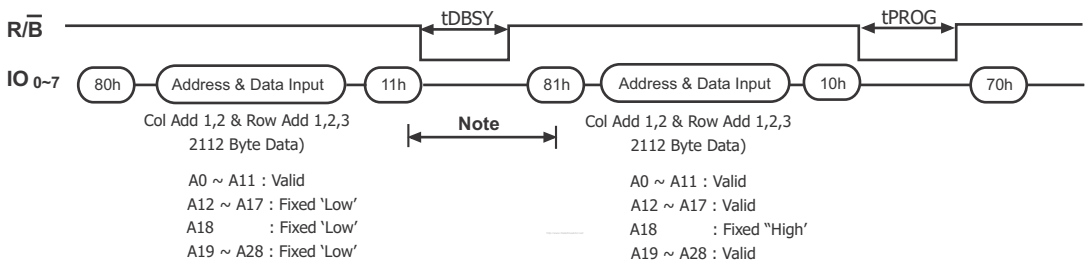


Figure 19: Block Erase Operation (Erase One Block)

Two-Plane Page Program Operation



Ex.) Tow-Plane Page Program



Note : Any command between 11h and 81h is prohibited except 70h and FFh

NOTES:

1) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case
2) **any command between 11h and 81h is prohibited except 70h, 78h and FFh**

Figure 20: Multiple plane page program (traditional protocol)

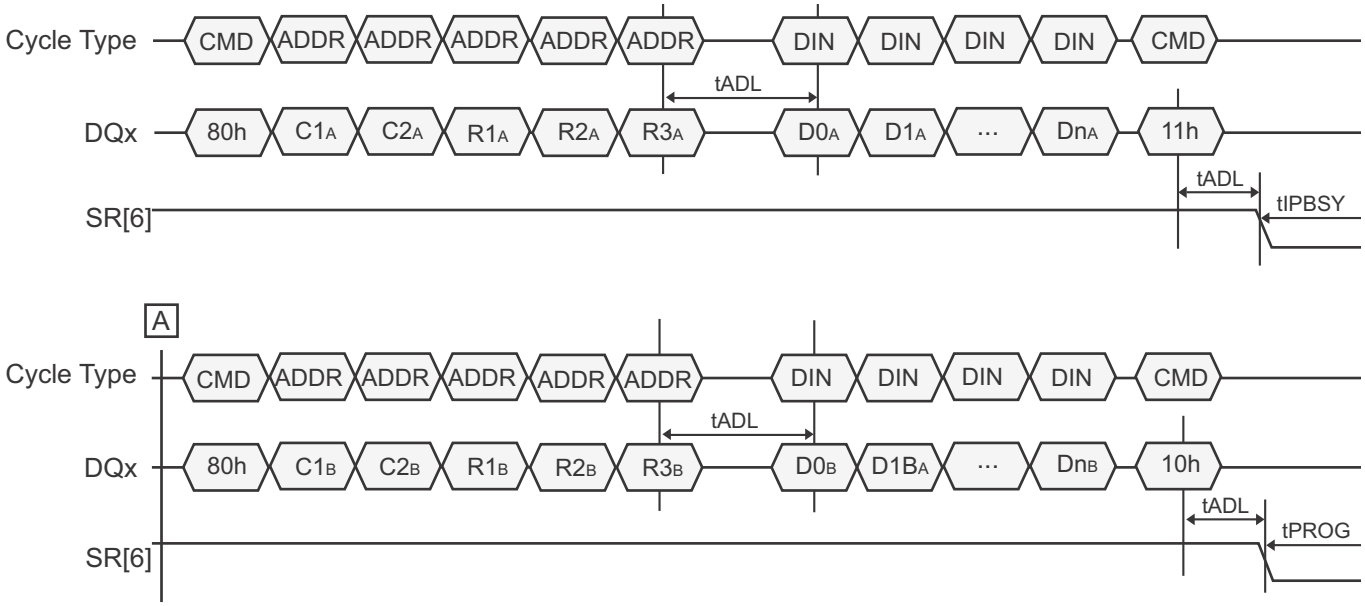
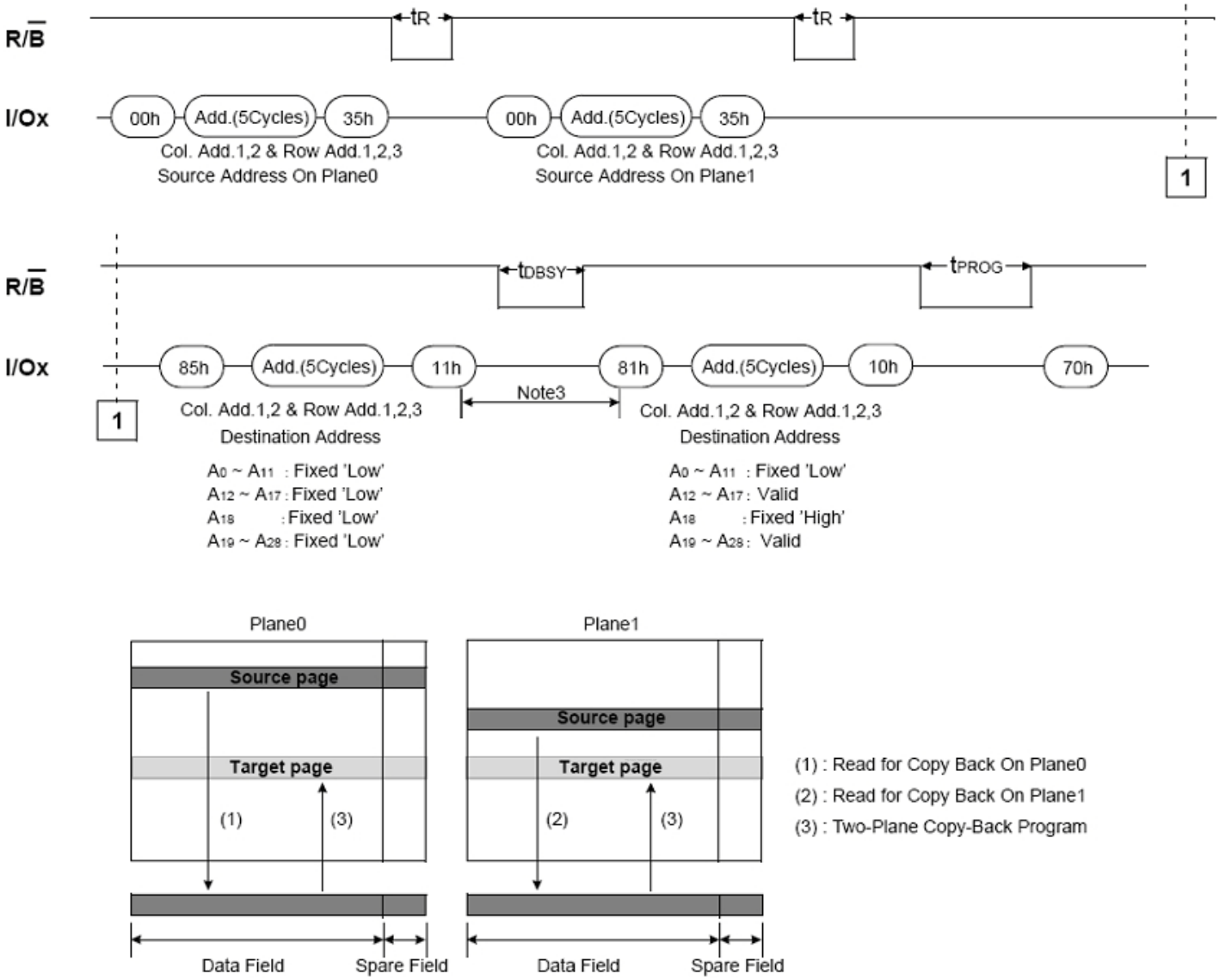


Figure 21 : Multiple plane page program (ONFI 1.0 protocol)

NOTES :
$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.
$D0_A$-Dn_A Data to program for page A.
$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.
$D0_B$-Dn_B Data to program for page B.

Same restrictions on address of pages A and B, and allowed commands as **Figure 20** apply



Note: 1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 22: Multiple plane copy back program (traditional protocol)

NOTE: the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

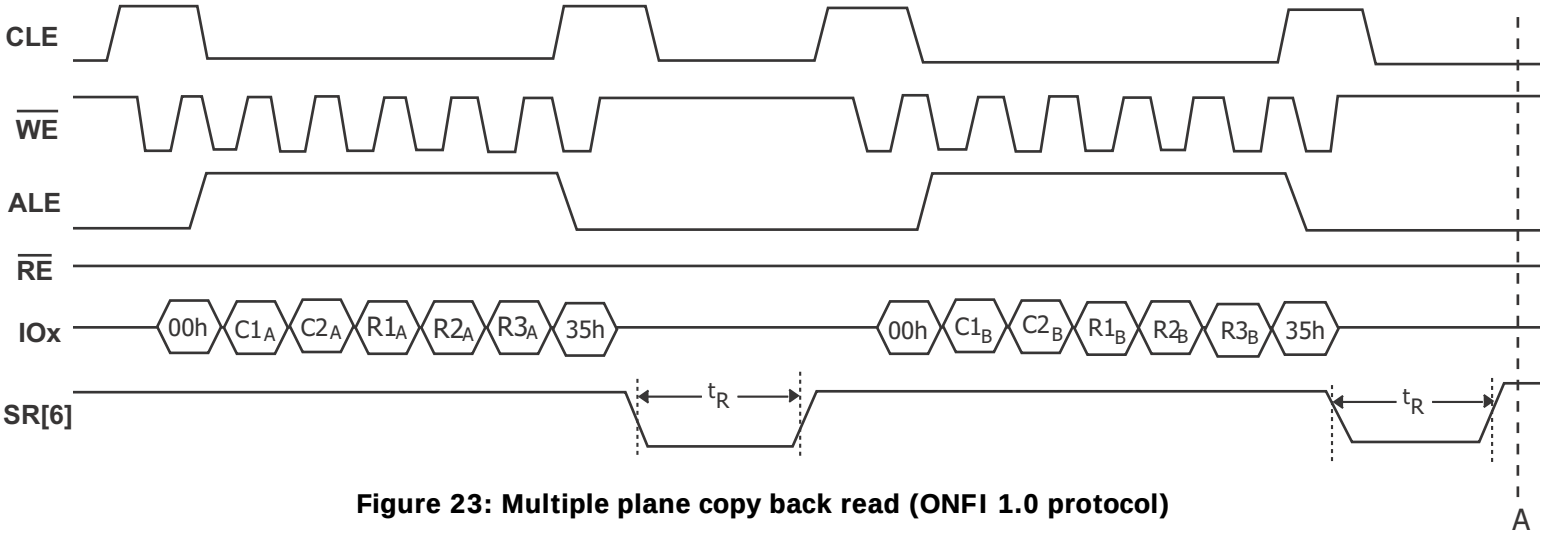


Figure 23: Multiple plane copy back read (ONFI 1.0 protocol)

NOTES:
$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

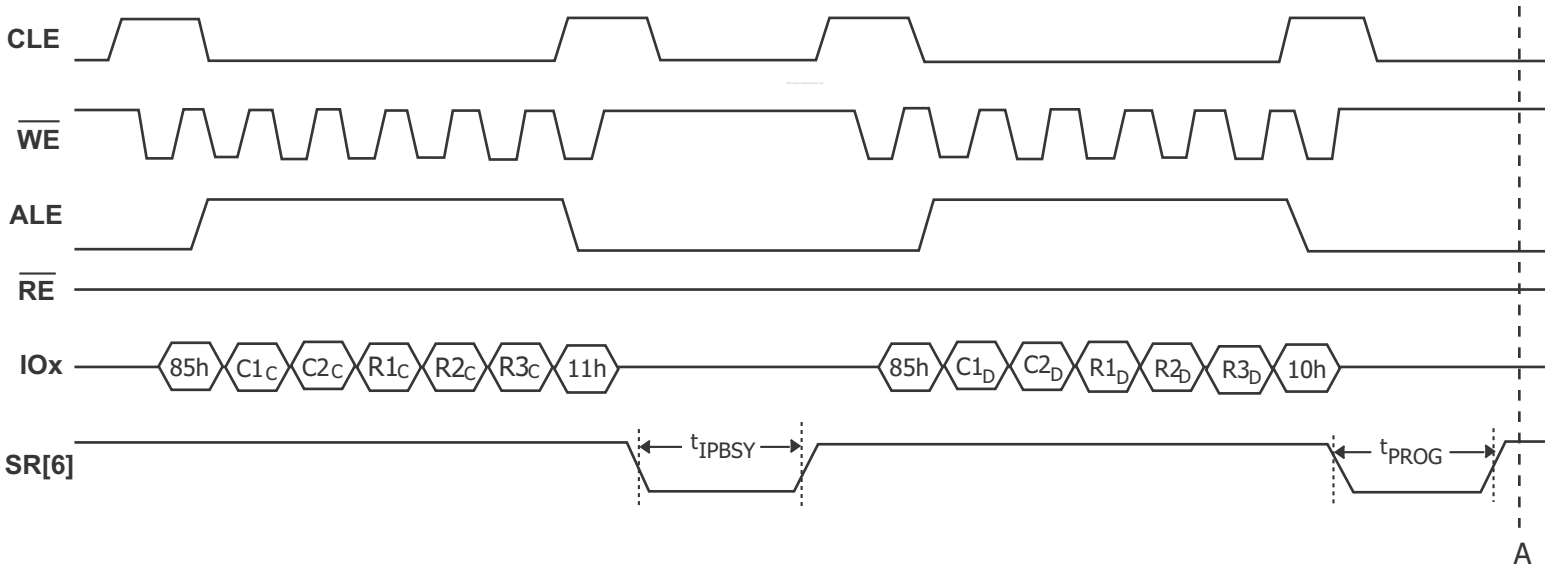
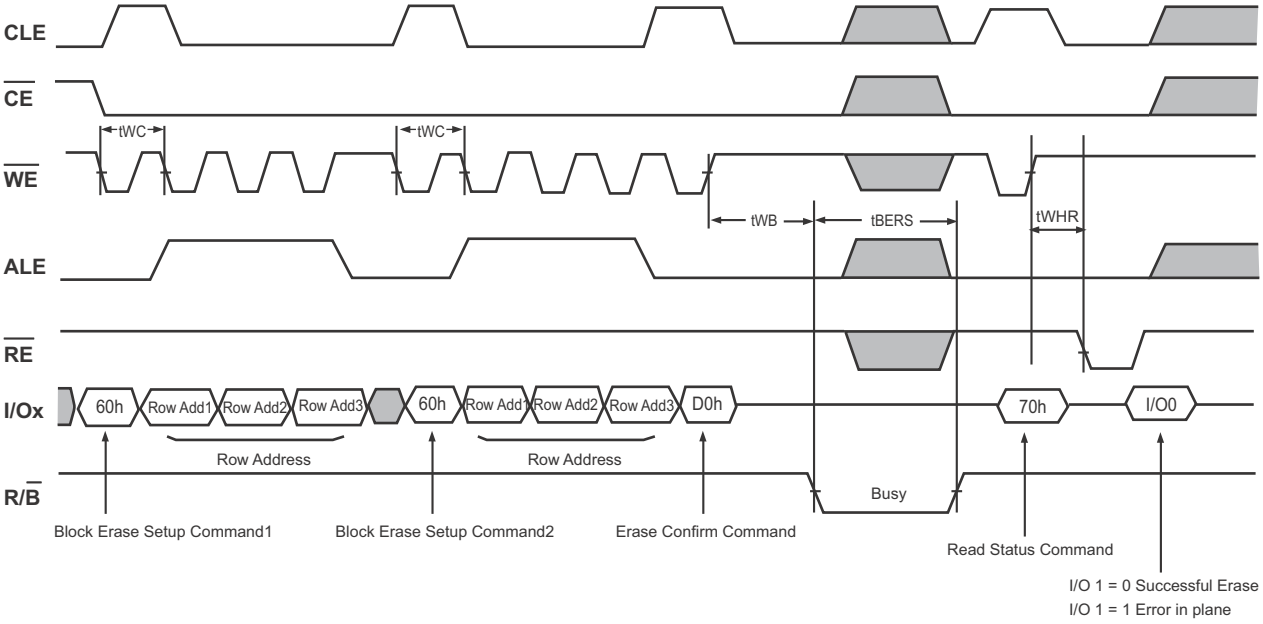


Figure 24: Multiple plane copy back program (ONFI 1.0 protocol)

NOTES:
$C1_C$-$C2_C$ Column address for page C. $C1_A$ is the least significant byte.
$R1_C$-$R3_C$ Row address for page C. $R1_A$ is the least significant byte.
$D0_C$-Dn_C Data to program for page C.
$C1_D$-$C2_D$ Column address for page D. $C1_B$ is the least significant byte.
$R1_D$-$R3_D$ Row address for page D. $R1_B$ is the least significant byte.
$D0_D$-Dn_D Data to program for page D.

Same restrictions on address of pages C and D, and allowed commands as **Figure 22** apply

Two-Plane Block Erase Operation



Ex.) Address Restriction for Two-Plane Block Erase Operation

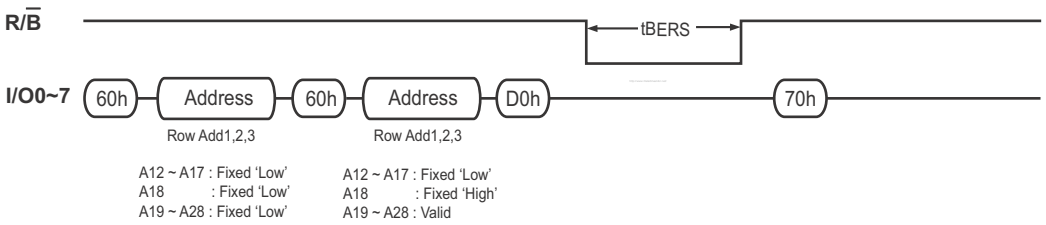
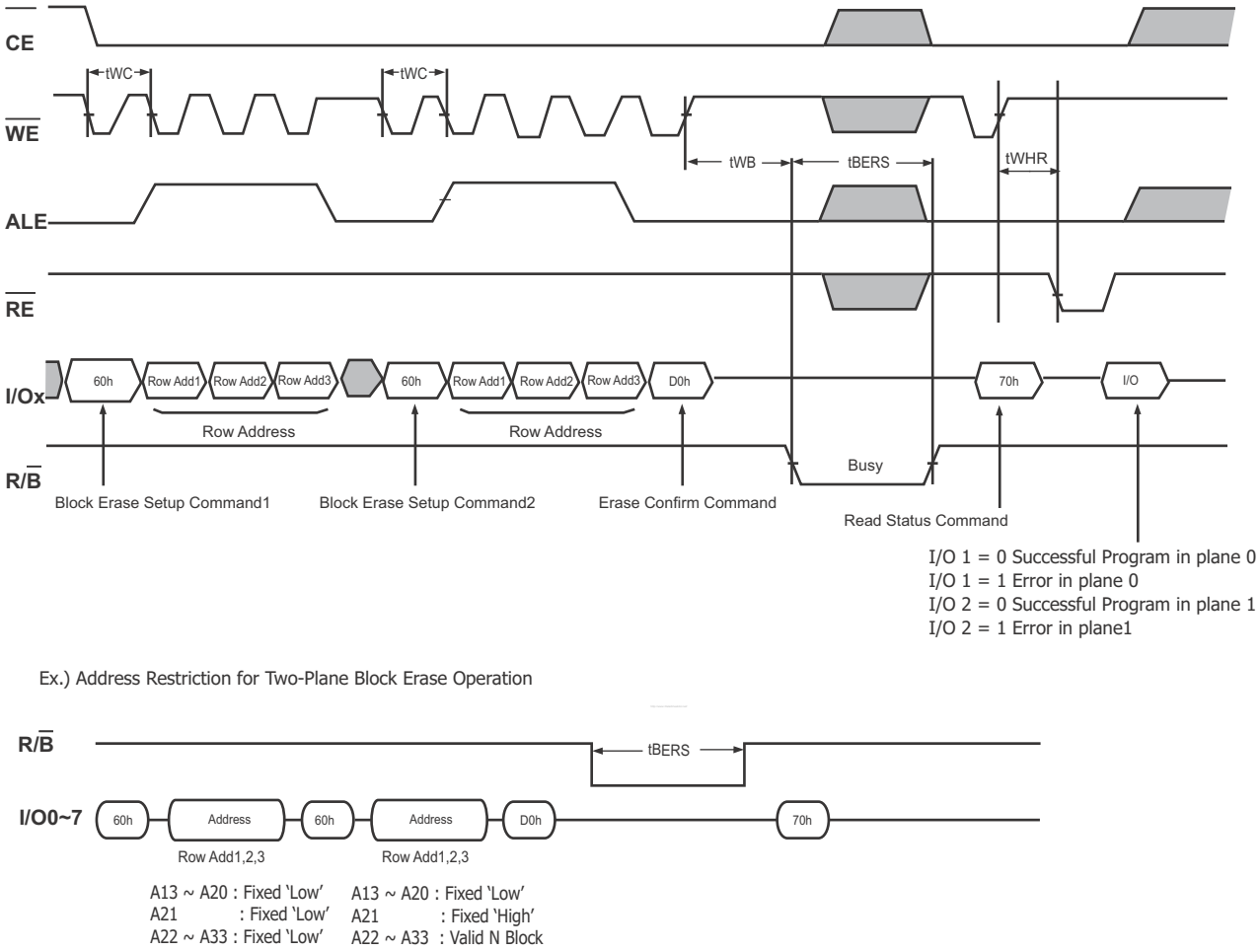


Figure 25: Multiple plane block erase (traditional protocol)

NOTE: the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case



Ex.) Address Restriction for Two-Plane Block Erase Operation

A13 ~ A20 : Fixed 'Low'
A21 : Fixed 'Low'
A22 ~ A33 : Fixed 'Low'

A13 ~ A20 : Fixed 'Low'
A21 : Fixed 'High'
A22 ~ A33 : Valid N Block

Figure 26: Multiple plane block erase (ONFI 1.0 protocol)

NOTES:

$R1_A$-$R3_A$ Row address for block on plane 0. $R1_A$ is the least significant byte.
$R1_B$-$R3_B$ Row address for block on plane 1. $R1_B$ is the least significant byte.

Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as **Figure 25** apply

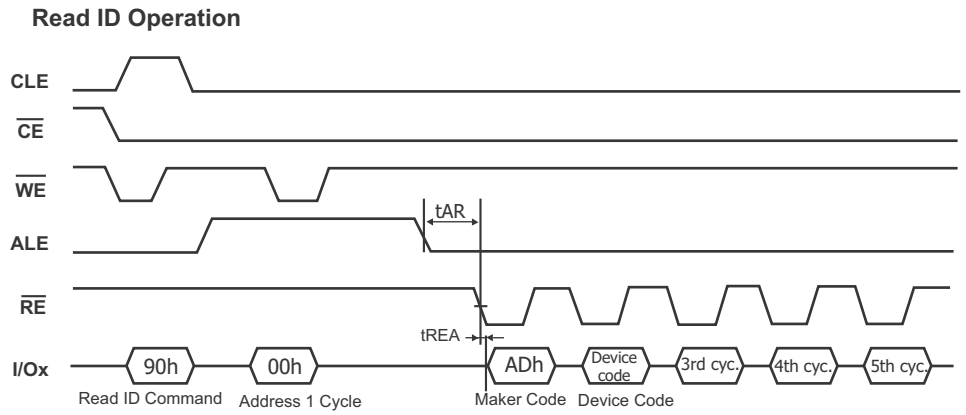


Figure 27: ID Read

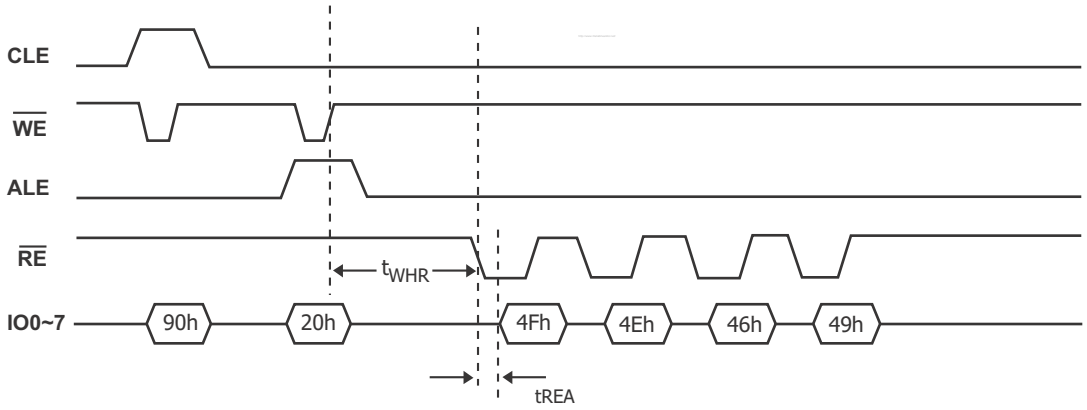


Figure 28: ONFI signature timing diagram

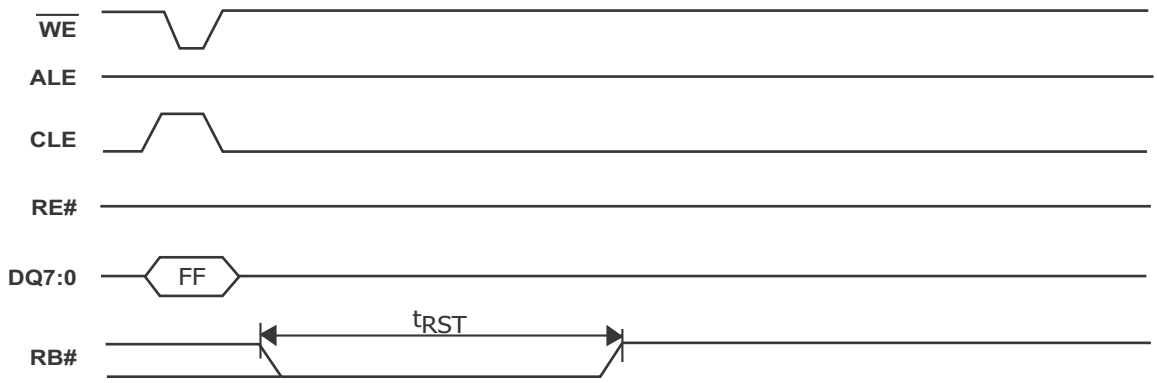


Figure 29: Reset operation timing

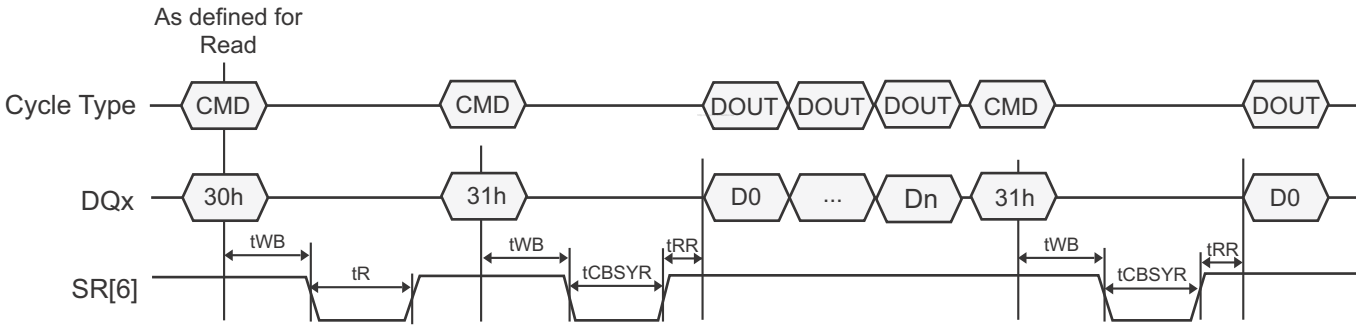


Figure 30: "sequential" read cache timings, start (and continuation) of cache operation

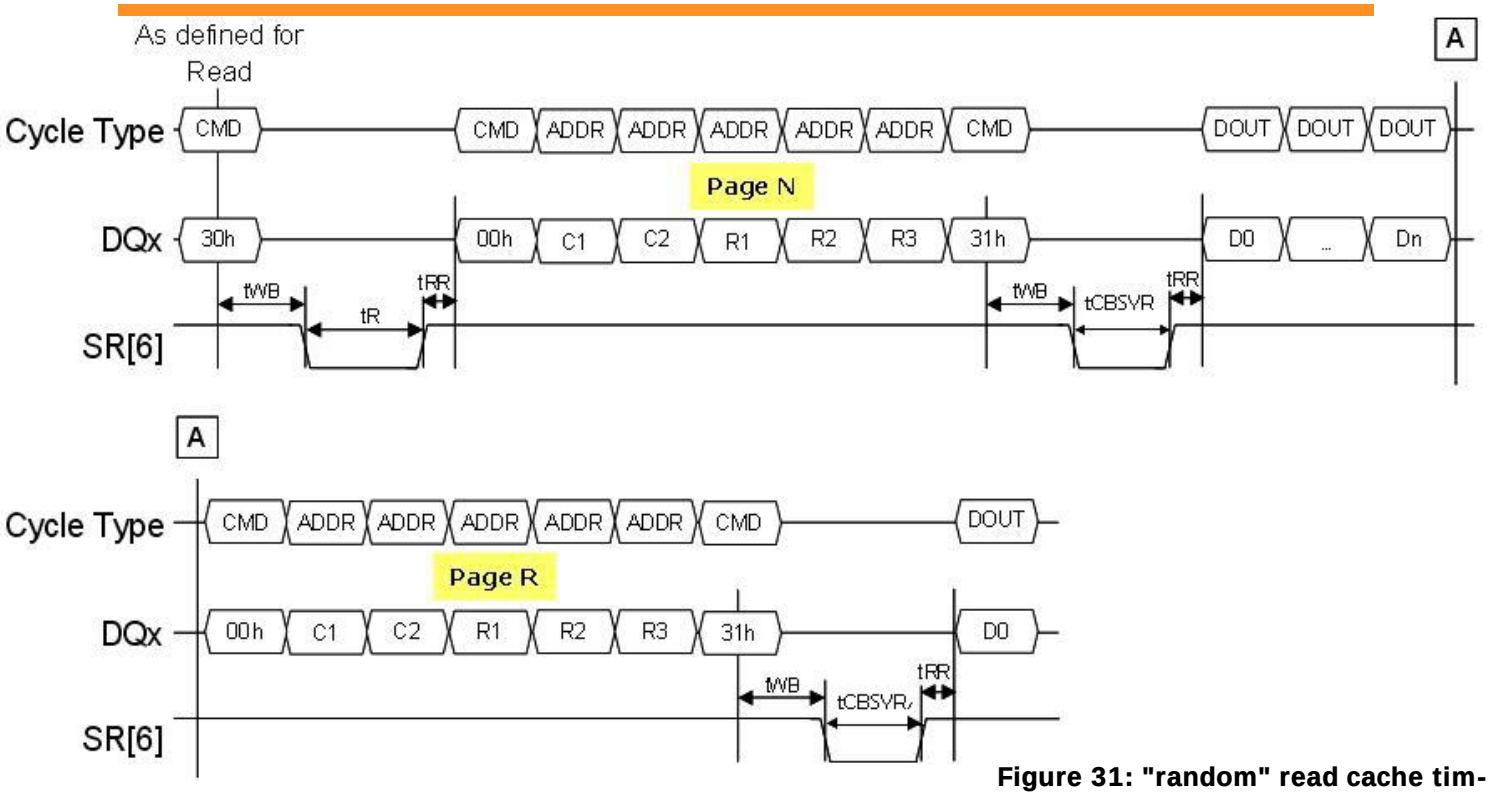
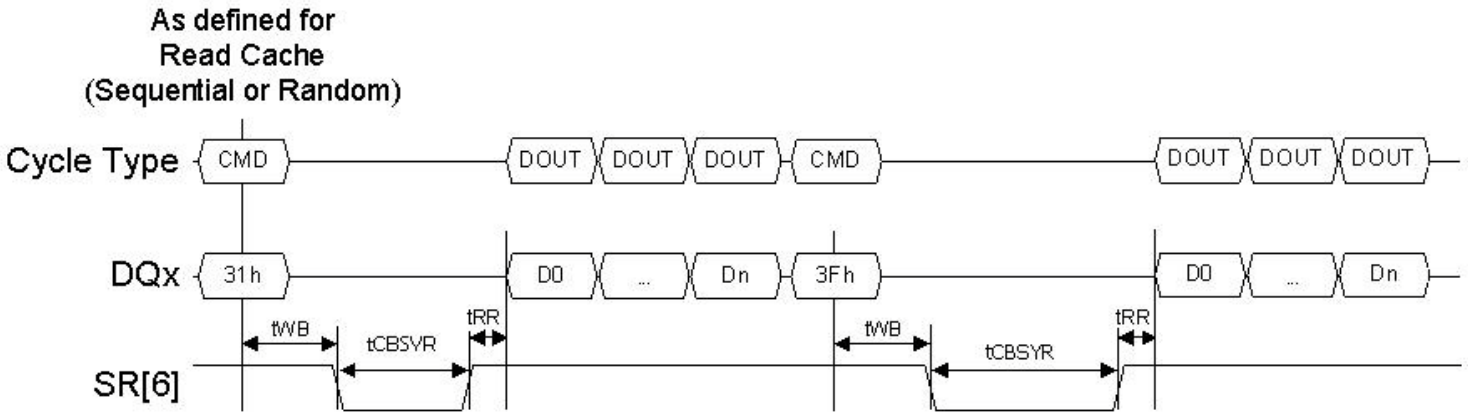


Figure 31: "random" read cache timings, start (and continuation) of cache operation

Figure 32 : read cache timings, end of cache operation



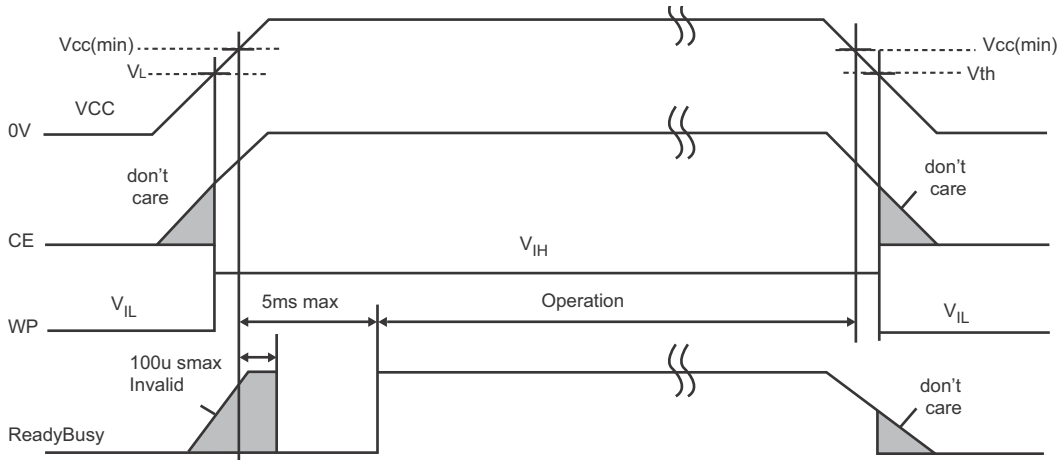
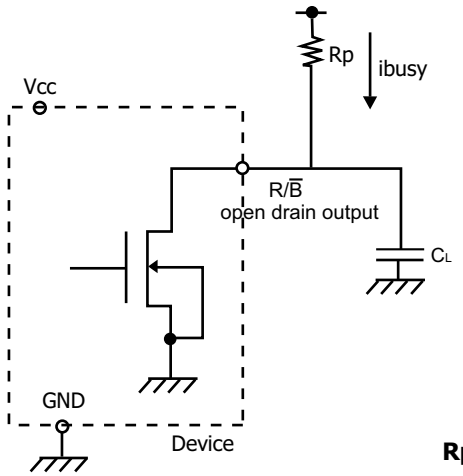
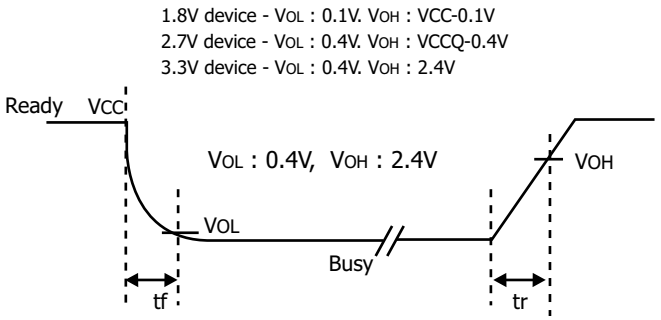


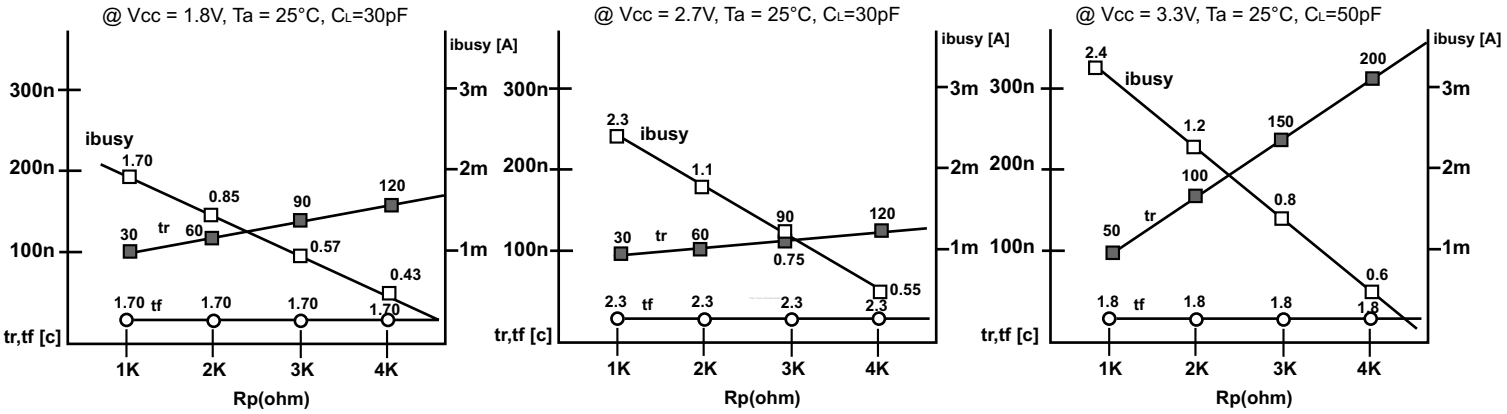
Figure 33: Power on and Data Protection timings

NOTE: V_{TH} = 1.2 Volt for 1.8 Volt Supply devices: 1.8 Volt for 3.0 Volt Supply devices.





Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min.\ 1.8V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.85V}{3mA + \sum I_L}$$ 1.8V version

$$Rp\ (min.\ 2.7V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{2.5V}{3mA + \sum I_L}$$

$$Rp\ (min.\ 3.3V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$ 3.0V version

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 34: Ready/Busy Pin electrical application

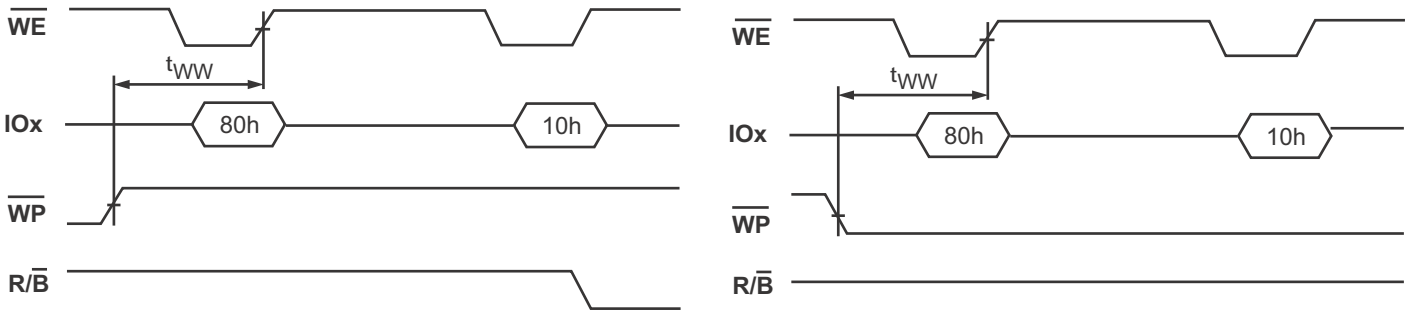


Figure 35: program Enabling / Disabling through WP# handling

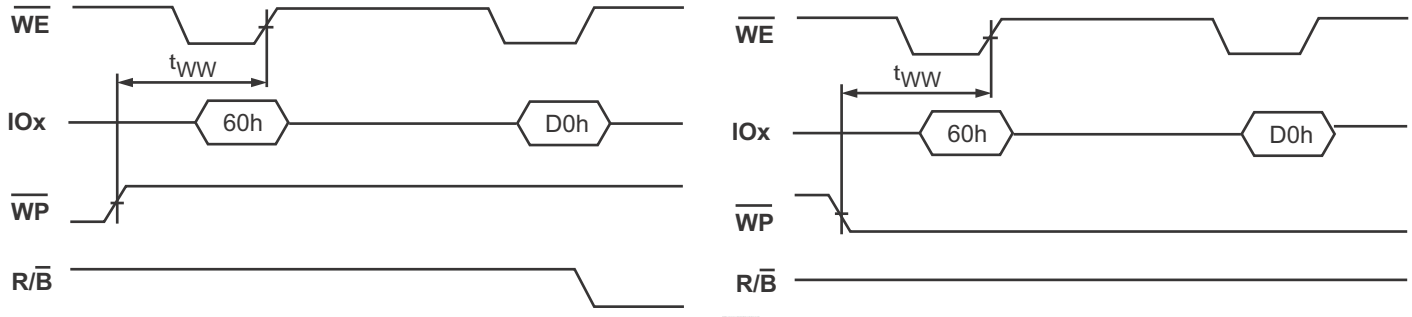


Figure 36: Erase Enabling / Disabling through WP# handling

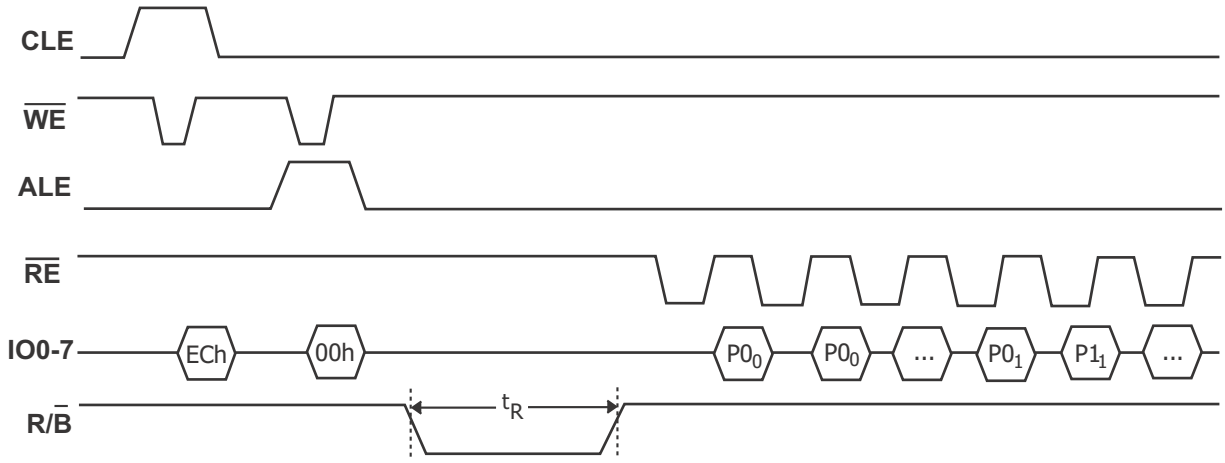


Figure 37: Read Parameter Page timings

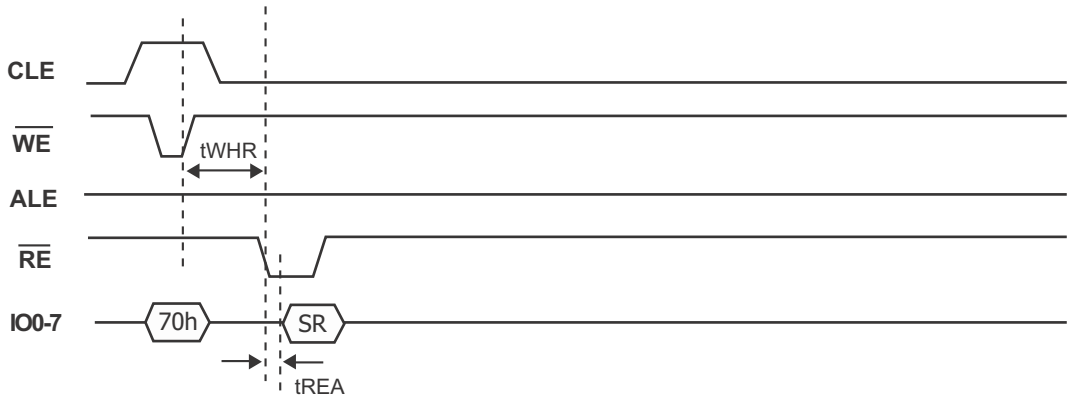


Figure 38: Read Status Timings

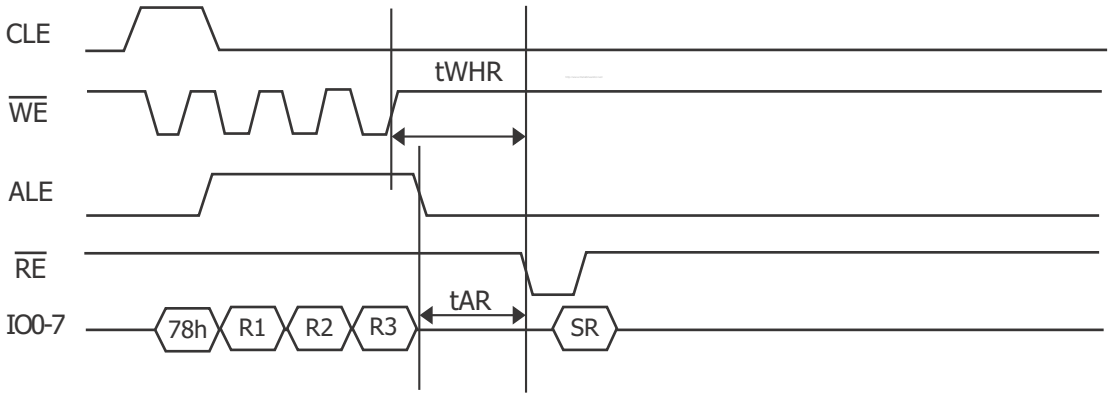


Figure 39: Read Status Enhanced timings

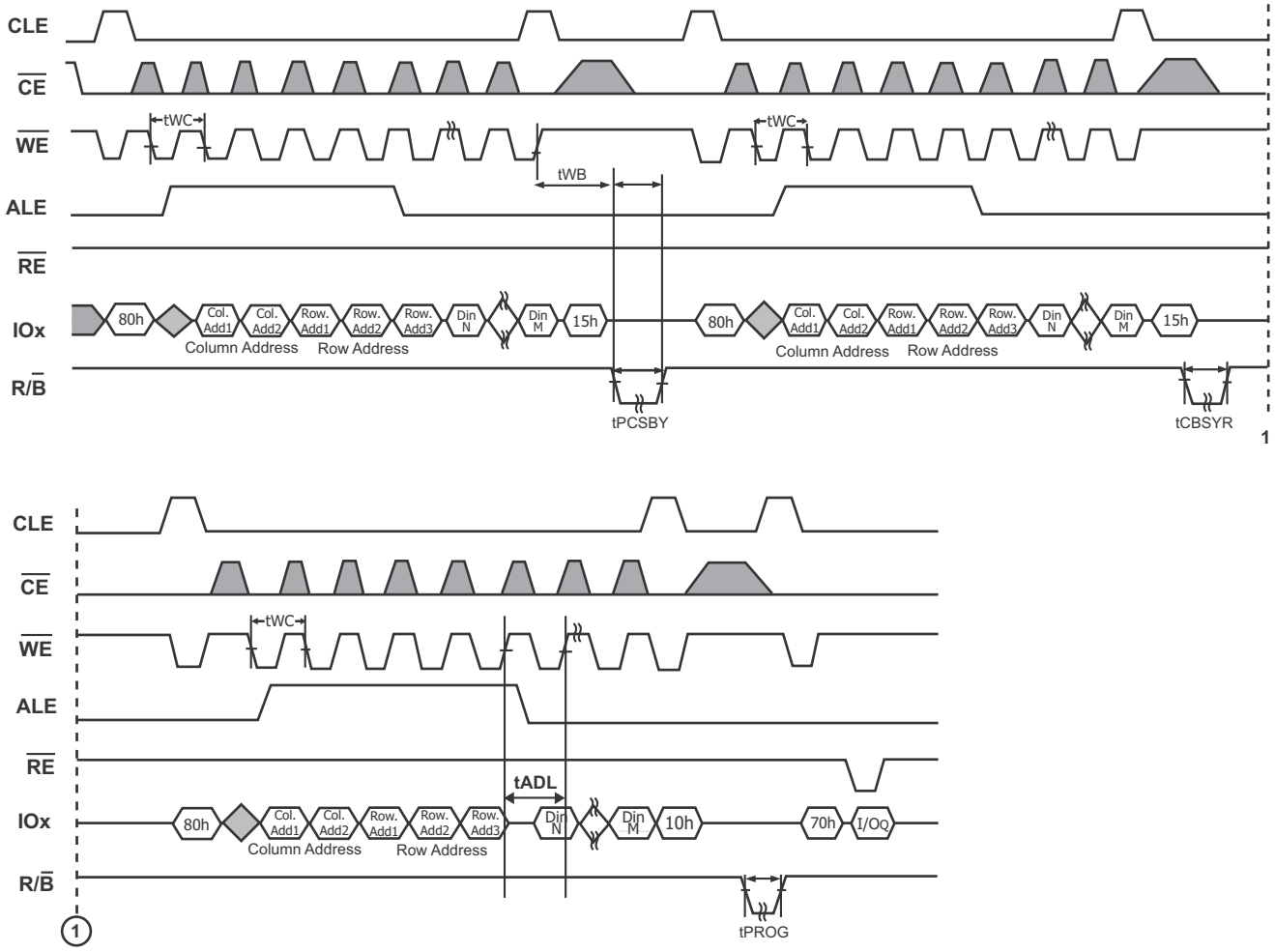


Figure 40: Cache program

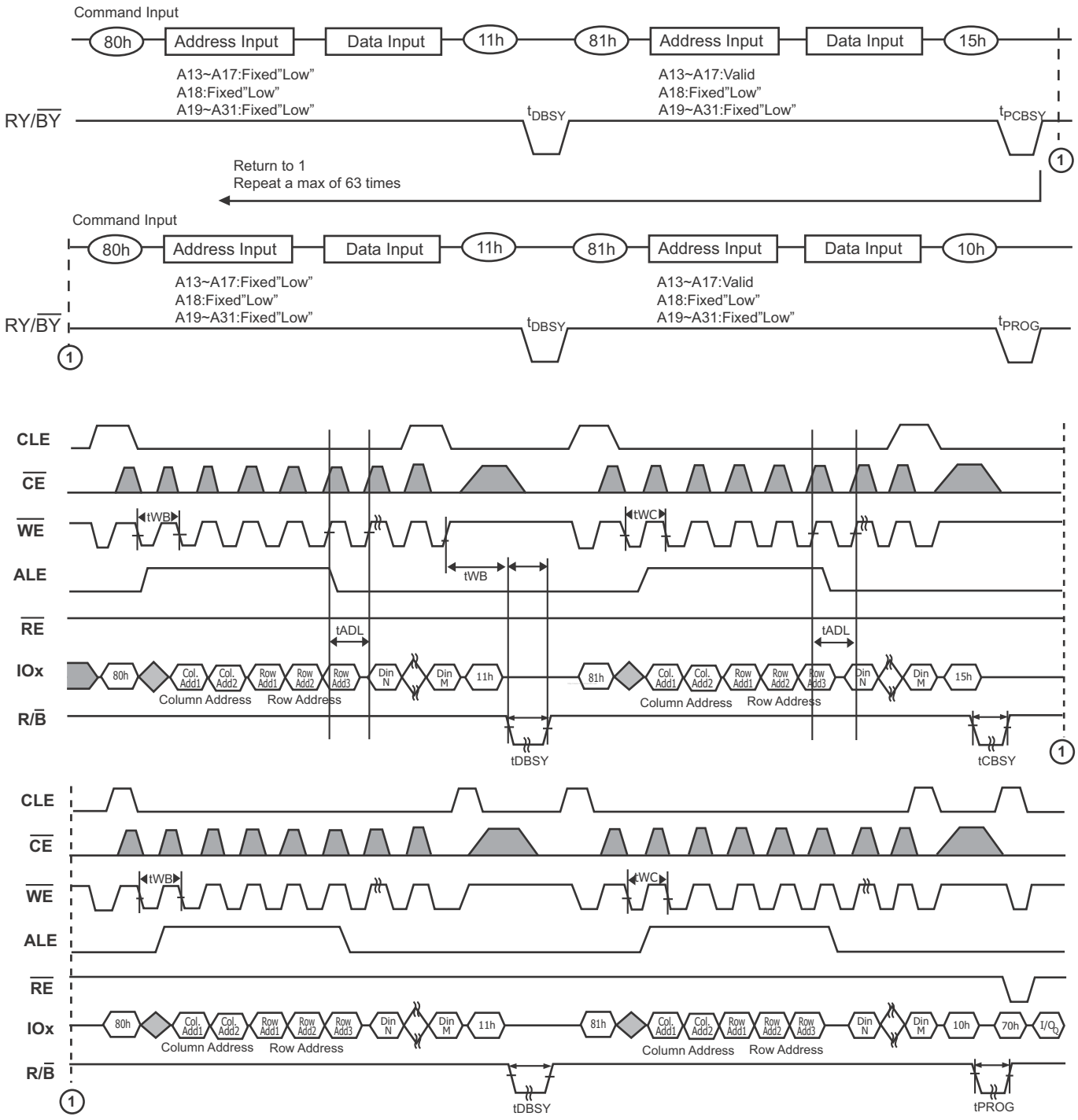


Figure 41: multi-plane cache program (traditional protocol)

NOTE:
1) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case
2) Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used

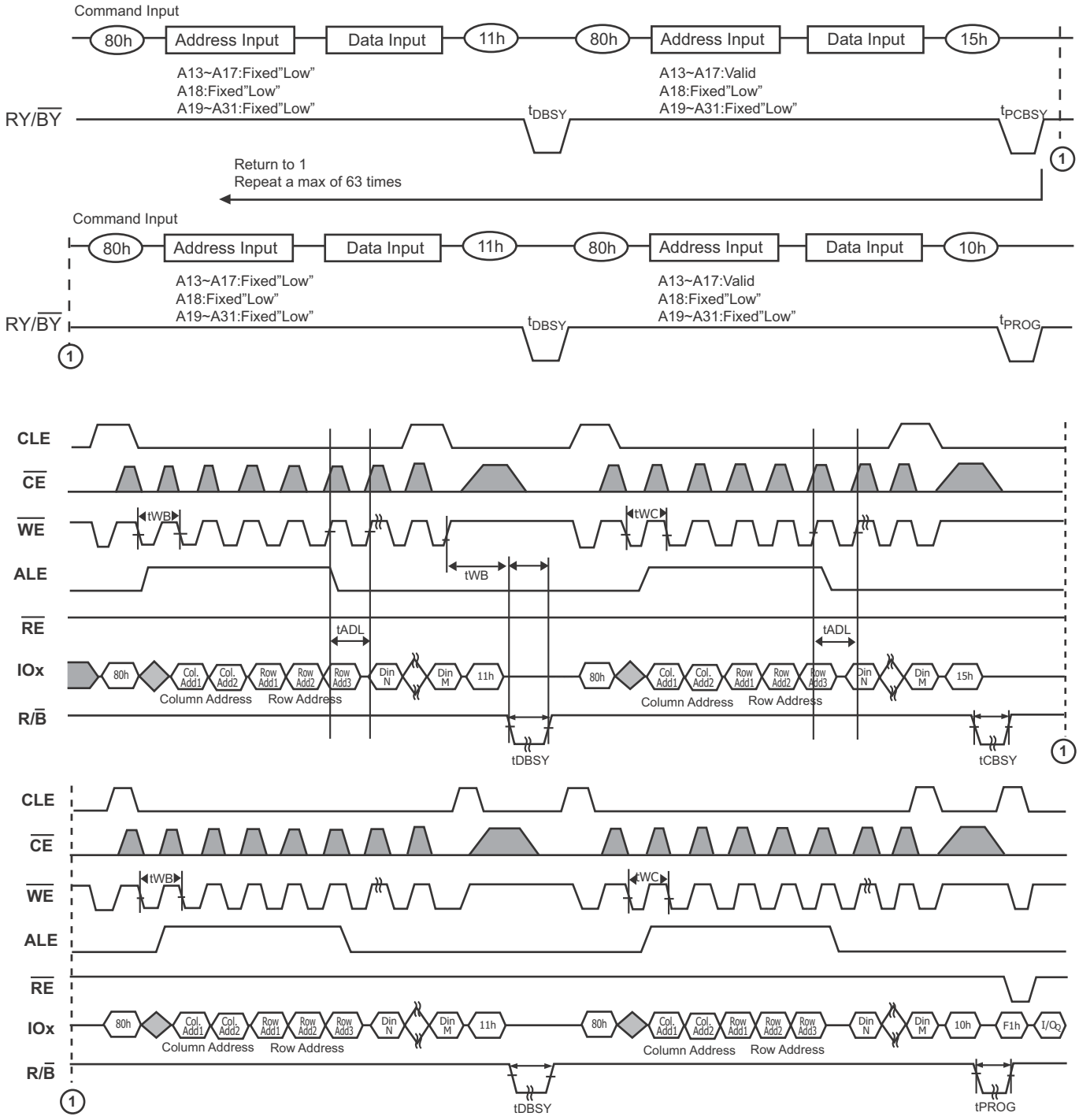


Figure 42: multi-plane cache program (ONFI protocol)

NOTE:

3) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

4) Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used

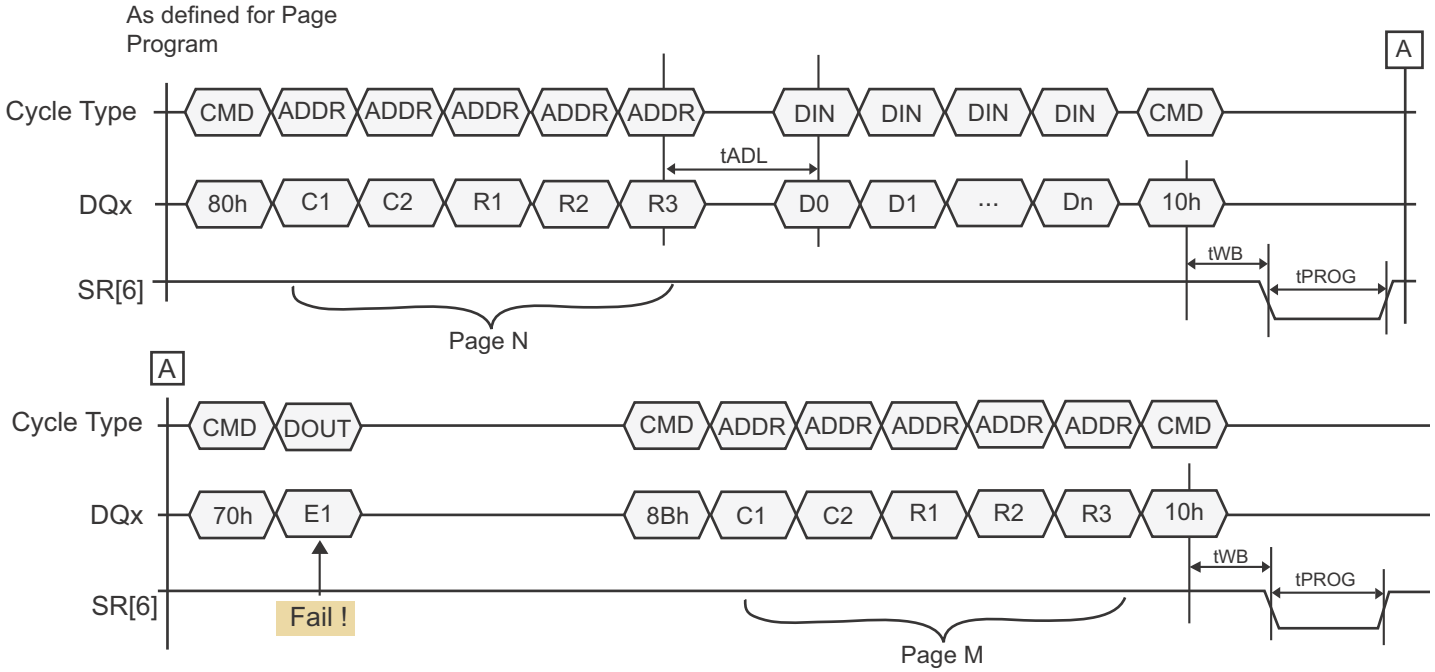


Figure 43: page re-program

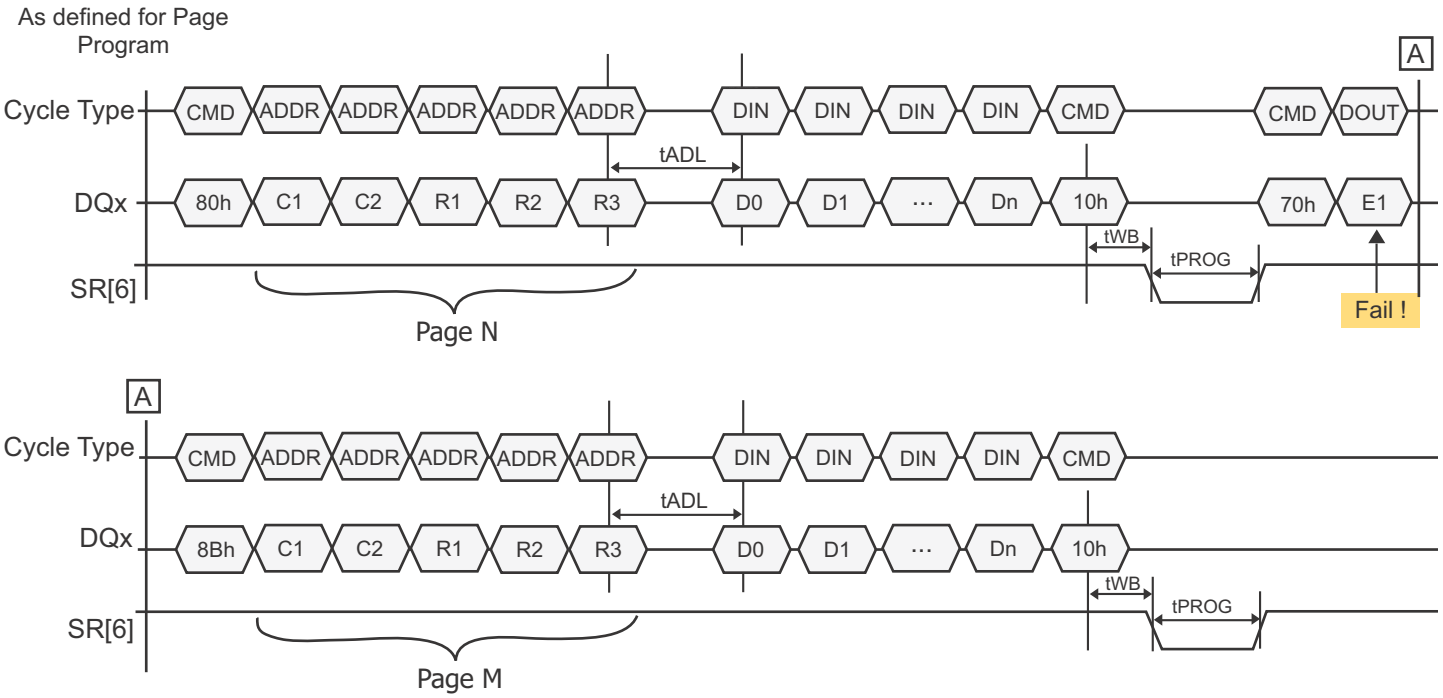


Figure 44: page re-program with data manipulation

Note: refer to **section 3.19** to properly use EDC

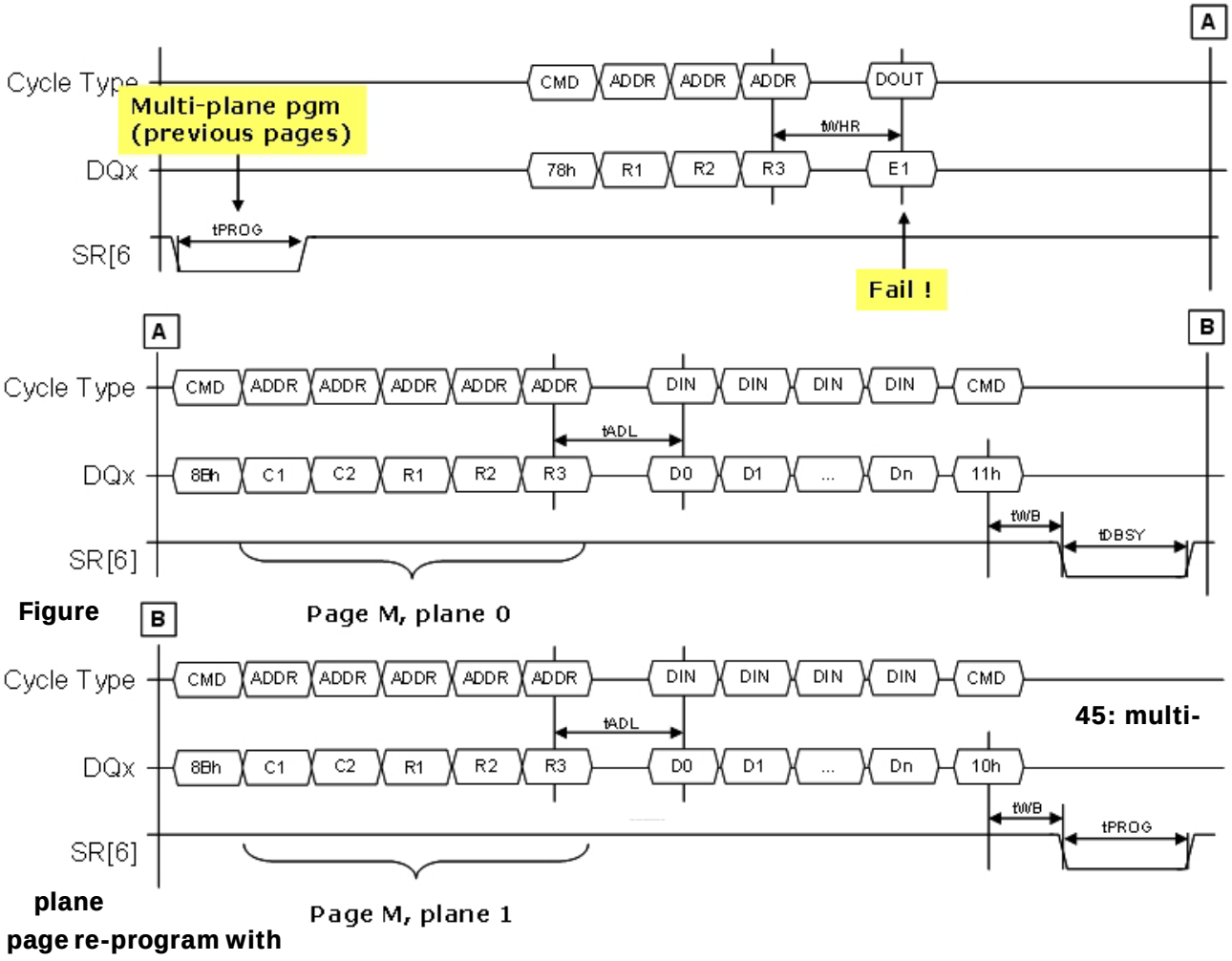


Figure 45: multi-plane page re-program with data manipulation

NOTES:

1) refer to **section 3.19** to properly use EDC
2) the same address restrictions as **Figure 19** apply
3) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

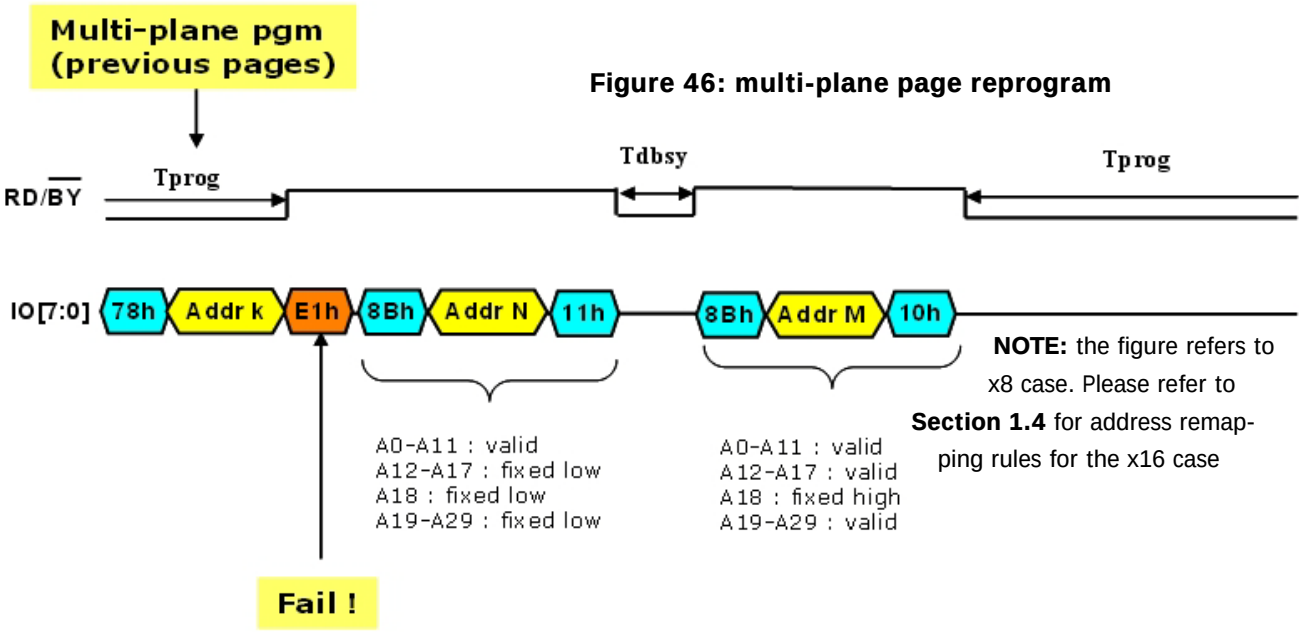


Figure 46: multi-plane page reprogram

NOTE: the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

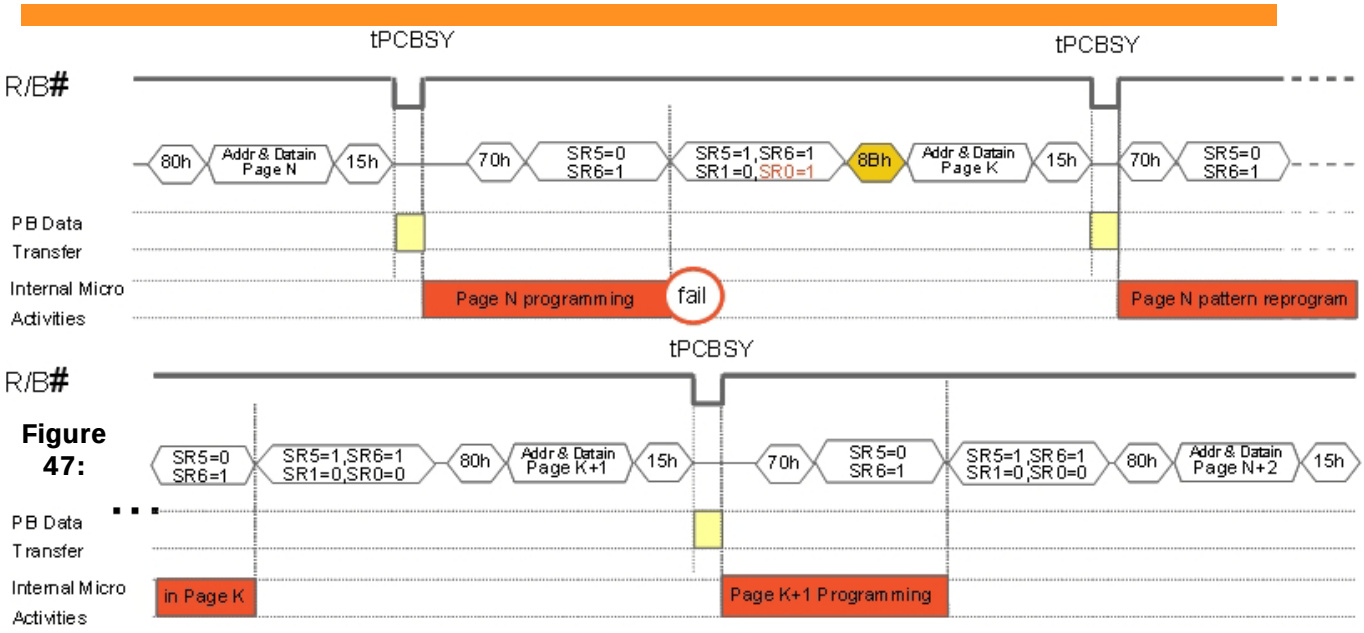


Figure 47:

cache re-program of page N (before cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.21** to properly use EDC.

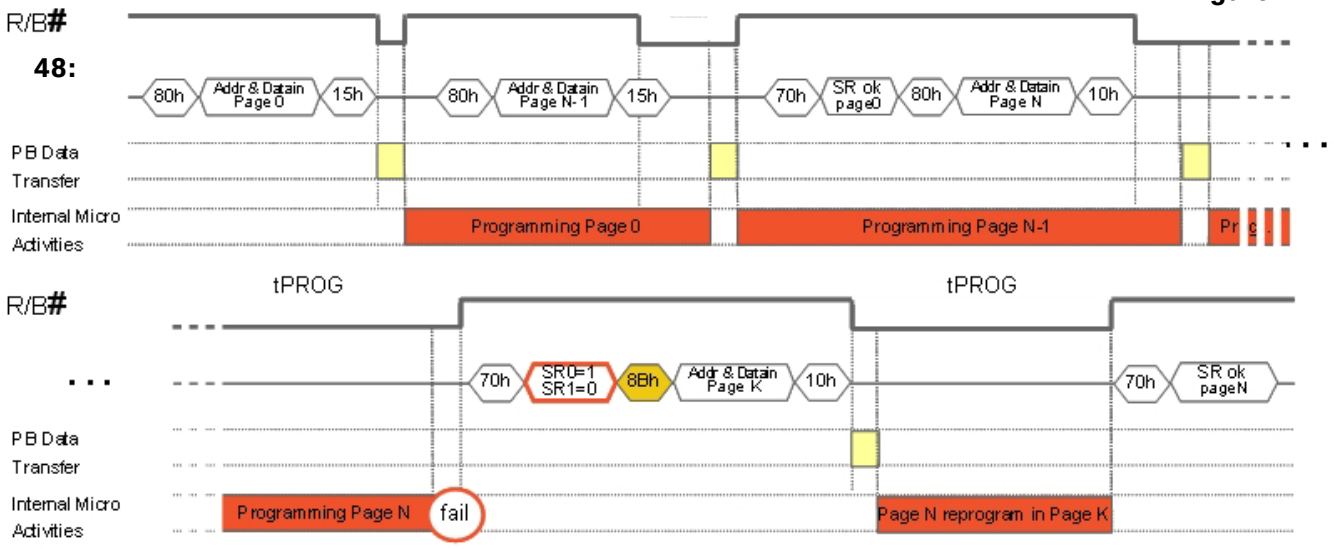


Figure 48:

cache re-program of page N (cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.21** to properly use EDC

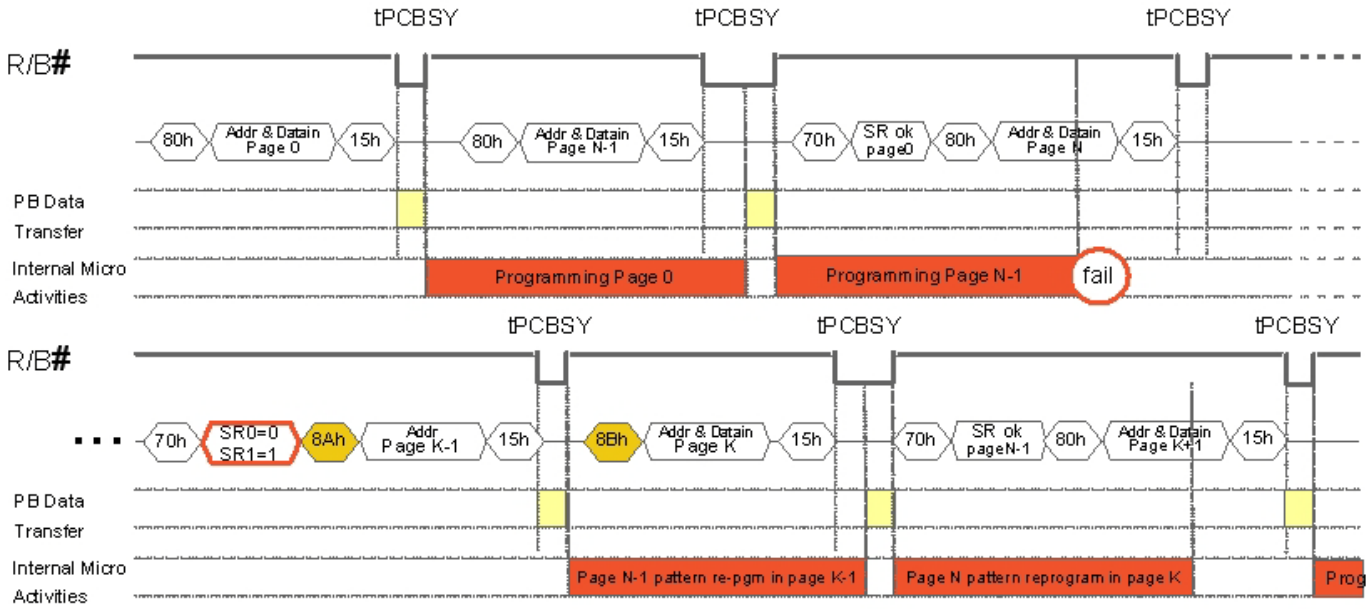


Figure 49: cache re-program of page N-1th (before program cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.21** to properly use EDC

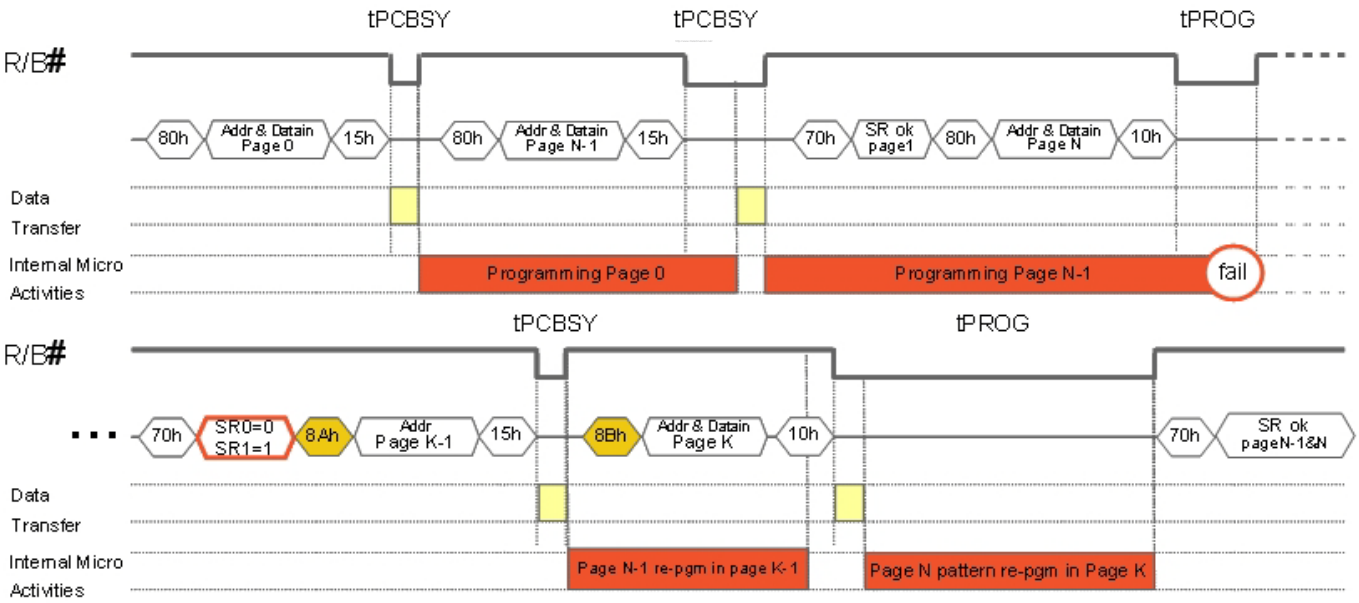


Figure 50: cache re-program of page N-1th (after program cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.21** to properly use EDC

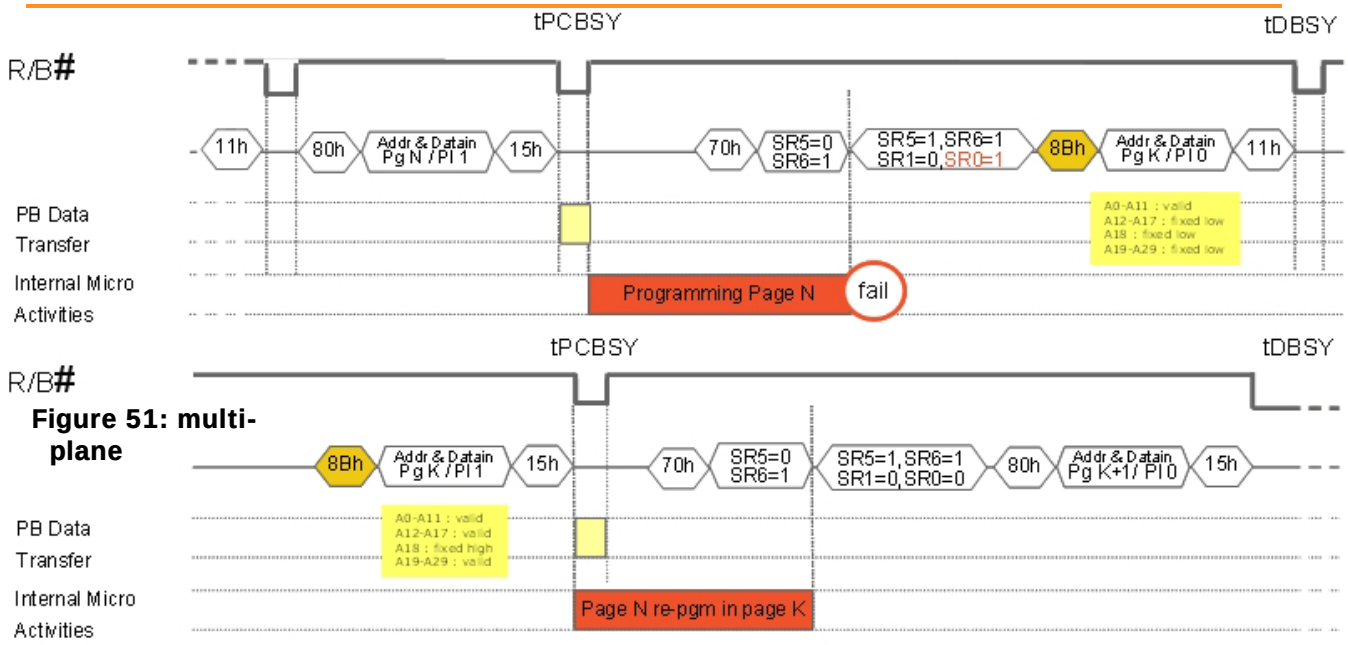
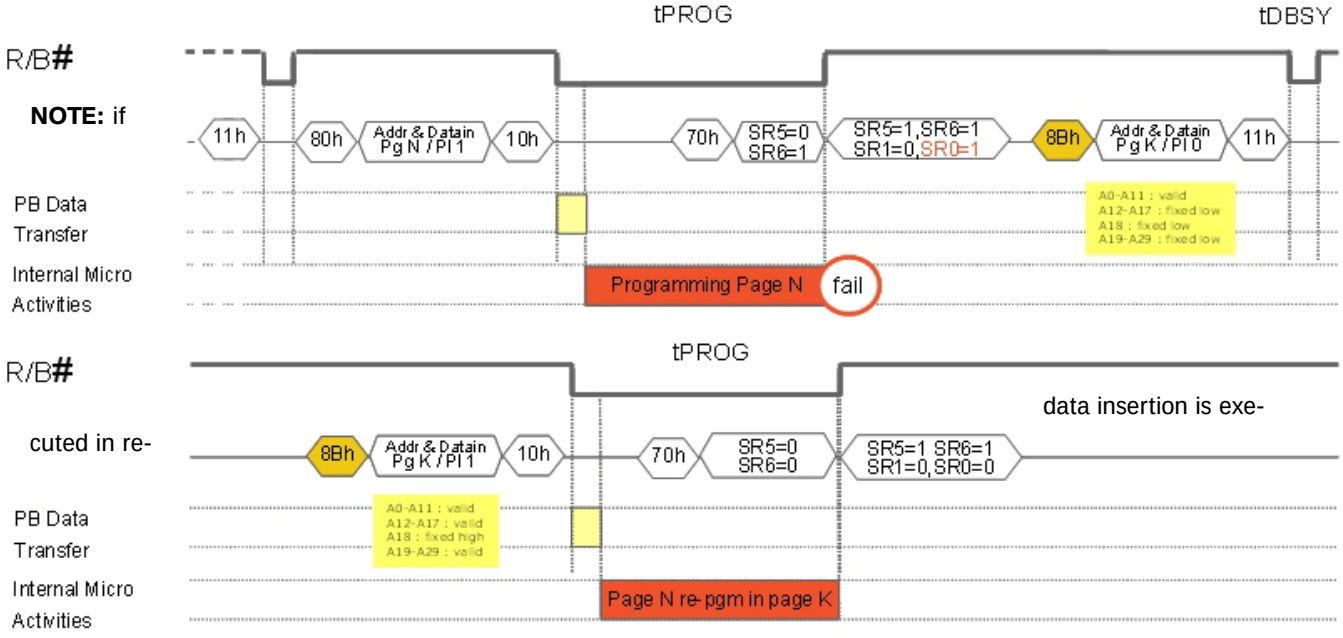


Figure 51: multi-plane cache re-program N[th] pages (before cache end)

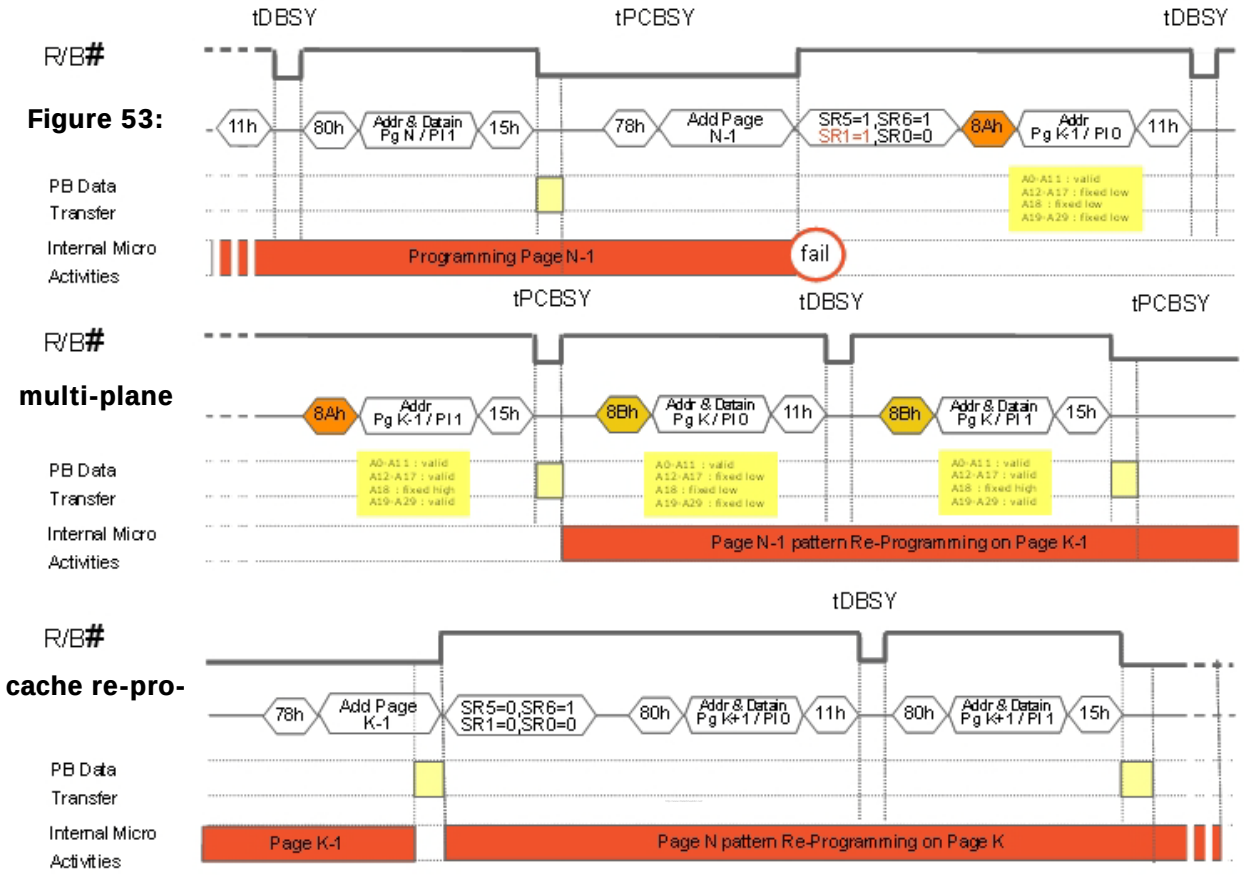
NOTE: if data insertion is executed in re-program of page N, refer to **section 3.22** to properly use EDC

Figure 52: multi-plane cache re-program N[th] pages (at cache end)



NOTE: if data insertion is executed in re-program of page N, refer to **section 3.22** to properly use EDC

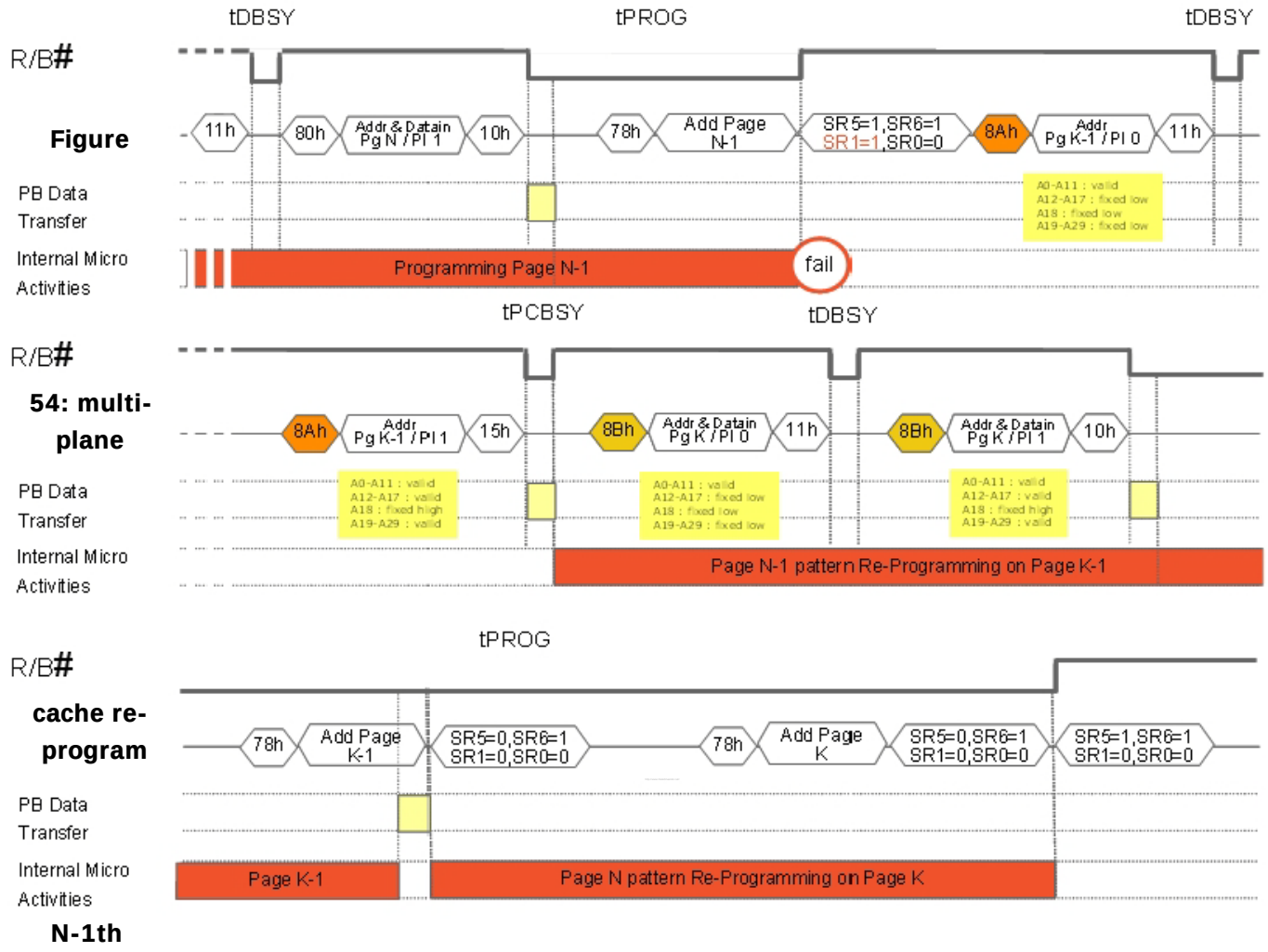
Figure 53:



gram N-1th pages (before cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.22** to properly use EDC

Figure



54: multi-plane

cache re-program

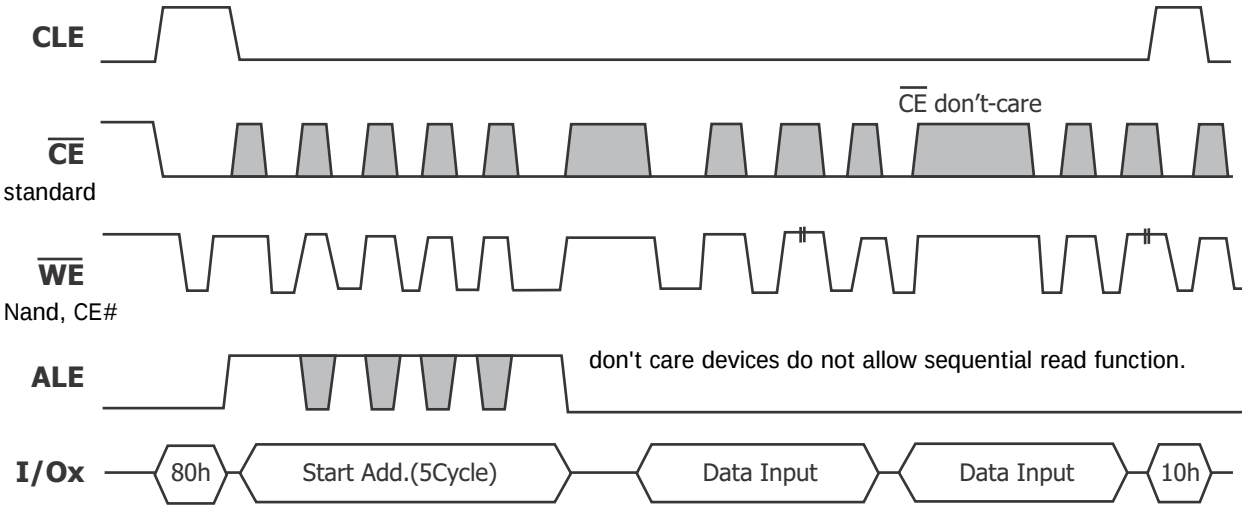
N-1th pages (at cache end)

NOTE: if data insertion is executed in re-program of page N, refer to **section 3.22** to properly use EDC

7 Application notes and comments

7.1 System Interface using CE# don't care

To simplify system interface, CE# may be un-asserted during data loading or sequential data-reading as shown below. By operating in this way, it is possible to connect NAND Flash to a microprocessor.
Contrary to



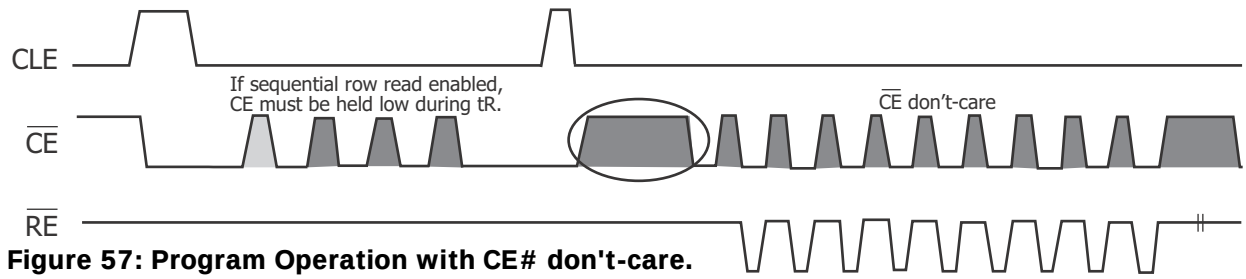
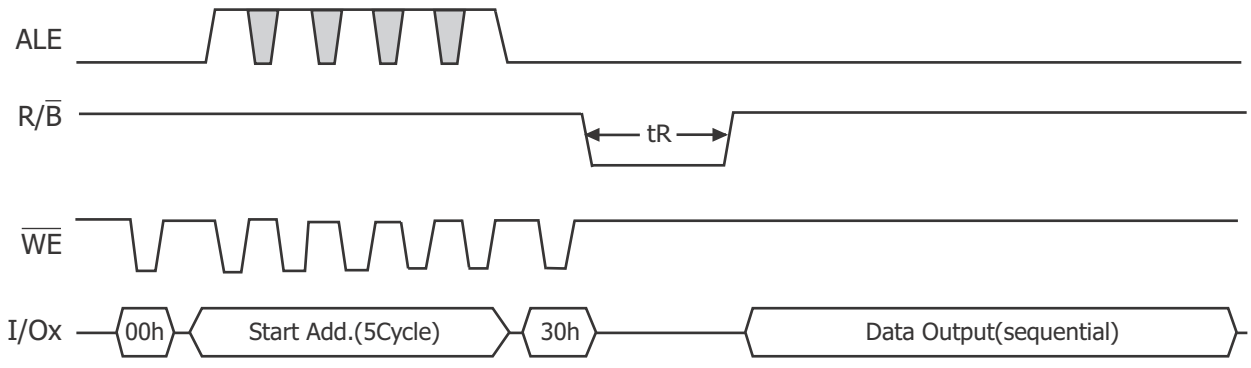


Figure 57: Program Operation with CE# don't-care.



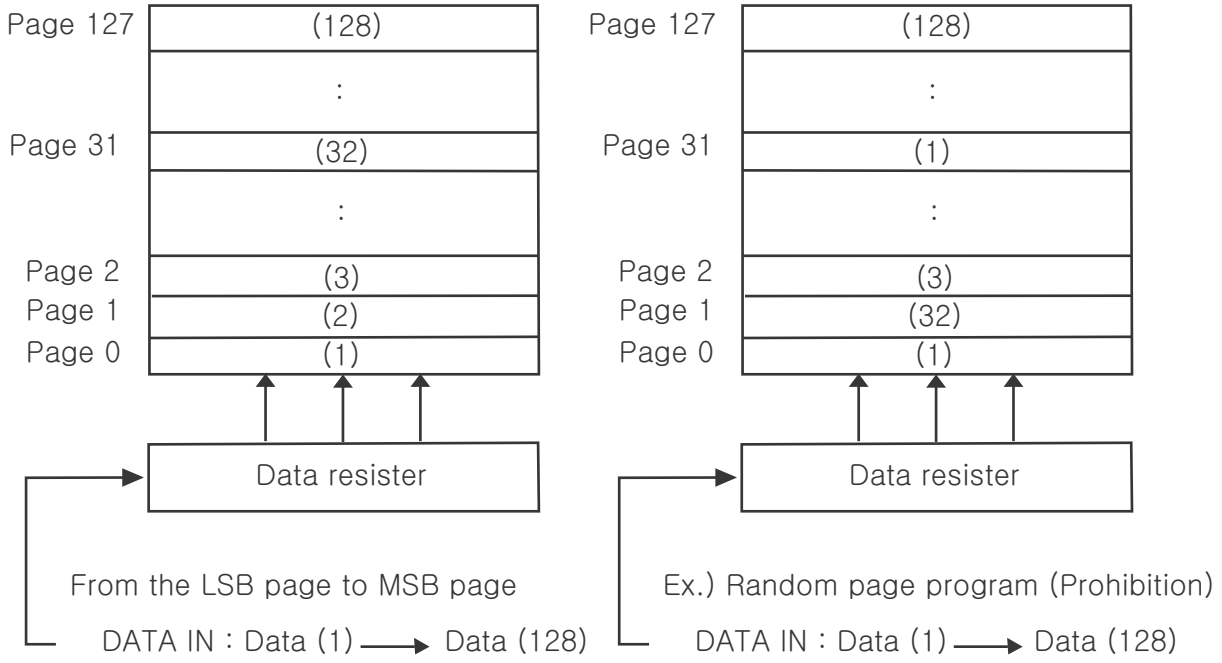


Figure 59: page programming within a block

7.2 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flow-

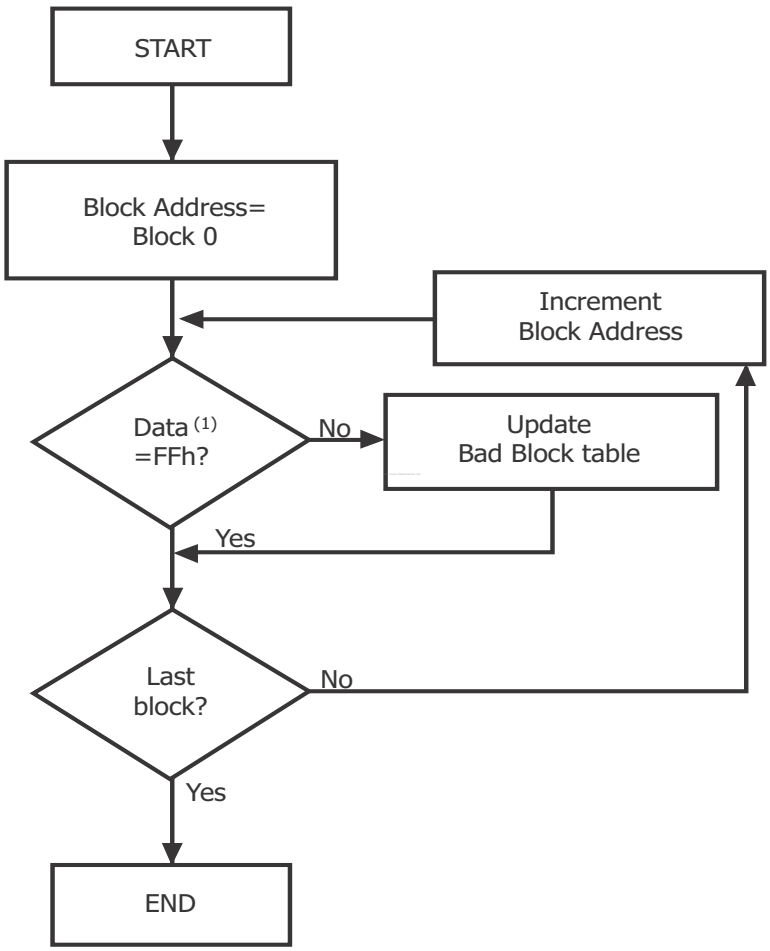


Figure 60: Bad Block Management Flowchart

NOTE :
1. Check FFh at 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad).

7.3 System Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case each bad block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will return "fail" after Read Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to **Table 37** and **Figure 59** for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Table 37: Block Failure

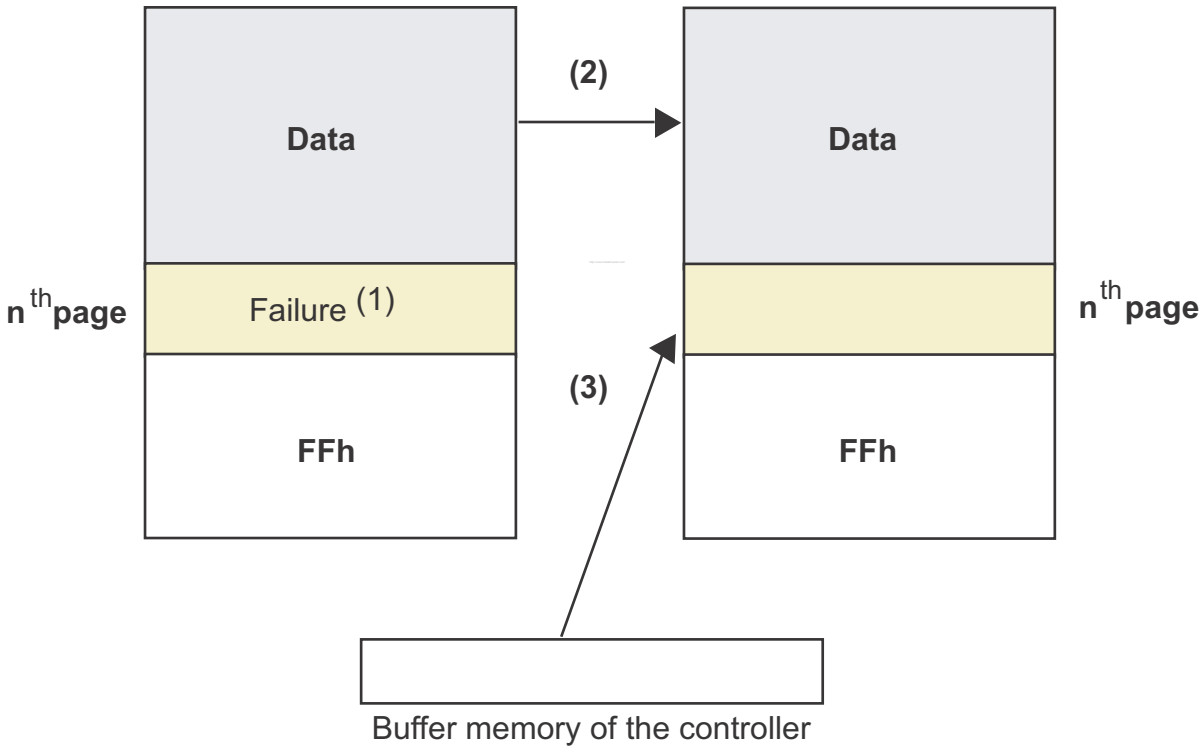


Figure 59 : Bad Block Replacement

NOTE:

1. An error occurs on N^{th} page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} page of block A which is in controller buffer memory is copied into N^{th} page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

2Gb (64Mbx32) Mobile DDR A-Die

DESCRIPTION

The Hynix mobile DDR SDRAMs is 2,147,483,648-bit CMOS Low Power Double Data Rate Synchronous DRAM (Mobile DDR SDRAM), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 16,777,216x32.

The Hynix mobile DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins.

The Hynix mobile DDR SDRAM offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (Mobile DDR SDRAM operates from a differential clock*: the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK*), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (*Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK*). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the Low Power DDR SDRAM (Mobile DDR SDRAM) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Hynix mobile DDR SDRAM provides for programmable read or write bursts of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multibank architecture of Low Power DDR SDRAM (Mobile DDR SDRAM) allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

The Hynix mobile DDR SDRAM also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half and quarter array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule). Only Read bursts in progress with auto precharge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Autoprecharge enabled and for Write bursts.

The Hynix mobile DDR SDRAM has the special Low Power function of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

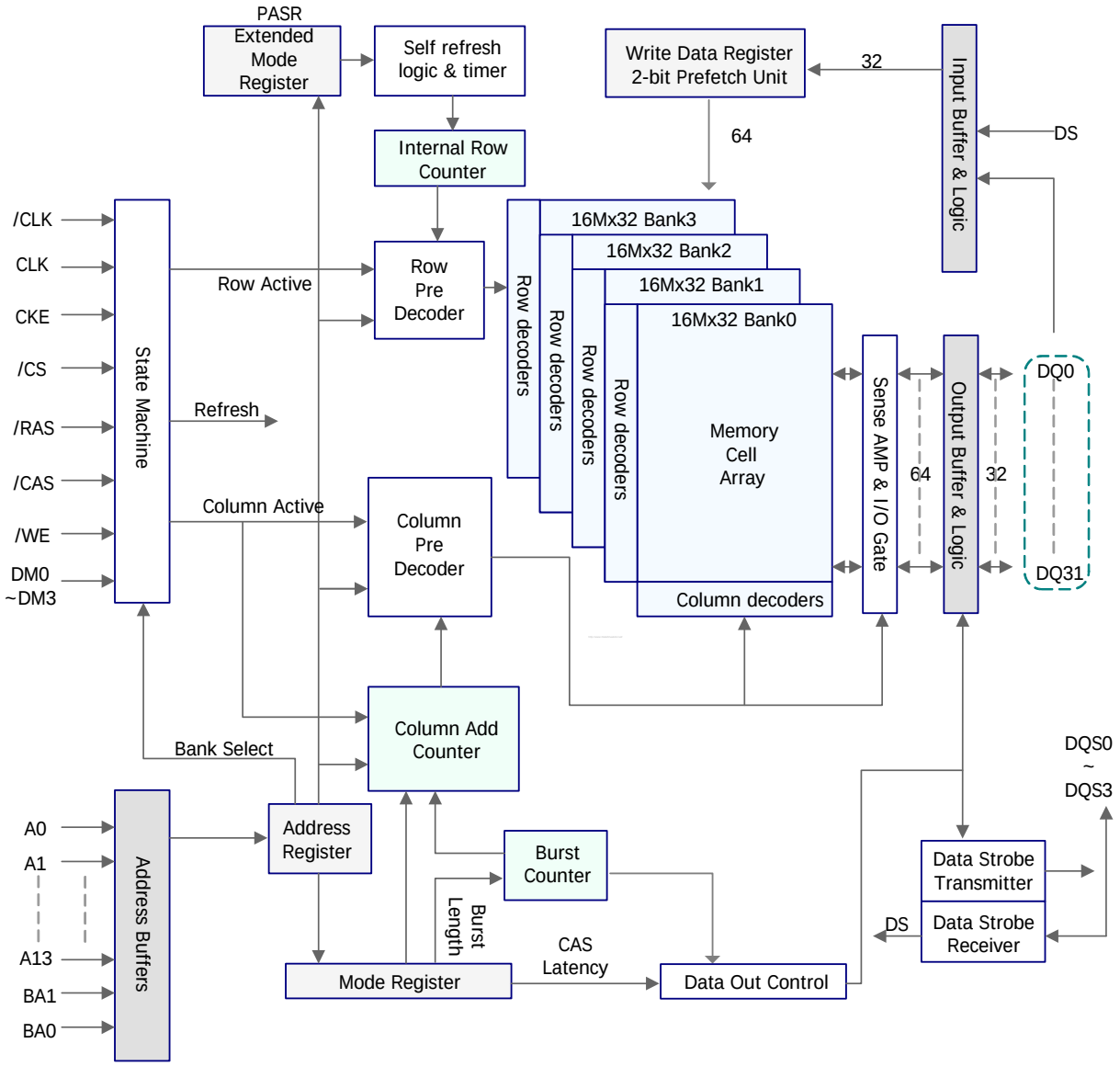
All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Mobile DDR SDRAM PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	INPUT	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	INPUT	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
$\overline{CS}$	INPUT	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered
BA0, BA1	INPUT	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS, EMRS).
A0 ~ A13	INPUT	Address inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. Row Address: A0 ~ A13 Column Address: A0 ~ A9 Auto-precharge flag: A10
DQ0 ~ DQ31	I/O	Data Bus: data input / output pin
DM0 ~ DM3	INPUT	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQS0 ~ DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
V_{DD}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground
V_{DDQ}	SUPPLY	I/O Power supply
V_{SSQ}	SUPPLY	I/O Ground
NC	-	No Connect: No internal electrical connection is present.

FUNCTIONAL BLOCK DIAGRAM

16Mbit x 4banks x 32 I/O Mobile DDR SDRAM



REGISTER DEFINITION I

Mode Register Set (MRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Length		

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

REGISTER DEFINITION II

Extended Mode Register Set (EMRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS			0	0	PASR		

DS (Drive Strength)

A7	A6	A5	Drive Strength
0	0	0	Full (Default)
0	0	1	Half
0	1	0	Quarter
0	1	1	Octant
1	0	0	Three-Quarters

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks (Default)
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

COMMAND TRUTH TABLE

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Autoprecharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Autoprecharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all Banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op code		10

DM TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:
1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with auto precharge disabled. This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among MRS, EMRS.
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH.

CKE TRUTH TABLE

CKEn-1	CKEn	Current State	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,8
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,9
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	H	See the other Truth Tables			

Note:
1. CKEn is the logic state of CKE at clock edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LP DDR immediately prior to clock edge *n*.
3. COMMAND*n* is the command registered at clock edge n, and ACTION*n* is the result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The clock must toggle at least one time during the t_{XP} period.
9. The clock must toggle at least once during the t_{XSR} time.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *n*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start read burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto recharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met.
   Once tRCD is met, the bank will be in the "row active" state.
   Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met.
   Once tRFC is met, the LP DDR will be in an "all banks idle" state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
   Once tMRD is met, the LP DDR will be in an "all banks idle" state.
   Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *m*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Pre-charging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Case Temperature	TC	-30 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.3 ~ VDDQ+0.3	V
Voltage on VDD relative to VSS	VDD	-0.3 ~ 2.7	V
Voltage on VDDQ relative to VSS	VDDQ	-0.3 ~ 2.7	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	0.7	W

AC and DC OPERATING CONDITIONS

OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.7	1.8	1.95	V	1
I/O Supply Voltage	VDDQ	1.7	1.8	1.95	V	1
Operating Case Temperature	TC	-30		85	°C	

CLOCK INPUTS (CK, $\overline{CK}$)

Parameter	Symbol	Min	Max	Unit	Note
DC Input Voltage	VIN	-0.3	VDDQ+0.3	V	
DC Input Differential Voltage	VID(DC)	0.4*VDDQ	VDDQ+0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6*VDDQ	VDDQ+0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4*VDDQ	0.6*VDDQ	V	3

Address And Command Inputs (A0~An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH	0.8*VDDQ	VDDQ+0.3	V	
Input Low Voltage	VIL	-0.3	0.2*VDDQ	V	

Data Inputs (DQ, DM, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Input High Voltage	VIHD(DC)	0.7*VDDQ	VDDQ+0.3	V	
DC Input Low Voltage	VILD(DC)	-0.3	0.3*VDDQ	V	
AC Input High Voltage	VIHD(AC)	0.8*VDDQ	VDDQ+0.3	V	
AC Input Low Voltage	VILD(AC)	-0.3	0.2*VDDQ	V	

Data Outputs (DQ, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9*VDDQ	-	V	
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1*VDDQ	V	

Leakage Current

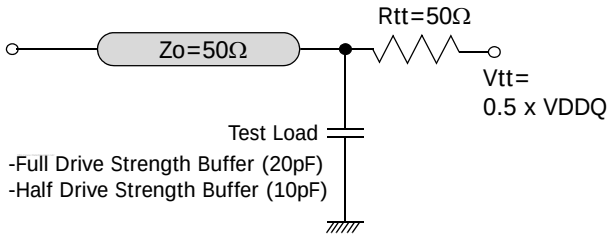
Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	4
Output Leakage Current	ILO	-1.5	1.5	uA	5

Note:
1. All voltages are referenced to VSS = 0V and VSSQ must be same potential and VDDQ must not exceed the level of VDD.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.
4. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.
5. DOUT is disabled. VOUT= 0 to 1.95V.

AC OPERATING TEST CONDITION

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.8*VDDQ/0.2*VDDQ	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note: 1. The circuit shown on the right represents the timing load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design and characterization. Use of IBIS or other simulation tools for system design validation is suggested.



Input / Output Capacitance

Parameter	Symbol	Speed		Unit	Note
		Min	Max		
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.5	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input/output capacitance, DQ, DM, DQS	CIO	2.0	4.5	pF	4

Note:
1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

Mobile DDR OUTPUT SLEW RATE CHARACTERRISTICS

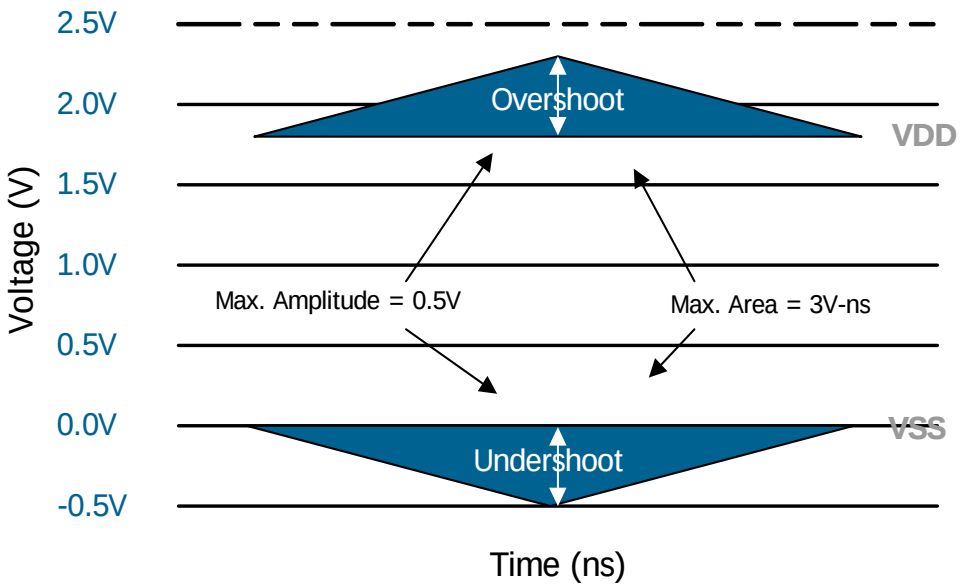
Parameter	Min	Max	Unit	Note
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1, 2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1, 2
Output Slew Rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

Note:
1. Measured with a test load of 20pF connected to VSSQ
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC)
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Mobile DDR AC OVERSHOOT / UNDERSHOOT SPECIFICATION

Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.5V
Maximum peak amplitude allowed for undershoot	0.5V
The area between overshoot signal and VDD must be less than or equal to	3V-ns
The area between undershoot signal and GND must be less than or equal to	3V-ns

Note:
1. This specification is intended for devices with no clamp protection and is guaranteed by design.



DC CHARACTERISTICS (Symbols)

Parameter	Symbol
Operating one bank active-precharge current	IDD0
Precharge power-down standby current	IDD2P
Precharge power-down standby current with clock stop	IDD2PS
Precharge non power-down standby current	IDD2N
Precharge non power-down standby current with clock stop	IDD2NS
Active power-down standby current	IDD3P
Active power-down standby current with clock stop	IDD3PS
Active non power-down standby current	IDD3N
Active non power-down standby current with clock stop	IDD3NS
Operating burst read current	IDD4R
Operating burst write current	IDD4W
Auto Refresh Current	IDD5
Self Refresh Current	IDD6

DC CHARACTERISTICS

Symbol	Test Condition	Max					Unit	Note
		DDR 400	DDR 370	DDR 333	DDR 266	DDR 200		
IDD0	tRC = tRC(min); tCK = tCK(min); CKE is HIGH; CS is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	75	70	65	60	55	mA	1
IDD2P	all banks idle; CKE is LOW; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	1.8					mA	
IDD2PS	all banks idle; CKE is LOW; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	1.8					mA	
IDD2N	all banks idle; CKE is HIGH; CS is HIGH, tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	7					mA	
IDD2NS	all banks idle; CKE is HIGH; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	5						
IDD3P	one bank active; CKE is LOW; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	5					mA	
IDD3PS	one bank active; CKE is LOW; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	4						
IDD3N	one bank active; CKE is HIGH; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	10					mA	
IDD3NS	one bank active; CKE is HIGH; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	8					mA	
IDD4R	one bank active; BL=4; CL=3; tCK=tCK(min); continuous read bursts; IOUT=0mA; address inputs are SWITCHING, 50% data change each burst transfer	100	95	90	80	70	mA	1
IDD4W	one bank active; BL=4; tCK=tCK(min); continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	90	85	80	70	60	mA	
IDD5	tRC=tRFC; tCK=tCK(min); burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	150					mA	tRFC= 138ns
IDD6	CKE is LOW; CK=LOW; CK=HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	See Next Page					uA	2

Note:
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is 1V/ns
3. Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$
   STABLE is defined as inputs stable at a HIGH or LOW level
   SWITCHING is defined as
   - address and command: inputs changing between HIGH and LOW once per two clock cycles
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle
     DM and DQS are STABLE
4. All IDD values are guaranteed by full range of operating voltage and temperature.
   VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30°C ~ +85°C

DC CHARACTERISTICS - IDD6

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
45	1800	1600	1400	uA
85	4000	2800	2400	uA

Note:
1. Related numerical values in this 45°C are examples for reference sample value only.
2. With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.

AC CHARACTERISTICS (Symbols - Sheet 1 of 2)

Parameter		Symbol	Unit
DQ Output Access Time (from CK, $\overline{CK}$)		tAC	ns
DQS Output Access Time (from CK, $\overline{CK}$)		tDQSCK	ns
Clock High-level Width		tCH	tCK
Clock Low-level Width		tCL	tCK
Clock Half Period		tHP	ns
System Clock Cycle Time	CL = 3	tCK3	ns
	CL = 2	tCK2	ns
DQ and DM Input Setup Time		tDS	ns
DQ and DM Input Hold Time		tDH	ns
DQ and DM Input Pulse Width		tDIPW	ns
Address and Control Input Setup Time		tIS	ns
Address and Control Input Hold Time		tIH	ns
Address and Control Input Pulse Width		tIPW	ns
DQ & DQS Low-impedance time from CK, $\overline{CK}$		tLZ	ns
DQ & DQS High-impedance time from CK, $\overline{CK}$		tHZ	ns
DQS - DQ Skew		tDQSQ	ns
DQ / DQS output hold time from DQS		tQH	ns
Data Hold Skew Factor		tQHS	ns
Write Command to 1st DQS Latching Transition		tDQSS	tCK
DQS Input High-Level Width		tDQSH	tCK
DQS Input Low-Level Width		tDQSL	tCK
DQS Falling Edge of CK Setup Time		tDSS	tCK
DQS Falling Edge Hold Time from CK		tDSH	tCK

AC CHARACTERISTICS (Symbols - Sheet 2 of 2)

Parameter		Symbol	Unit
MODE REGISTER SET Command Period		tMRD	tCK
Write Preamble Setup Time		tWPRES	ns
Write Postamble		tWPST	tCK
Write Preamble		tWPRE	tCK
Read Preamble	CL = 3	tRPRE3	tCK
	CL = 2	tRPRE2	tCK
Read Postamble		tRPST	tCK
ACTIVE to PRECHARGE Command Period		tRAS	ns
ACTIVE to ACTIVE Command Period		tRC	ns
AUTO REFRESH to ACTIVE/AUTO REFRESH Command Period		tRFC	ns
ACTIVE to READ or WRITE Delay		tRCD	ns
PRECHARGE Command Period		tRP	ns
ACTIVE Bank *A* to ACTIVE Bank *B* Delay		tRRD	ns
WRITE Recovery Time		tWR	ns
Auto Precharge Write Recovery + Precharge Time		tDAL	tCK
Internal Write to Read Command Delay		tWTR	tCK
Self Refresh Exit to next valid Command Delay		tXSR	ns
Exit Power Down to next valid Command Delay		tXP	ns
CKE *min.* Pulse Width (High and Low)		tCKE	tCK
Average Periodic Refresh Interval		tREFI	us
Refresh Period		tREF	ms

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 1 of 2)

Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tAC	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tDQSCK	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tHP	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	ns	1,2
tCK3	5	-	5.4	-	6.0	-	7.5	-	10	-	ns	3
tCK2	12		12		12		12	-	15	-	ns	
tDS	0.48		0.54		0.6		0.8		1.1		ns	4,5,6
tDH	0.48		0.54		0.6		0.8		1.1		ns	4,5,6
tDIPW	1.8	-	1.8	-	1.8	-	1.8	-	2.2	-	ns	7
tIS	0.9		1.0		1.1		1.3		1.5		ns	6,8,9
tIH	0.9		1.0		1.1		1.3		1.5		ns	6,8,9
tIPW	2.3	-	2.3	-	2.3	-	2.6	-	3.0	-	ns	7
tLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	10
tHZ		5.0		5.0		5.0		6.0		7.0	ns	10
tDQSQ		0.4		0.45		0.5		0.6		0.7	ns	11
tQH	tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		ns	2
tQHS		0.5		0.5		0.65		0.75		1.0	ns	2
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
tDQSH	0.4		0.4		0.4		0.4		0.4		tCK	
tDQSL	0.4		0.4		0.4		0.4		0.4		tCK	
tDSS	0.2		0.2		0.2		0.2		0.2		tCK	
tDSH	0.2		0.2		0.2		0.2		0.2		tCK	

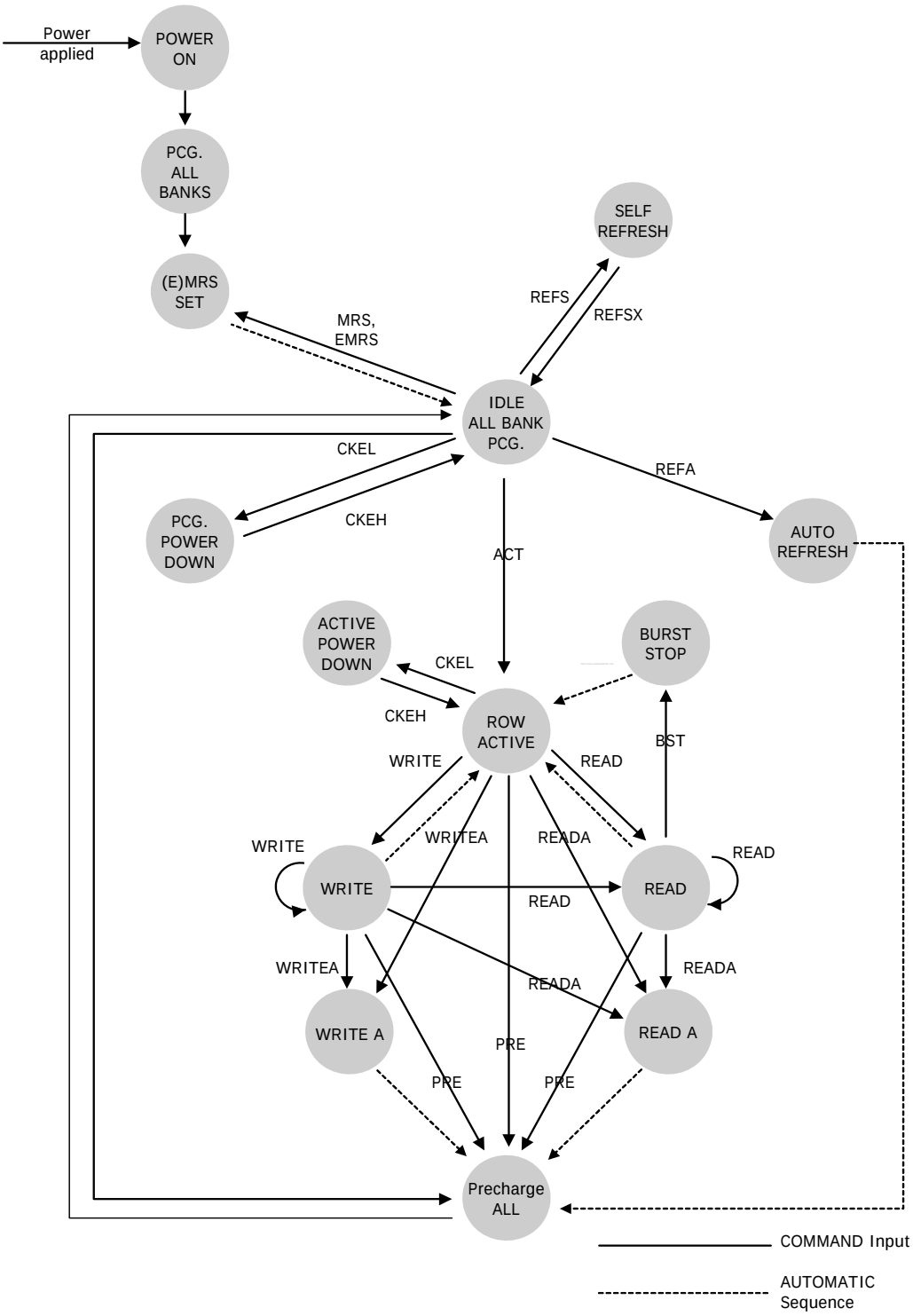
AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 2 of 2)

Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
tWPRES	0	-	0	-	0	-	0	-	0	-	ns	12
tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	13
tWPRE	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
tRPRE3	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	14
tRPRE2	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	tCK	14
tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRAS	40	70,000	42	70,000	42	70,000	45	70,000	50	70,000	ns	
tRC	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	ns	
tRFC	90	-	90	-	90	-	90	-	90	-	ns	
tRCD	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRP	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRRD	10	-	10.8	-	12	-	15	-	15	-	ns	
tWR	15	-	15	-	15	-	15	-	15	-	ns	
tDAL	(tWR/tCK) + (tRP/tCK)										tCK	16
tWTR	2	-	2	-	1	-	1	-	1	-	tCK	
tXSR	140	-	140	-	140	-	140	-	140	-	ns	
tXP	1CLK	-	1CLK	-	1CLK	-	1CLK	-	1CLK	-	ns	19
tCKE	1	-	1	-	1	-	1	-	1	-	tCK	
tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	17
tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note:

1. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH})
2. t_{QH} = t_{HP} - t_{QHS}, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
4. The transition time for DQ, DM and DQS inputs is measured between V_{IL}(DC) to V_{IH}(AC) for rising input signals, and V_{IH}(DC) to V_{IL}(AC) for falling input signals.
5. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
6. Input slew rate ≥ 1.0 V/ns.
7. These parameters guarantee device timing but they are not necessarily tested on each device.
8. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
9. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
10. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
11. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
15. Speed bin (CL-t_{RCD}-t_{RP}) = 3-3-3 for DDR400, DDR200, DDR266, DDR333 and DDR 370
16. In case of above 33MHz (tCK=30ns) condition, tDAL should be minimum of 3*tCK.
    tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms above, if not already an integer, round to the next higher integer.
17. A maximum of eight Refresh commands can be posted to any given Low Power DDR SDRAM (Mobile DDR SDRAM), meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*t_{REFI}.
18. All AC parameters are guaranteed by full range of operating voltage and temperature.
    VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30^{o}C ~ 85^{o}C
19. There must be at least one clock pulse during the tXP period. Please refer to the 'Power Down Mode' Section

Mobile DDR SDRAM OPERATION



ACT :
Active

BST :
Burst

CKEL :
Enter Power-Down

CKEH :
Exit Power-Down

EMRS :
Ext. Mode Reg. Set

MRS :
Mode Register Set

PRE :
Precharge

PREALL :
Precharge All Banks

REFA :
Auto Refresh

REFS :
Enter Self Refresh

REFSX :
Exit Self Refresh

READ :
Read w/o Auto Precharge

READA :
Read with Auto Precharge

WRITE :
Write w/o Auto Precharge

WRITEA :
Write with Auto Precharge

DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

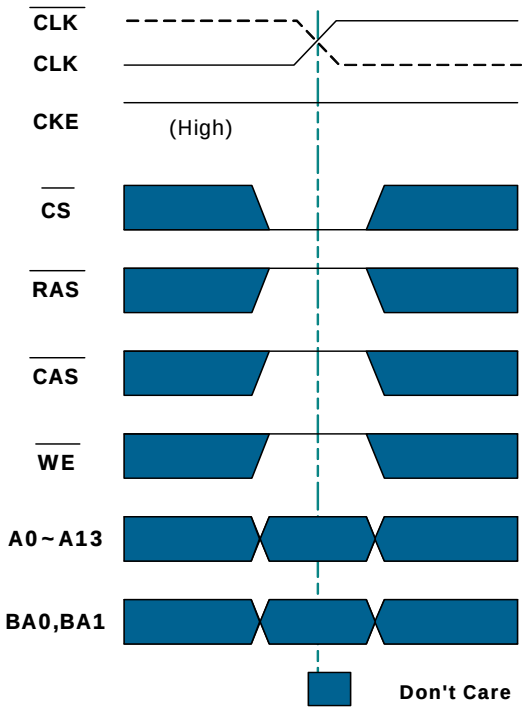
NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a Mobile DDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

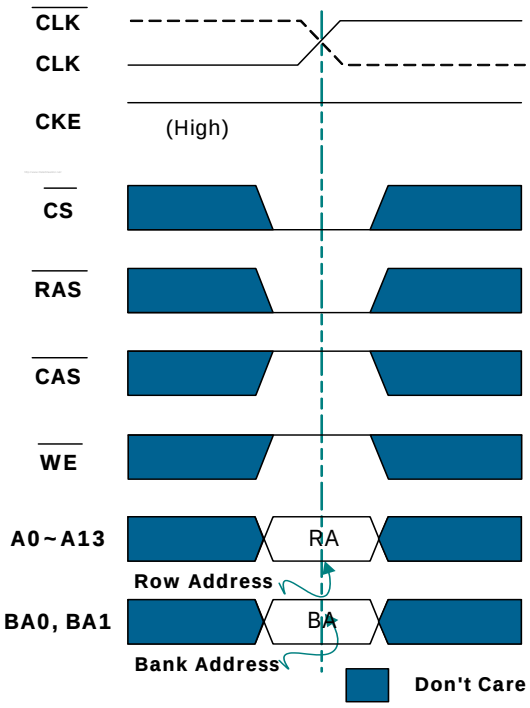
ACTIVE

The Active command is used to activate a row in a particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A13 selects the row. (see to next figure)

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.
The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.
A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.



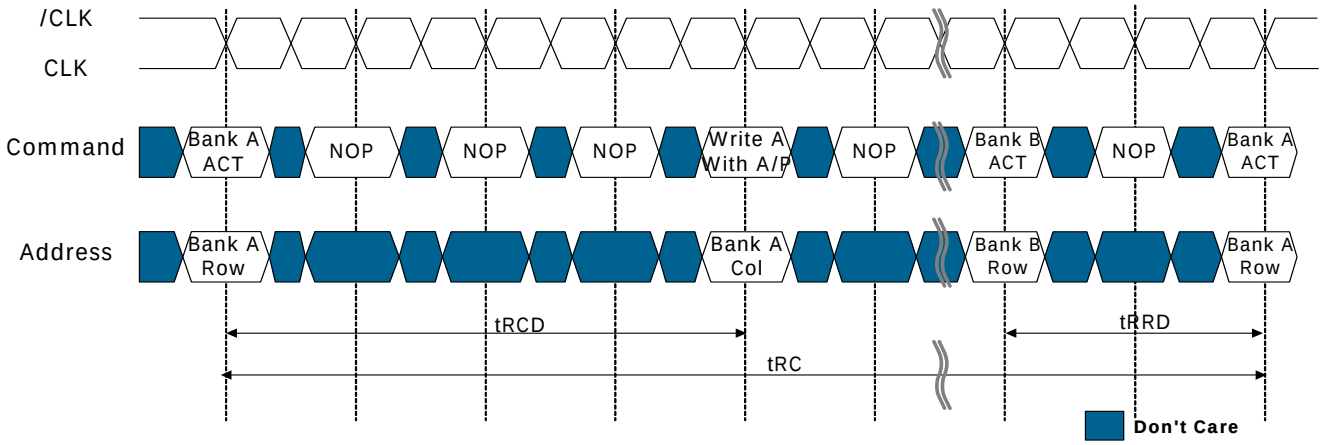
NOP Command



ACTIVE Command

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (*MIN*) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

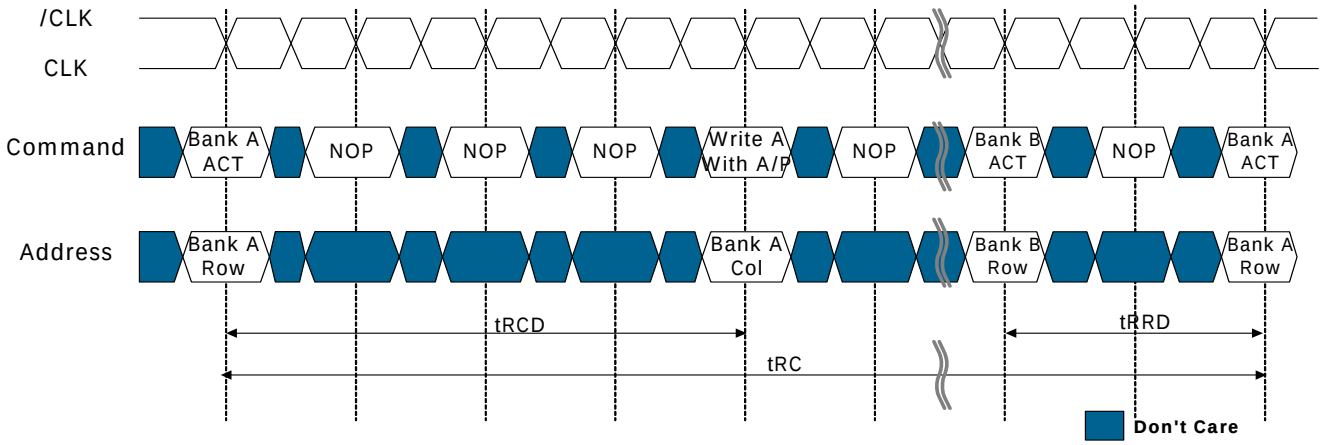
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.



Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (*MIN*) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

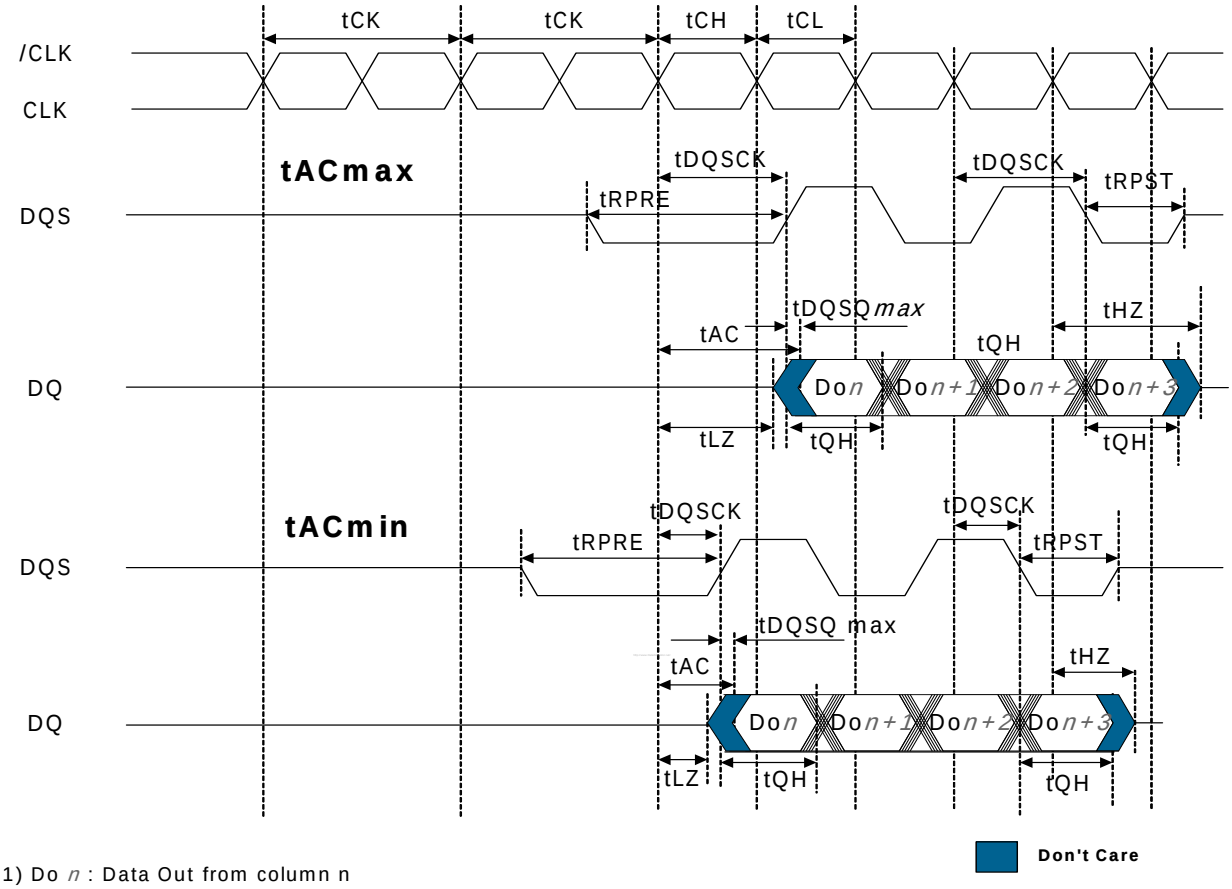
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.



Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

READ

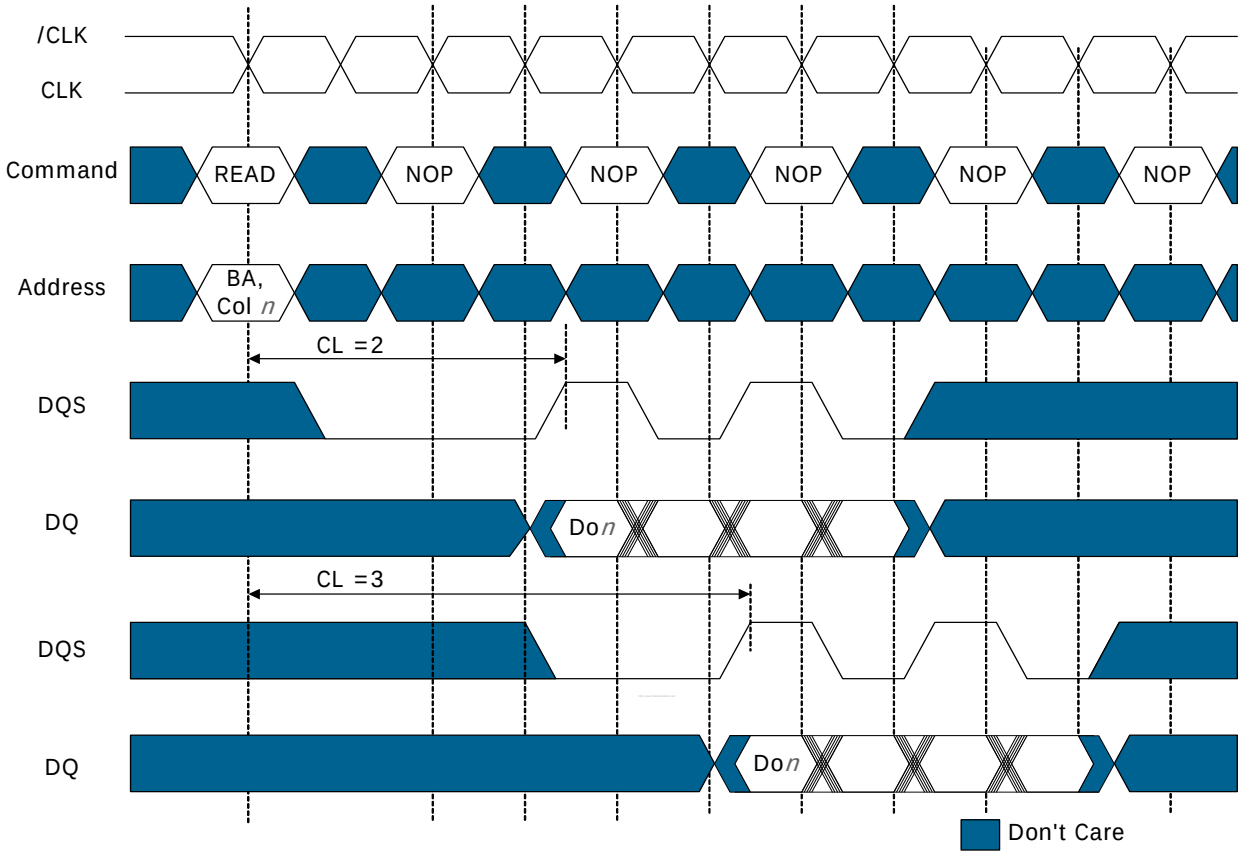
The basic Read timing parameters for DQ are shown next figure (Basic Read Timing Parameters). They apply to all Read operations. During Read bursts, DQS is driven by the Mobile DDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble.



1) Do *n* : Data Out from column n
2) All DQ are vaild tAC after the CK edge
   All DQ are vaild tDQSQ after the DQS edge, regardless of tAC

Basic Read Timing Parameters

The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in next figure with a CAS latency of 2 and 3.
Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

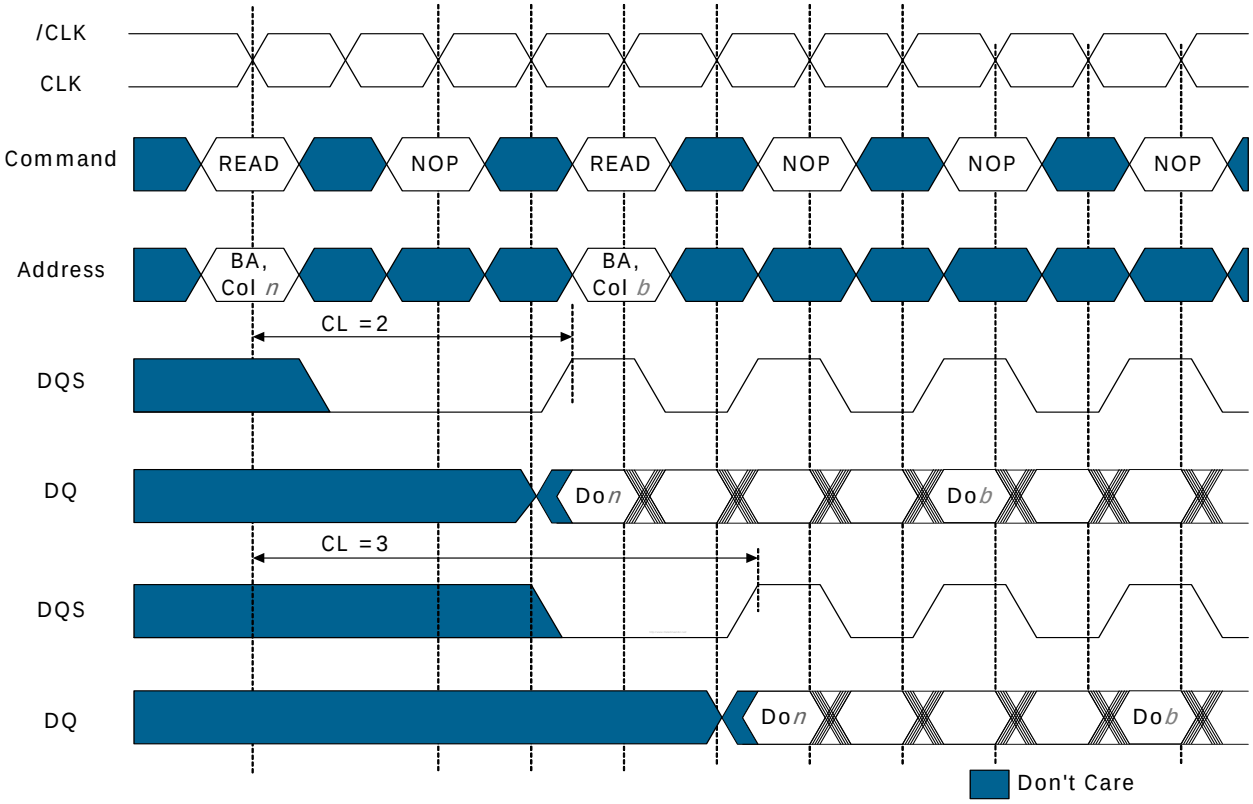


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 4; 3 subseqnent elements of Data Out appear in the programmed order following Do *n*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Read Burst Showing CAS Latency

READ to READ

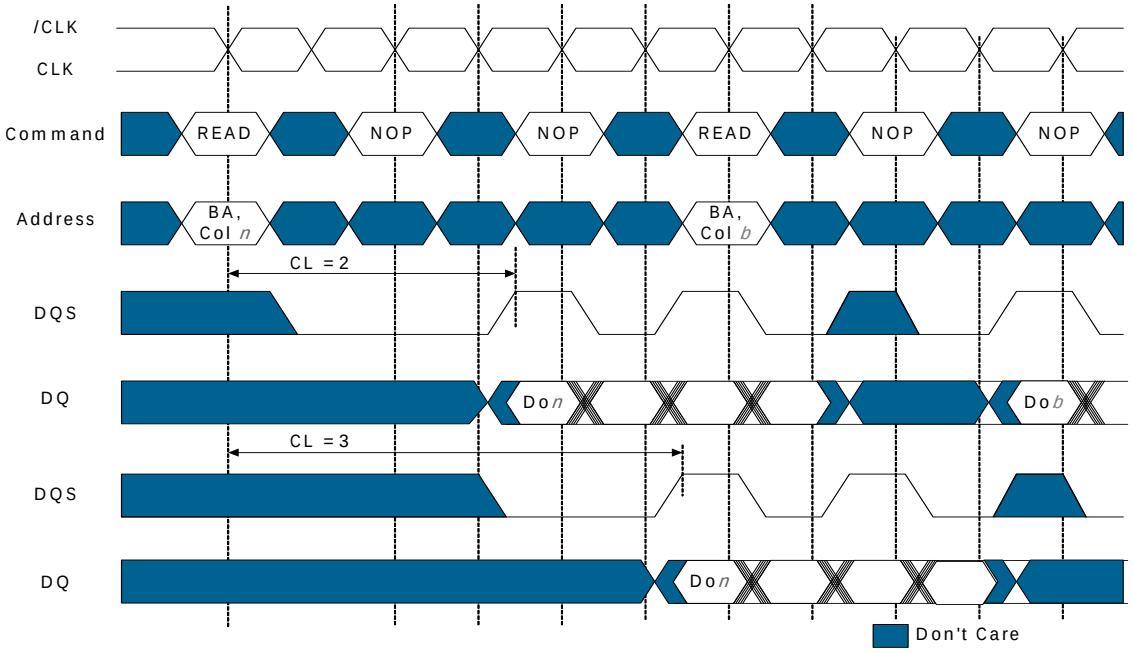
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
4) Read bursts are to an active row in any bank
5) Shown with nominal tAC, tDQSCK and tDQSQ

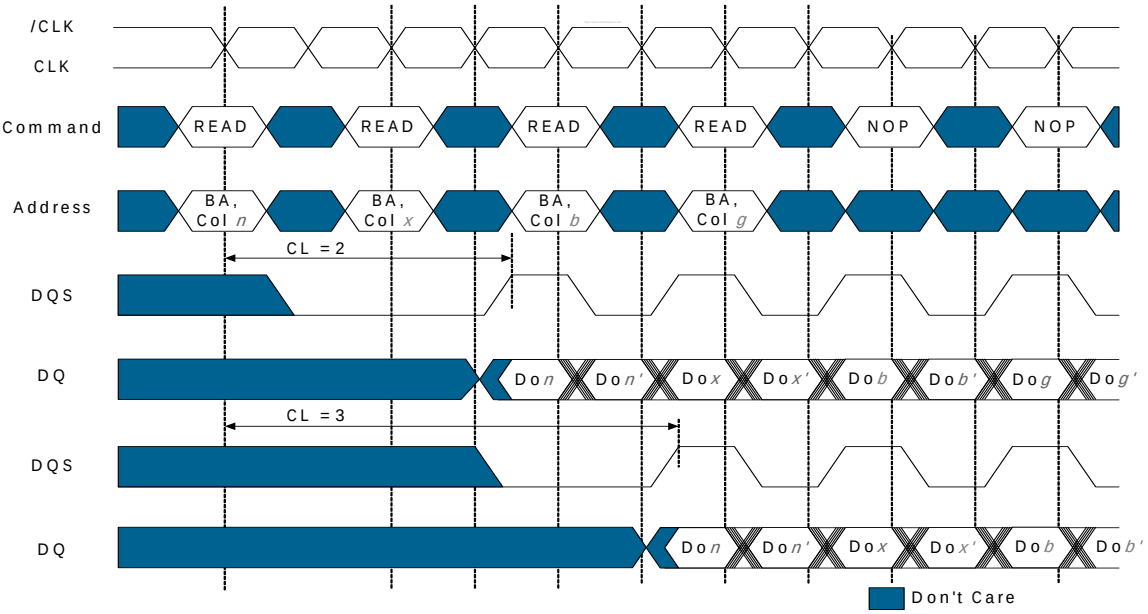
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in the first figure of next page. Random read accesses within a page or pages can be performed as shown in second figure of next page.



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n* (*b*) = Bank A, Column n (b)
3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following Do *n* (*b*)
4) Shown with nominal tAC, tDQSCK and tDQSQ

Non-Consecutive Read Bursts

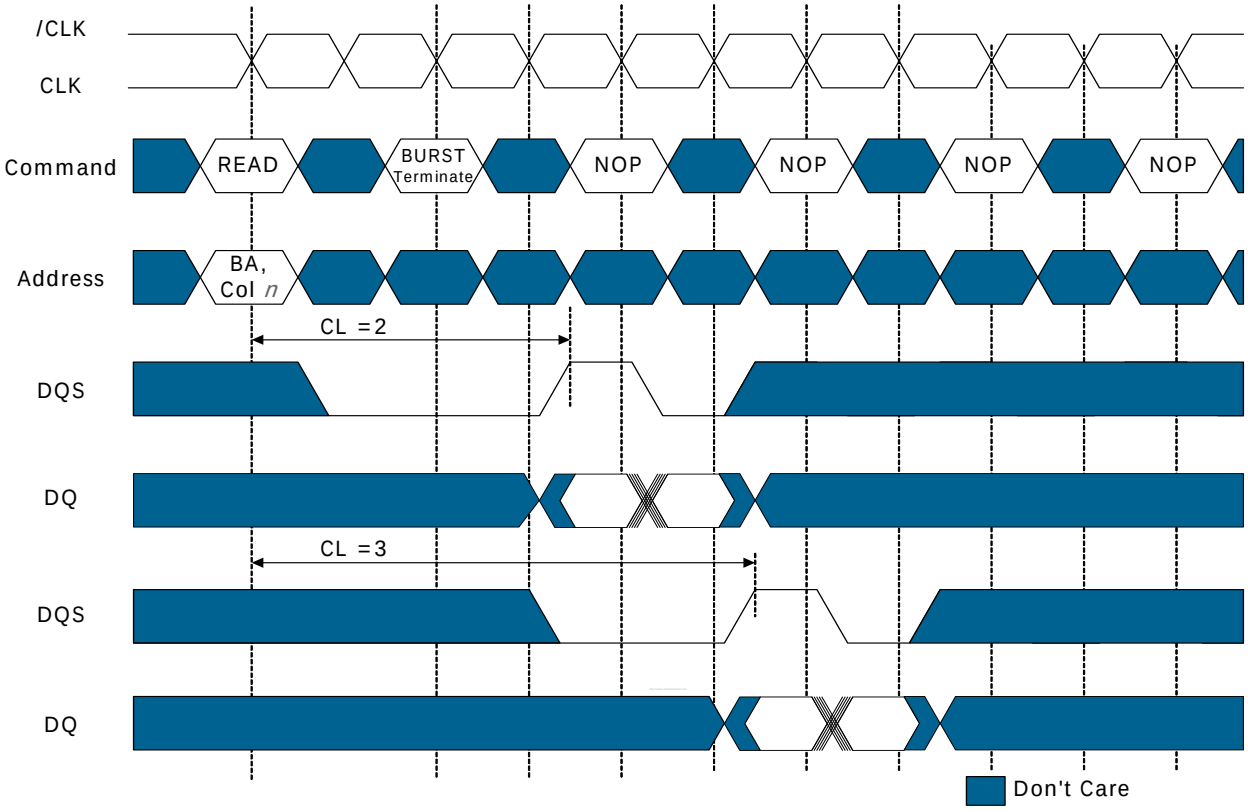


1) Do*n*, etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 2, 4 or 8 in cases shown (if burst of 4 or 8, the burst is interrupted)
4) Read are to active rows in any banks

Random Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

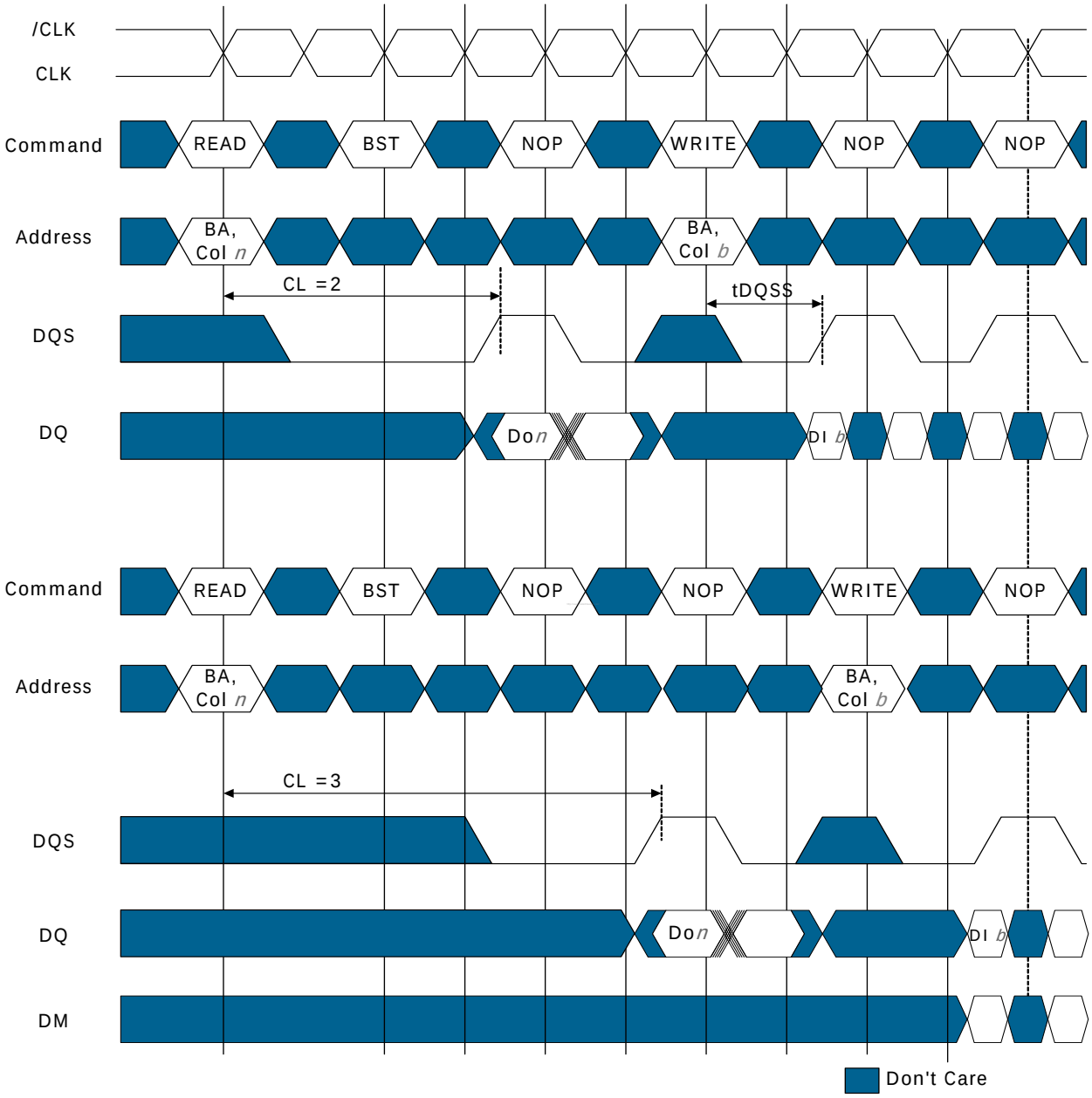


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Cases shown are bursts of 4 or 8 terminated after 2 data elements
4) Shown with nominal tAC, tDQSCK and tDQSQ

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig. for the case of nominal tDQSS.

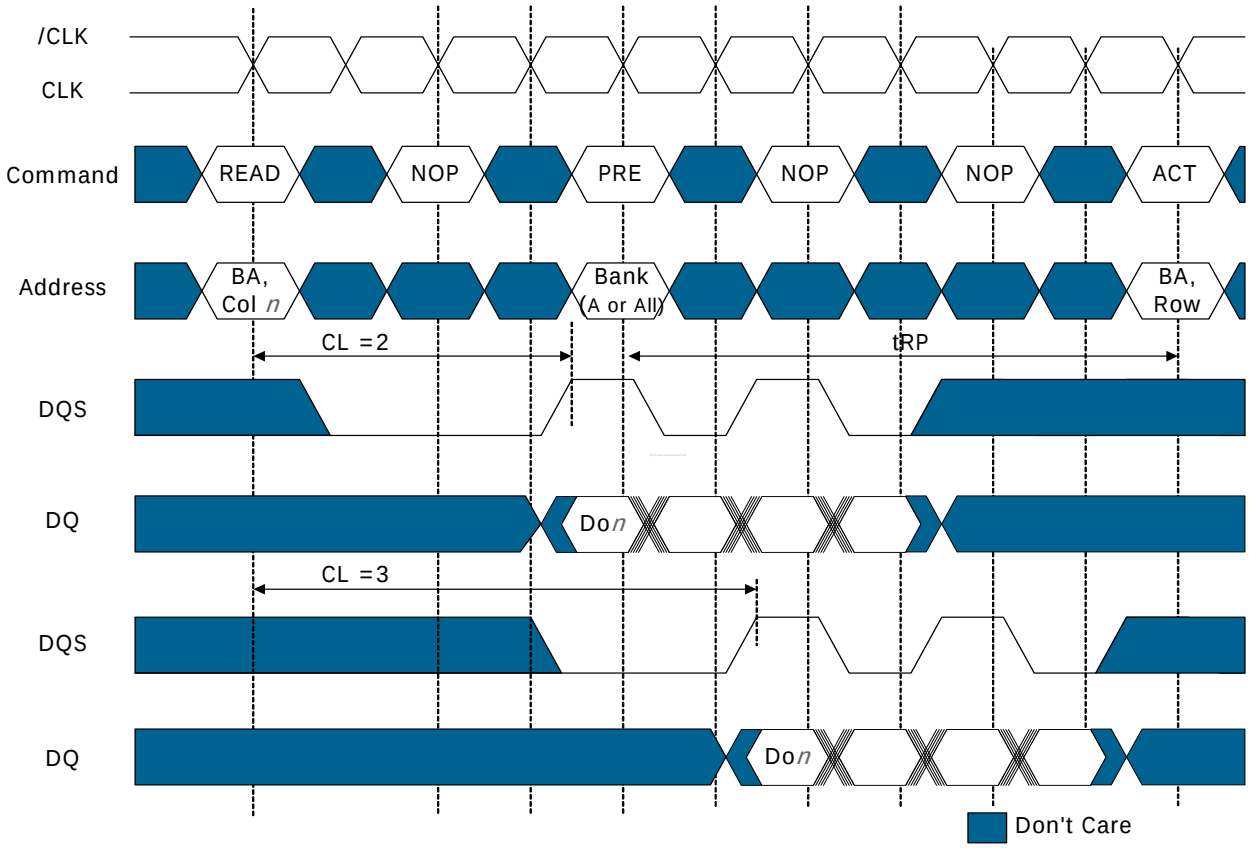


1) DO *n* = Data Out from column n; DI b = Data In to column b
2) Burst length = 4 or 8 in the cases shown; if the burst length is 2, the BST command can be ommitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

Read to Write

READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.
Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled.
The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

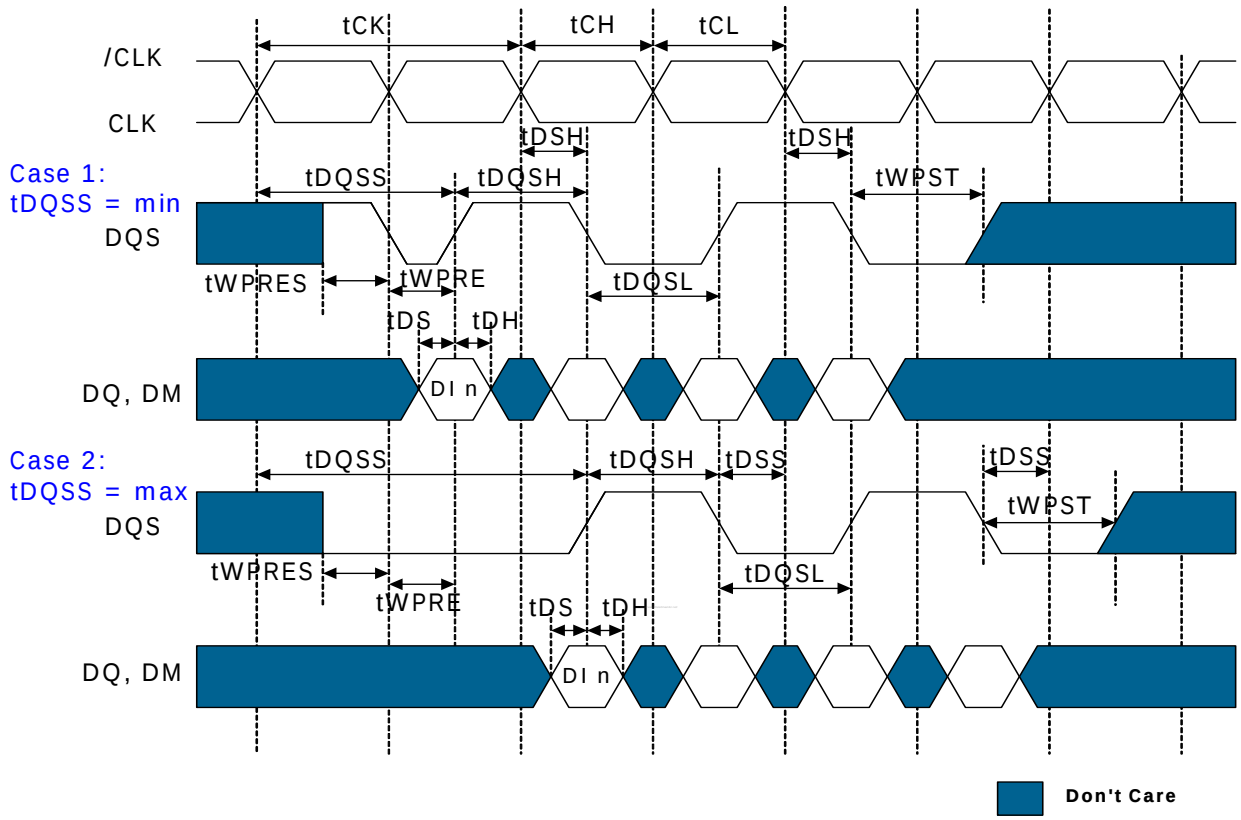


1) DO *n* = Data Out from column n
2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8
3) Shown with nominal tAC, tDQSCK and tDQSQ
4) Precharge may be applied at (BL / 2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

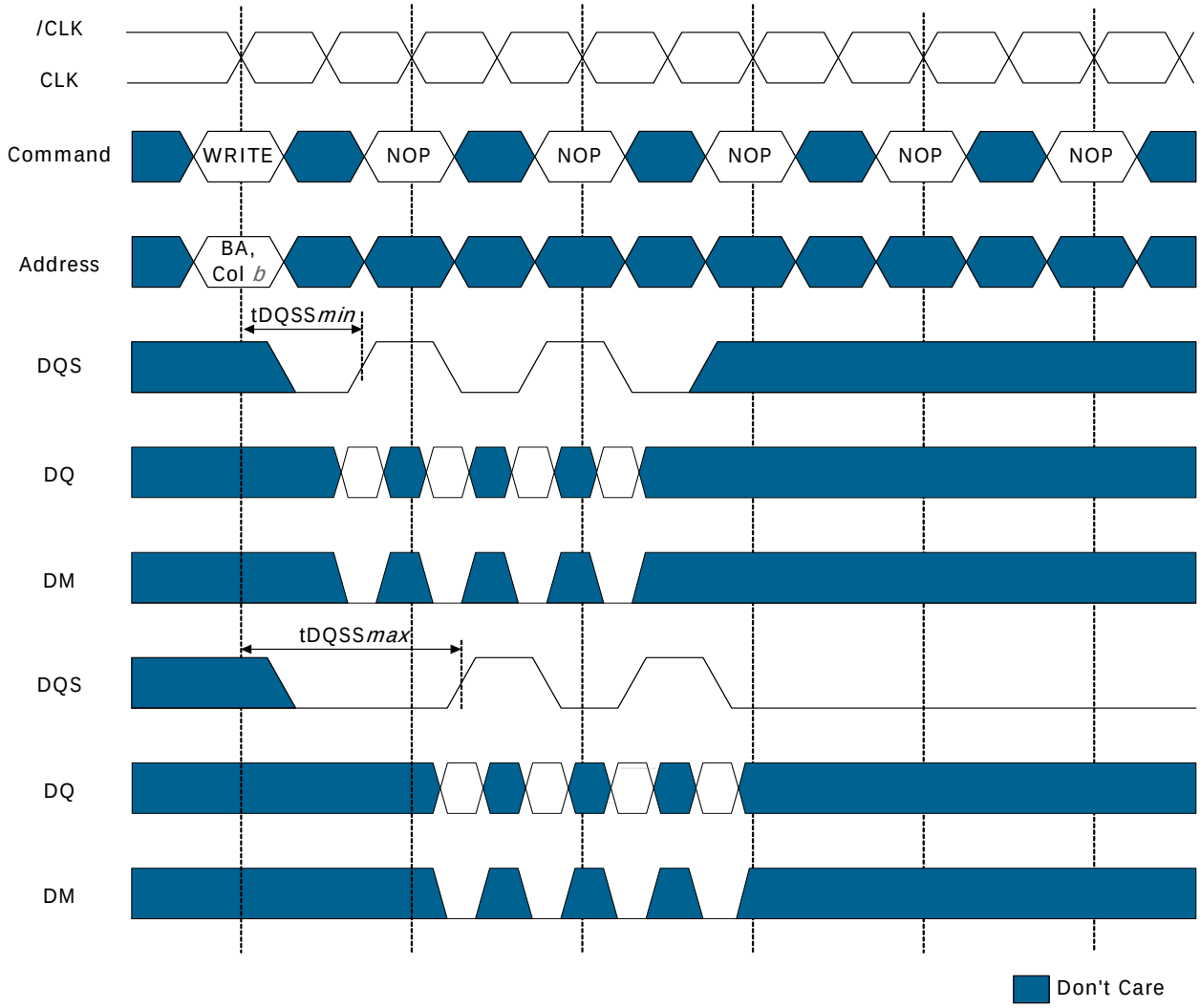
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
Basic Write timing parameters for DQ are shown in Figure; they apply to all Write operations.



1) DI n: Data in for column n
2) 3 subsequent elements of Data in are applied in the programmed order following DI n
3) tDQSS : each rising edge of DQS must fall within the +/-25 (percentage) window of the corresponding positive clock edge

Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.
The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Next fig. shows the two extremes of t_{DQSS} for a burst of 4.
Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain high-Z and any additional input data will be ignored.

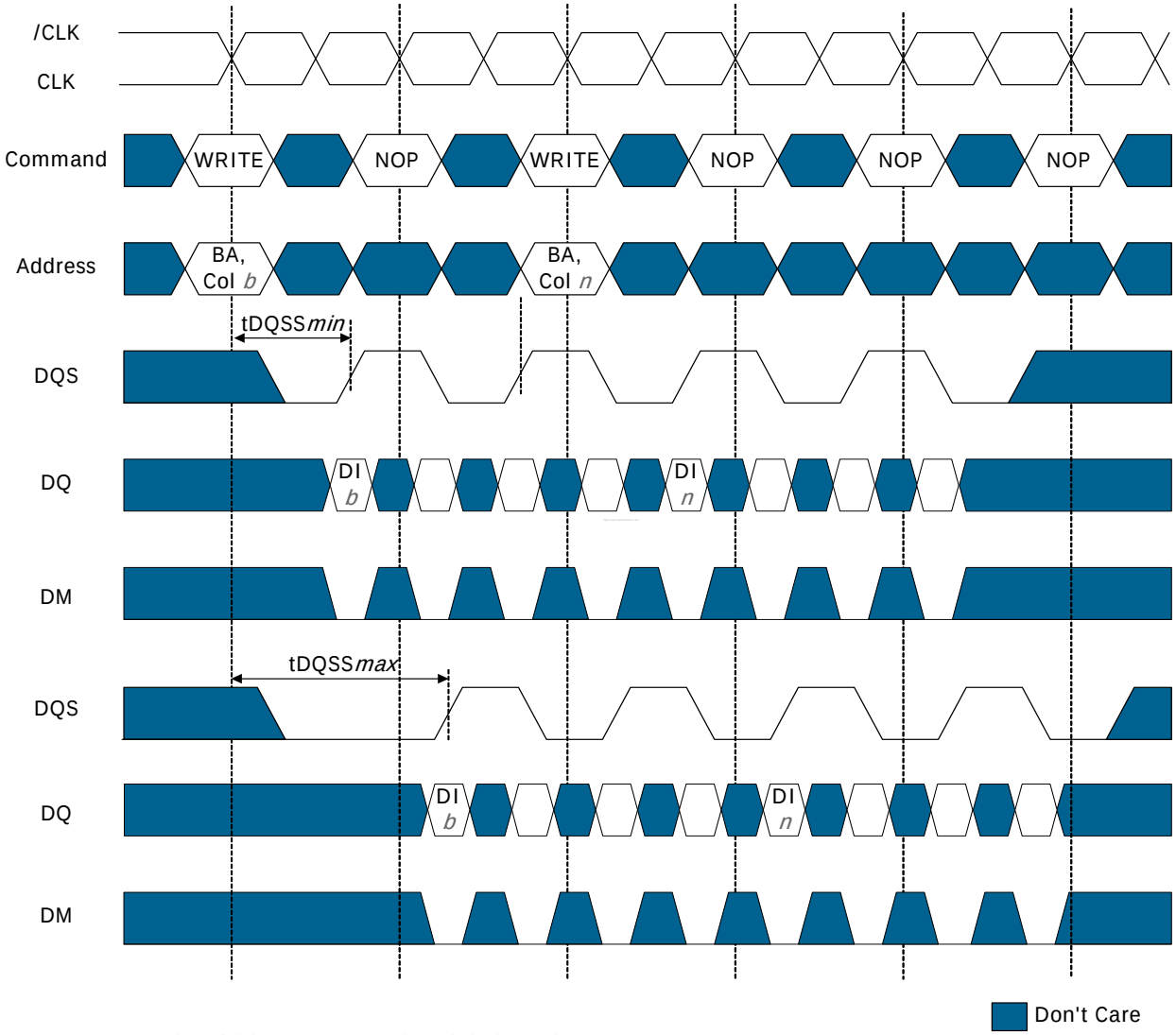


1) DI b = Data In to column b
2) 3 subsequent elements of Data In are applied in the programmed order following DI b
3) A non-interrupted burst of 4 is shown
4) A10 is low with the WRITE command (Auto Precharge is disabled)

Write Burst (min. and max. tDQSS)

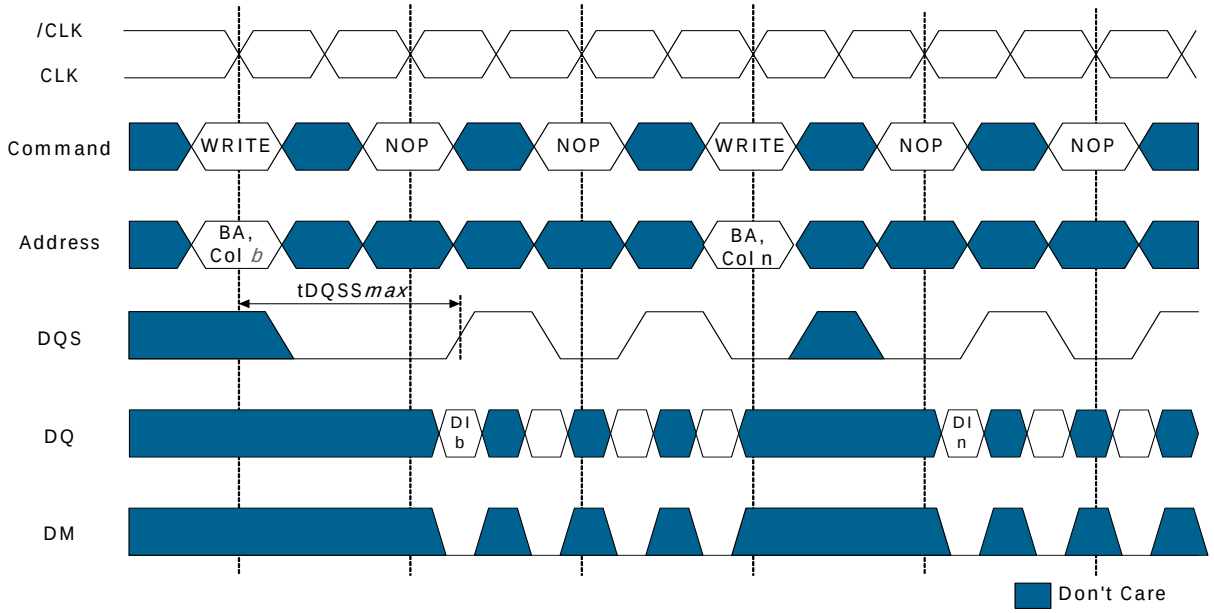
WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.



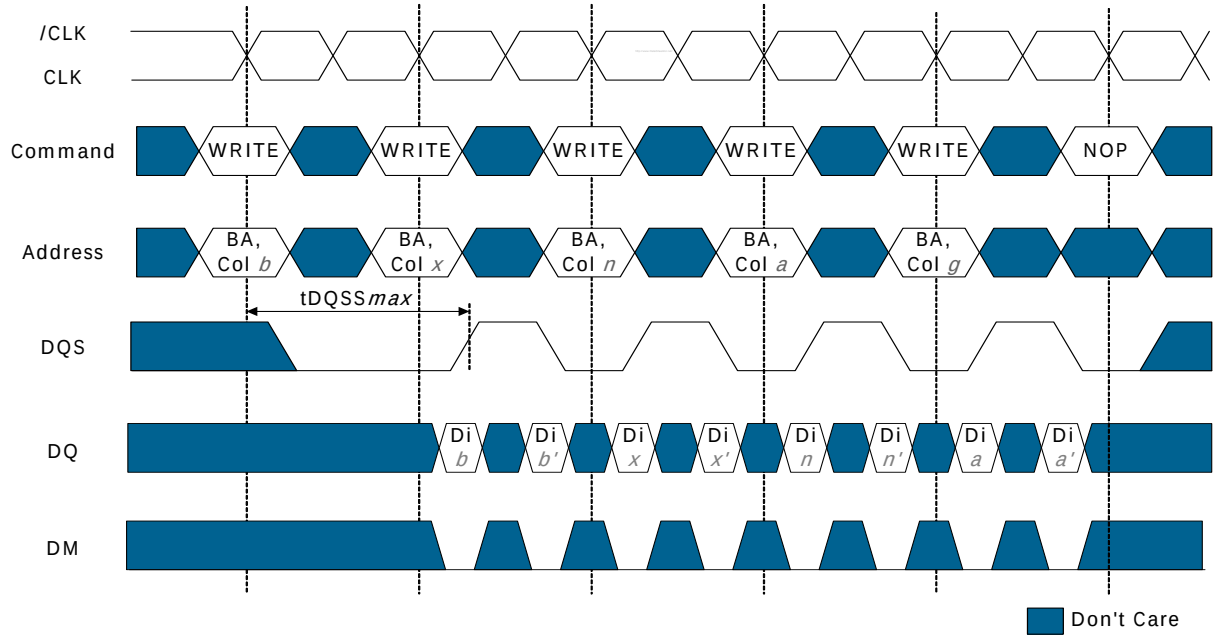
1) DI *b* (*n*) = Data In to column b (column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
   3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

Concatenated Write Bursts



1) DI *b* (*n*) = Data In to column b (or column n).
2) 3 subsequent elements of Data In are applied in the programmed order following DI *b*.
   3 subsequent elements of Data In are applied in the programmed order following DI *n*.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

Non-Concatenated Write Bursts

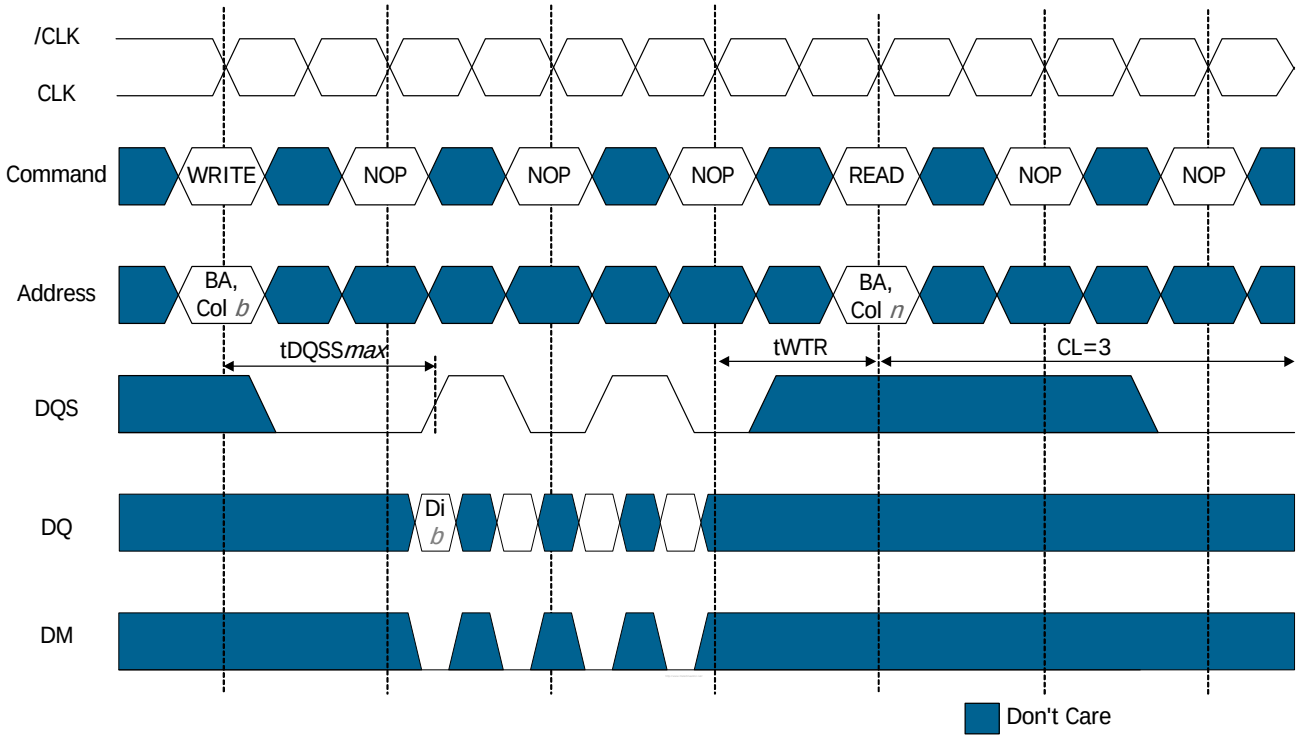


1) DI b etc. = Data In to column b, etc.
   ; b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4 or 8 in cases shown. If burst of 4 or 8, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

Random Write Cycles

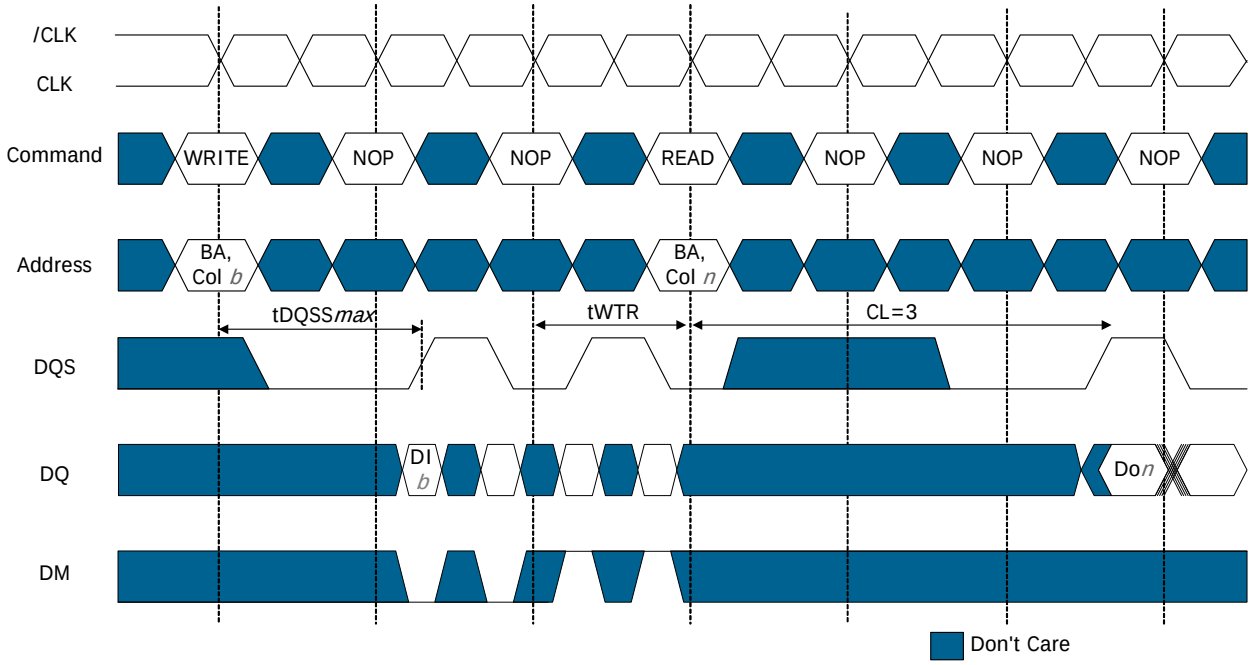
WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Figure.



1) DI *b* = Data In to column b . 3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

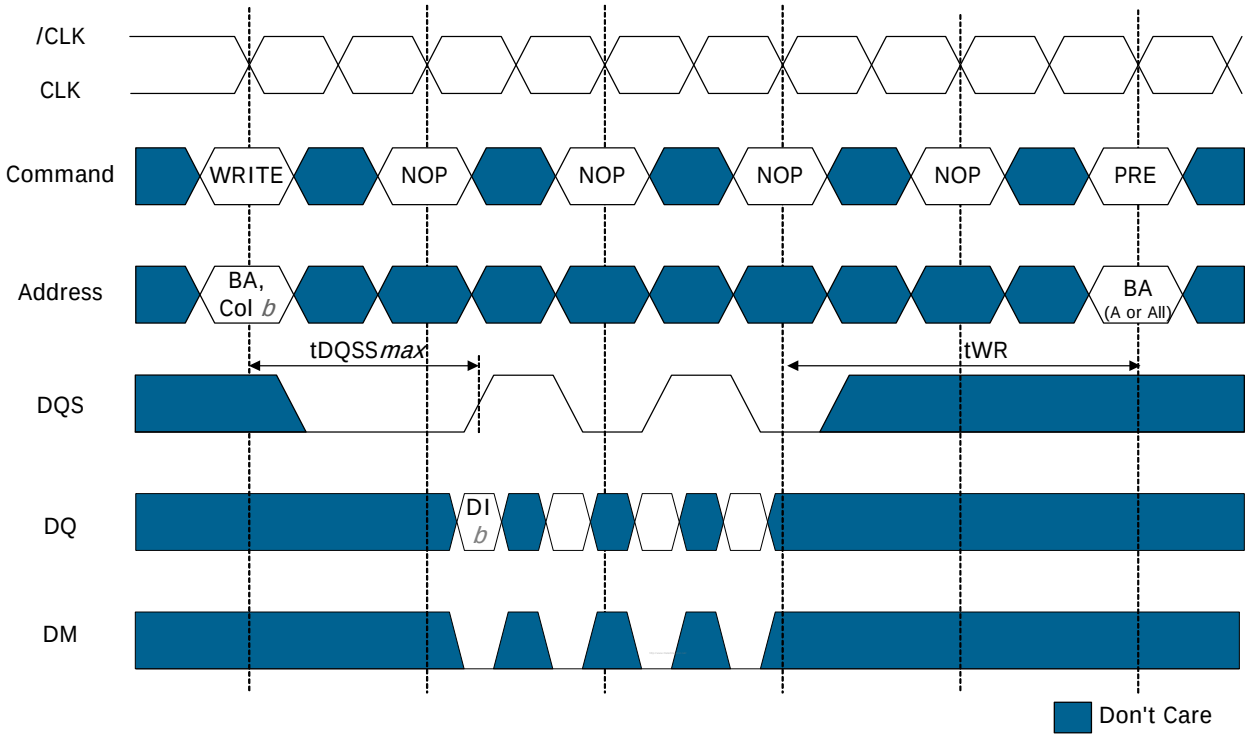


1) DI *b* = Data In to column b. DO *n* = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Interrupting Write to Read

WRITE to PRECHARGE

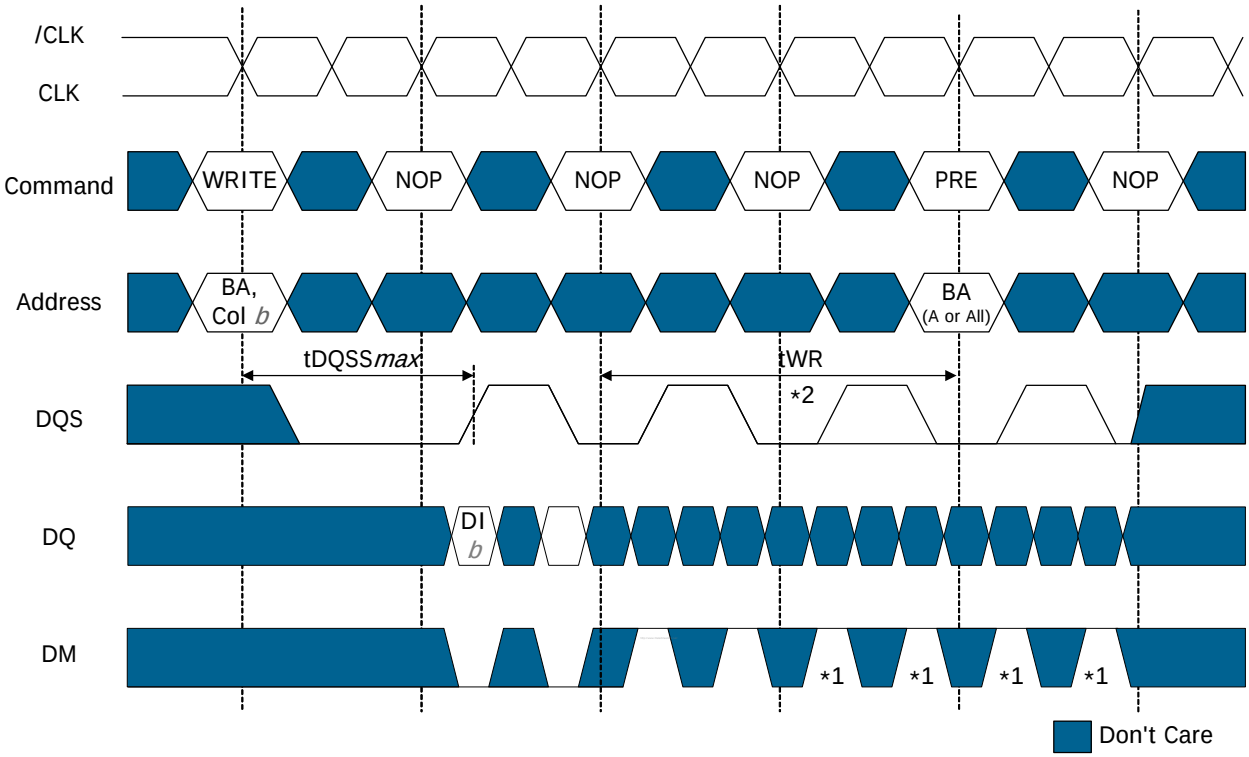
Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in Fig.



1) DI b (n) = Data In to column b (column n)
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted bursts of 4 are shown.
3) tWR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Non-Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

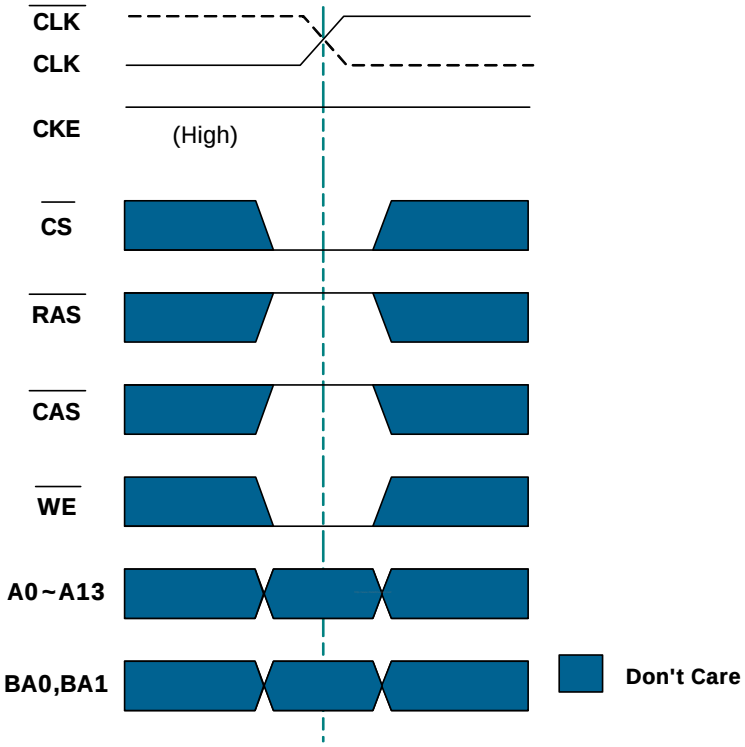


1) DI b = Data In to column b .
2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
3) tWR is referenced from the positive clock edge after the last desired Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) *1 = can be Don't Care for programmed burst length of 4
6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Interrupting Write to Precharge

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

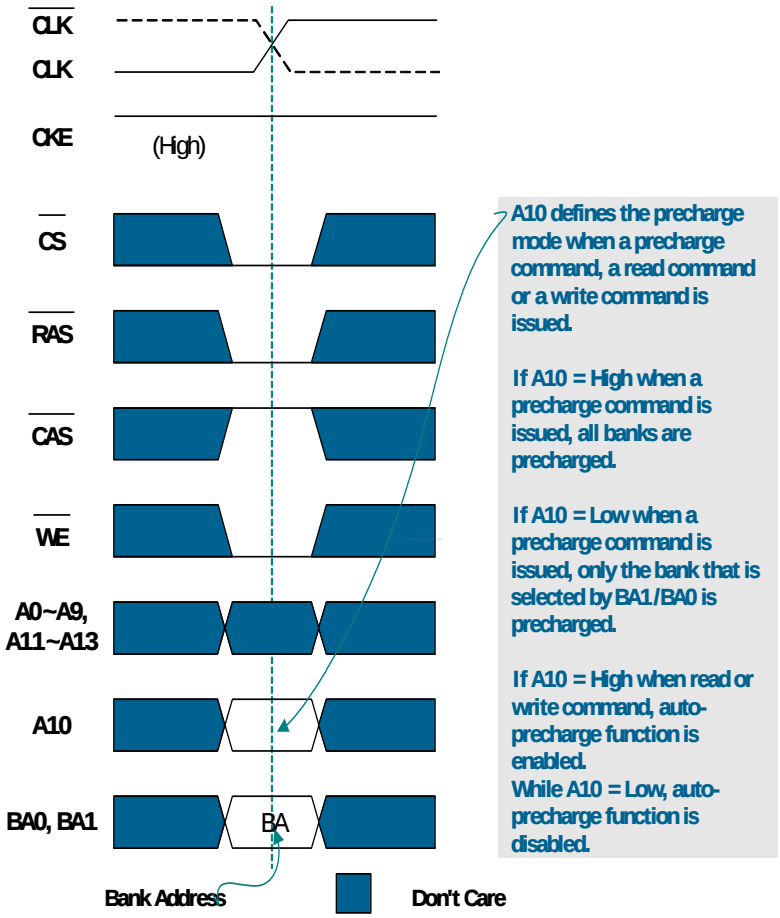


BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

Mobile DDR devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

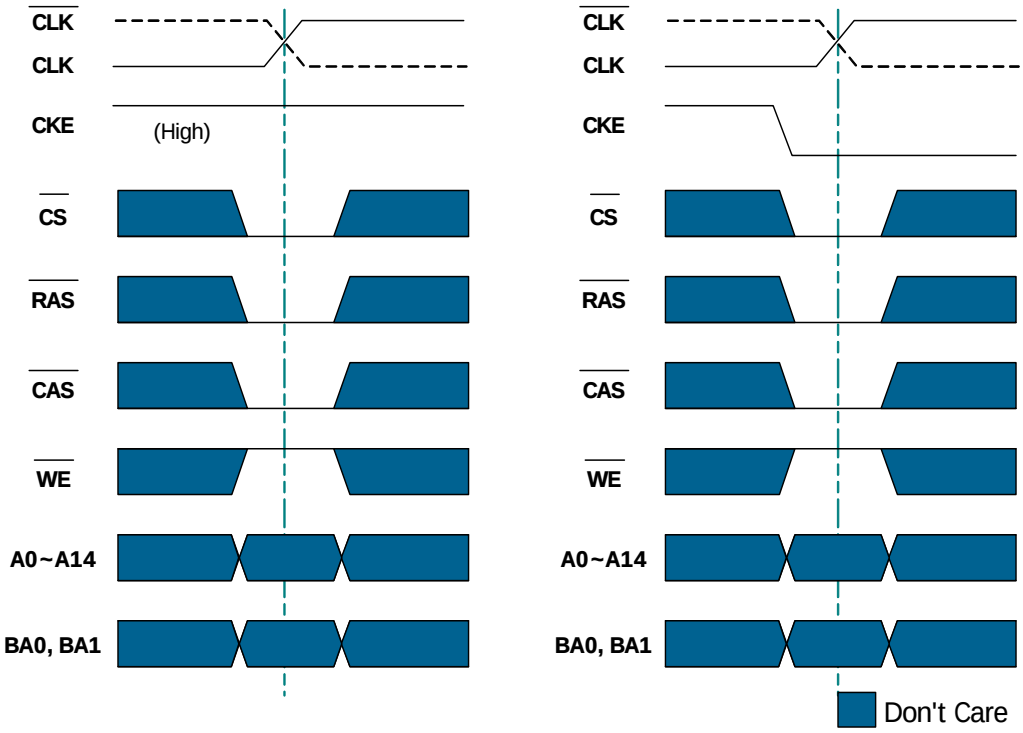
- AUTO REFRESH.

This command is used during normal operation of the Mobile DDR. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Mobile DDR requires AUTO REFRESH commands at an average periodic interval of tREFI.
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile DDR, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

-SELF REFRESH.

This state retains data in the Mobile DDR, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile DDR and may vary and may not meet tREFI time.
"Don't Care" except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high. NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress.
The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.
The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). The Mobile DDR can accomplish an special Self Refresh operation by the specific modes (PASR) programmed in extended mode registers. The Mobile DDR can control the refresh rate automatically by the temperature value of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR (Partial Array Self Refresh). The Mobile DDR can reduce the self refresh current(IDD6) by using these two modes.

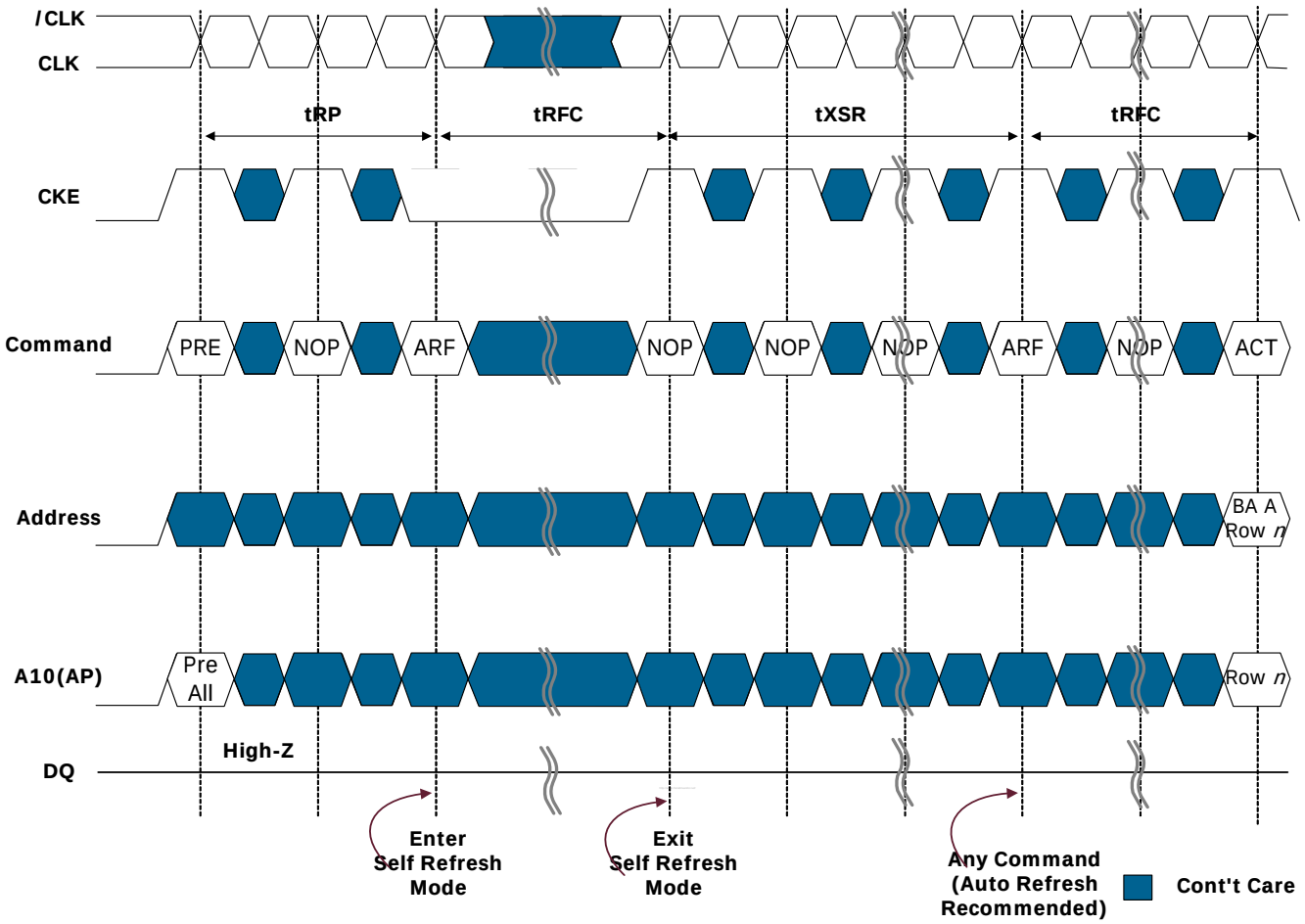
The figure of next page shows in case of 2KByte page size. If the page size is 4KByte, A0~A13 are provided.



Auto Refresh Command

Self Refresh Command

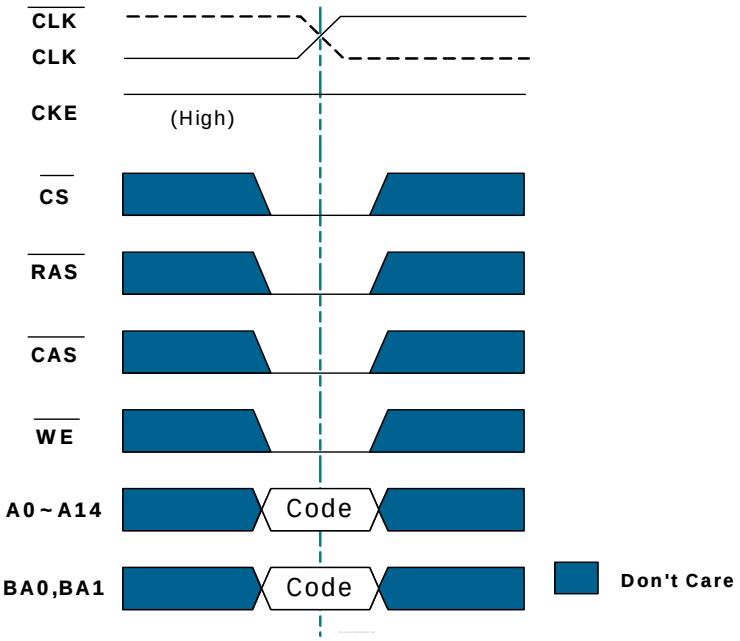
(A14 is used as 2Kbytes Reduced page)



SELF REFRESH ENTRY AND EXIT

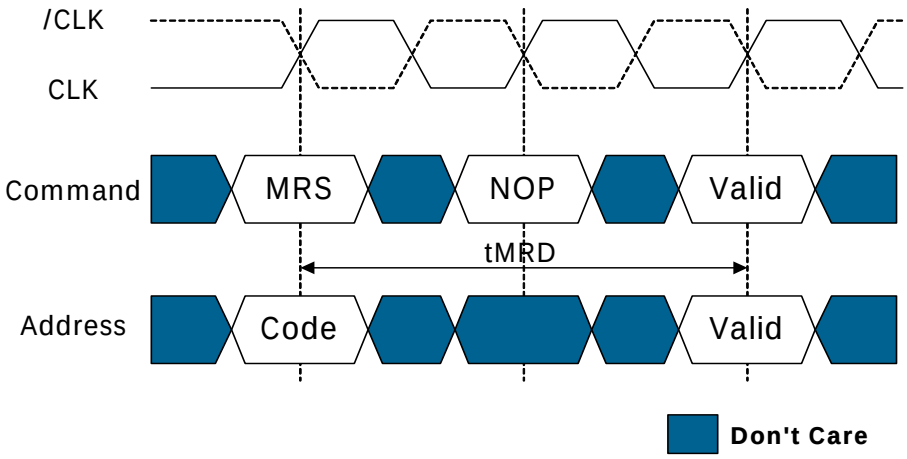
MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address bits. BA0 and BA1 are used to select among the Mode Register, the Extended Mode Register and Status Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.
The below figure shows in case of 2KByte page size. If the page size is 4KByte, A0~A13 are provided.



MODE REGISTER SET COMMAND

(A14 is used as 2Kbytes Reduced page)

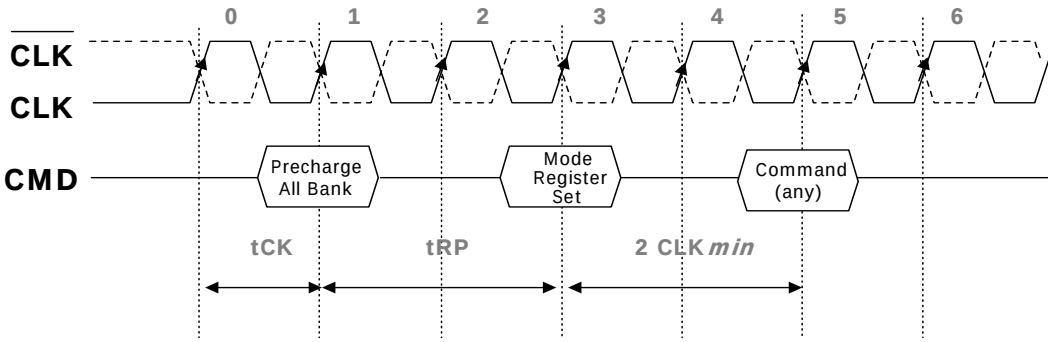


Code = Mode Register / Extended Mode Register selection
(BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

Mode Register

The mode register contains the specific mode of operation of the Mobile DDR SDRAM. This register includes the selection of a burst length(2, 4 or 8), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.



Mode Register Set

BURST LENGTH

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Page10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved.

CAS LATENCY

The CAS latency is the delay between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at a clock edge *n* and the latency is 3 clocks, the first data element will be valid at *n* + 2tCK + tAC. If a READ command is registered at a clock edge *n* and the latency is 2 clocks, the first data element will be valid at *n* + tCK + tAC.

Extended Mode Register

The Extended Mode Register contains the specific features of self refresh operation of the Mobile DDR SDRAM. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, or the device loses power. The Extended Mode Register should be loaded when all Banks are idle and no bursts are in progress, and subsequent operation should only be initiated after t_{MRD}. Violating these requirements will result in unspecified operation.

The Extended Mode Register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0. The state of address pins A0 ~ A14 (or A13 which depends on page size) and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

This register includes the selection of partial array to be refreshed (full array, half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

PARTIAL ARRAY SELF REFRESH (PASR)

With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array and 1/4 array could be selected.

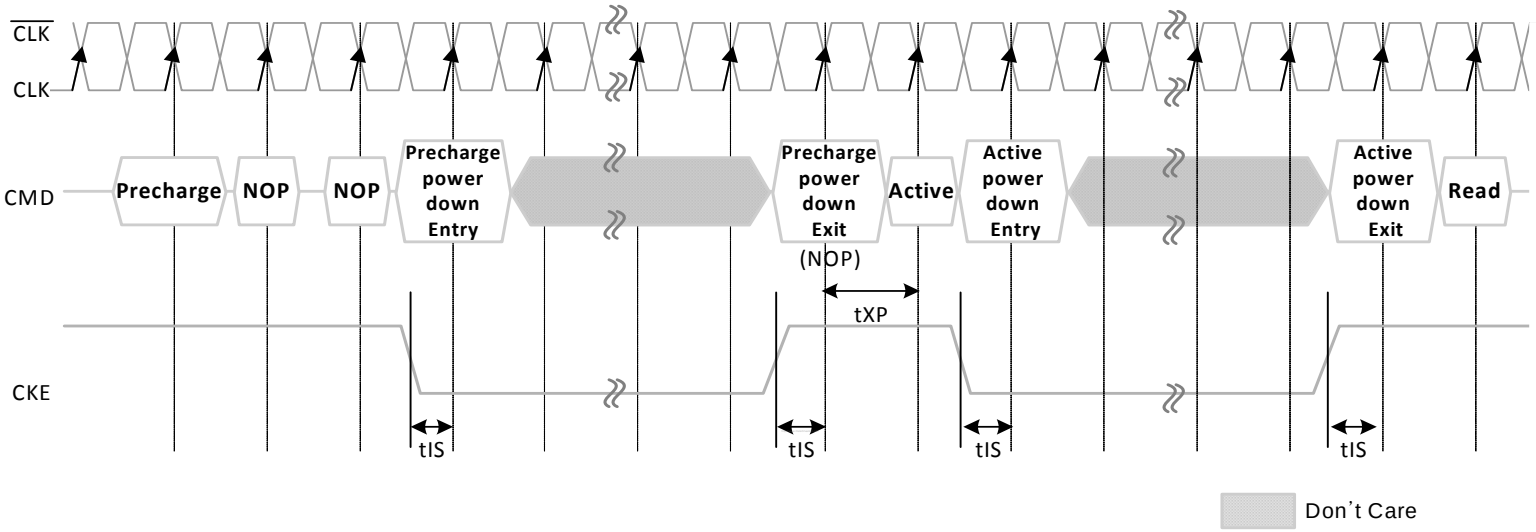
DRIVE STRENGTH (DS)

The drive strength could be set to full or half via address bits A5 and A6. The half drive strength is intended for lighter loads or point-to-point environments.

POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
A valid command can be issued after tXP. For Clock stop during power down mode, please refer to the Clock Stop sub-section in Operation section of this datasheet.

NOTE: This case shows CKE low coincident with NO OPERATION.
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.

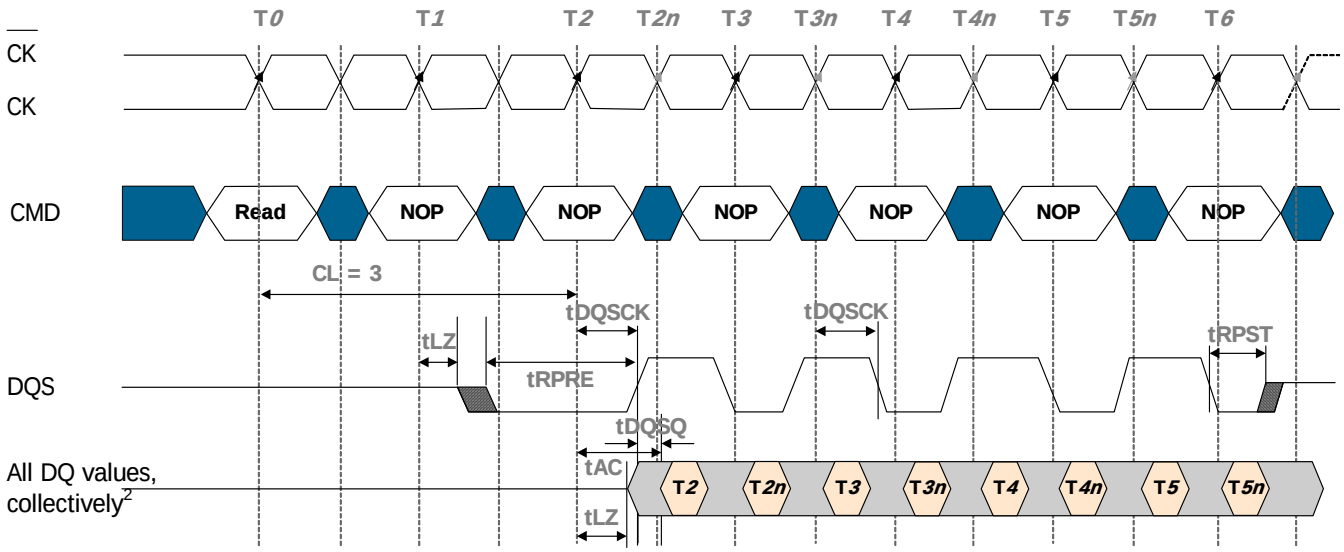


Mobile DDR SDRAM Power-Down Entry and Exit Timing

CAS LATENCY DEFINITION

CAS latency definition of Mobile DDR SDRAM must be must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation.

CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (See Figure 2)



CAS LATENCY DEFINITION

NOTE

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CK, and is the long term component of DQ skew.

Clock Stop Mode

Clock stop mode is a feature supported by Mobile DDR SDRAM devices. It reduces clock-related power consumption during idle periods of the device.

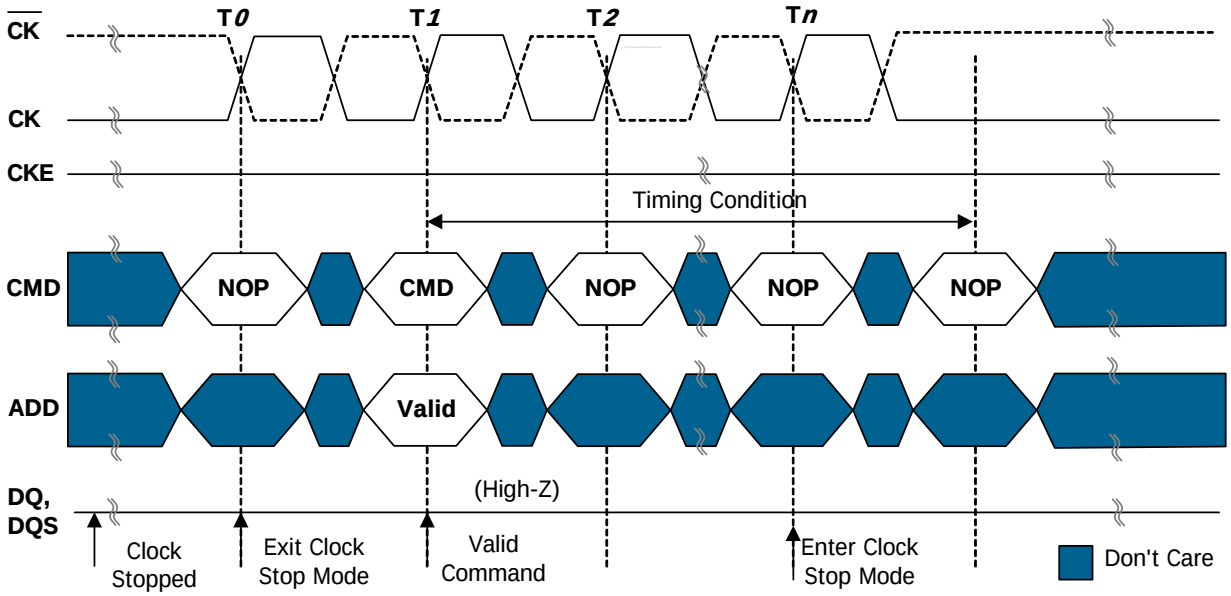
Conditions: the Mobile DDR SDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and $\overline{CK}$ held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure1 illustrates the clock stop mode:

- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T*1* a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- T*n* is the last clock pulse required by the access command latched with T*1*.
- The timing condition of this access command is met with the completion of T*n*; therefore Tn is the last clock pulse required by this command and the clock is then stopped.



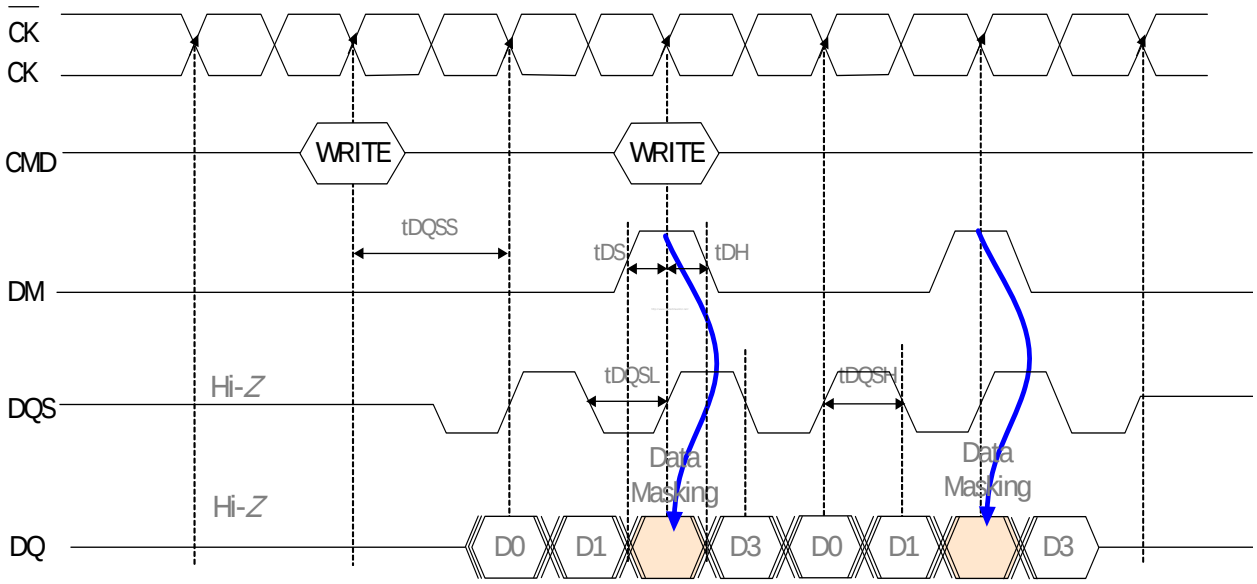
Clock Stop Mode

Data mask[1,2)

Mobile DDR SDRAM uses a DQ write mask enable signal (DM) which masks write data.
Data masking is only available in the write cycle for Mobile DDR SDRAM. Data masking is available during write, but data masking during read is not available.
DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero.
For x32 data I/O, Mobile DDR SDRAM is equipped with DM0, DM1, DM2 and DM3 which control DQ0~DQ7, DQ8~DQ15, DQ16~DQ23 and DQ24~DQ31 respectively.

Note:
1) Mobile SDR SDRAM can mask both read and write data, but the read mask is not supported by Mobile DDR SDRAM.
2) Differences in Functions and Specifications (next table)

Item	Mobile DDR SDRAM	Mobile SDR SDRAM
Data mask	Write mask only	Write mask/Read mask



Data Masking (Write cycle: BL=4)

POWER-UP AND INITIALIZATION SEQUENCES

Mobile DDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other thank those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

- Step1: Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that V_{DD} and V_{DDQ} are from the same power source. Also assert and hold CLOCK ENABLE (CKE) to a LVCMOS logic high level.

- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

- Step 3: There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.

- Step 4: Issue a PRECHARGE ALL command.

- Step 5: Provide NOPs or DESELECT commands for at least t_{RP} time.

- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time.
  Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.

- Step 7: Using the MRS command, load the base mode register. Set the desired operating modes.

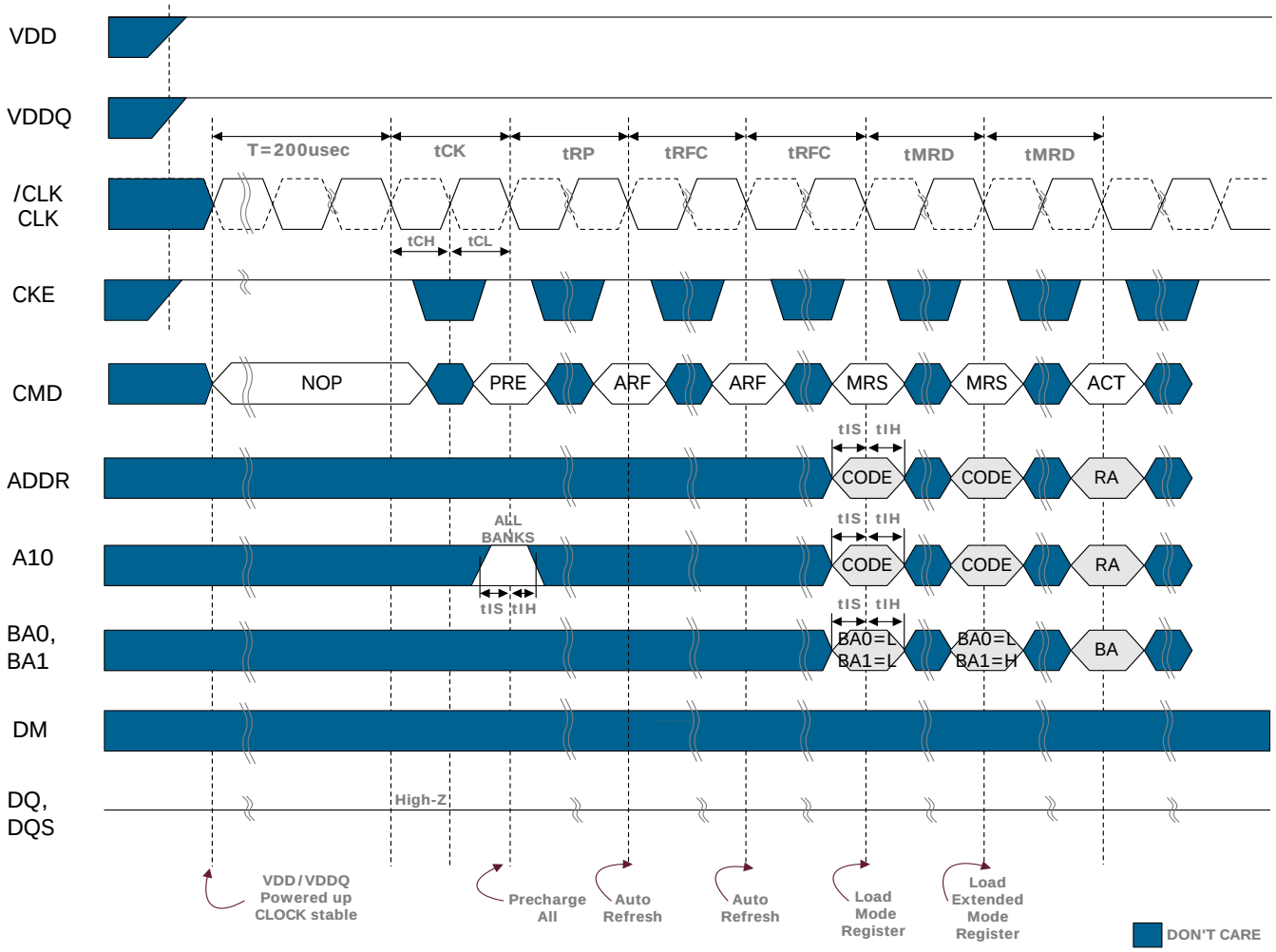
- Step 8: Provide NOPs or DESELECT commands for at least t_{MRD} time.

- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

- Step 10: Provide NOP or DESELCT commands for at least t_{MRD} time.

- Step 11: The DRAM has been properly initialized and is ready for any valid command.

The Initialization flow sequence is below.



Initialization Waveform Sequence