

H7N0405LD, H7N0405LS, H7N0405LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1367-0100

Rev.1.00

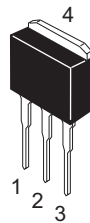
Sep 25, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 4.0 \text{ m}\Omega$ typ.
- Low drive current.
- Capable of 4.5 V gate drive

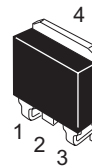
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



H7N0405LD

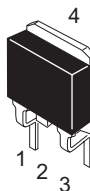
RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



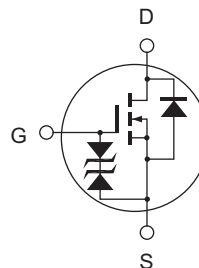
H7N0405LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDKPAK (S)-(2))



H7N0405LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	80	A
Drain peak current	I_D (pulse) ^{Note1}	320	A
Body drain diode reverse drain current	I_{DR}	80	A
Avalanche current	I_{AP} ^{Note3}	40	A
Avalanche energy	E_{AR} ^{Note3}	213	mJ
Channel dissipation	P_{ch} ^{Note2}	80	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. $T_c = 25^\circ C$ 3. $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

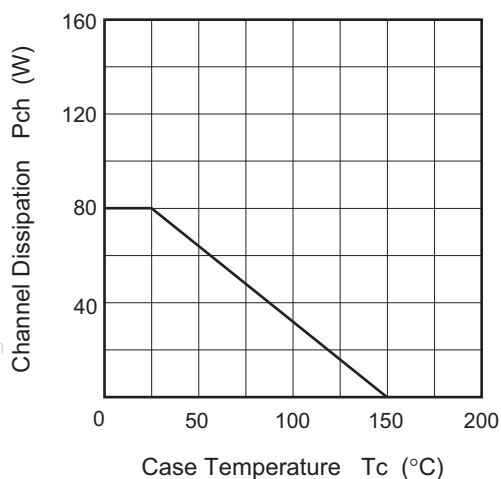
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source break down voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cut off voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Static drain to source on state resistance	$R_{DS(on)}$	—	4.0	5.0	mΩ	$I_D = 40 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
		—	6.2	8.7	mΩ	$I_D = 40 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	54	90	—	S	$I_D = 40 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	5600	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	825	—	pF	
Reverse transfer admittance	C_{rss}	—	550	—	pF	
Total gate charge	Q_g	—	100	—	nC	$V_{DD} = 25 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
Gate to source charge	Q_{gs}	—	25	—	nC	
Gate to drain charge	Q_{gd}	—	25	—	nC	
Turn-off delay time	$t_{d(on)}$	—	40	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 40 \text{ A}$, $R_L = 0.75 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	400	—	ns	
Body-drain diode forward voltage	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	26	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.94	—	V	$I_F = 80 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 80 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu s$

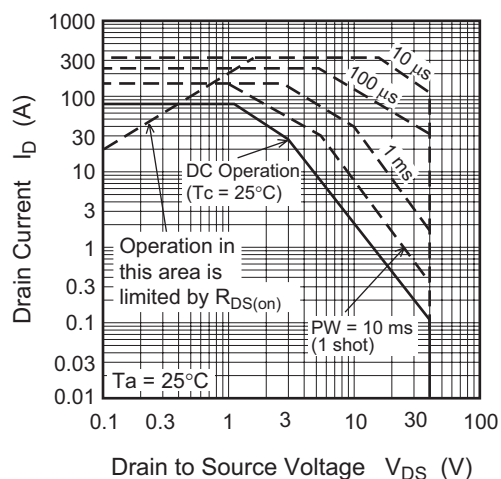
Notes: 4. Pulse test

Main Characteristics

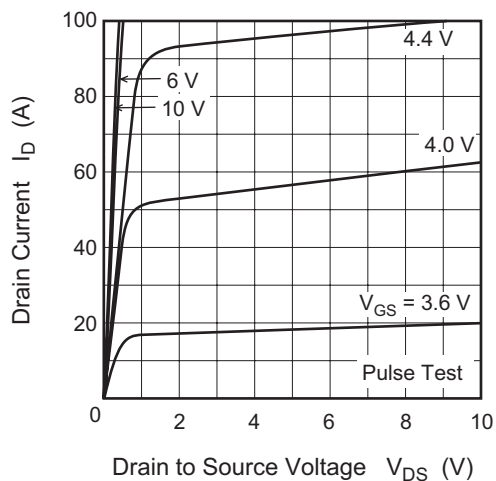
Power vs. Temperature Derating



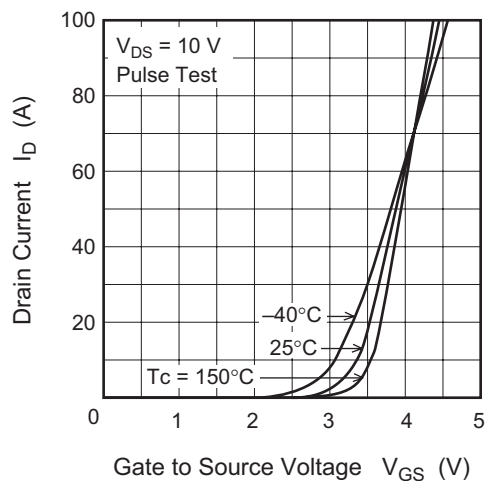
Maximum Safe Operation Area



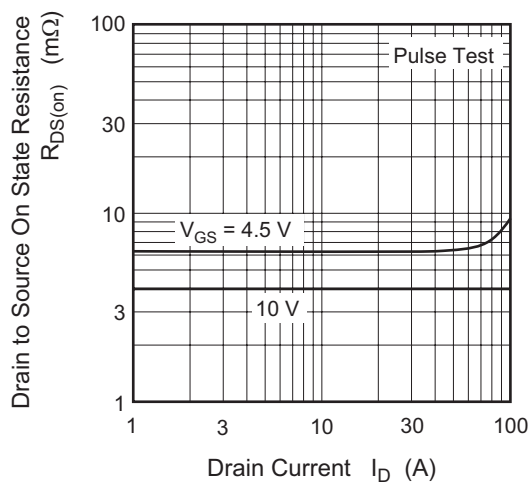
Typical Output Characteristics



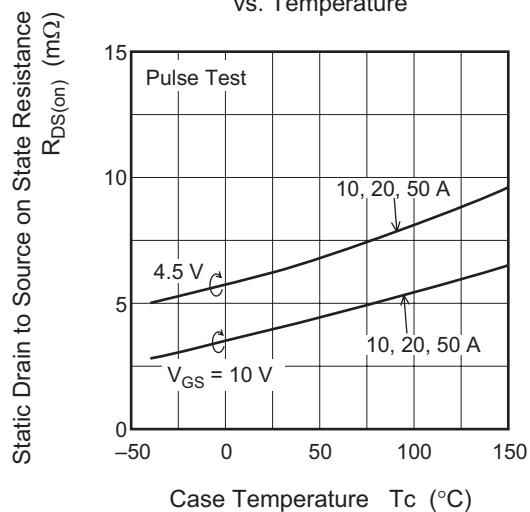
Typical Transfer Characteristics

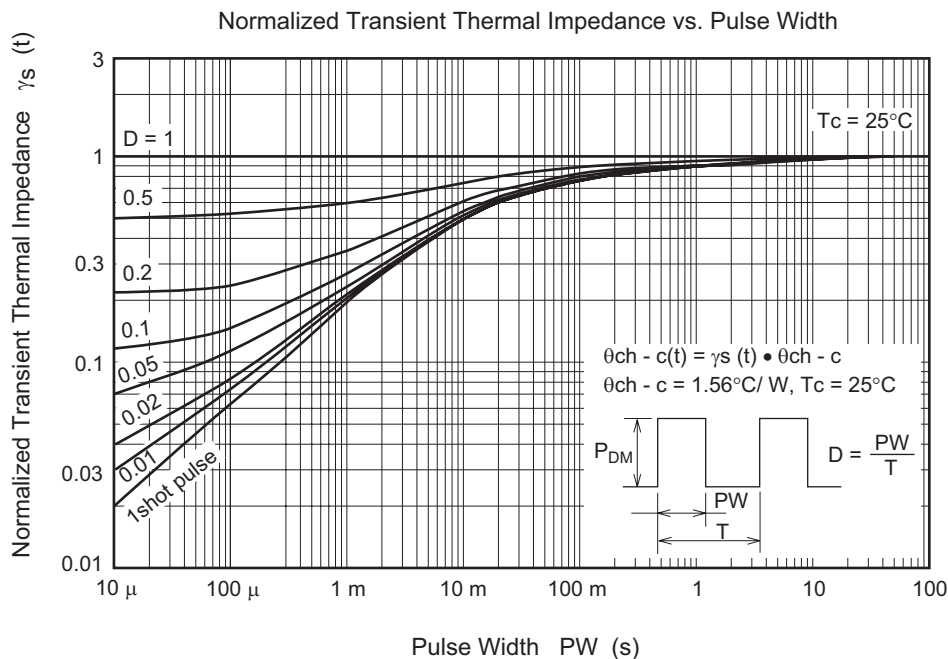
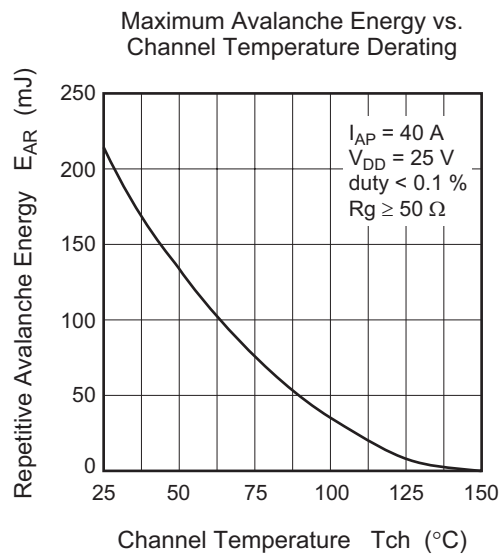
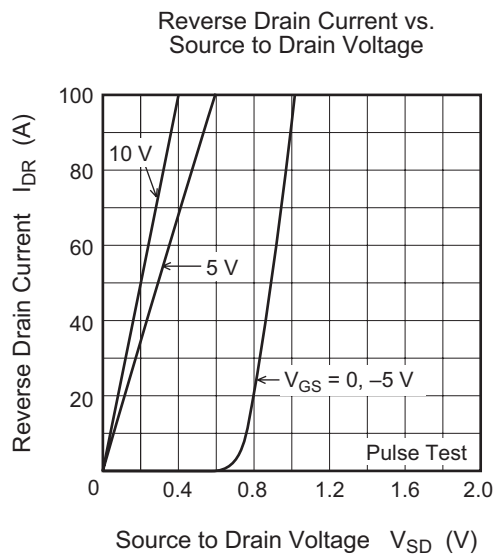
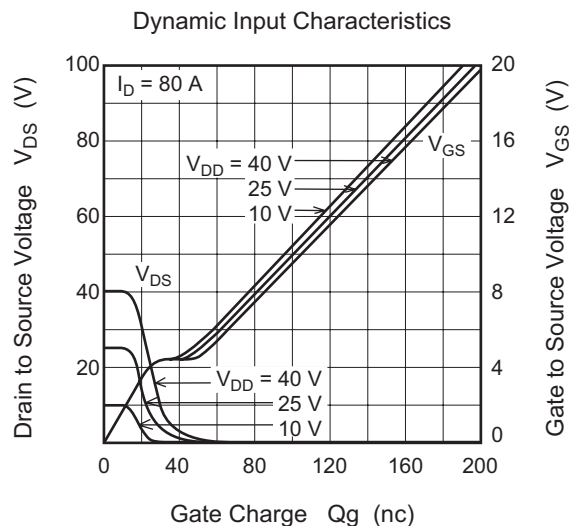
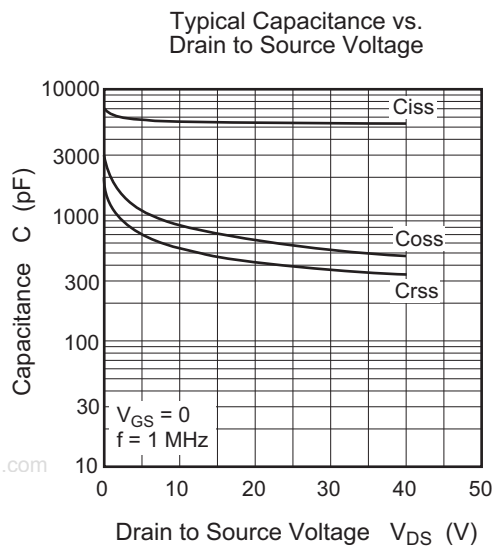


Static Drain to Source on State Resistance vs. Drain Current

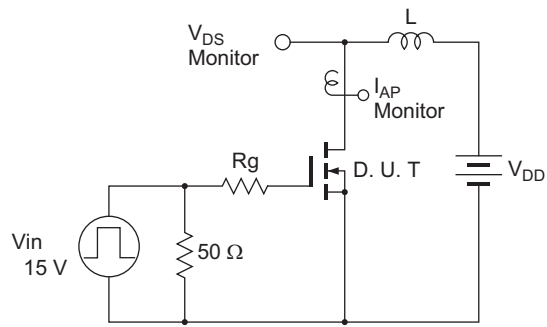


Static Drain to Source on State Resistance vs. Temperature



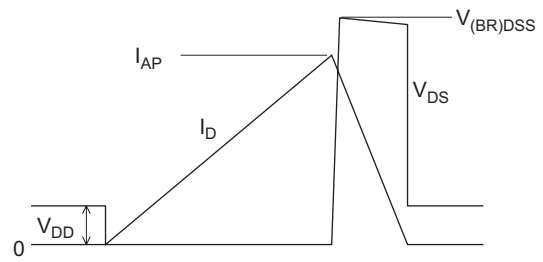


Avalanche Test Circuit

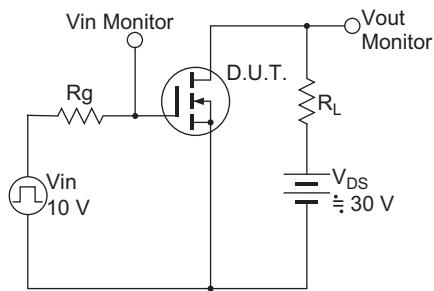


Avalanche Waveform

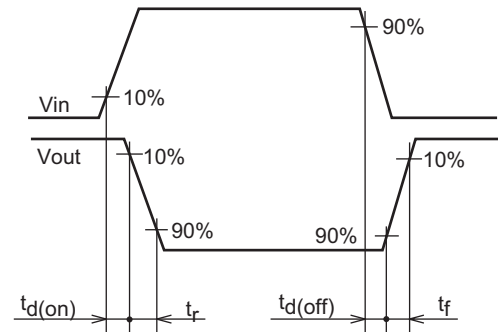
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

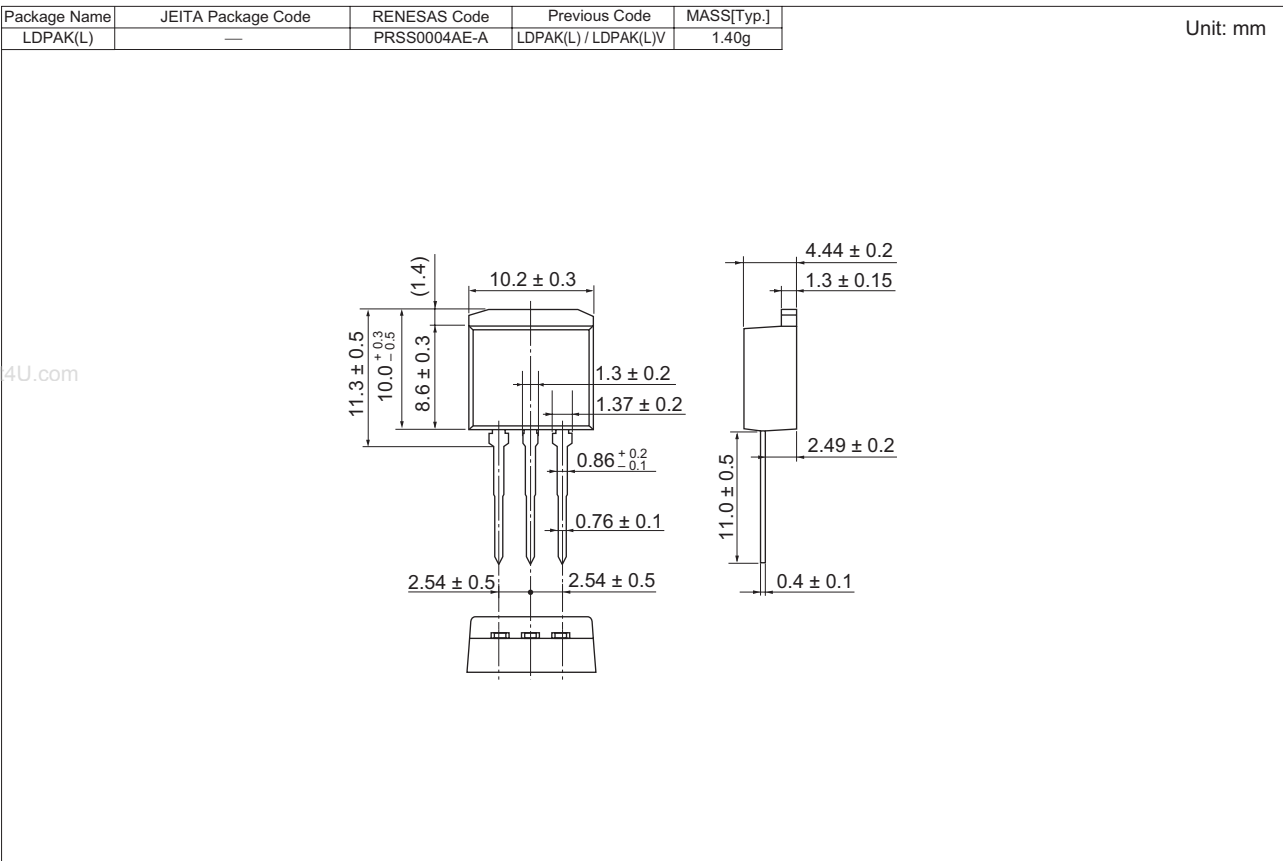


Switching Time Waveform

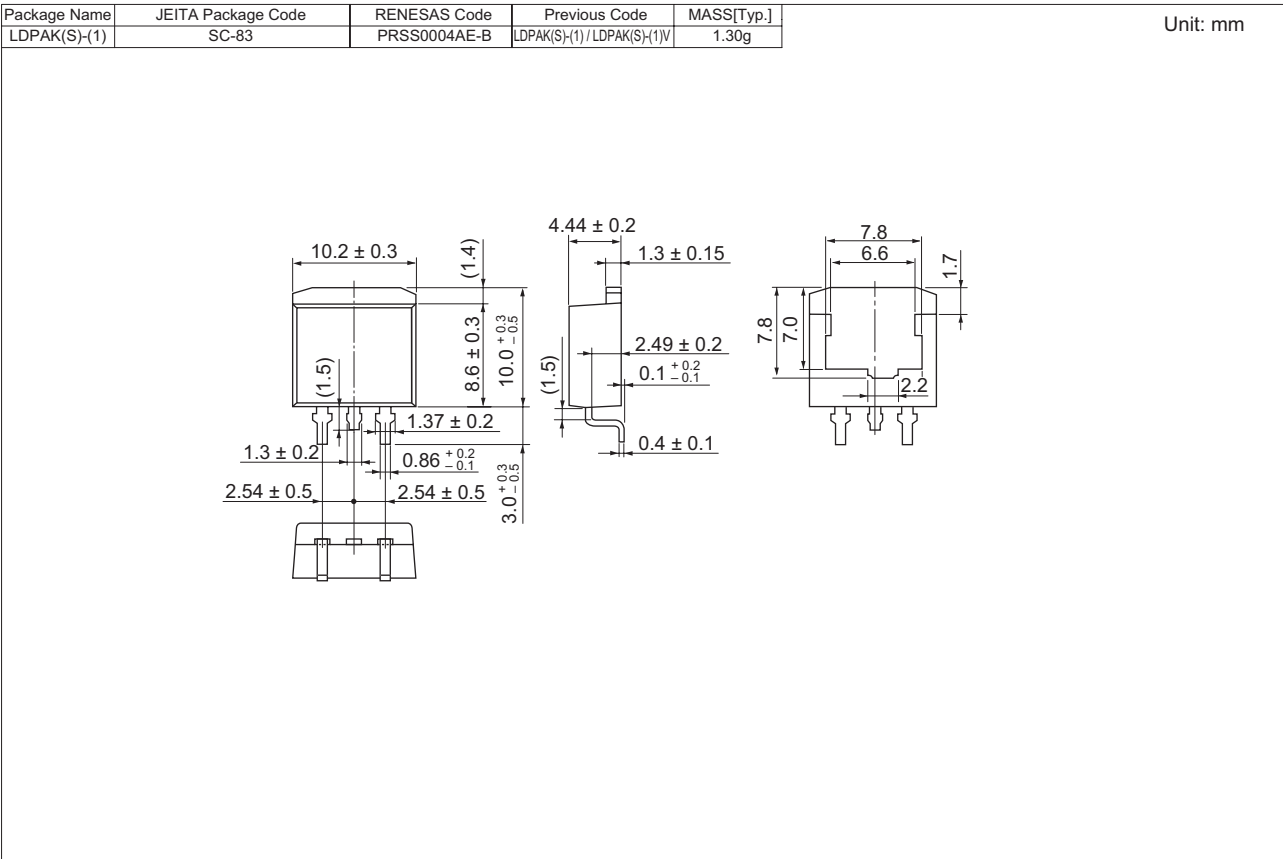


Package Dimensions

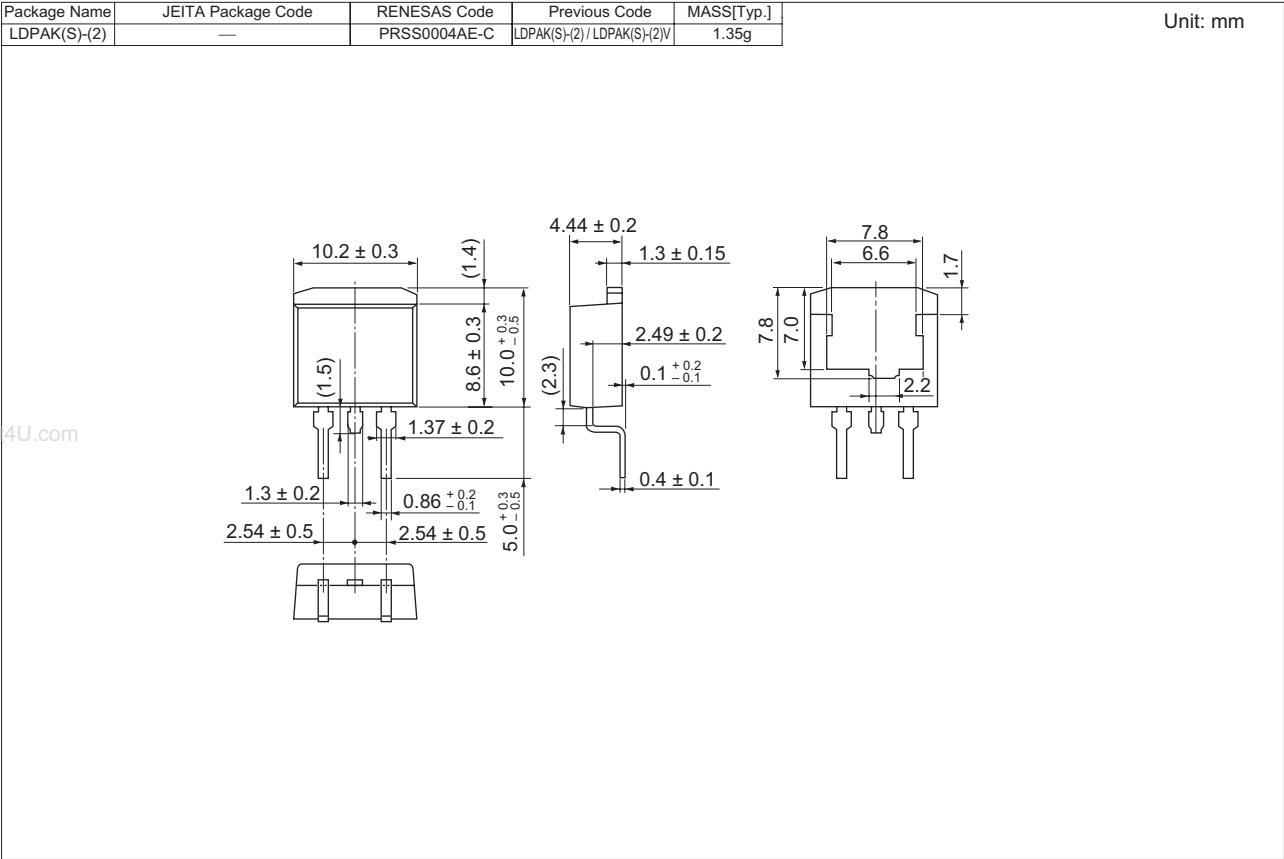
• H7N0405LD



• H7N0405LS



• H7N0405LM



Ordering Information

Part Name	Quantity	Shipping Container
H7N0405LD-E	500 pcs	Box (Conductive Sack)
H7N0405LSTL-E	1000 pcs	Taping
H7N0405LMTL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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