1Gb DDR3 SDRAM

(Preliminary version)

H5TQ1G43AFP-xxC

H5TQ1G83AFP-xxC

H5TQ1G63AFP-xxC

**** Since DDR3 Specification has not been defined completely yet in JEDEC, this document may contain items under discussion.**

**** Contents may be changed at any time without any notice.**

Revision History

Revision No.	History	Draft Date	Remark
0.1	Preliminary	2007-11	

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1. DESCRIPTION

Preliminary The H5TQ1G43AFP-xxC, H5TQ1G83AFP-xxC and H5TQ1G63AFP-xxC are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it.

The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

1.1 Device Features and Ordering Information

1.1.1 FEATURES

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- JEDEC standard 78ball FBGA(x4/x8) , 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- On Die Thermal Sensor supported (JEDEC optional)
- 8 bit pre-fetch

1.1.2 ORDERING INFORMATION

Part No.	Configuration	Package
H5TQ1G43AFP-xx*C	256M x 4	78ball FBGA
H5TQ1G83AFP-xx*C	128M x 8	
H5TQ1G63AFP-xx*C	64M x 16	96ball FBGA

* XX means Binning grade (Speed/IDD...)

1.1.3 OPERATING FREQUENCY

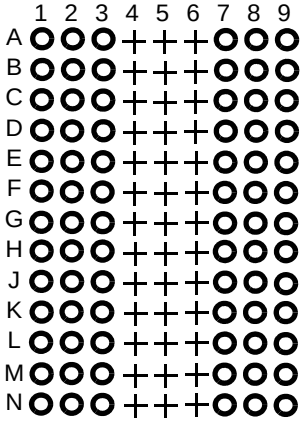
Grade	Frequency [MHz]						Remark (CL-tRCD-tRP)
	CL5	CL6	CL7	CL8	CL9	CL10	
-S5							DDR3-800 5-5-5
-S6							DDR3-800 6-6-6
-G7							DDR3-1066 7-7-7
-G8							DDR3-1066 8-8-8
-H8							DDR3-1333 8-8-8
-H9							DDR3-1333 9-9-9

1.2 Package Ballout

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C	NC	NC		NC				NC		NC	NC	C
D												D
E												E
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	F
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		G
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		J
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		K
L		NC	VSS	RAS#				CK	VSS	NC		L
M		ODT	VDD	CAS#				CK#	VDD	CKE		M
N		NC	CS#	WE#				A10/AP	ZQ	NC		N
P		VSS	BA0	BA2				A15	VREFCA	VSS		P
R		VDD	A3	A0				A12/BC#	BA1	VDD		R
T		VSS	A5	A2				A1	A4	VSS		T
U		VDD	A7	A9				A11	A6	VDD		U
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	V
W												W
Y												Y
AA	NC	NC		NC				NC		NC	NC	AA
AB												AB
AC	NC	NC		NC				NC		NC	NC	AC
		1	2	3	4	5	6	7	8	9		

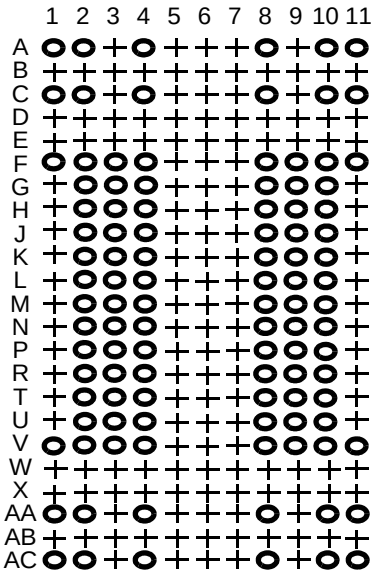
Note1.
Green NC balls indicate mechanical support balls with no internal connection
Any of the support ball locations may or may not be populated with a ball

MO-207 Variation DT-z (x8)



O Populated ball
+ Ball not populated

MO-207 Variation DW-z (x8)
with support balls



1.3 ROW AND COLUMN ADDRESS TABLE

1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A15
Column Address	A0 - A9, A11, A13	A0 - A9, A11	A0 - A9
Page size [1]	2 KB	2 KB	2 KB

Note1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS}$ * ORG ÷ 8

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

1.4 Pin Functional Description

Input / output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage
ZQ	Supply	Reference Pin for ZQ calibration

Note:
Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, DM, and RESET#) do not supply termination.

2. Command Description

2.1 Command Truth Table

(a) note 1,2,3,4 apply to the entire Command Truth Table

(b) Note 5 applies to all Read/Write command

[BA=Bank Address, RA=Rank Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA3	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7,8,9,12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA3	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

2.2 CKE Truth Table

a) Notes 1-7 apply to the entire CKE Truth Table.
b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State[2]	CKE		Command (N)[3] RAS#, CAS#, WE#, CS#	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See “2.1 Command Truth Table” on page 10..					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. tCKEmin of [TBD] clocks means CKE must be registered on [TBD] consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the [TBD] clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + [TBD] + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions **see 8.2.1 on page 44**.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100		, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4. Operating Conditions

4.1 OPERATING TEMPERATURE CONDITION

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature (Tcase)	0 to 85	°C	2
	Extended Temperature Range	85 to 95	°C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

4.2 RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC paramaters are measured with VDD and VDDQ tied together.

5. AC and DC Input Measurement Levels

5.1 AC and DC Logic Input Levels for Single-Ended Signals

Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	TBD	V	1
VIL(DC)	DC input logic low	TBD	Vref - 0.100	V	1
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	VDDQ/2 - TBD	VDDQ/2 + TBD		

Notes:
1. For DQ and DM, Vref = VrefDQ. For input any pins except RESET#, Vref = VrefCA.
2. The “t.b.d.” entries might change based on overshoot and undershoot specification.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{Ref(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in below Figure. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise).
VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 1.
Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD.

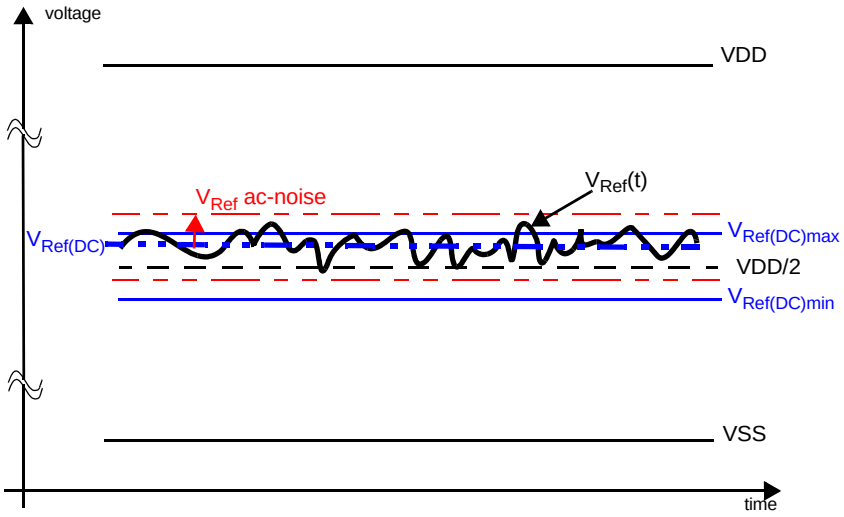


Illustration of Vref(DC) tolerance and Vref ac-noise limits

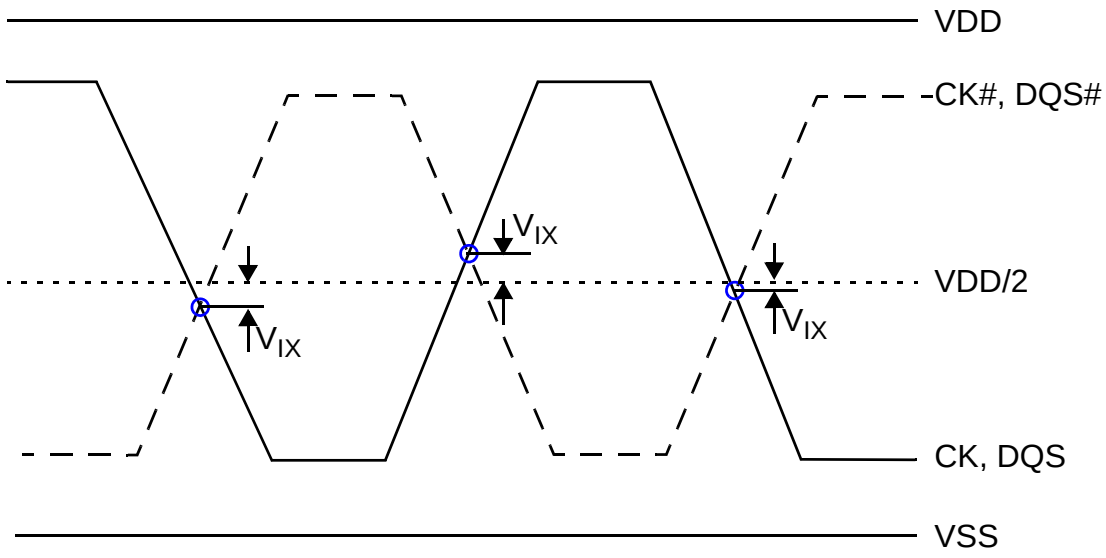
5.2 AC and DC Logic Input Levels for Differential Signals

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1.
Refer to "Overshoot and Undershoot Specification on page 23"

5.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	150	mV	

5.4 Slew Rate Definitions for Single Ended Input Signals

5.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

5.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef.

Single-Ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH(AC)min	$\frac{\text{VIH(AC)min-Vref}}{\text{Delta TRS}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL(AC)max	$\frac{\text{Vref-VIL(AC)max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	VIL(DC)max	Vref	$\frac{\text{Vref-VIL(DC)max}}{\text{Delta TFH}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH(DC)min	Vref	$\frac{\text{VIH(DC)min-Vref}}{\text{Delta TRH}}$	

Input Nominal Slew Rate Definition for Single-Ended Signals

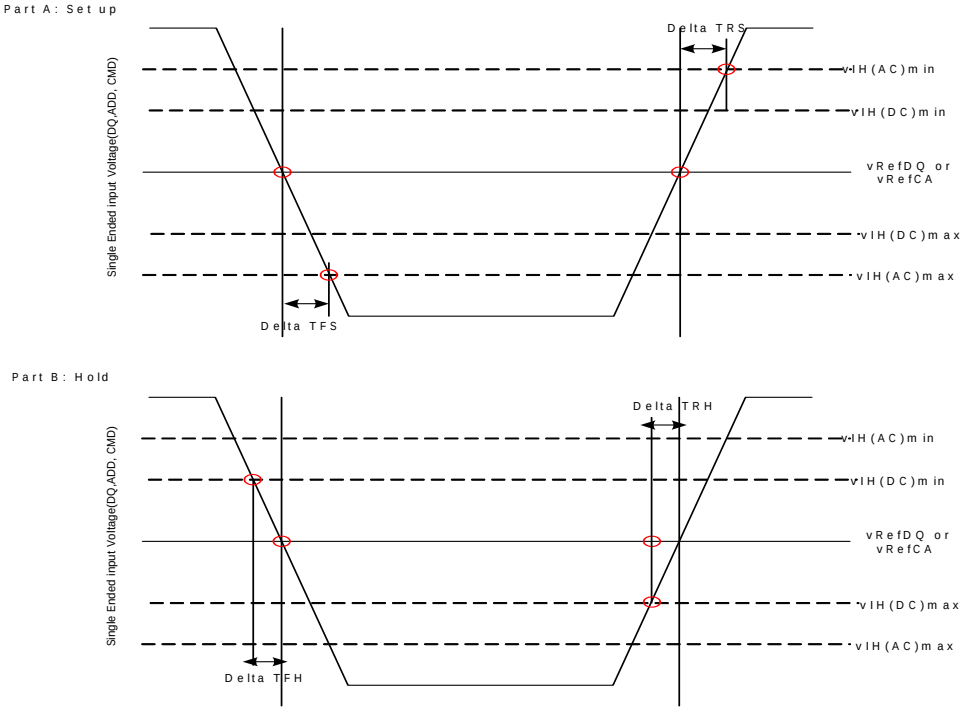


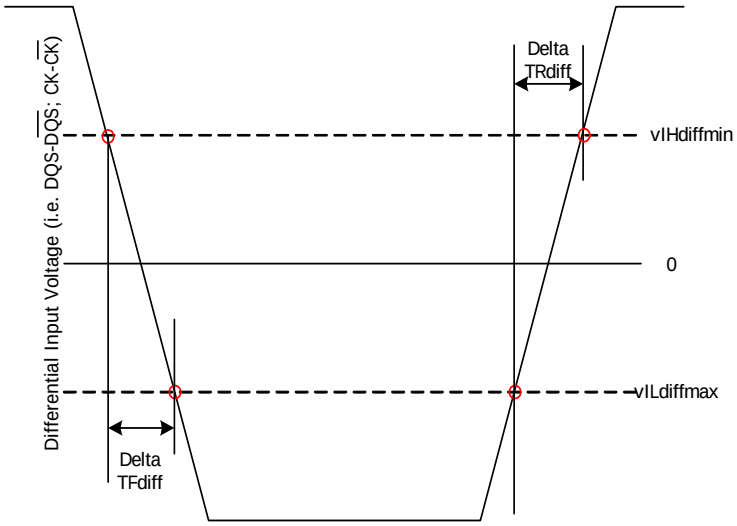
Figure 82 ? Input Nominal Slew Rate Definition for Single-Ended Signals

5.5 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	VIHdiffmin-VILdiffmax / $\overline{DeltaTRdiff}$
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	VIHdiffmin-VILdiffmax / $\overline{DeltaTFdiff}$

Note:
The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

6. AC and DC Output Measurement Levels

6.1 Single Ended AC and DC Output Levels

Table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

6.1.1 Differential AC and DC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for outtput SR)	- 0.2 x VDDQ	V	1

1. The swing of ± 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

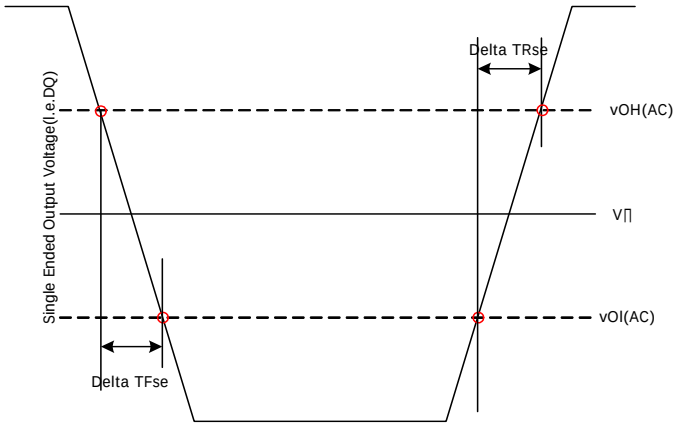
6.2 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table and Figure.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{\text{VOH(AC)-VOL(AC)}}{\overline{\text{DeltaTRse}}}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{\text{VOH(AC)-VOL(AC)}}{\overline{\text{DeltaTFse}}}$

Note:
Output slew rate is verified by design and characterisation, and may not be subject to production test.

Fig. Single Ended Output Slew Rate Definition



Single Ended Output Slew Rate Definition

Table. Output Slew Rate (single-ended)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns

***** For Ron = RZQ/7 setting**

6.3 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table and Figure .

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) DeltaTFdiff

Note:
Output slew rate is verified by design and characterization, and may not be subject to production test.

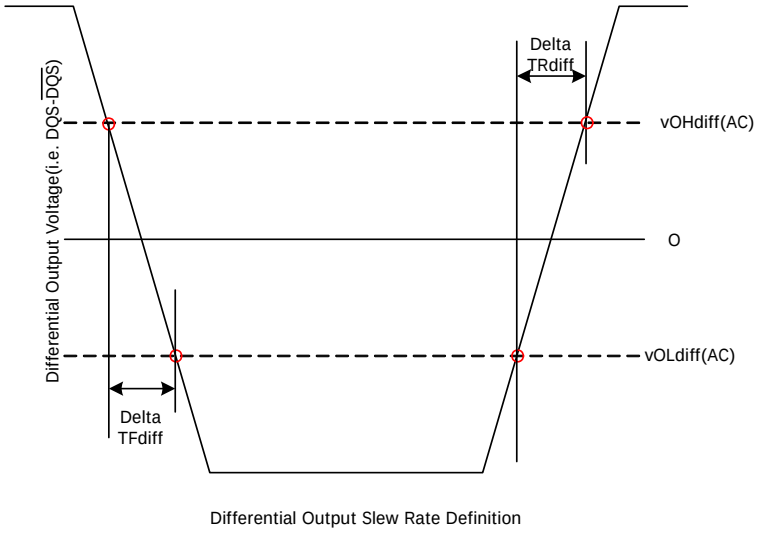


Fig. Differential Output Slew Rate Definition

Table. Differential Output Slew Rate

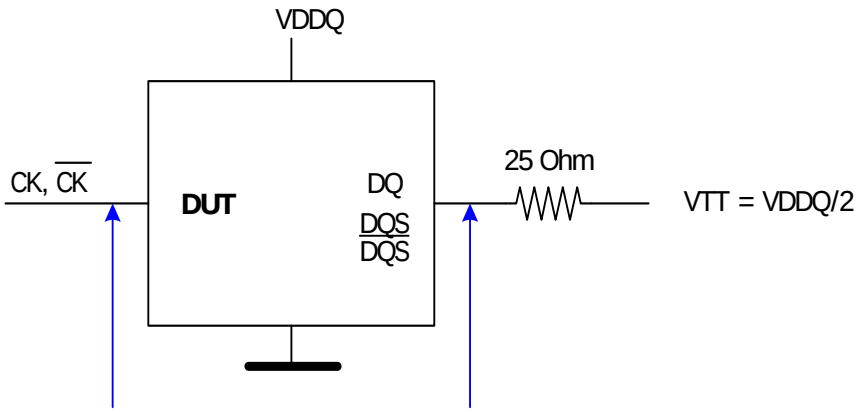
Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	TBD	10	V/ns

***For Ron = RZQ/7 setting**

6.4 Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



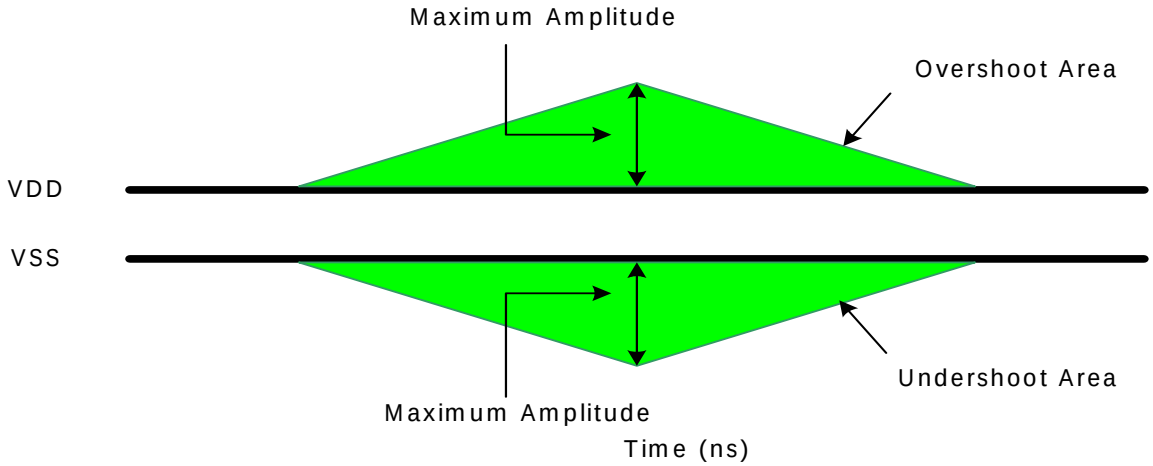
Reference Load for AC Timing and Output Slew Rate

7. Overshoot and Undershoot Specifications

7.1 Address and Control Overshoot and Undershoot Specifications

Table. AC Overshoot/Undershoot Specification for Address and Control Pins

Description	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

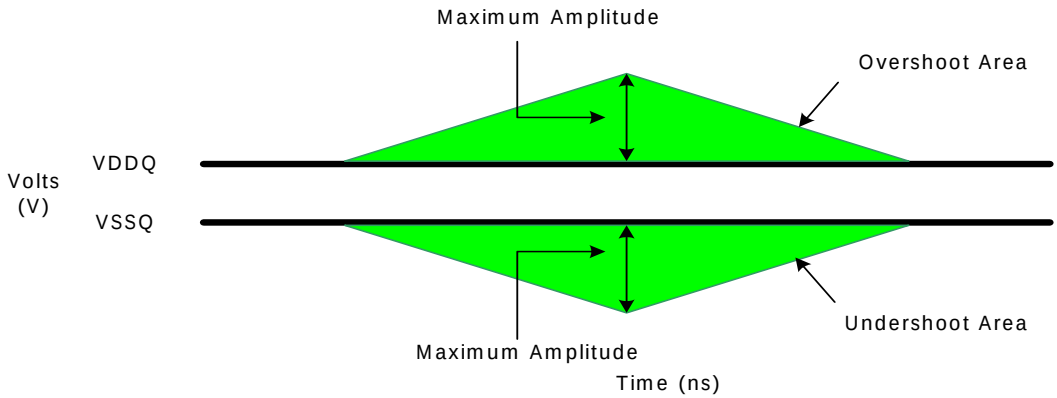


Address and Control Overshoot and Undershoot Definition

7.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Table. AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Description	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

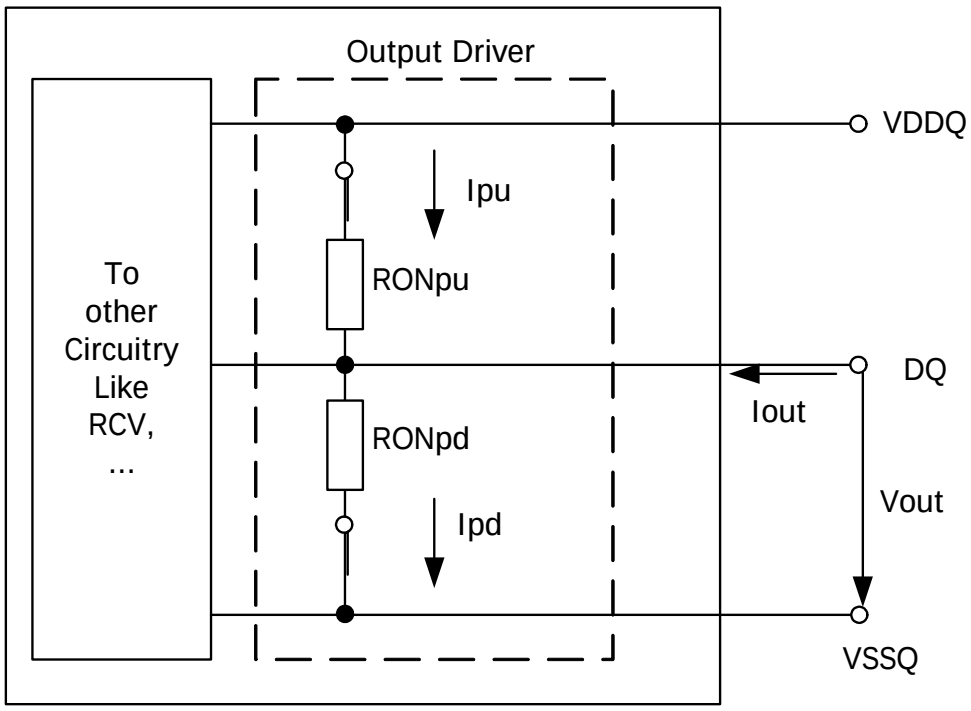
7.3 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure . Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:
RON34 = RZQ / 7 (nominal 34.3 W ±10% with nominal RZQ = 240 W ± 1%)
The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

$$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ **under the condition that RONPd is turned off**

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ **under the condition that RONPu is turned off**

Chip in Drive Mode



Output Driver: Definition of Voltages and Currents

Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω ; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
	RON_{34Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5 × V_{DDQ}	-10		+10	%	1, 2, 4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
Measure RONPu and RONPd, both at 0.5 x VDDQ:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

7.4 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .
DT = T - T(@calibration); DV= VDDQ - VDDQ(@calibration); VDD = VDDQ
dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

	min	max	unit
RONPU@ V_{OHdc}	0.6 - $dR_{ON}dTH*\|\Delta T\|$ - $dR_{ON}dVH*\|\Delta V\|$	1.1 + $dR_{ON}dTH*\|\Delta T\|$ + $dR_{ON}dVH*\|\Delta V\|$	RZQ/7
RON@ V_{OMdc}	0.9 - $dR_{ON}dTM*\|\Delta T\|$ - $dR_{ON}dVM*\|\Delta V\|$	1.1 + $dR_{ON}dTM*\|\Delta T\|$ + $dR_{ON}dVM*\|\Delta V\|$	RZQ/7
RONPD@ V_{OLdc}	0.6 - $dR_{ON}dTL*\|\Delta T\|$ - $dR_{ON}dVL*\|\Delta V\|$	1.1 + $dR_{ON}dTL*\|\Delta T\|$ + $dR_{ON}dVL*\|\Delta V\|$	RZQ/7

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	TBD	%/mV

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	TBD	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

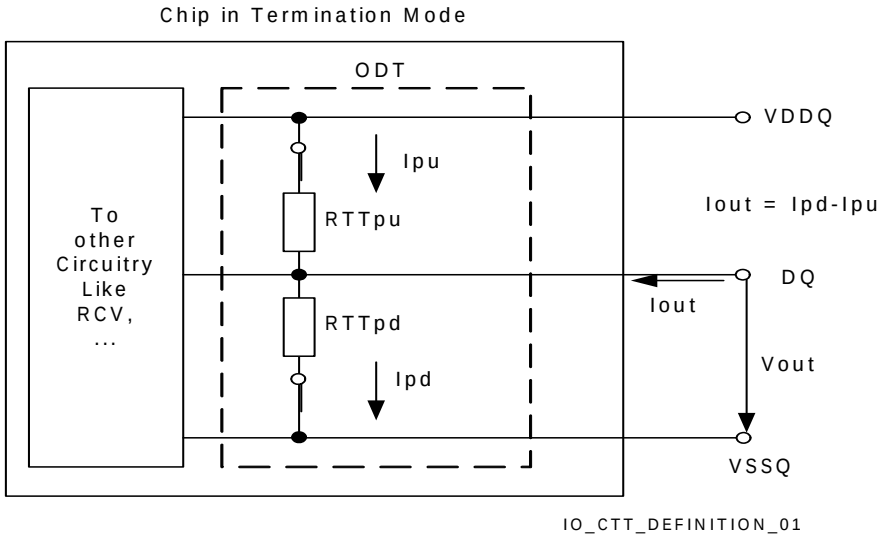
7.5 On-Die Termination (ODT) Levels and I-V Characteristics

7.5.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.
ODT is applied to the DQ, DM, DQS/DQS# and TDQS/TDQS# (x8 devices only) pins.
A functional representation of the on-die termination is shown in Figure . The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ under the condition that RTTPd is turned off

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RTTPu is turned off



On-Die Termination : Definition of Voltages and Currents

7.5.2 ODT DC Electrical Characteristics

A below table provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60 , RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
		$RTT_{120Pu240}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
		RTT_{120}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/2	1) 2) 5)
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/2	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/2	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/2	1) 2) 3) 4)
		$RTT_{60Pu120}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/2	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/2	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/2	1) 2) 3) 4)
		RTT_{60}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/4	1) 2) 5)

ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/3	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/3	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/3	1) 2) 3) 4)
		RTT_{40Pu80}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/3	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/3	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/3	1) 2) 3) 4)
		RTT_{40}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/6	1) 2) 5)
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/4	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/4	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/4	1) 2) 3) 4)
		RTT_{30Pu60}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/4	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/4	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/4	1) 2) 3) 4)
		RTT_{30}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/8	1) 2) 5)
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/6	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/6	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/6	1) 2) 3) 4)
		RTT_{20Pu40}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/6	1) 2) 3) 4)
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/6	1) 2) 3) 4)
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/6	1) 2) 3) 4)
		RTT_{20}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/12	1) 2) 5)
Deviation of V_M w.r.t. V_{DDQ}/2, DV_M				-5		+5	%	1) 2) 5) 6)

The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.

Not a specification requirement, but a design guide line.

Measurement definition for RTT:

Apply VIH(ac) to pin under test and measure current I(VIH(ac)), then apply VIL(ac) to pin under test and measure current I(VIL(ac)) respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

Measurement definition for VM and DVM :

Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \bullet V_M}{V_{DDQ}} - 1\right) \bullet 100$$

7.5.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .

DT = T - T(@calibration); DV= VDDQ - VDDQ(@calibration); VDD = VDDQ

ODT Sensitivity Definition

	min	max	unit
RTT	0.9 - $dR_{TT}dT*\|\Delta T\|$ - $dR_{TT}dV*\|\Delta V\|$	1.6 + $dR_{TT}dT*\|\Delta T\|$ + $dR_{TT}dV*\|\Delta V\|$	RZQ/2,4,6,8,12

ODT Voltage and Temperature Sensitivity

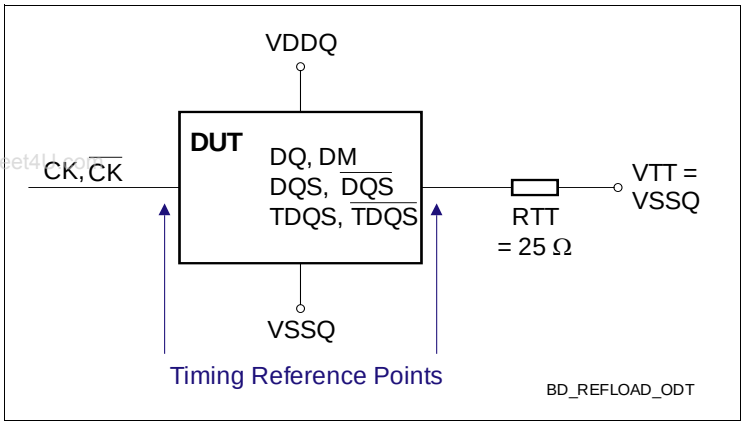
	min	max	unit
$dR_{TT}dT$	0	1.5	%/^{o}C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization

7.6 ODT Timing Definitions

7.6.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure .



7.6.2 ODT Timing Reference Load

ODT Timing Definitions

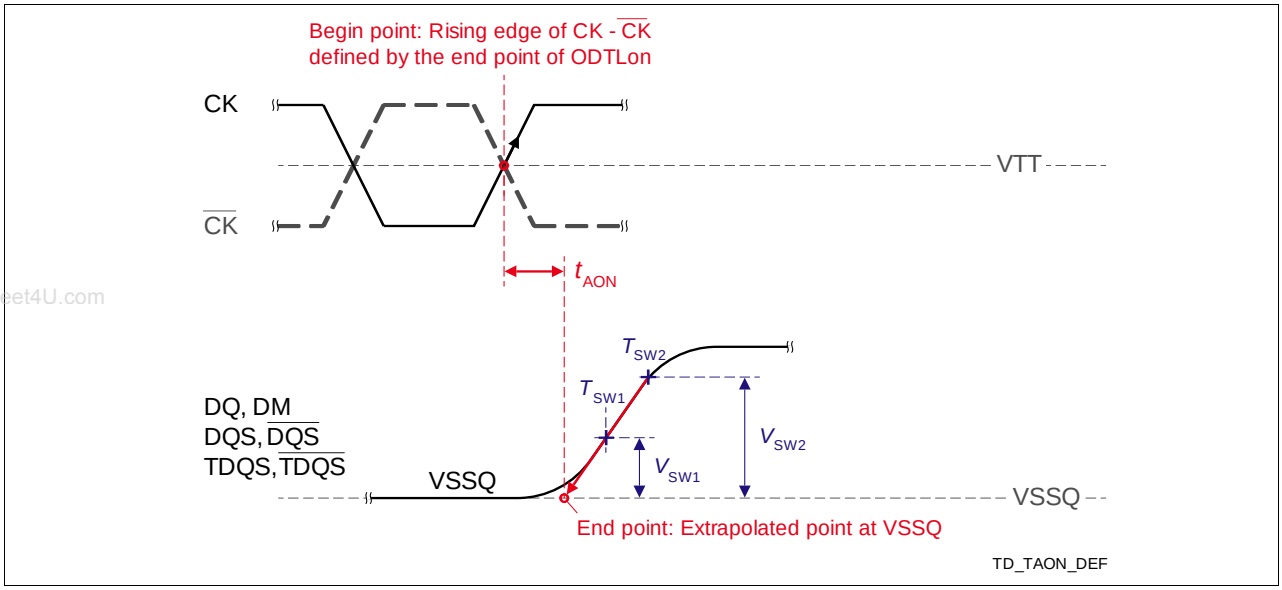
Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in the table and subsequent figures. Measurement reference settings are provided in the table.

ODT Timing Definitions

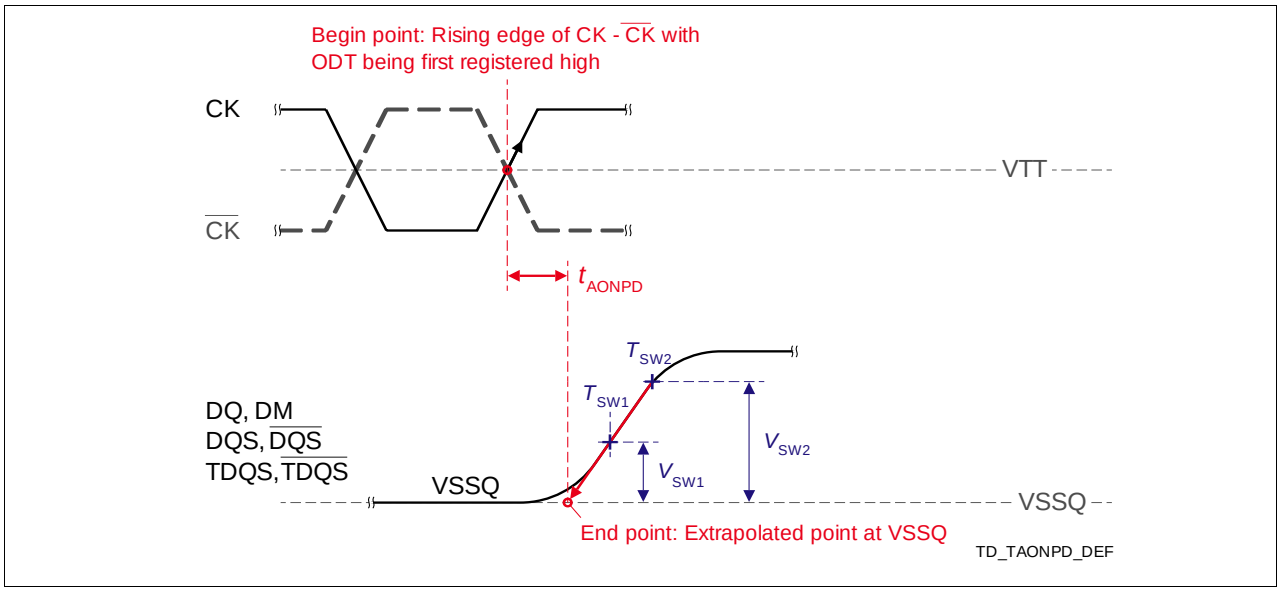
Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - CK# defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure
t_{AONPD}	Rising edge of CK - CK# with ODT being first registered high	Extrapolated point at VSSQ	Figure
t_{AOF}	Rising edge of CK - CK# defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure
t_{AOFPD}	Rising edge of CK - CK# with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure
t_{ADC}	Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure

Reference Settings for ODT Timing Measurements

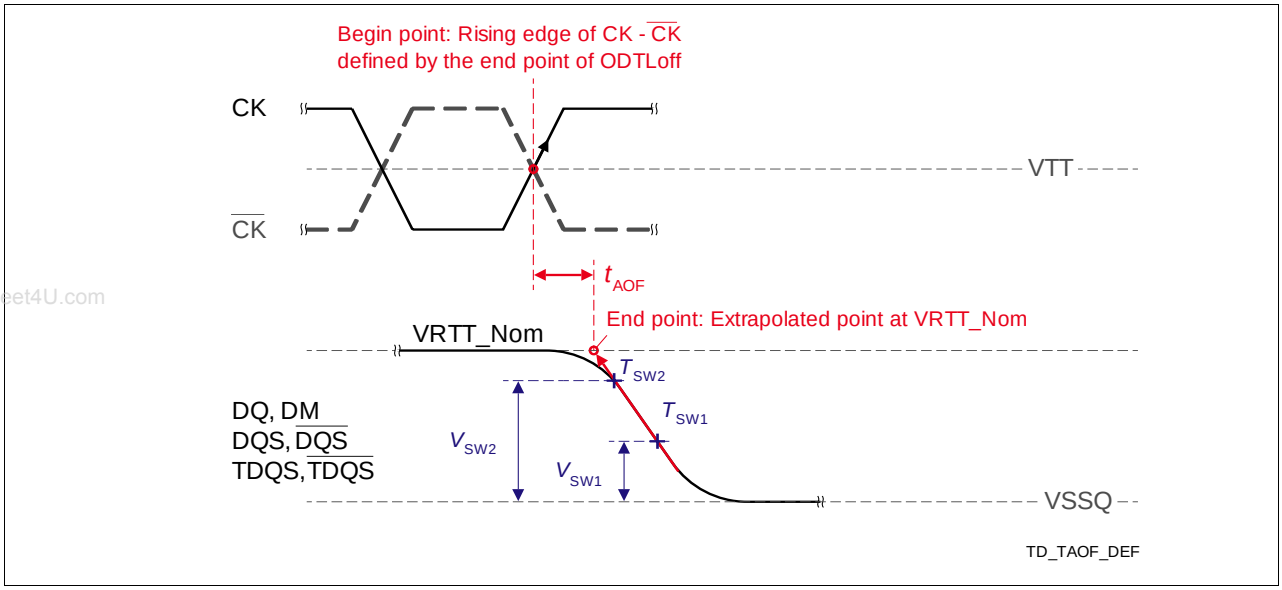
Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	



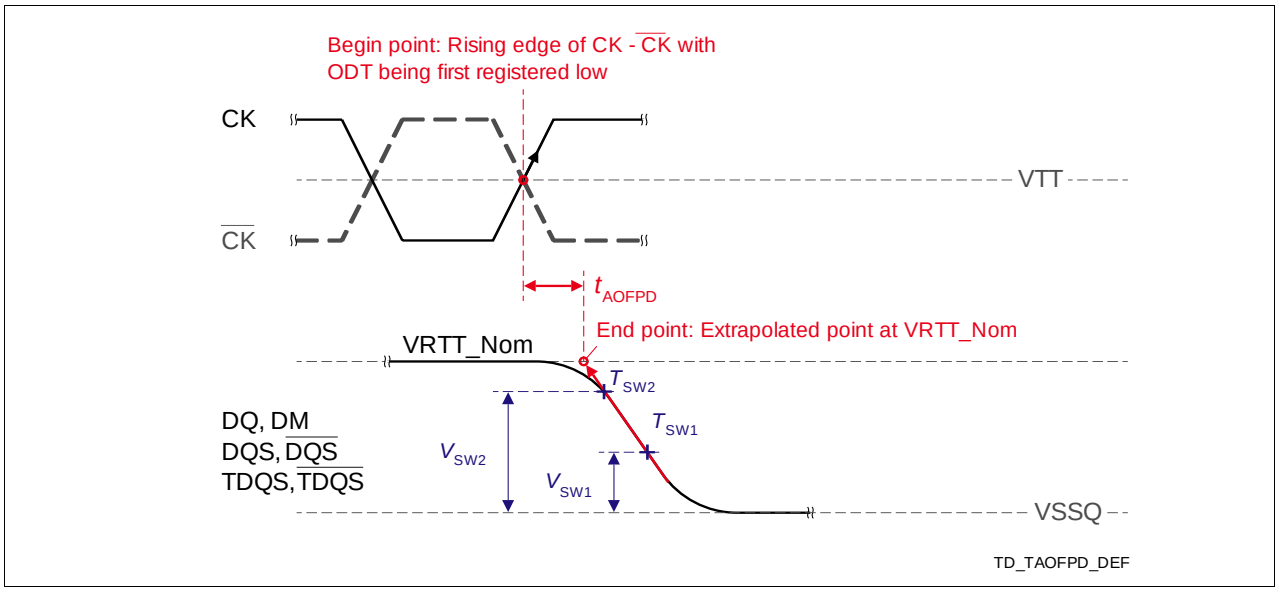
Definition of tAON



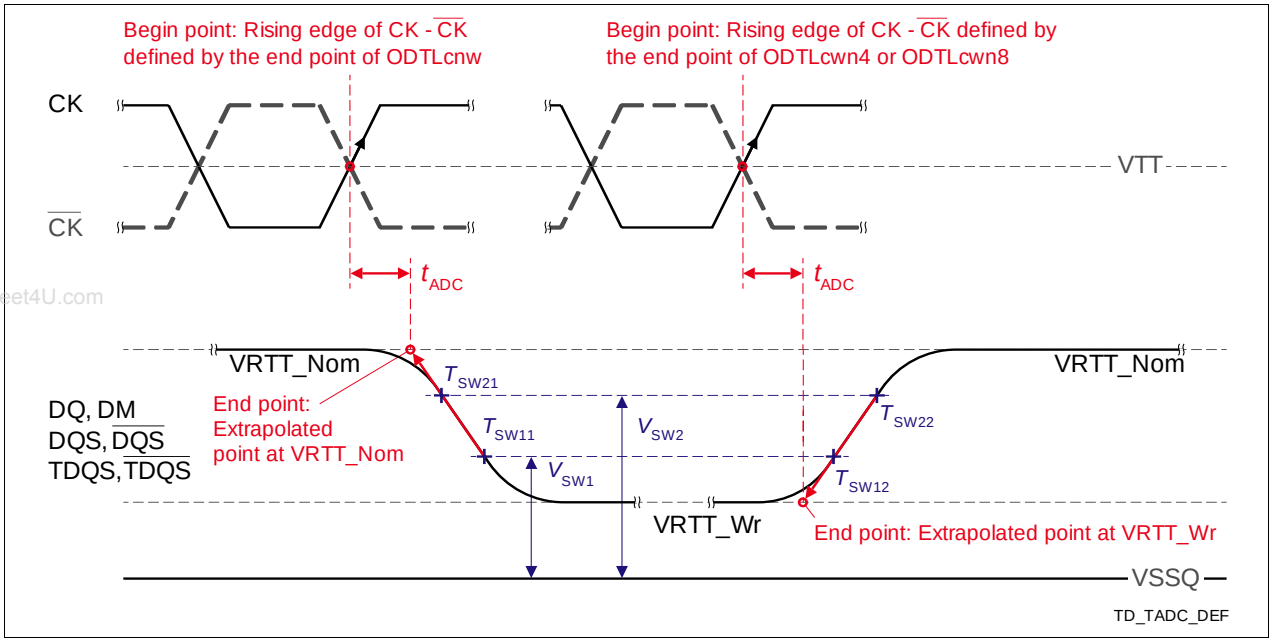
Definition of tAONPD



Definition of tAOF



Definition of tAOFPD



Definition of tADC

8. IDD Specification Parameters and Test Conditions

8.1 IDD Measurement Conditions

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

Table number	Measurement Conditions
Table on page 36	IDD0 and IDD1
Table on page 37	IDD2N, IDD2Q, IDD2P(0), IDD2P(1)
Table on page 38	IDD3N and IDD3P
Table on page 38	IDD4R, IDD4W, IDD7
Table on page 40	IDD7 for different Speed Grades and different tRRD, tFAW conditions
Table on page 40	IDD5B
Table on page 41	IDD6, IDD6ET (optional), IDD6TC (optional)

Within the tables about IDD measurement conditions, the following definitions are used:

LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.).

STABLE is defined as inputs are stable at a HIGH or LOW level.

FLOATING is defined as inputs are VREF = VDDQ / 2.

SWITCHING is defined as described in the following 2 tables.

Definition of SWITCHING for Address and Command Input Signals

SWITCHING for **Address (row, column) and Command Signals ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)** is defined as:	
Address (row, column)	If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax ..... please see each IDDx definition for details
Bank address	If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } = {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } = {HIGH, HIGH,HIGH,HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details and figures 1,2,3 as examples.

Definition of SWITCHING for Data (DQ)

SWITCHING for **Data (DQ)** is defined as	
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures 1,2,3 as examples.
Data Masking (DM)	NO Switching; DM must be driven LOW all the time

Timing parameters are listed in the following table:

For IDD testing the following parameters are utilized.

Parameter Bin		DDR3-800		DDR3-1066			DDR3-1333			DDR3-1600			Unit
		5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	8-8-8	9-9-9	101010	
t_{CKmin}(IDD)		2.5		1.875			1.5			1.25			ns
CL(IDD)		5	6	6	7	8	7	8	9	8	9	10	
t_{RCDmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{RCmin}(IDD)		50	52.5	48.75	50.63	52.50	46.5	48	49.5	tbd	tbd	tbd	ns
t_{RASmin}(IDD)		37.5	37.5	37.5	37.5	37.5	36	36	36	tbd	tbd	tbd	ns
t_{RPmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{FAW}(IDD)	x4/x8	40	40	37.5	37.5	37.5	30	30	30	30	30	30	ns
	x16	50	50	50	50	50	45	45	45	40	40	40	ns
t_{RRD}(IDD)	x4/x8	10	10	7.5	7.5	7.5	6.0	6.0	6.0	6.0	6.0	6.0	ns
	x16	10	10	10	10	10	7.5	7.5	7.5	7.5	7.5	7.5	ns
t_{RFC}(IDD) -512Mb		90	90	90	90	90	90	90	90	90	90	90	ns
t_{RFC}(IDD) -1 Gb		110	110	110	110	110	110	110	110	110	110	110	ns
t_{RFC}(IDD) - 2 Gb		160	160	160	160	160	160	160	160	160	160	160	ns
t_{RFC}(IDD) - 4 Gb		tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	ns

The following conditions apply:

IDD specifications are tested after the device is properly initialized.

Input slew rate is specified by AC Parametric test conditions.

IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0 -> One Bank Activate -> Precharge**	**Operating Current 1 -> One Bank Activate -> Read -> Precharge**
Measurement Condition		
Timing Diagram Example		Figure 1
CKE	HIGH	HIGH
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	t_{RCmin}(IDD)	t_{RCmin}(IDD)
t_{RAS}	t_{RASmin}(IDD)	t_{RASmin}(IDD)
t_{RCD}	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.
CL	n.a.	CL(IDD)
AL	n.a.	0
$\overline{CS}$	HIGH between. Activate and Precharge Commands	HIGH between Activate, Read and Precharge
Command Inputs ($\overline{CS}$,$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in table only exceptions are Activate and Precharge commands; example of IDD0 pattern: **A0**DDDDDDDDDDDDD **P0** (DDR3-800: t_{RAS} = 37.5ns between (A)ctivate and (P)recharge to bank 0; Definition of D and $\overline{D}$: see <Hyperlink>Table)	SWITCHING as described in Table ; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: **A0**DDDD**R0**DDDDDDDDD **P0** (DDR3-800 -555: t_{RCD} = 12.5ns between (A)ctivate and (R)ead to bank **0**; Definition of D and $\overline{D}$: see Table)
Row, Column Addresses	Row addresses SWITCHING as described in Table ; Address Input A10 must be LOW all the time!	Row addresses SWITCHING as described in Table ; Address Input A10 must be LOW all the time!
Bank Addresses	bank address is fixed (bank 0)	bank address is fixed (bank 0)
Data I/O	SWITCHING as described in <Hyperlink>Table	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA, the output buffer should be switched off by MR1 Bit A12 set to "1". When there is no read data burst from DRAM, the DQ I/O should be FLOATING.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-RD-PRE loop

IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0 -> One Bank Activate -> Precharge**	**Operating Current 1 -> One Bank Activate -> Read -> Precharge**
Idle banks	all other	all other
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.

IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

Current	I_{DD2N}	I_{DD2P}(1) [a]	I_{DD2P}(0)	I_{DD2Q}
Name	**Precharge Standby Current**	**Precharge Power Down Current Fast Exit - MRS A12 Bit = 1**	**Precharge Power Down Current Slow Exit - MRS A12 Bit = 0**	**Precharge Quiet Standby Current**
Measurement Condition				
Timing Diagram Example	Figure			
CKE	HIGH	LOW	LOW	HIGH
External Clock	on	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE	STABLE	HIGH
Bank Address, Row Addr. and Command Inputs	SWITCHING as described in Table	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.	n.a.	n.a.
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	Fast Exit / 1 (any valid command after tXP[b])	Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL)	n.a.

a. In DDR3, the MRS Bit 12 defines DLL on/off behaviour ONLY for precharge power down. There are 2 different Precharge Power Down state possible: one with DLL on(fast exit, bit 12=1) and one with DLL off(slow exit, bit 12=0).

b. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh Mode-Register Set, Enter-Self Refresh.

IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

Current	I_{DD3N}	I_{DD3P}
Name	**Active Standby Current**	**Active Power-Down Current[a] Always Fast Exit**
Measurement Condition		
Timing Diagram Example	Figure	
CKE	HIGH	LOW
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE
Addr. and cmd Inputs	SWITCHING as described in Table	STABLE
Data inputs	SWITCHING as described in Table	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all	all
Idle banks	none	none
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	n.a.(Active Power Down Mode is always "Fast Exit" with DLL on)

a.DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit 12 will be used to switch between two different precharge power down modes.

IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
Measurement Condition			
Timing Diagram Example	<Hyperlink>Figure		
CKE	HIGH	HIGH	HIGH
External Clock	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	t_{RCmin}(IDD)
t_{RAS}	n.a.	n.a.	t_{RASmin}(IDD)
t_{RCD}	n.a.	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.	t_{RRDmin}(IDD)
CL	CL(IDD)	CL(IDD)	CL(IDD)
AL	0	0	t_{RCDmin} - 1 t_{CK}

IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
$\overline{CS}$	HIGH btw. valid cmds	HIGH btw. valid cmds	HIGH btw. valid cmds
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table; exceptions are Read commands => IDD4R Pattern: **R0**D$\overline{DD}$**R1**D$\overline{DD}$**R2**D$\overline{DD}$**R3** .D$\overline{DD}$ **R4** ..... Rx = Read from bank x; Definition of D and $\overline{D}$: see Table	SWITCHING as described in Table; exceptions are Write commands => IDD4W Pattern: **W0**D$\overline{DD}$**W1**D$\overline{DD}$**W2**D$\overline{DD}$**W3** D$\overline{DD}$ **W4** ... Wx = Write to bank x; Definition of D and $\overline{D}$: see Table	For patterns see Table
Row, Column Addresses	column addresses SWITCHING as described in Table; Address Input A10 must be LOW all the time!	column addresses SWITCHING as described in Table; Address Input A10 must be LOW all the time!	STABLE during DESELECTs
Bank Addresses	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...), see pattern in Table
DQ I/O	Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.	Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle. DM is low all the time.	Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	all	all	all, rotational
Idle banks	none	none	none
Precharge Power Down Mode / Mode Register Bit	n.a.	n.a.	n.a.

IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

Speed	Bin	Org.	tFAW	tFAW	tRRD	tRRD	IDD7 Pattern[a]
Mb/s			[ns]	[CLK]	[ns]	[CLK]	(Note this entire sequence is repeated.)
800	all	x4/x8	40	16	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D
	all	x16	50	20	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
1066	all	x4/x8	37.5	20	7.5	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	50	27	10	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D
1333	all	x4/x8	30	20	6	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D
1600	all	x4/x8	30	24	6	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D
	all	x16	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D D D D D D

a.A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

IDD Measurement Conditions for IDD5B

Current	I_{DD5B}
Name	Burst Refresh Current
Measurement Condition	
CKE	HIGH
External Clock	on
t_{CK}	t_{CKmin}(IDD)
t_{RC}	n.a.
t_{RAS}	n.a.
t_{RCD}	n.a.
t_{RRD}	n.a.
t_{RFC}	t_{RFCmin}(IDD)
CL	n.a.
AL	n.a.
$\overline{CS}$	HIGH btw. valid cmds
Addr. and cmd Inputs	SWITCHING
Data inputs	SWITCHING
Output Buffer DQ,DQS / MR1 bit A12	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]

IDD Measurement Conditions for IDD5B

Current	I_{DD5B}
Name	**Burst Refresh Current**
Burst length	n.a.
Active banks	Refresh command every tRFC=tRFCmin
Idle banks	none
Precharge Power Down Mode / Mode Register Bit	n.a.

IDD Measurement Conditions for IDD6, IDD6ET, and IDD6TC

Current	I_{DD6}	I_{DD6ET} **(Optional)**	**IDD6TC(Optional)**
Name	**Self-Refresh Current Normal Temperature Range** T_{CASE} = 0 .. 85 ℃	**Self-Refresh Current Extended Temperature Range** [a] T_{CASE} = 0 .. 95 ℃	**Auto Self Refresh Current TCASE-See Table**
Measurement Condition			
Temperature	T_{CASE} = 85 ℃	T_{CASE} = 95 ℃	**TCASE-See Table**
Auto Self Refresh (ASR) / MR2 Bit A6	Disabled / "0"	Disalbed / "0"	Enabled / "1"
Self Refresh Temperature Range (SRT) / MR2 Bit A7	Normal / "0"	Extended / "1"	Disabled / "0"
CKE	LOW	LOW	LOW
External Clock	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW
t_{CK}	n.a.	n.a.	n.a.
t_{RC}	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.
$\overline{CS}$	FLOATING	FLOATING	FLOATING
Command Inputs ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	FLOATING	FLOATING	FLOATING
Row, Colum Addresses	FLOATING	FLOATING	FLOATING
Bank Addresses	FLOATING	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.	n.a.
Active banks	all during self-refresh actions	all during self-refresh actions	all during self-refresh actions

IDD Measurement Conditions for IDD6, IDD6ET, and IDD6TC

Current	I_{DD6}	I_{DD6ET} (Optional)	IDD6TC(Optional)
Name	**Self-Refresh Current Normal Temperature Range** T_{CASE} = 0 .. 85 ℃	**Self-Refresh Current Extended Temperature Range** [a] T_{CASE} = 0 .. 95 ℃	**Auto Self Refresh Current TCASE-See Table**
Idle banks	all btw. Self-Refresh actions	all btw. Self-Refresh actions	all btw. Self-Refresh actions
Precharge Power Down Mode / MR0 bit A12	n.a.	n.a.	n.a.

a. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

8.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} Specification

Speed Grade Bin	DDR3 - 800 5-5-5	DDR3 - 1066 7-7-7	DDR3 - 1333 8-8-8	DDR3 - 1600 9-9-9	Unit	Notes
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	TBD	TBD	TBD	TBD	mA	x4/x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD1}	TBD	TBD	TBD	TBD	mA	x4/x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD2P} (0) slow exit	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD2P} (1) fast exit	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD2N}	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD2Q}	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD3P} (fast exit)	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD3N}	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD4R}	TBD	TBD	TBD	TBD	mA	x4
	TBD	TBD	TBD	TBD	mA	x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD4W}	TBD	TBD	TBD	TBD	mA	x4
	TBD	TBD	TBD	TBD	mA	x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD5B}	TBD	TBD	TBD	TBD	mA	x4/x8/x16
I_{DD6}	TBD	TBD	TBD	TBD	mA	x4/x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD6ET}	TBD	TBD	TBD	TBD	mA	x4/x8
	TBD	TBD	TBD	TBD	mA	x16
I_{DD7}	TBD	TBD	TBD	TBD	mA	x4/x8
	TBD	TBD	TBD	TBD	mA	x16

8.2.1 IDD6 Current Definition

Symbol	Parameter/Condition
I_{DD6}	Normal Temperature Range Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 0.
I_{DD6ET}	Extended Temperature Range Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 1.
I_{DD6TC}	Auto Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable when ASR is enabled by MR2 settings A6 = 1 and A7 = 0.

8.2.2 IDD6TC Specification (see notes 1~2)

Symbol	Temperature Range	Value	Unit	Notes
I_{DD6}	0 - 85 ^{o}C		mA	3,4
I_{DD6ET}	0 - 95 ^{o}C		mA	5,6
I_{DD6TC}	0 ^{o}C ~ T_a		mA	6,7,8
	T_b ~ T_y		mA	6,7,8
	T_z ~ $T_{OPERmax}$		mA	6,7,8

1. Some IDD currents are higher for x16 organization due to larger page size architecture.
2. Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6=0 and A7=0.
4. Supplier data sheets include a max value for IDD6.
5. Applicable for MR2 settings A6=0 and A7=1. IDD6ET is only specified for devices which support the Extended Temperature Range feature.
6. Refer to the supplier data sheet for the value specification method (e.g. max, typical) for IDD6ET and IDD6TC
7. Applicable for MR2 settings A6=1 and A7=0. IDD6TC is only specified for devices which support the Auto Self Refresh feature.
8. The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of TOPER. Refer to supplier data sheet for more information.

9. Input/Output Capacitance

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	TBD	TBD	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
Input capacitance delta CK and CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	C_I	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	pF	2,3,6
Input capacitance delta, DQS and DQS#	C_{DDQS}	0	0.20	0	0.20	0	0.15	0	0.15	pF	2,3,5
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, DQS#)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11

Notes:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#.
5. The minimum C_{CK} will be equal to the minimum C_I.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CTRL pins defined as ODT, CS and CKE.
8. C_{DI_CTRL}=C_I(CNTL) - 0.5 * C_I(CLK) + C_I(CLK#))
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(CLK#))
11. C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))

10. Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-800 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50..								
Speed Bin			**DDR3-800D**		**DDR3-800E**		**Unit**	**Notes**
CL - nRCD - nRP			**5-5-5**		**6-6-6**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	12.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	12.5	—	15	—	ns	
PRE command period		t_{RP}	12.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	50	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1)2)3)
Supported CL Settings			5, 6		6		n_{CK}	
Supported CWL Settings			5		5		n_{CK}	

DDR3-1066 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50.

Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL - nRCD - nRP			6-6-6		7-7-7		8-8-8			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	11.25	—	13.125	—	15	—	ns	
PRE command period		t_{RP}	11.25	—	13.125	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75	—	50.625	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	
Supported CWL Settings			5, 6		5, 6		5, 6		n_{CK}	

DDR3-1333 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50..

Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Unit	Note
CL - nRCD - nRP			7-7-7		8-8-8		9-9-9		10-10-10			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	10.5	20	12	20	13.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	10.5	—	12	—	13.5	—	15	—	ns	
PRE command period		t_{RP}	10.5	—	12	—	13.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	46.5	—	48	—	49.5	—	51	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9		5, 6, 7, 8, 9		6, 8, 9		6, 8, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	

DDR3-1600 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50..

Speed Bin			DDR3-1600G (optional)		DDR3-1600H		DDR3-1600J		DDR3-1600K (optional)		Unit	Note
CL - nRCD - nRP			8-8-8		9-9-9		10-10-10		11-11-11			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	10	20	11.25	20	12.5	20	13.75	20	ns	
ACT to internal read or write delay time		t_{RCD}	10	—	11.25	—	12.5	—	13.75	—	ns	
PRE command period		t_{RP}	10	—	11.25	—	12.5	—	13.75	—	ns	
ACT to ACT or REF command period		t_{RC}	45	—	46.25	—	47.5	—	48.75	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	Reserved		ns	1,2,3,4,8
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9, 10		5, 6, 7, 8, 9, 10		5, 6, 7, 8, 9, 10		6, 8, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

11. Electrical Characteristics and AC Timing

Timing Parameters by Speed Bin

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See "10. Standard Speed Bins" on page 46.								ps	f
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Absolute Clock Period	tCK (abs)	tCK (avg) min + tJIT (per) min	tCK (avg) max + tJIT (per) max	tCK (avg) min + tJIT (per) min	tCK (avg) max + tJIT (per) max	tCK (avg) min + tJIT (per) min	tCK (avg) max + tJIT (per) max	tCK (avg) min + tJIT (per) min	tCK (avg) max + tJIT (per) max	ps	
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT(per)	- 100	100	- 90	90	- 80	80	- 70	70	ps	

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Clock Period Jitter during DLL locking period	tJIT (per, lck)	- 90	90	- 80	80	- 70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		140		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	180		160		140		120		ps	
Duty Cycle jitter	tJIT (duty)	-	-	-	-	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR (2per)	-147	147	-132	132	-118	118	-103	103	ps	
Cumulative error across 3 cycles	tERR (3per)	-175	175	-157	157	-140	140	-122	122	ps	
Cumulative error across 4 cycles	tERR (4per)	-194	194	-175	175	-155	155	-136	136	ps	
Cumulative error across 5 cycles	tERR (5per)	-209	209	-188	188	-168	168	-147	147	ps	
Cumulative error across 6 cycles	tERR (6per)	-222	222	-200	200	-177	177	-155	155	ps	
Cumulative error across 7 cycles	tERR (7per)	-232	232	-209	209	-186	186	-163	163	ps	
Cumulative error across 8 cycles	tERR (8per)	-241	241	-217	217	-193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR (9per)	-249	249	-224	224	-200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR (10per)	-257	257	-231	231	-205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR (11per)	-263	263	-237	237	-210	210	-184	184	ps	
Cumulative error across 12 cycles	tERR (12per)	-269	269	-242	242	-215	215	-188	188	ps	
Cumulative error across n = 13, 14, ...49, 50 cycles	tERR (nper)	tERR(nper)min = (1 + 0.68ln(n)) * JIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * JIT(per)max								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQ low-impedance time from CK, CK#	tLZ(DQ)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, a
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, a

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75		25		TBD		TBD		ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150		100		TBD		TBD		ps	d, 17
Data Strobe Timing											
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note	0.9	Note	0.9	Note	0.9	Note	tCK (avg)	13, 19 b
DQS, DQS# differential READ Postamble	tRPST	0.3	Note	0.3	Note	0.3	Note	0.3	Note	tCK (avg)	11, 13, b
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK (avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK (avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	- 400	400	- 300	300	- 255	255	- 225	225	ps	13, a
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, a
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	ps	13, 14 a
DQS, DQS# differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	- 0.25	0.25	- 0.25	0.25	- 0.25	0.25	- 0.25	0.25	tCK (avg)	c

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.2	-	tCK (avg)	c
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.2	-	tCK (avg)	c
Command and Address Timing											
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e, 18
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK , 15ns)	-	max (12nCK , 15ns)	-	max (12nCK , 15ns)	-	max (12nCK , 15ns)	-		
ACT to internal read or write delay time	tRCD	Refer to Table on pages 46 to pages 49									e
PRE command period	tRP	Refer to Table on pages 46 to pages 49									e
ACT to ACT or REF command period	tRC	Refer to Table on pages 46 to pages 49									e
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))								nCK	
End of MPR Read burst to MSR for MPR(exit)	tMPRR	1	-	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See “10. Standard Speed Bins” on page 46.									e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK , 10ns)	-	max (4nCK , 7.5ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK, 10ns)	-	max (4nCK, 10ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	ns	e

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	200		125		65		TBD		ps	b, 16
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	275		200		140		TBD		ps	b, 16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	-	-	-	-	65+125		TBD+ 125		ps	b, 16, 27
Calibration Timing											
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	64	-	nCK	23
Reset Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-		
Self Refresh Timings											
Exit Self Refresh to commands not requiring a locked DLL	tXS	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-		
Exit Self Refresh to com-mands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE (min) + 1 nCK	-	tCKE (min) + 1 nCK	-	tCKE (min) + 1 nCK	-	tCKE (min) + 1 nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-		

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5nCK, 10 ns)	-		
Power Down Timings											
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK, 6ns)	-	max (3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK , 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK , 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9 * tREFI	tCKE (min)	9 * tREFI	tCKE (min)	9 * tREFI	tCKE (min)	9 * tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR / tCK (avg))	-	WL4+ (tWR / tCK (avg))	-	WL+4 + (tWR / tCK (avg))	-	WL+4+ (tWR / tCK (avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+ WR + 1	-	WL+4+ WR+ 1	-	WL+4 + WR + 1	-	WL+4+ WR + 1	-	nCK	10

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+ (tWR / tCK (avg))	-	WL+2+ (tWR / tCK (avg))	-	WL+2 + (tWR / tCK (avg))	-	WL+2+ (tWR / tCK (avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL+2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	1	-	nCK	,
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-		
ODT Timings											
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	1	9	1	9	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	ps	7, a
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	8, a
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	a
Write Leveling Timings											
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	3

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 57 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	195	-	TBD	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	195	-	TBD	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	

0.1 Jitter Notes

Specific Note a	When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <=12.(output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR-800 SDRAM has tERR(mper),act,min = -172 ps and tERR(mper),act,max =+ 193 ps, then t DQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = -400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps+ 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!) Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <=12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12
Specific Note b	When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps =+ 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)
Specific Note c	These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
Specific Note d	These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.
Specific Note e	For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
Specific Note f	These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in Table .

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

7. For definition of RTT turn-on time tAON See 4.2.2 “Timing Parameters” on page 93.
8. For definition of RTT turn-off time tAOF See 4.2.2 “Timing Parameters” on page 93.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum postamble is bound by tHZDQS(max)
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Address / Command Setup, Hold and Derating” on page 60.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Data Setup, Hold and Slew Rate Derating” on page 68..
18. Start of internal write transaction is definited as follows:
    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by tLZDQS(min)
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection)of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdrifrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula.

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities. For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as :

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 = 128ms$$

24. n = from 13 cycles to 50 cycles.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following fall ing edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of der ating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier refer ence point [(175 mV - 150 mV) / 1 V/ns].

Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 1) to the ΔtIS and ΔtIH derating value (see Table 2) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 2). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 4).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 3). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 4).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 4).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 2, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 1 — ADD/CMD Setup and Hold Base-Values for 1V/ns

unit [ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	reference
tIS(base)	200	125	65	TBD	$V_{IH/L(ac)}$
tIH(base)	275	200	140	TBD	$V_{IH/L(dc)}$
tIH(base)AC150	-	-	65 + 125	TBD + 125	$V_{IH/L(dc)}$

Note: - (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

- The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns]

Table 2 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based

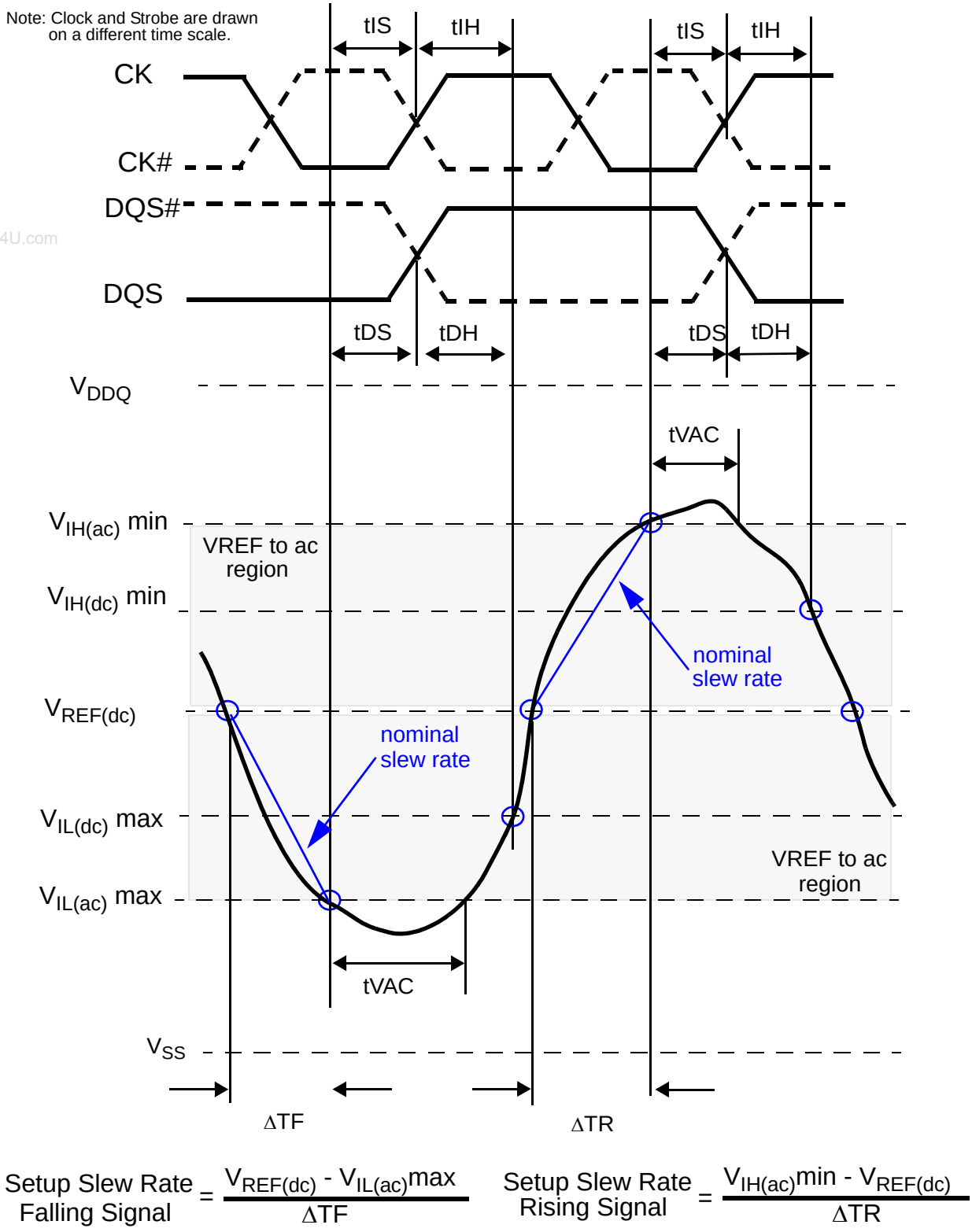
ΔtIS, ΔtIH derating in [ps] AC/DC based AC175 Threshold -> VIH(ac) = VREF(dc) + 175mV, VIL(ac)=VREF(dc) - 175mV																
		CK,CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD / ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 3 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC150 Threshold -> VIH(ac) = VREF(dc) + 150mV, VIL(ac)=VREF(dc) - 150mV																
		CK,CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD / ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 4 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

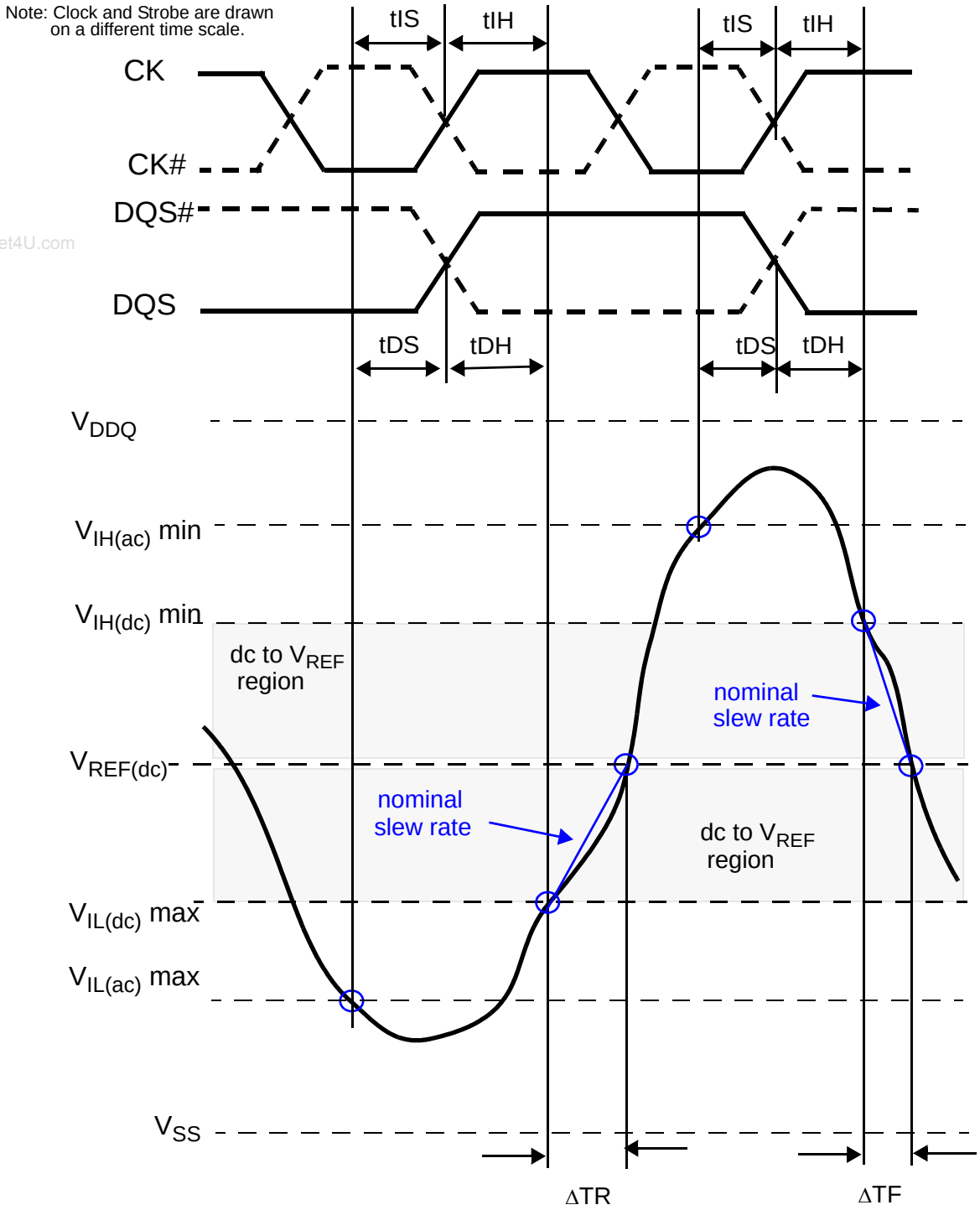
Slew Rate [V/ns]	t_{VAC} @ 175 mV [ps]		t_{VAC} @ 150 mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 1 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 2 — Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

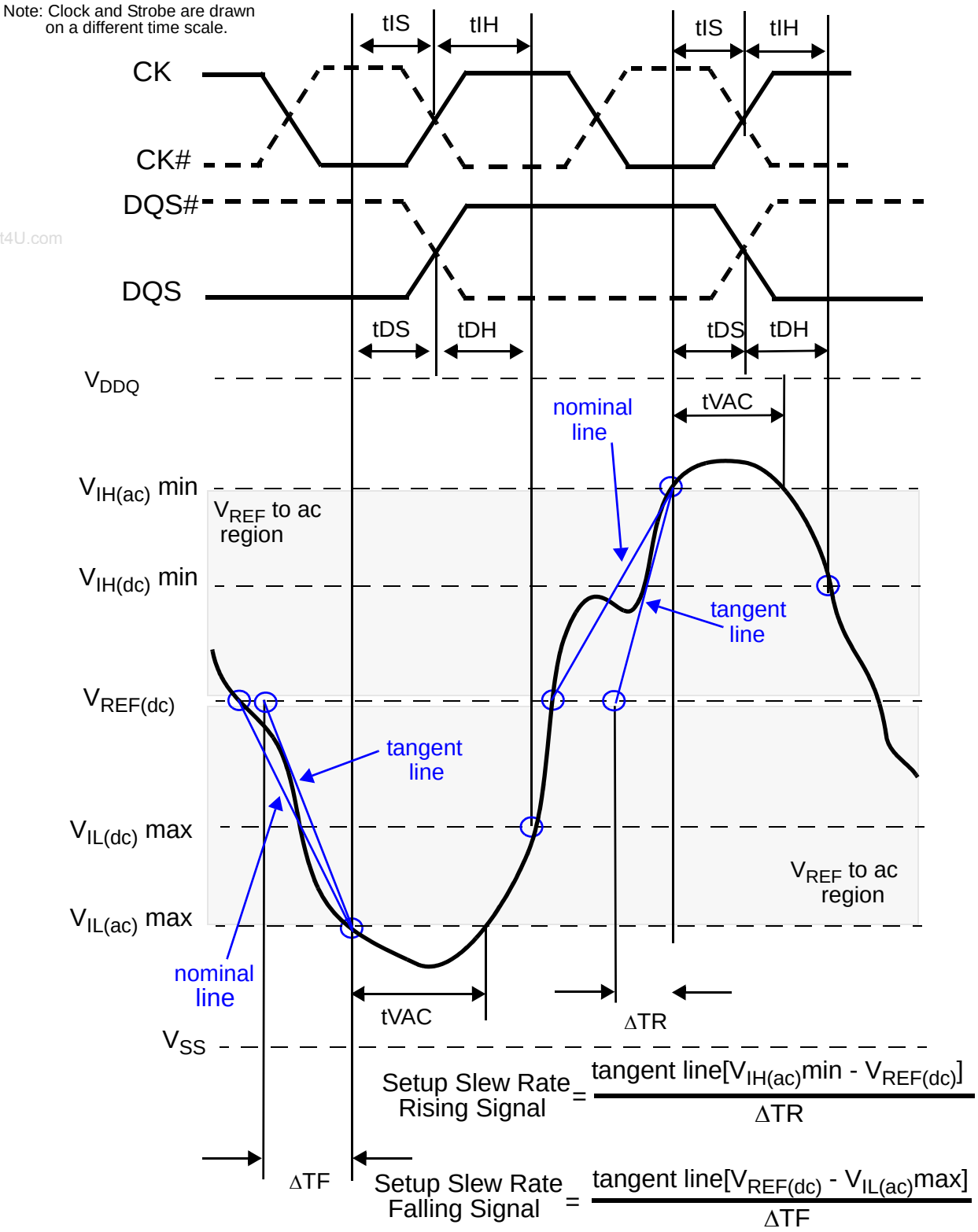
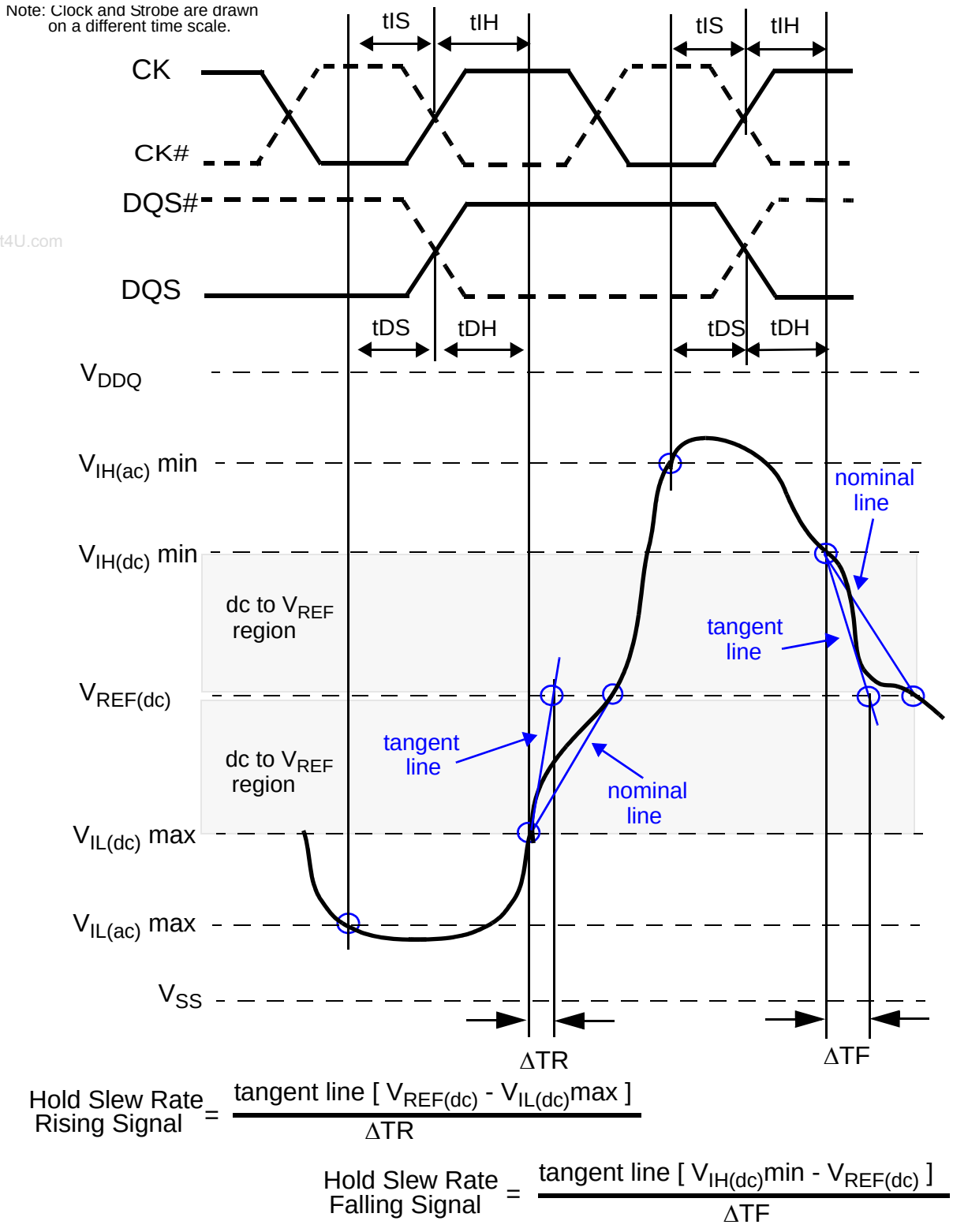


Figure 3 — Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(dc)} - V_{IL(dc)}\text{max} \,]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\, V_{IH(dc)}\text{min} - V_{REF(dc)} \,]}{\Delta TF}$$

Figure 4 — Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 5) to the DtDS and DtDH (see Table 6) derating value respectively. Example: tDS (total setup time) = tDS(base) + DtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 5). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 7).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 6). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see figure 7).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 7).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 5 — Data Setup and Hold Base-Values

Units [ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	reference
tDS(base)	75	25	-10	TBD	$V_{IH/L(ac)}$
tDH(base)	150	100	65	TBD	$V_{IH/L(dc)}$

Note: (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS-slew rate)

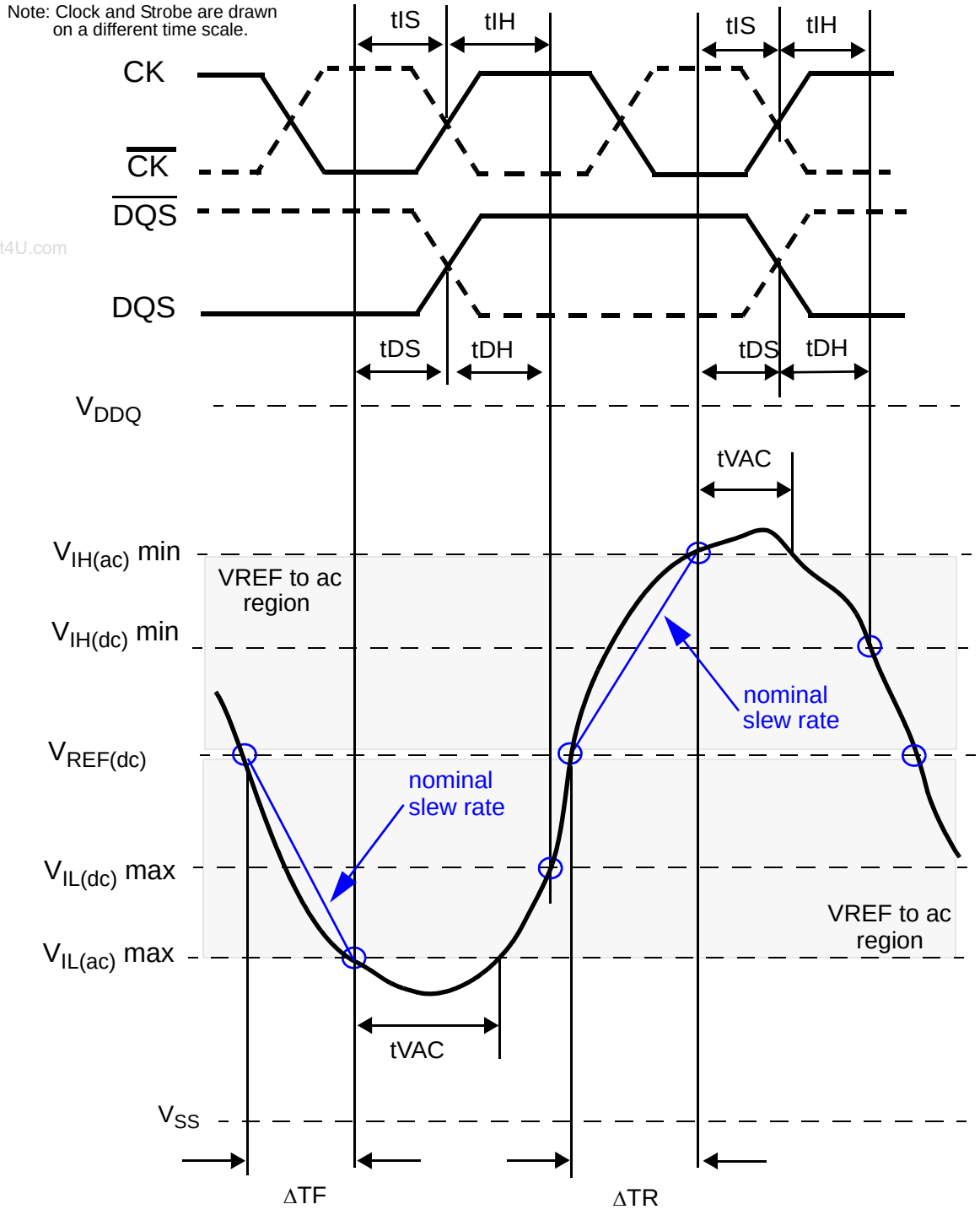
Table 6 — Derating values DDR3-800/1066 tDS/tDH - ac/dc based

ΔtDS, ΔDH derating in [ps] AC/DC based [a]																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

a.Cell contents shaded in red are defined as 'not supported'.

Table 7 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

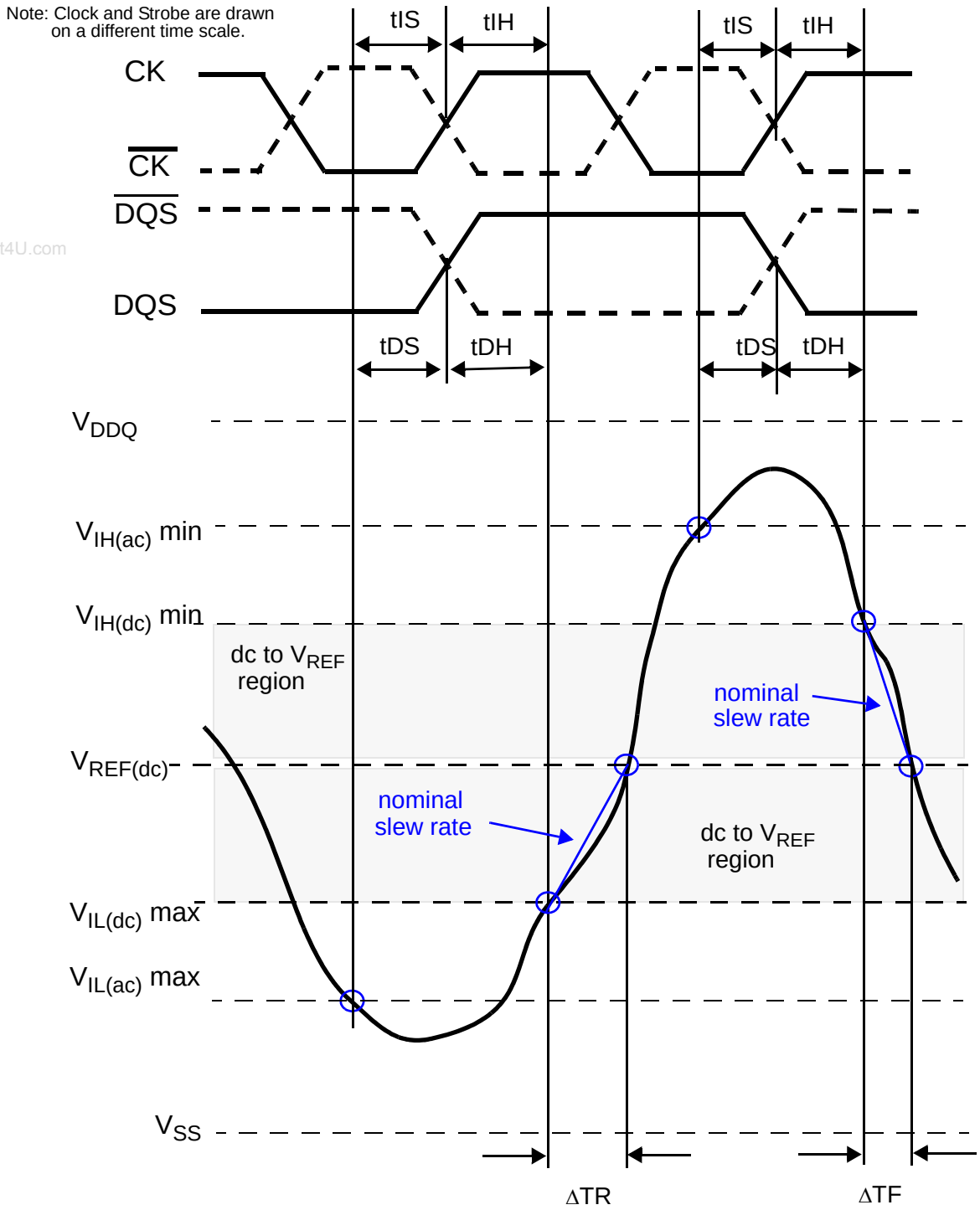
Slew Rate [V/ns]	t_{VAC} [ps]	
	min	max
> 2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
< 0.5	0	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 5 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 6 — Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

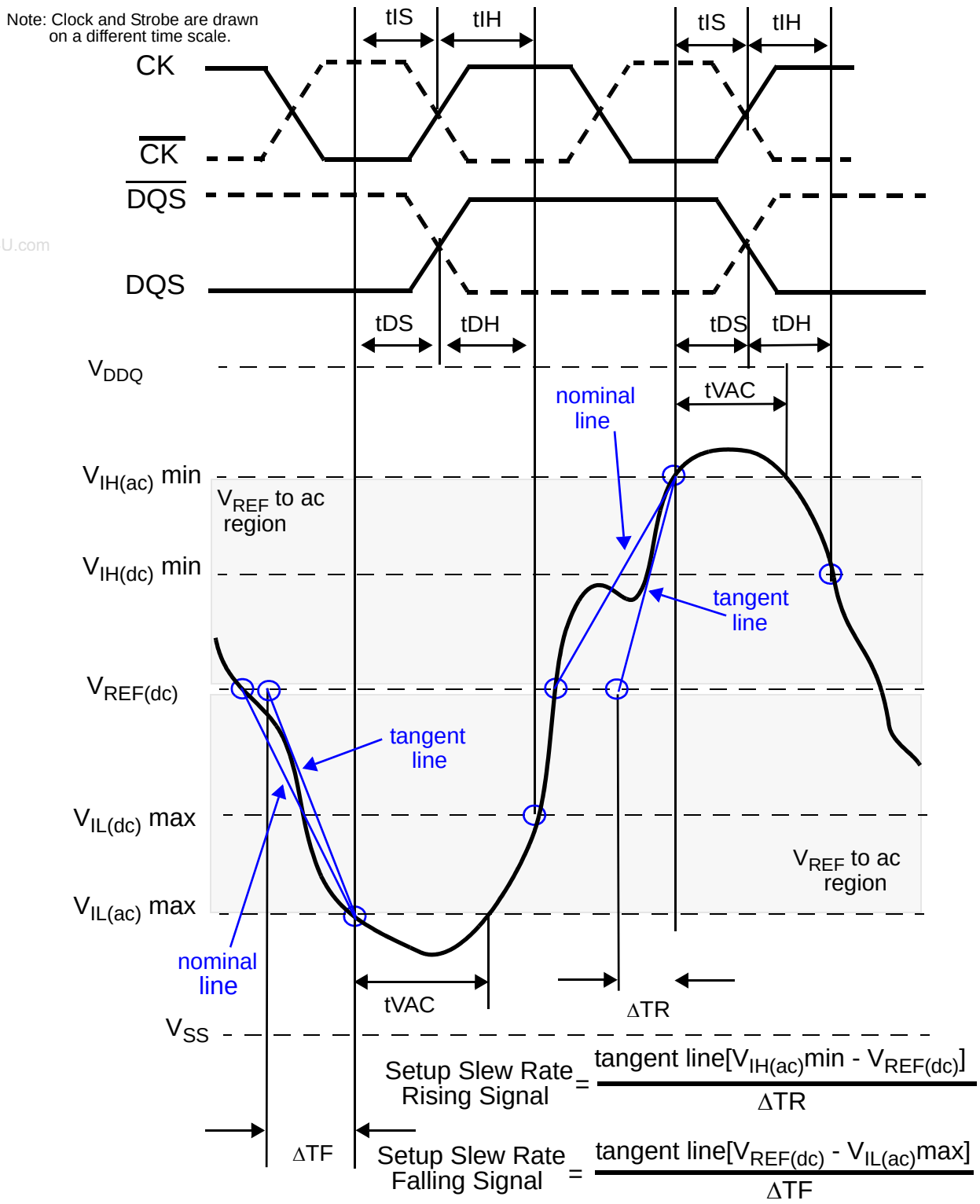


Figure 7 — Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

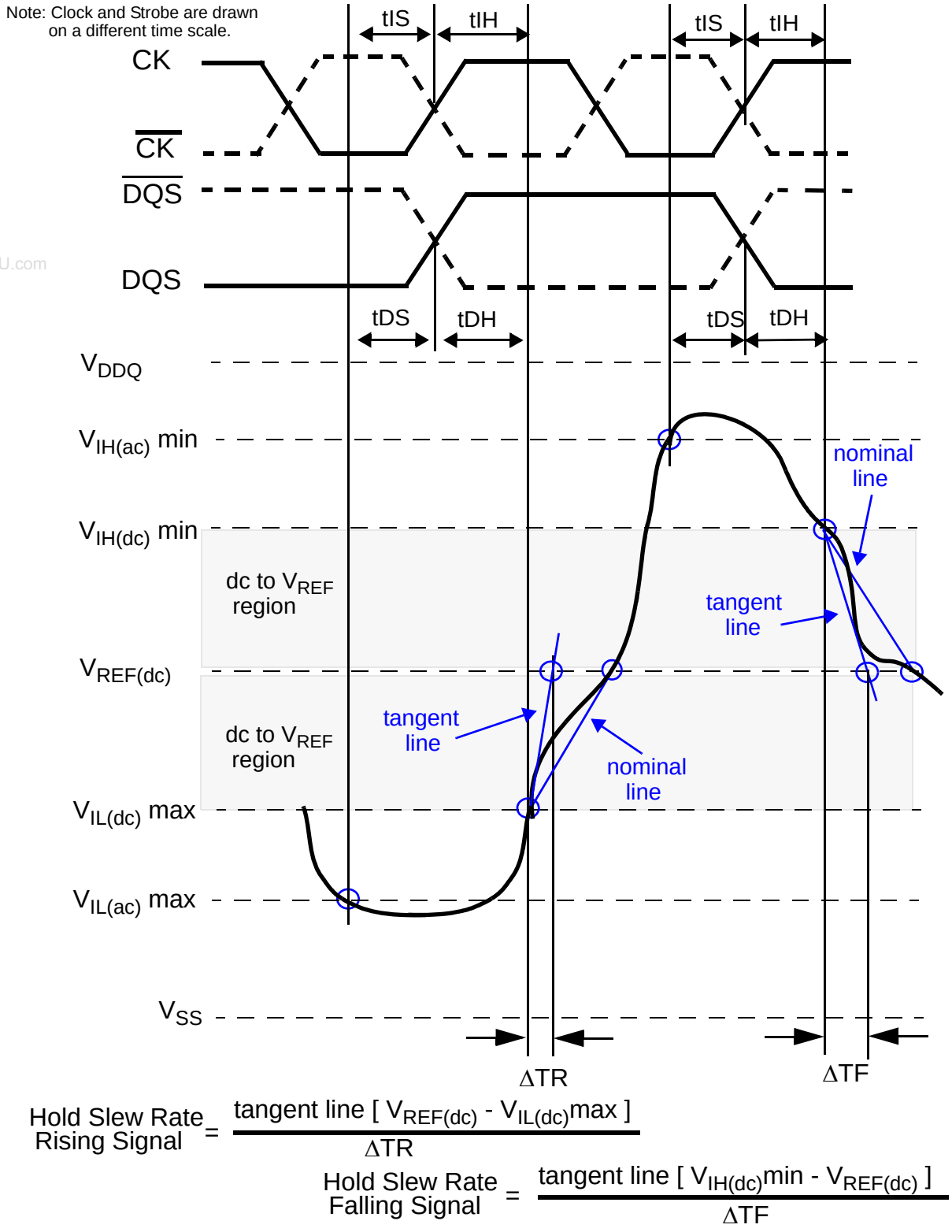
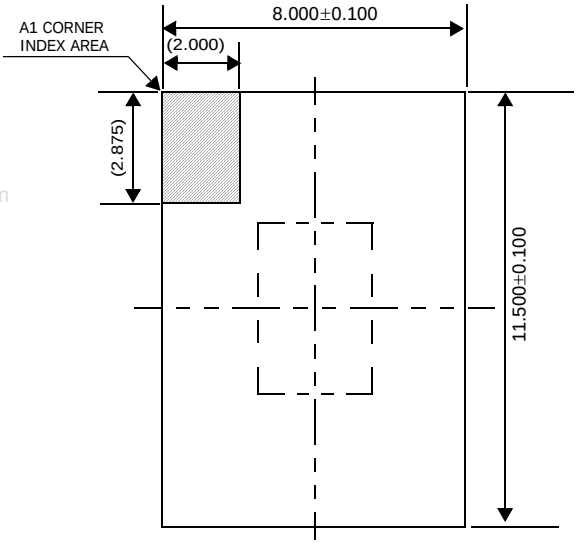


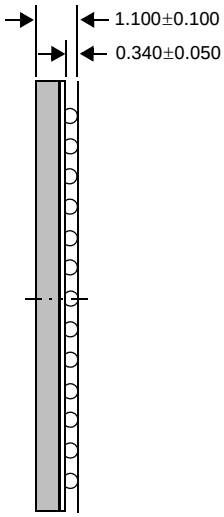
Figure 8 — Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

12. Package Dimensions

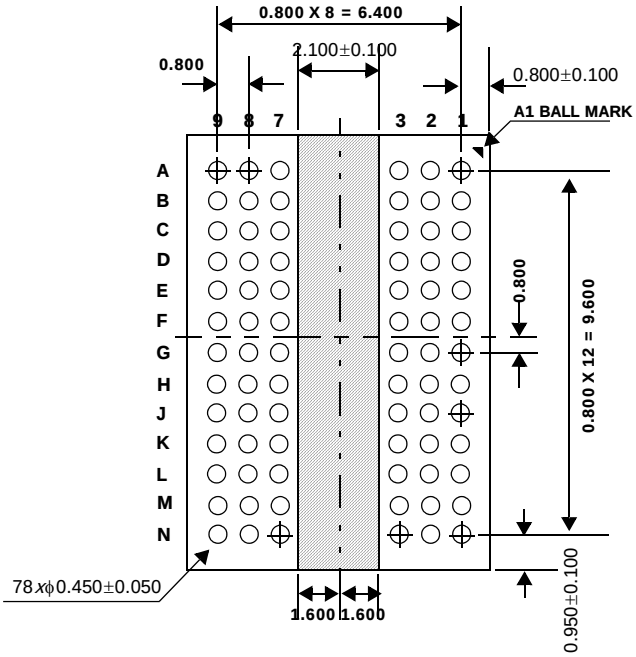
12.1 Package Dimension(x4/x8) ; 78Ball Fine Pitch Ball Grid Array Outline



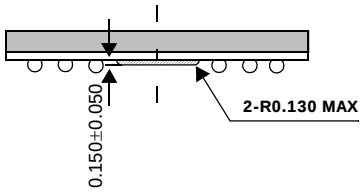
TOP VIEW



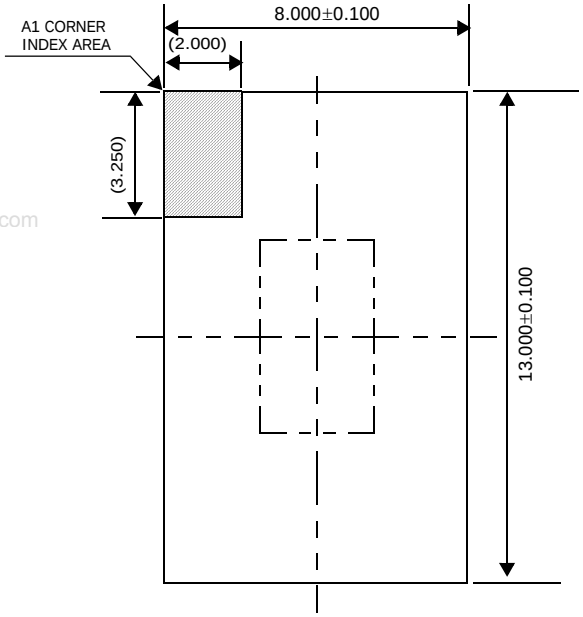
SIDE VIEW



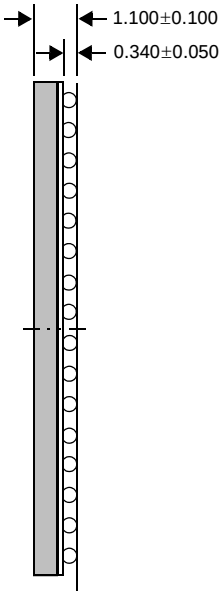
BALL VIEW



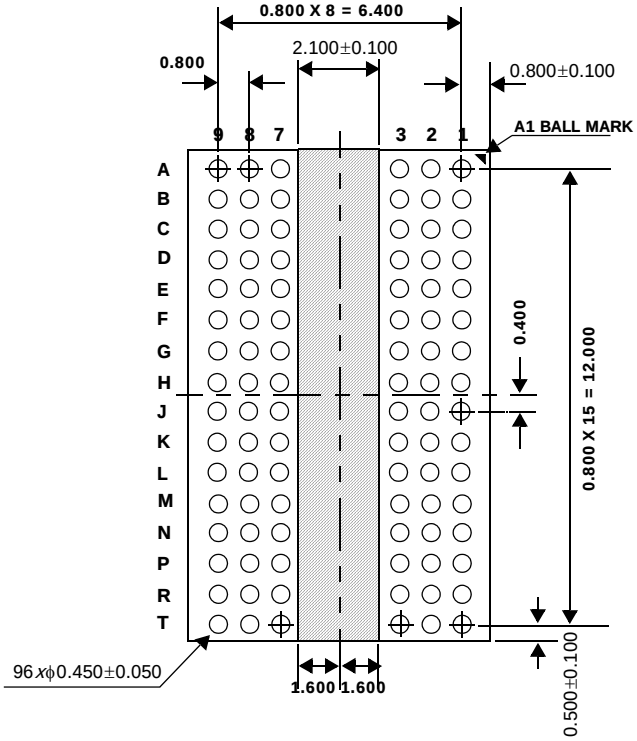
12.2 Package Dimension(x16) ; 96Ball Fine Pitch Ball Grid Array Outline



TOP VIEW



SIDE VIEW



BALL VIEW