H5N3005LD, H5N3005LS, H5N3005LM

Silicon N Channel MOS FET
High Speed Power Switching

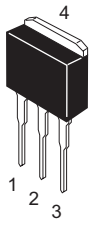
REJ03G1315-0400
Rev.4.00
Nov 08, 2005

Features

- Low on-resistance
- Low leakage current
- High speed switching

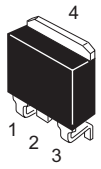
Outline

RENESAS Package code: PRSS0004AE-A
(Package name LDPAK(L))



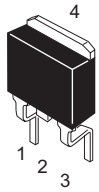
H5N3005LD

RENESAS Package code: PRSS0004AE-B
(Package name LDPAK(S)-(1))

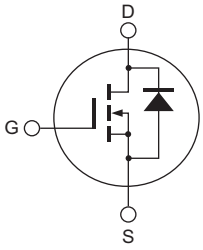


H5N3005LS

RENESAS Package code: PRSS0004AE-C
(Package name LDPAK(S)-(2))



H5N3005LM



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	300	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	15	A
Drain peak current	$I_{D\ (pulse)}$ Note1	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}$ Note1	60	A
Avalanche current	I_{AP} Note3	15	A
Avalanche energy	E_{AR} Note3	13.5	mJ
Channel dissipation	Pch Note2	75	W
Channel to case thermal impedance	θch-c	1.67	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. STch = 25°C, Tch ≤ 150°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	300	—	—	V	I_D = 10 mA, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 300 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 7.5 A, V_{DS} = 10 V Note4
Static drain to source on state resistance	$R_{DS(on)}$	—	0.210	0.255	Ω	I_D = 7.5 A, V_{GS} = 10 V Note4
Input capacitance	Ciss	—	1300	—	pF	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	155	—	pF	
Reverse transfer capacitance	Crss	—	50	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 7.5 A V_{GS} = 10 V R_L = 20 Ω Rg = 10 Ω
Rise time	t_r	—	30	—	ns	
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	
Fall time	t_f	—	15	—	ns	
Total gate charge	Qg	—	49	—	nC	V_{DD} = 240 V V_{GS} = 10 V I_D = 15 A
Gate to source charge	Qgs	—	8	—	nC	
Gate to drain charge	Qgd	—	25	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.86	1.30	V	I_F = 15 A, V_{GS} = 0 Note4
Body-drain diode reverse recovery time	t_{rr}	—	190	—	ns	I_F = 15 A, V_{GS} = 0 di_F/dt = 100 A/µs
Body-drain diode reverse recovery charge	Q_{rr}	—	1.3	—	µC	

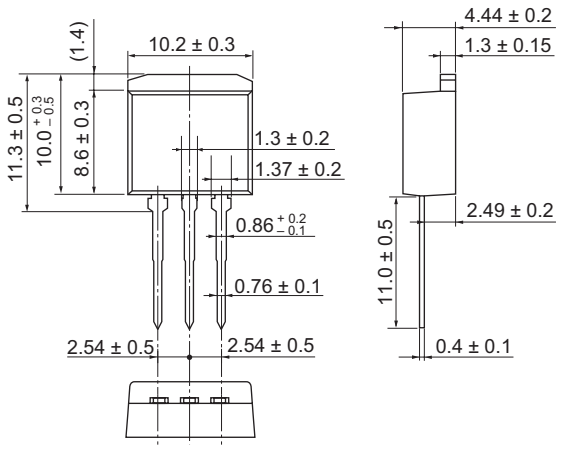
Notes: 4. Pulse test

Package Dimensions

• H5N3005LD

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(L)	—	PRSS0004AE-A	LDPAK(L) / LDPAK(L)V	1.40g

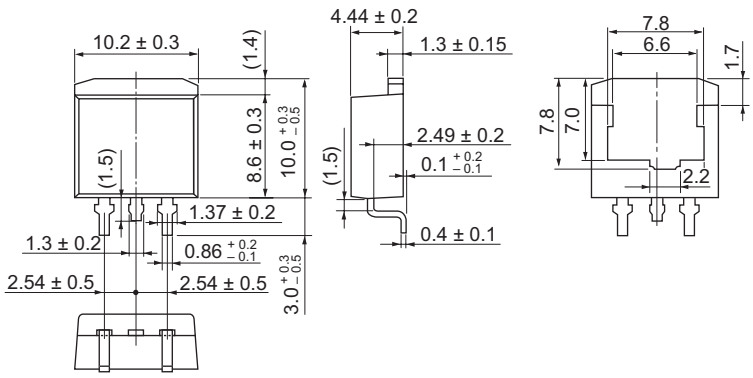
Unit: mm



• H5N3005LS

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(1)	SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g

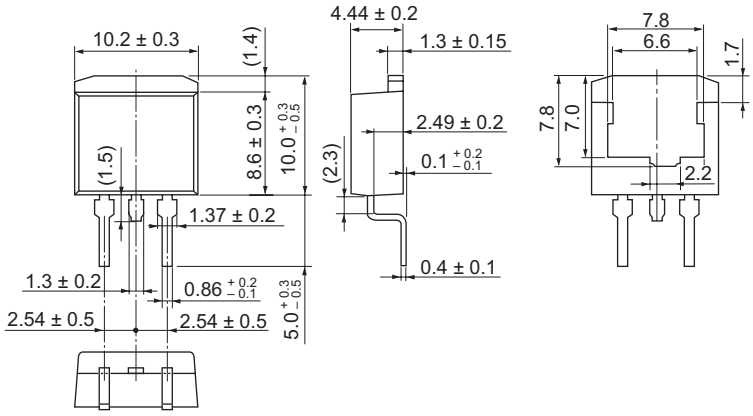
Unit: mm



• H5N3005LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(2)	—	PRSS0004AE-C	LDPAK(S)-(2) / LDPAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H5N3005LSTL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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