H2525

- 239dot (W) x 20 dot (H) graphic and alpha-numeric display
- Control LSI HD61830 attachment type (see page 76)

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 220W x 53H x 15D (max) mm
Effective display area . . . . . 163W x 17H mm
Number of dots . . . . . 239W x 20H dot
Dot size . . . . . 0.55W x 0.55H mm
Pitch . . . . . 0.65W x 0.65H mm
Weight . . . . . about 100g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V
Input "high" voltage (V_{iH}) . . . . . 0.7 x V_{DD}V min.
Input "low" voltage (V_{iL}) . . . . . 0.3 x V_{DD}V max.
Clock frequency (f_{CL2}) . . . . . 210 kHz min.
300 kHz typ.
390 kHz max.
Power supply current (I_{DD}) . . . . . 3mA typ.
(I_{EE}) . . . . . 1 mA typ.
D_1, D_2 = GND, f_{CL2}=300 kHz
Power supply for LCD drive (Recommended) (V_O-V_{EE})
Du=1/20
at Ta= 0°C . . . . . 5.5V typ.
at Ta=25°C . . . . . 5.0V typ.
at Ta=50°C . . . . . 4.0V typ.

OPTICAL DATA . . . . . See page 8

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM single indicates the begining of each display cycle.
2	M	H/L	Control signal for a.c. driving
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	CL2	H→L	Clock signal for shifting the serial data
6	V_{DD}(+5V)	–	Power supply for logic circuit
7	V_{SS}(GND)	–	Ground
8	V_{EE}(−5V)	–	Power supply for LC driving
9	V_O	–	Operating voltage for LC driving
10	NC	–	No connection

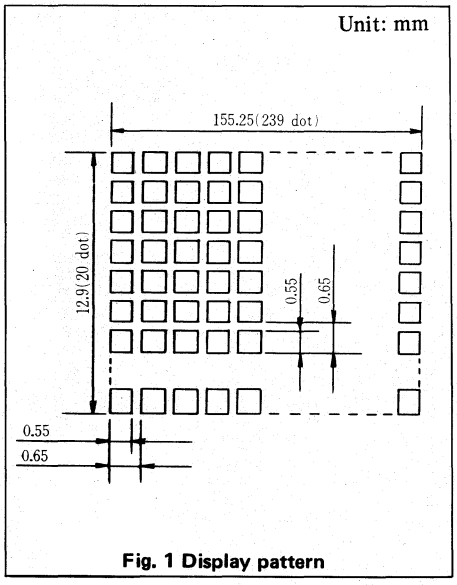


Fig. 1 Display pattern

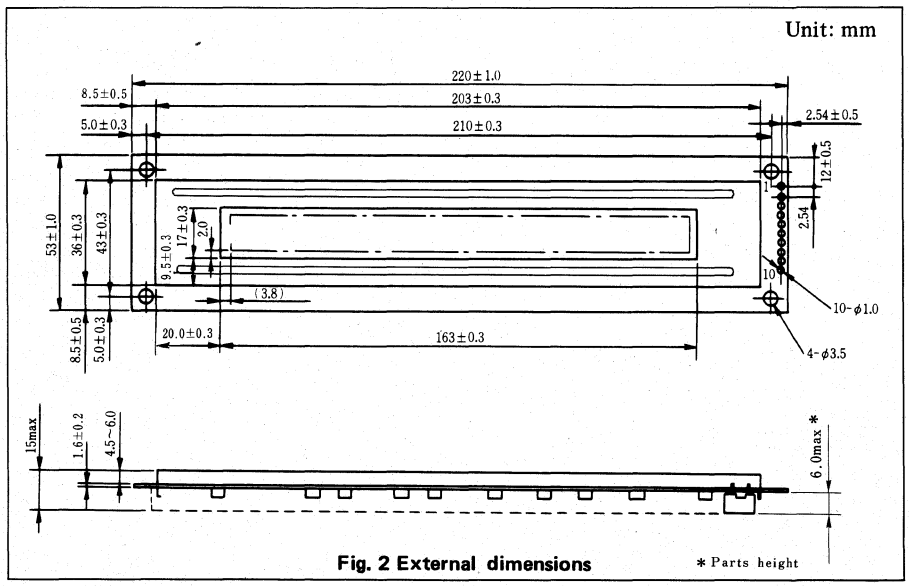


Fig. 2 External dimensions

HITACHI

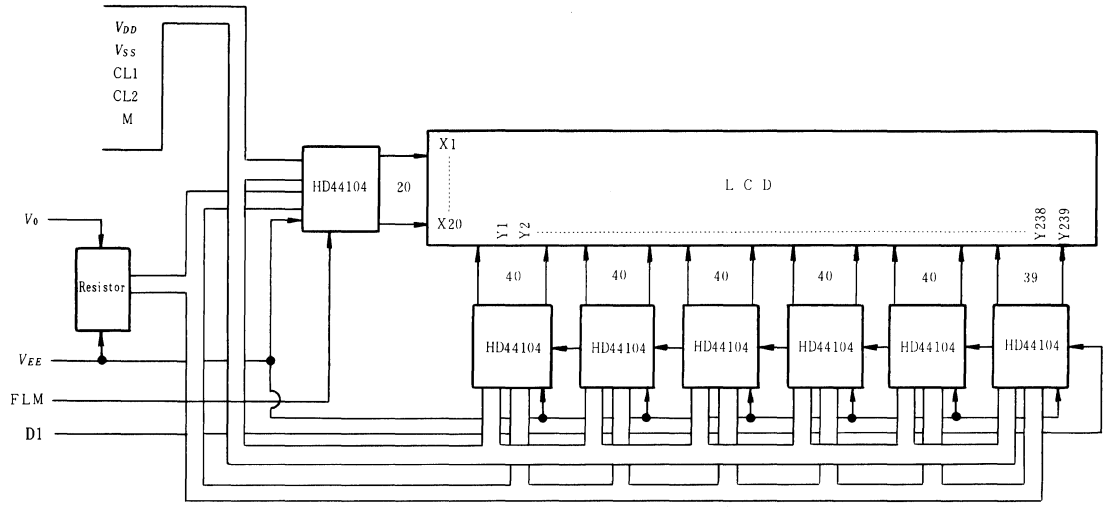
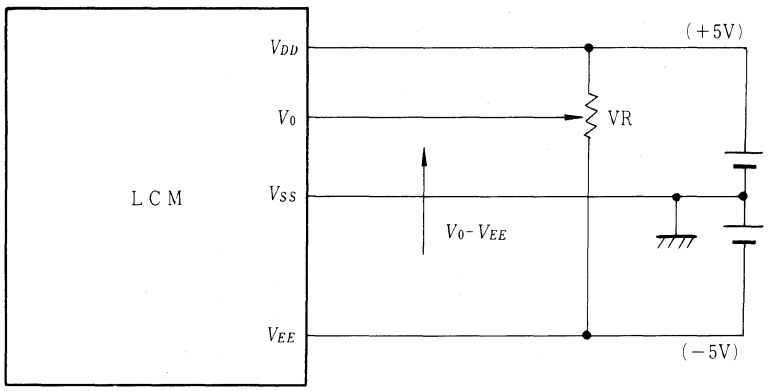


Fig. 3 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Note 1. Optimum frequency for the highest contrast is different by the type of module.

Note 2. Timing of M signal to CLI may be in the range of ±1000ns.

Note 3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50Hz±2Hz or 60Hz ±2Hz) to prevent LCD flicker.

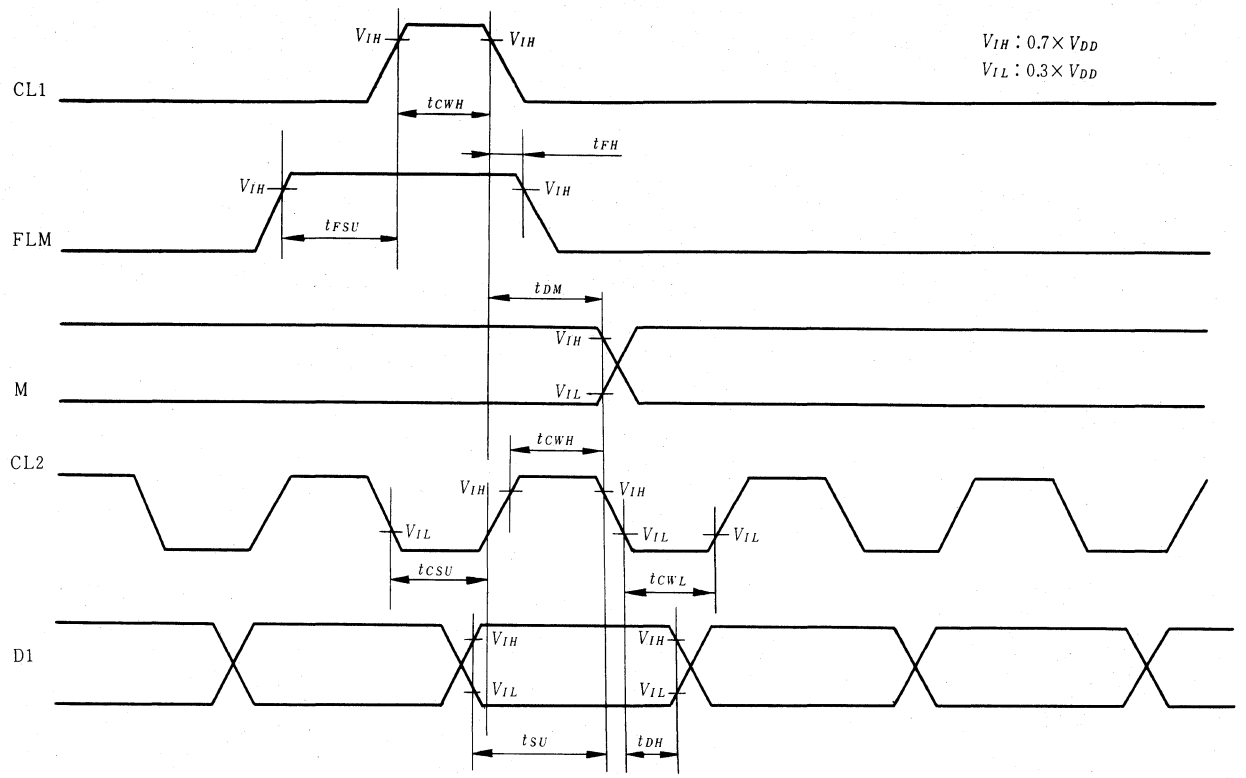


Fig. 5 Interface timing (data write)

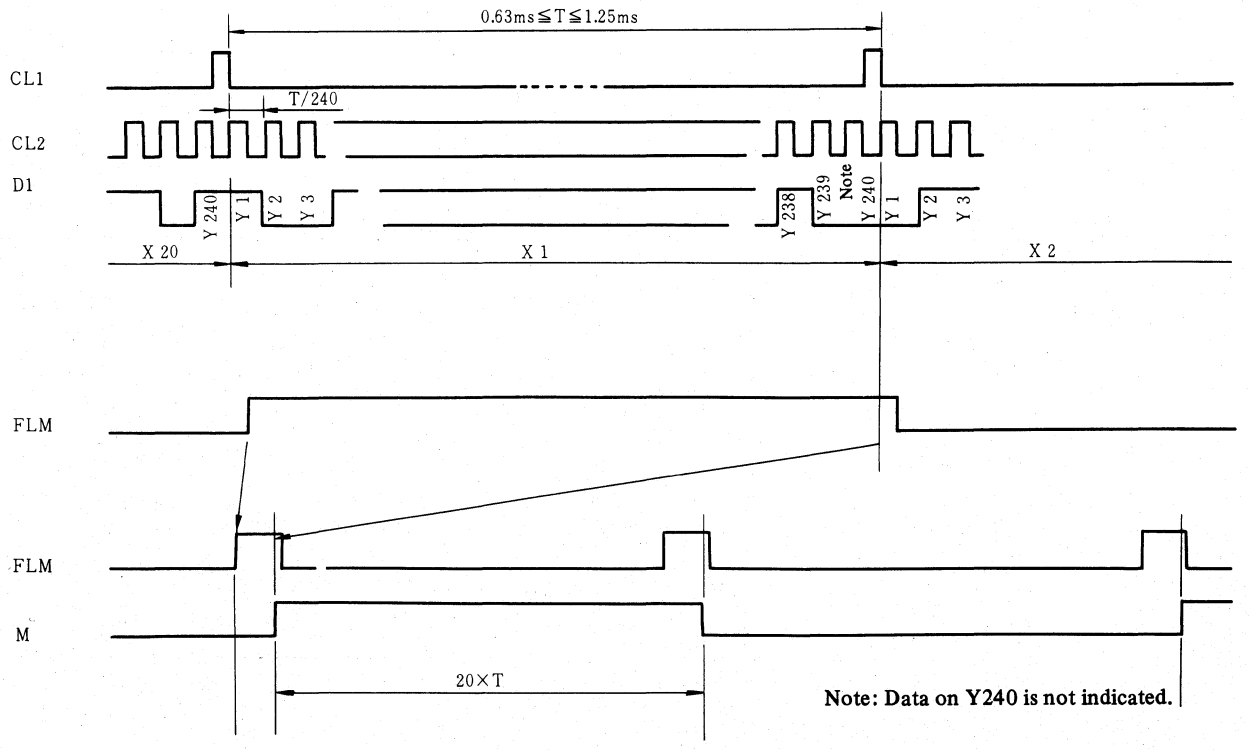


Fig. 6 Interface timing (data read)