GT7122

10MHz, Low Power, CMOS, Rail-to-Rail Dual Operational Amplifier

Advanced

1. Features

- Single-Supply Operation from +2.2V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 10MHz (Typ.)
- Low Input Bias Current: 10pA (Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 800μA per Amplifier (Typ.)
- Operating Temperature: -40°C ~ +125°C
- Available in SOP8 and MSOP8 Packages

2. General Description

The GT7122 is wideband, low-noise, low-distortion dual operational amplifier, that offer rail-to-rail inputs/outputs and single-supply operation down to 2.2V. They draw 1.6mA of quiescent supply current while featuring ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (15nV/√Hz) and low input current-noise density (0.5fA/√Hz). These features make the devices an ideal choice for applications that require low distortion and/or low noise.

These amplifiers have inputs and outputs which swing rail-to-rail and their input common-mode voltage range includes ground. The maximum input offset of these amplifiers is less than 5mV. The GT7122 are unity-gain stable with a gain-bandwidth product of 10MHz.The GT7122 is available in SOP8 and MSOP8 packages. The extended temperature range of -40°C to +125°C over all supply voltages offers additional design flexibility.

3. Applications

- Portable Equipment
- Mobile Communications
- Smoke Detector
- Sensor Interface
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

4. Pin Configuration

4.1 GT7122 SOP8 and MSOP8 (Top View)

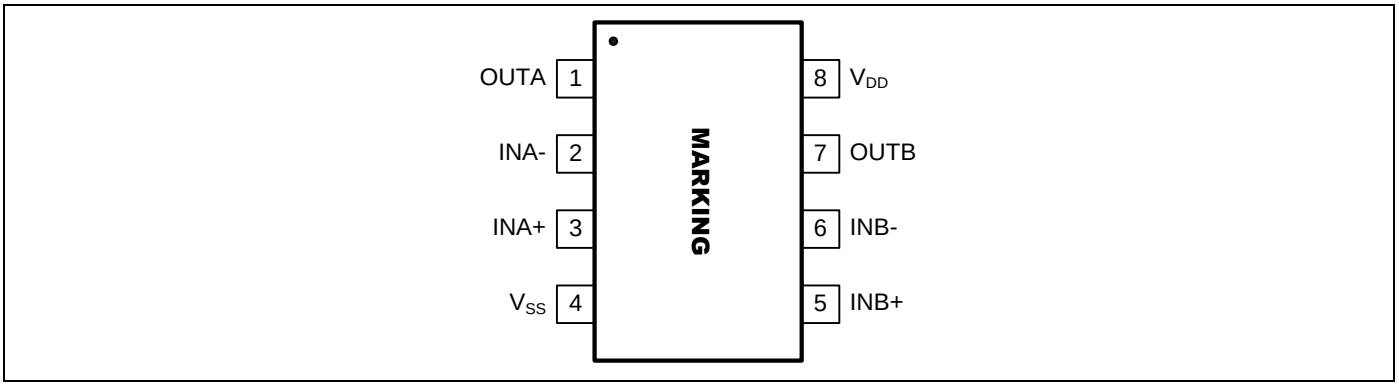


Figure 1. Pin Assignment Diagram (SOP8 and MSOP8 Package)

Note: Please see section "**Part Markings**" for detailed Marking Information.

5. Application Information

5.1 Size

GT7122 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the GT7122 series packages save space on printed circuit boards and enable the design of smaller electronic products.

5.2 Power Supply Bypassing and Board Layout

GT7122 series operates from a single 2.2V to 5.5V supply or dual ±1.1V to ±2.75V supplies. For best performance, a 0.1μF ceramic capacitor should be placed close to the V_{DD} pin in single supply operation. For dual supply operation, both V_{DD} and V_{SS} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors.

5.3 Low Supply Current

The low supply current (typical 800μA) of GT7122 series will help to maximize battery life. They are ideal for battery powered systems

5.4 Operating Voltage

GT7122 series operate under wide input supply voltage (2.2V to 5.5V). In addition, all temperature specifications apply from -40 °C to +125 °C. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

5.5 Rail-to-Rail Input

The input common-mode range of GT7122 series extends 100mV beyond the supply rails (V_{SS}-0.1V to V_{DD}+0.1V). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

5.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of GT7122 series can typically swing to less than 10mV from supply rail in light resistive loads (>100kΩ), and 60mV of supply rail in moderate resistive loads (10kΩ).

5.7 Capacitive Load Tolerance

The GT7122 series can directly drive 250pF capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor R_{ISO} in series with the capacitive load, as shown in ***Figure 2***.

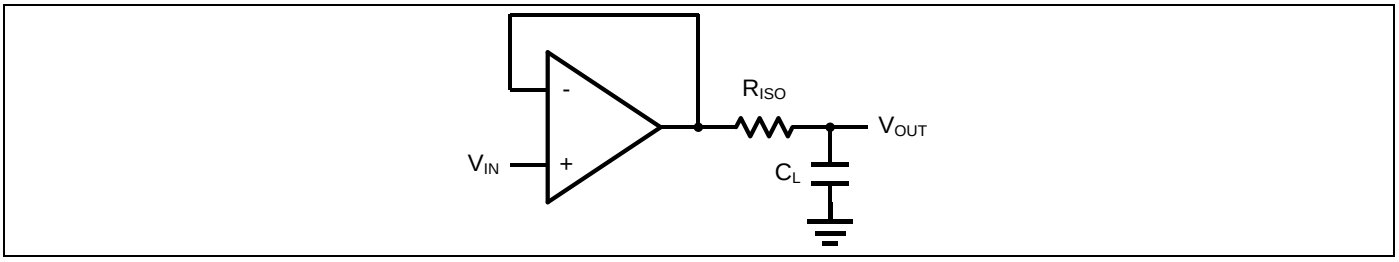


Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load R_L in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.

The circuit in ***Figure 3*** is an improvement to the one in ***Figure 2***. R_F provides the DC accuracy by feed-forward the V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased

by increasing the value of C_F. This in turn will slow down the pulse response.

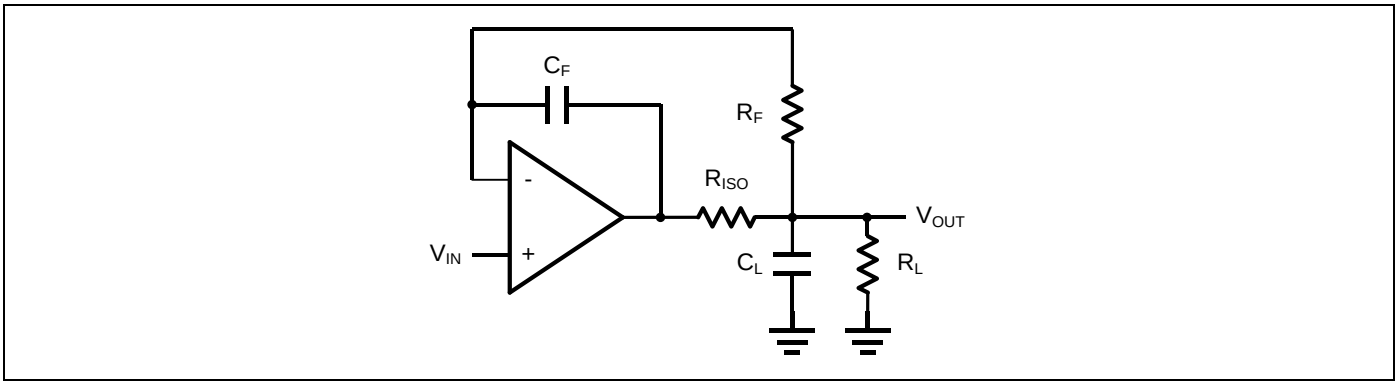


Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy

5.8 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. ***Figure 4.*** shown the differential amplifier using GT7122.

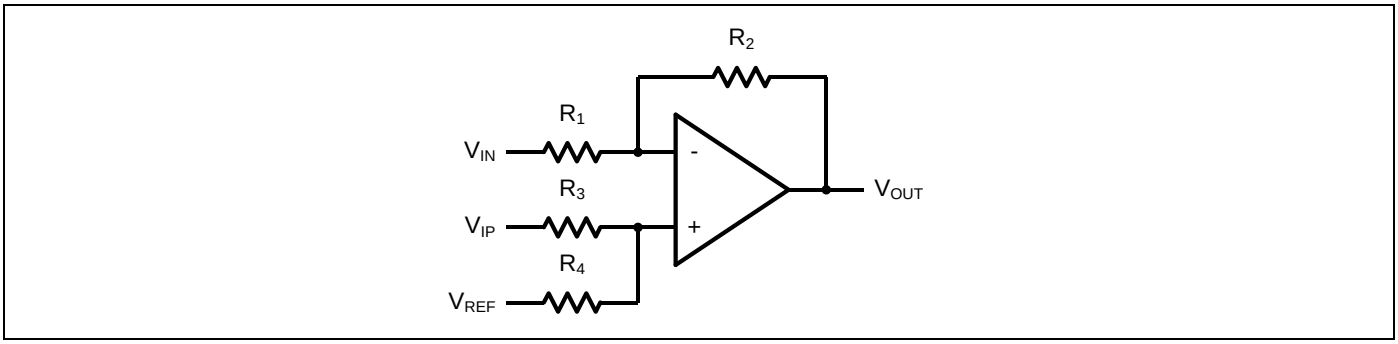


Figure 4. Differential Amplifier

$$V_{OUT} = (\frac{R1+R2}{R3+R4})\frac{R4}{R1}V_{IN} - \frac{R2}{R1}V_{IP} + (\frac{R1+R2}{R3+R4})\frac{R3}{R1}V_{REF}$$

If the resistor ratios are equal (i.e. R_1=R_3 and R_2=R_4), then

$$V_{OUT} = \frac{R2}{R1}(V_{IP} - V_{IN}) + V_{REF}$$

5.9 Instrumentation Amplifier

The input impedance of the previous differential amplifier is set by the resistors R1, R2, R3, and R4. To maintain the high input impedance, one can use a voltage follower in front of each input as shown in the following two instrumentation amplifiers.

5.10 Three-Op-Amp Instrumentation Amplifier

The dual GT7122 can be used to build a three-op-amp instrumentation amplifier as shown in ***Figure 5***.

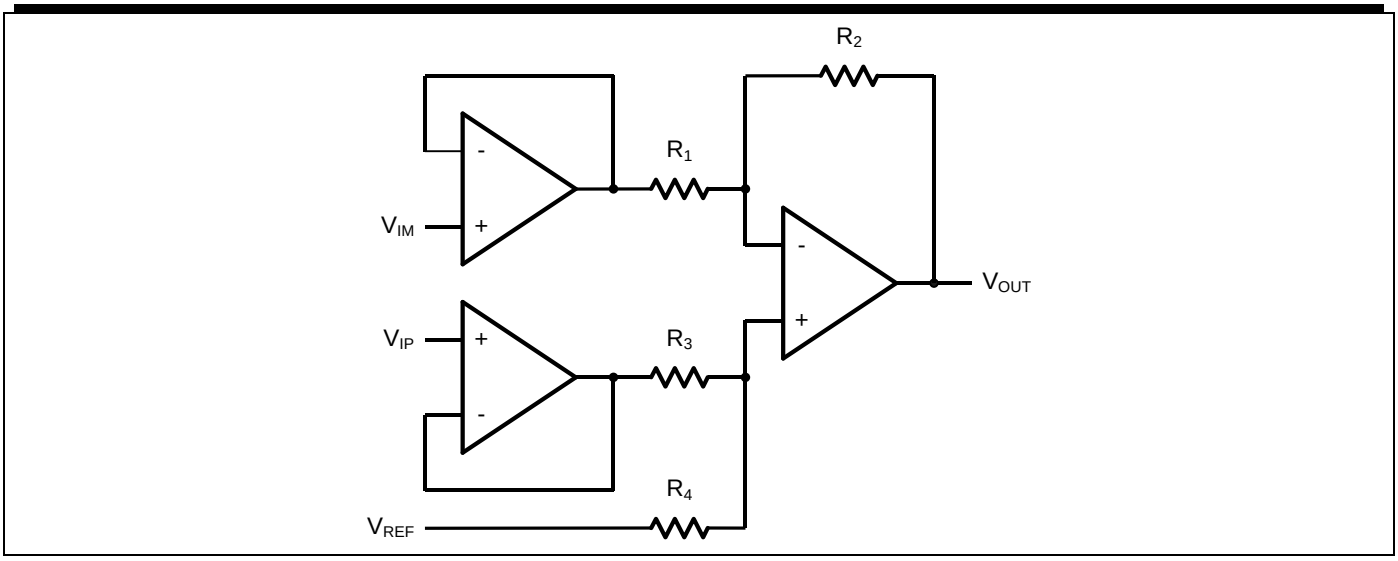


Figure 5. Three-Op-Amp Instrumentation Amplifier

The amplifier in ***Figure 5*** is a high input impedance differential amplifier with gain of R_2/R_1. The two differential voltage followers assure the high input impedance of the amplifier.

$$Vo = (1+\frac{R_4}{R_3})(V_{IP} - V_{IN})$$

5.11 Two-Op-Amp Instrumentation Amplifier

GT7122 can also be used to make a high input impedance two-op-amp instrumentation amplifier as shown in ***Figure 6***.

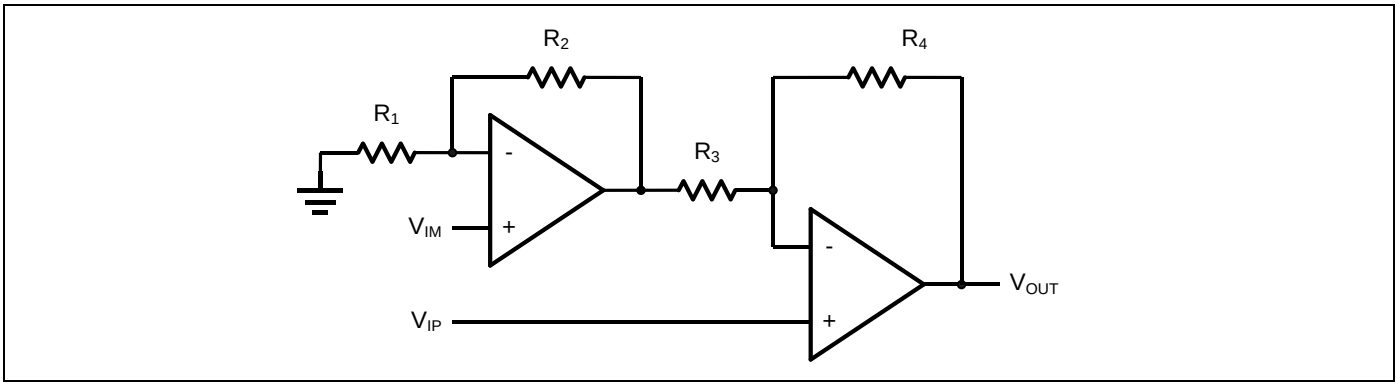


Figure 6. Two-Op-Amp Instrumentation Amplifier

Where $R_1=R_3$ and $R_2=R_4$. If all resistors are equal, then $V_o=2(V_{IP}-V_{IN})$

5.12 Single-Supply Inverting Amplifier

The inverting amplifier is shown in Figure 6. The capacitor C_1 is used to block the DC signal going into the AC signal source V_{IN}. The value of R_1 and C_1 set the cut-off frequency to $f_C=1/(2\pi R_1C_1)$. The DC gain is defined by $V_{OUT}=-(R_2/R_1)V_{IN}$

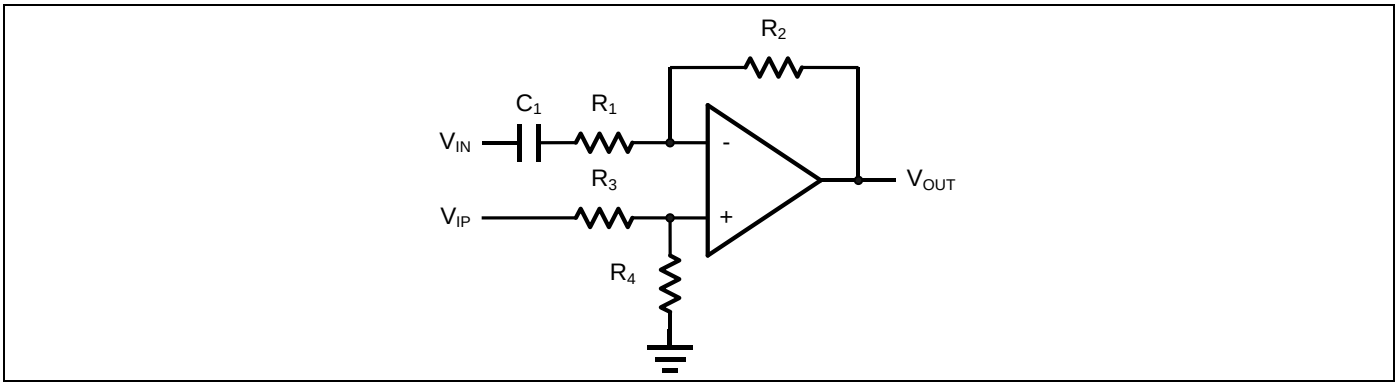


Figure 7. Single Supply Inverting Amplifier

5.13 Low Pass Active Filter

The low pass active filter is shown in ***Figure 8***. The DC gain is defined by $-R_2/R_1$. The filter has a -20dB/decade roll-off after its corner frequency $f_C=1/(2\pi R_3C_1)$.

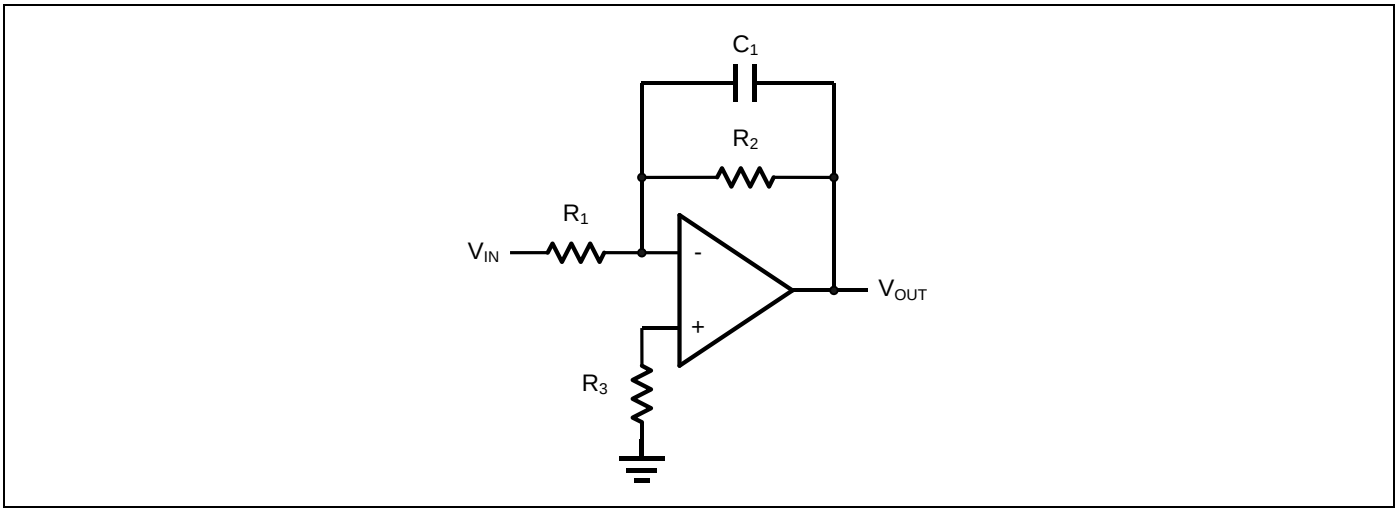


Figure 8. Low Pass Active Filter

5.14 Sallen-Key 2nd Order Active Low-Pass Filter

GT7122 can be used to form a 2nd order Sallen-Key active low-pass filter as shown in ***Figure 9***. The transfer function from V_{IN} to V_{OUT} is given by

$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{\frac{1}{C_1C_2R_1R_2}A_{LP}}{S^2+S(\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2})+\frac{1}{C_1C_2R_1R_2}}$$

Where the DC gain is defined by $A_{LP}=1+R_3/R_4$, and the corner frequency is given by

$$\omega C=\sqrt{\frac{1}{C_1C_2R_1R_2}}$$

The pole quality factor is given by

$$\frac{\omega C}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}$$

Let R1=R2=R and C1=C2=C, the corner frequency and the pole quality factor can be simplified as below

$$\omega_C = \frac{1}{CR}$$

And $Q=2-R_3/R_4$

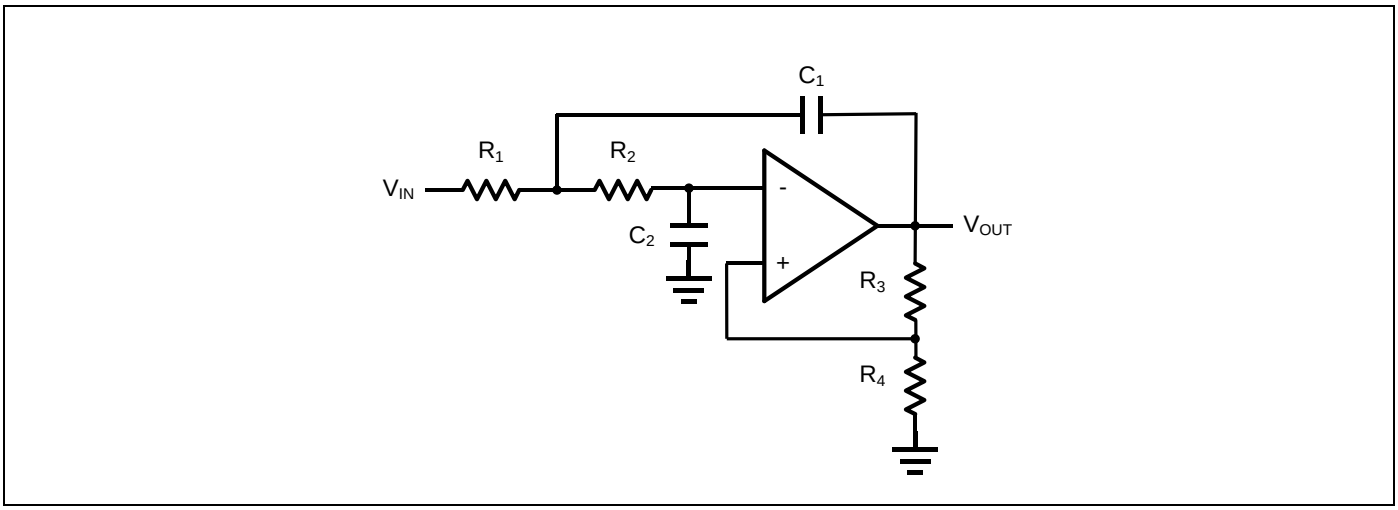


Figure 9. Sanllen-Key 2nd Order Active Low-Pass Filter

5.15 Sallen-Key 2nd Order high-Pass Active Filter

The 2nd order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components R_1, R_2, C_1, and C_2 as shown in ***Figure 10***.

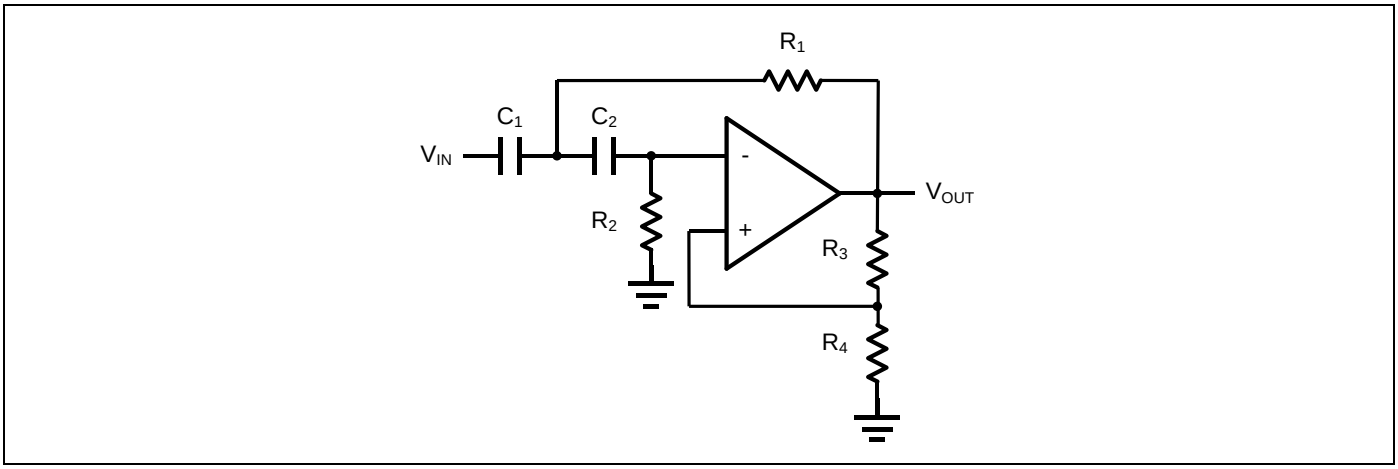


Figure 10. Sanllen-Key 2nd Order Active High-Pass Filter

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1-A_{HP}}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where $A_{HP}=1+R_3/R_4$

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to Vss)	-0.5V	+7V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	V_{DD}+0.5V
PDB Input Voltage	Vss-0.5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance (T_A=+25℃)		
SOP8, θ_{JA}	130°C	
MSOP8, θ_{JA}	210°C	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Electrical Characteristics

(V_{DD} = +5V, Vss = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L=100K tied to V_{DD}/2, SHDNB = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Notes 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.2	-	5.5	V
Quiescent Supply Current (per Amplifier)	I_{DD}	V_{DD} = 3V	-	0.8	-	mA
		V_{DD} = 5V	-	0.8	1.2	
Input Offset Voltage	V_{OS}	T_A = +25°C	-	-	±5	mV
		T_A = -40°C to +85°C	-	-	-	
		T_A = -40°C to +125°C	-	-	±1.5	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	±0.3	±6	μV/°C
Input Bias Current	I_B	(Note 3)	-	±1	±100	pA
Input Offset Current	I_{OS}	(Note 3)	-	±1	±100	pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the T_A = 25°C	-0.2	-	V_{DD}+0.2	V
		CMRR test T_A = -40°C to +125°C	0	-	V_{DD}0	
Common-Mode Rejection Ratio	CMRR	Vss-0.2V≤V_{CM}≤V_{DD}+0.2V T_A = +25°C	-	75	-	dB
		Vss≤V_{CM}≤5V T_A = +25°C	65	80	-	
		Vss-0.2V≤V_{CM}≤V_{DD}+0.2V T_A = -40°C to +125°C	-	65	-	
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.2V to +5.5V	75	90	-	dB
Open-Loop Voltage Gain	A_V	R_L=100kΩ to V_{DD}/2, 100mV≤V_O≤V_{DD} -125mV	90	100	-	dB
		R_L=1kΩ to V_{DD}/2, 200mV≤V_O≤V_{DD} -250mV	75	85	-	
		R_L=500Ω to V_{DD}/2, 350mV≤V_O≤V_{DD} -500mV	55	65	-	
Output Voltage Swing	V_{OUT}	|V_{IN+}-V_{IN-}| ≥ 10mV V_{DD}-V_{OH}	-	10	35	mV
		R_L = 10kΩ to V_{DD}/2 V_{OL}-V_{SS}	-	10	30	
		|V_{IN+}-V_{IN-}| ≥ 10mV V_{DD}-V_{OH}	-	80	200	
		R_L = 1kΩ to V_{DD}/2 V_{OL}-V_{SS}	-	50	150	
		|V_{IN+}-V_{IN-}| ≥ 10mV V_{DD}-V_{OH}		100	350	

		R_L = 500Ω to V_{DD}/2 V_{OL}-V_{SS}		80	260	
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	-	±50	-	mA
PDB Logic Low	V_{IL}		-	-	0.8	V
PDB Logic High	V_{IH}		2	-	-	V
Turn-On Time	T_{ON}		-	2.2	-	µs
Turn-Off Time	T_{OFF}		-	0.8	-	µs
Output Leakage Current	I_{LEAK}	Shutdown Mode (PDB = V_{SS}), V_{OUT} = V_{SS} to V_{DD}	-	±0.001	±1.0	µA
Input Capacitance	C_{IN}			10		pF
Gain Bandwidth Product	GBW	A_V = +1V/V	-	10	-	MHz
Slew Rate	SR	A_V = +1V/V	-	4.5	-	V/µs
Full Power Bandwidth		Av = +1V/V	-	0.4	-	MHz
Phase Margin	ϕ_m	Av = +1V/V	-	55	-	deg
Gain Margin	G_m	Av = +1V/V	-	12	-	dB
Settling Time	t_S	To 0.01%, V_{OUT} = 2V step A_V = +1V/V	-	1	-	µs
Capacitive-Load Stability	C_{LOAD}	No sustained oscillations. Av = +1V/V	-	200	-	pF
Peak-to-Peak Input Noise Voltage (Note 5)	e_n(p-p)	f = 0.1Hz to 10Hz	-	5	-	µVp-p
Input Voltage Noise Density	e_n	f = 10Hz f = 1kHz f = 30kHz	- - -	60 30 15	- - -	nV/√Hz
Input Current Noise Density	i_n	f = 1kHz				fA/√Hz
Total Harmonic Distortion plus Noise	THD+N	V_{OUT} = 2Vp-p, Av = +1V/V, f = 1kHz RL = 10kΩ to GND f = 20kHz V_{OUT} = 2Vp-p, Av = +1V/V, f = 1kHz RL = 1kΩ to GND f = 20kHz	- - - -	0.0001 0.002 0.0002 0.004	- - - -	%

Note 1: All devices are 100% production tested at T_A = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

Note 2: Parameter is guaranteed by design.

Note 3: Peak-to-peak input noise voltage is defined as six times RMS value of input noise voltage.

7. Ordering Information

GT XXXX - XX X X

Temperature Range

I Industrial: -40°C~+125°C

Pb Status

G GREEN

Package Type:

G SOP

S MSOP

Part Number

Giantec Prefix

GT Giantec

Order Number	Package Description	Package Option
GT7122-GGI-TR	SOP8	Tape and Reel 4000
GT7122-SGI-TR	MSOP8	Tape and Reel 4000

8. Part Markings

8.1 GT7122-GGI (Top View)

G	T	7	1	2	2	G	G	I
				Lot Number				
●		Y	Y	W	W	S	V	

GT7122GGI

Lot Number	States the last 9 characters of the wafer lot information
●	Pin 1 Indicator
YY	Seal Year
	00 = 2000
	01 = 2001
	99 = 2099
WW	Seal Week
	01 = Week 1
	02 = Week 2
	.
	.
	.
	51 = Week 51
	52 = Week 52
S	Subcon Code
	J = ASESH
	L = ASEKS
V	Die Version

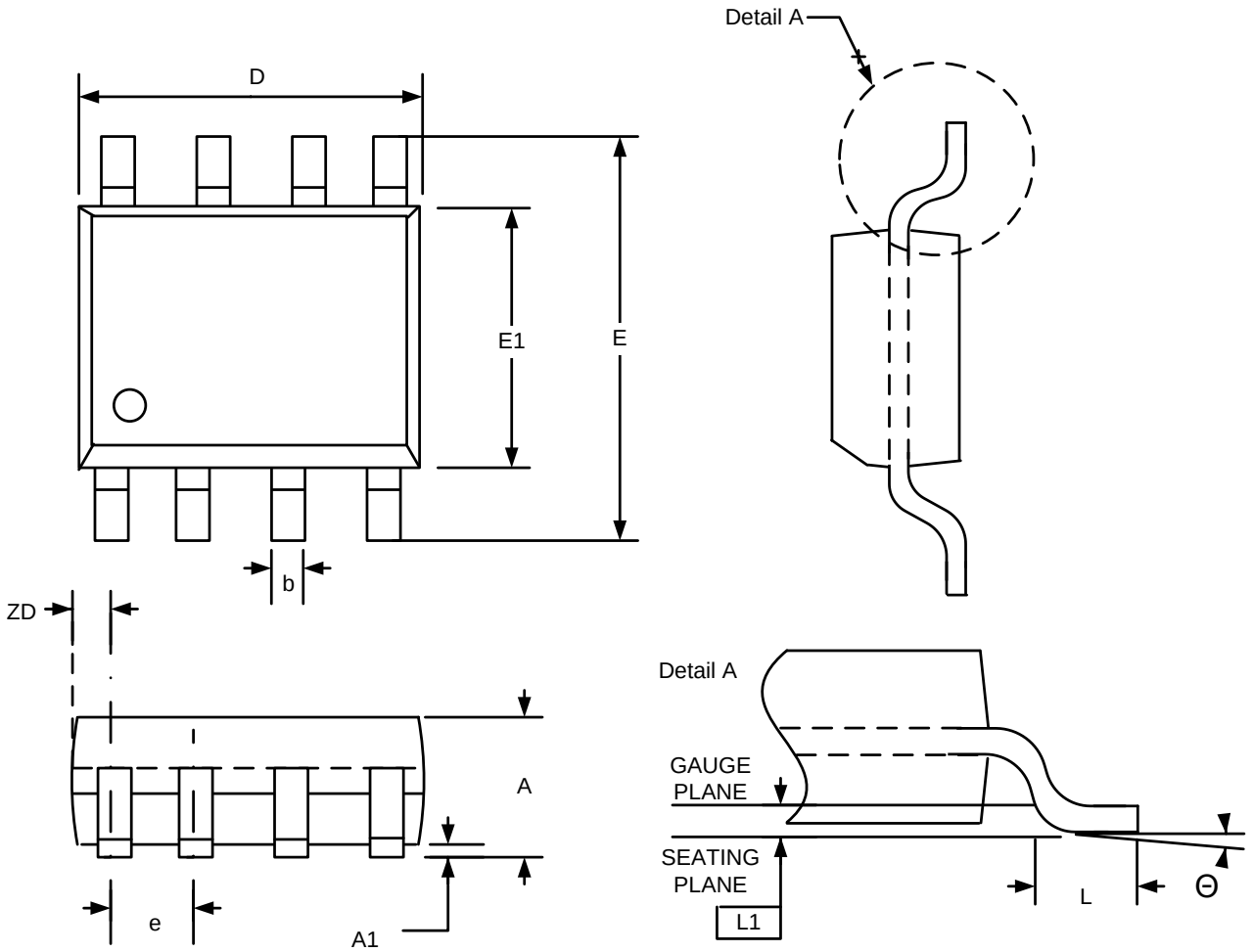
8.2 GT7122-SGI (Top View)

G	T	7	1	2	2		
				Lot Number			
●		Y	Y	W	W	S	V

GT7122	GT7122-SGI
Lot Number	States the last 9 characters of the wafer lot information
●	Pin 1 Indicator
YY	Seal Year
	00 = 2000
	01 = 2001
	99 = 2099
WW	Seal Week
	01 = Week 1
	02 = Week 2
	.
	.
	.
	51 = Week 51
	52 = Week 52
S	Subcon Code
	J = ASESH
	L = ASEKS
V	Die Version

9. Package Information

9.1 SOP8

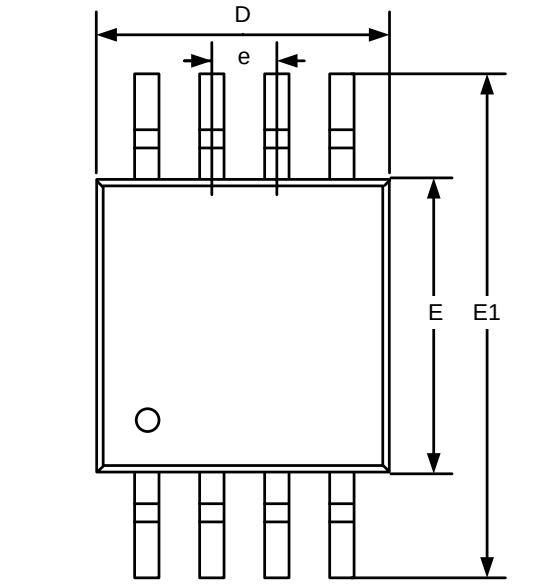


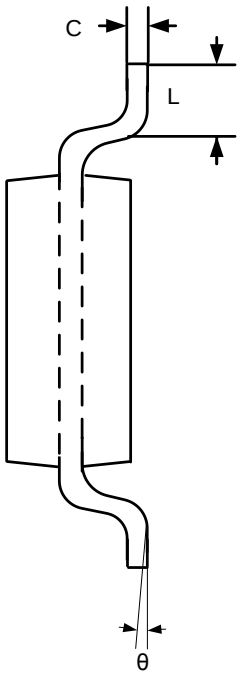
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

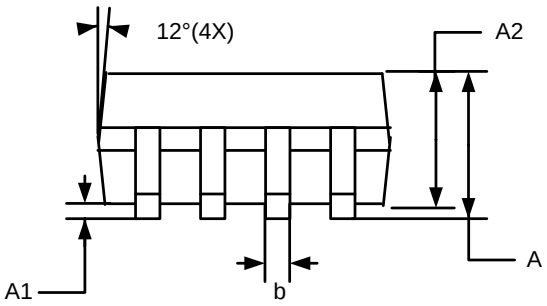
Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.2 MSOP8







SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.25	--	0.40	0.010	--	0.016
C	0.13	--	0.23	0.005	--	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.90 BSC			0.193 BSC		
e	0.65 BSC			0.026 BSC		
L	--	--	0.55	--	--	0.022
Θ	0	--	7°	0	--	7°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Refer to Jedec standard MO187
4. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
A0	Oct.,2011	Initial Version