High Performance Single Synchronous Buck Converter

Features

- Adjustable Relative Constant on-time for fast dynamic response
- Programmable VOUT range = 0.7V~20V
- VIN range = 3V~28V
- Wide Output Load Range: 0 to 15A
- 1% reference accuracy over load and line
- Low voltage DC current sense using low-side $R_{DS\_ON\_L}$ Sensing or sense resistor
- Resistor programmable frequency
- Cycle-by-cycle current limit
- 3-Step Current Limit During Soft-start
- Over-voltage/under-voltage fault protection
- Low quiescent power dissipation
- Power good indicator/ Power save option
- Integrated gate drivers with fast transmission scheme
- Enable pin
- Over temperature protection(Non-Latch)
- TQFN40-5x5 Package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Notebook computers
- CPU core/IO Supplies
- Chip/RAM Supplies

General Description

The GS9215 is small size chip with a relative constant on-time synchronous buck converter suitable for applications in notebook computers and other battery operated portable devices. Features include very wide input voltage range, high efficiency and a fast dynamic response with internal fast response scheme.

The GS9215 have a unique power save mode, which can save battery power supply by decreasing frequency when load current falls down below preset critical current point.

The fast dynamic transient response means that buck applications based on GS9215 will provide about 100ns-order response to load when output voltage falls down or rises up. The frequency will increase or decrease to meet the change in output load. Moreover, the GS9215 will take the same method to regulate the output voltage when input voltage changes. When transient response regulated, the controller will maintain a new steady-state operation. Both the transient response state and the new state, the GS9215 always has the same on-time.

The GS9215 is suitable for the solutions which have the output voltage between 0.7V and 20V. An external setting resistor and output voltage can set the on-time, duty-cycle and frequency for the controller. The integrated gate drivers feature adaptive shoot-through protection, fast signal transmission. Additional features include current limit, soft-start, over-voltage and under-voltage protection, a Power Good flag and soft discharge upon shutdown. The GS9215 is available in package TQFN40-5x5.

Typical Application

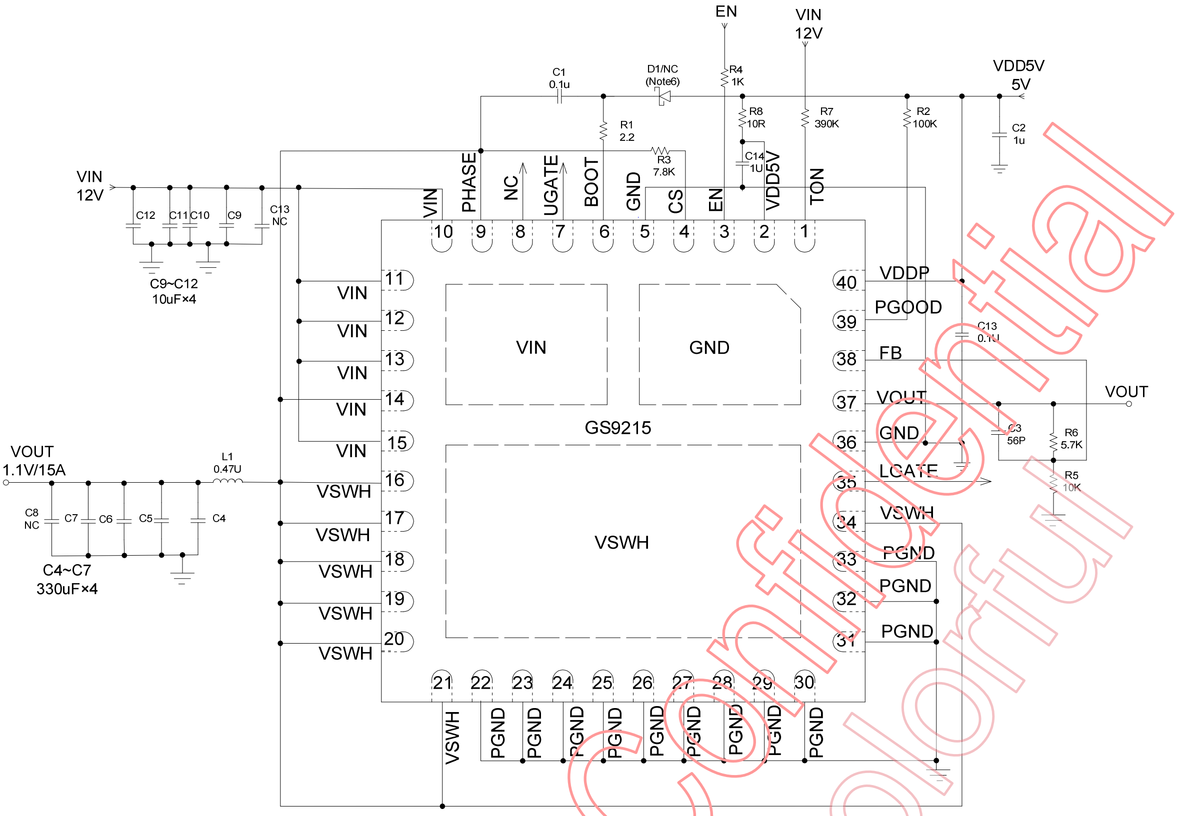


Figure 1a Typical Application of GS9215 for VOUT<2.5V

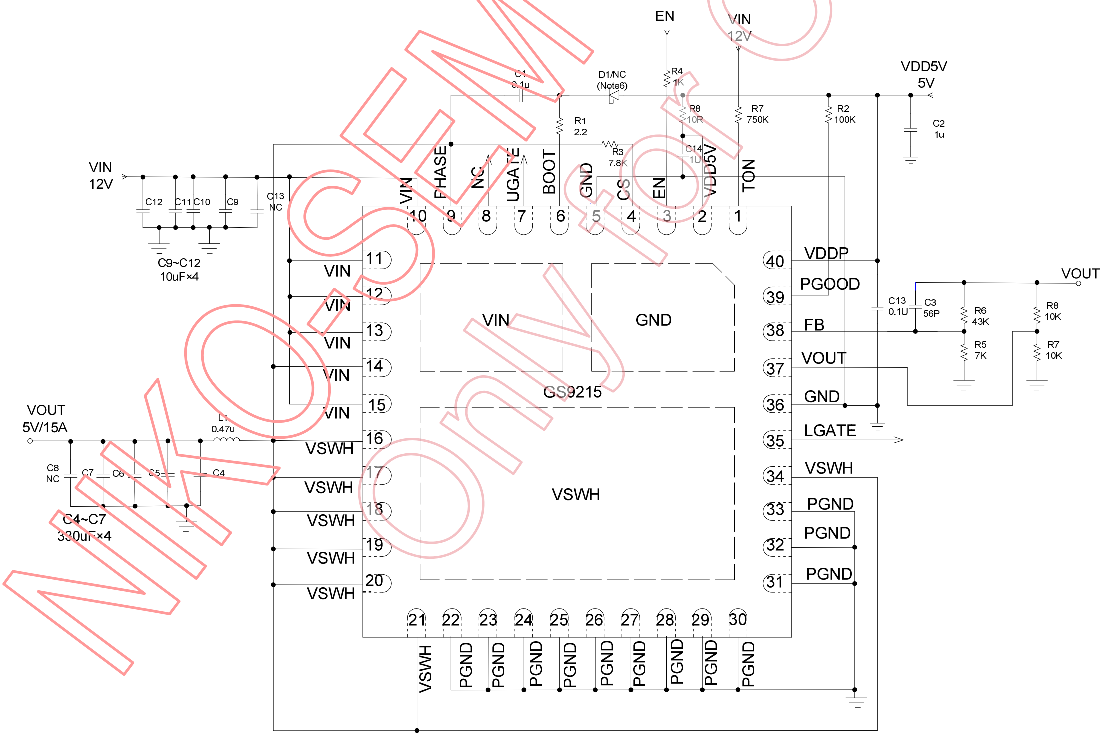


Figure 1b Typical Application of GS9215 for VOUT>2.5V

Function Block Diagram

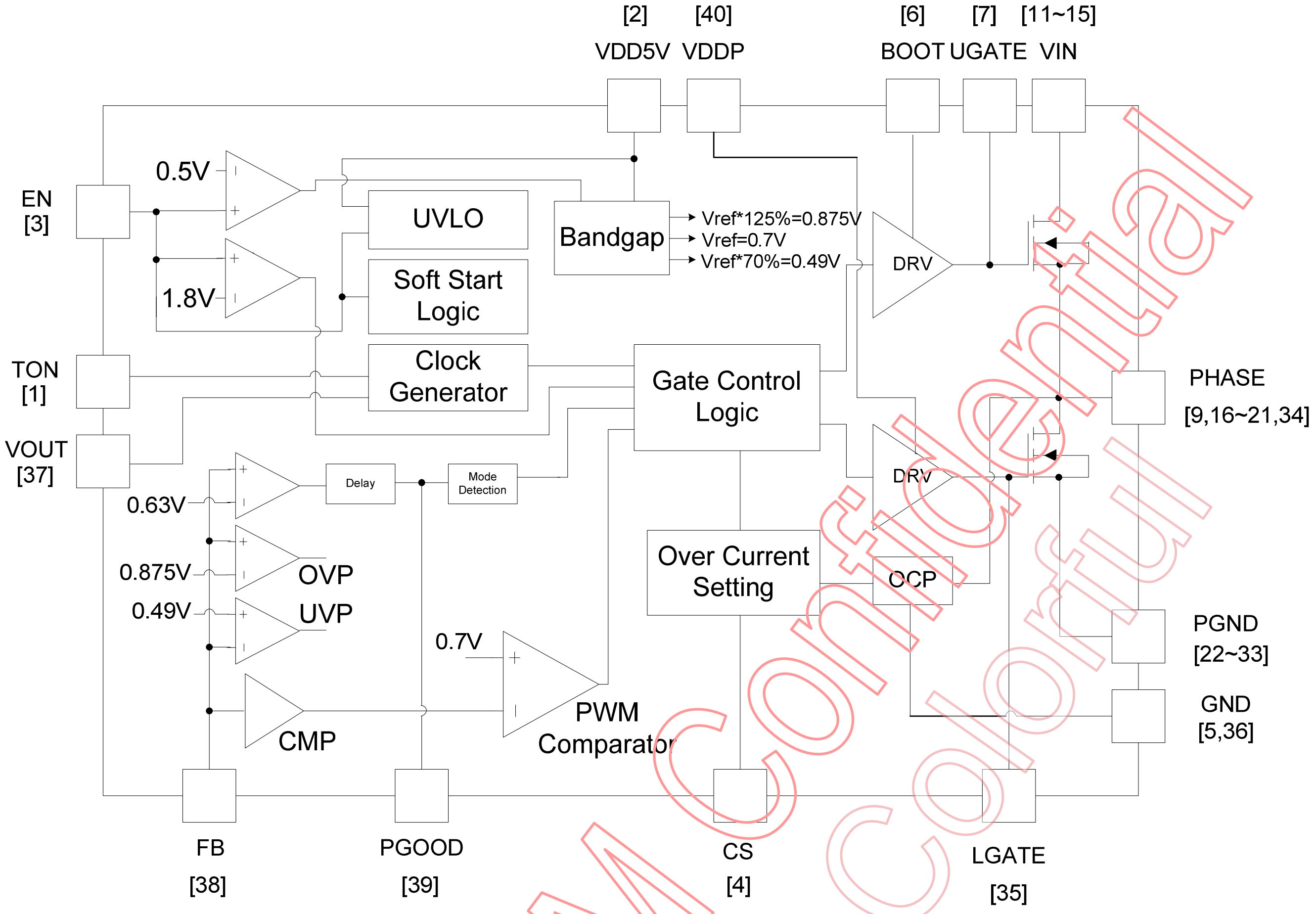


Figure 2 Function Block Diagram

Pin Configuration

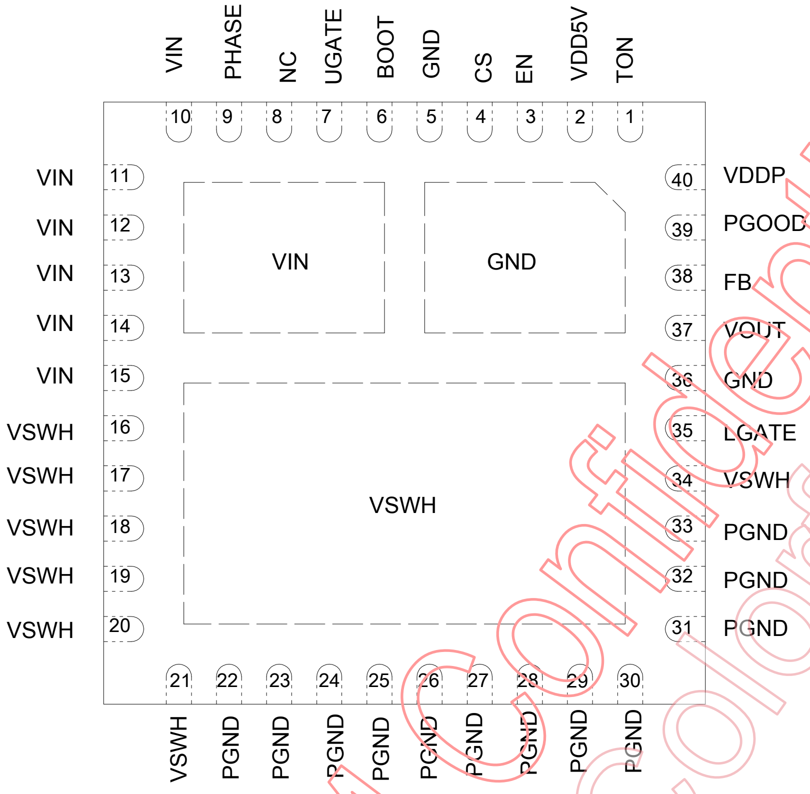


Figure 3 TQFN40-5x5 Package

Pin Descriptions

No.	Name	I/O type	Pin Function
1	TON	I	Inner Ton Time Control Pin. Connect an external pull up resistor to VIN.
2	VDD5V	I	Analog and Digital Power Input; Minimum 1uF ceramic capacitor is needed.
3	EN	I	Enable Control Pin. EN=Low, Shutdown; EN=Floating, Forced PWM CCM Mode; EN=High, PWM with Skip Mode.
4	CS	I	Current Limit Detecting Input Pin. Connect to PHASE pin though an external resistor to set the current limit threshold.
5,36	GND	I	Ground PIN Of The Controller.
6	BOOT	I	UGATE Driver Power Supply for Buck Controller. Bootstrap voltage pin. Use a ceramic capacitor connecting to the external diode with this pin.
7	UGATE	O	High side gate signal, Must be floated.
8	NC		

9	PAHSE	O	Switch node for Bootstrap capacitor.
10~15	VIN	I	Power Input voltage.
16~21,34	VSWH	O	Switch node, the output of the convertor.
22~33	PGND	I	Power Ground of the Power-MOS.
35	LGATE	O	Low side gate signal, Must be floated
37	VOUT	O	Buck Output Voltage (0~2.5V) Sense Input. Control the inner TON Time.
38	FB	I	Buck Output Voltage Feedback Input. Used to control output voltage range through a resistor voltage divider.
39	PGOOD	O	Buck controller power good indicator. Internal open drain structure. Connect to an external pull-up resistor. This Pin will be pulled high when output voltage reaches to the target range.
40	VDDP	I	Power Input, Minimum 0.1uF ceramic capacitor is needed.

Ordering Information

GS9215PP-R

1. Package ← PP   R → 2. Shipping

No	Item	Contents
1	Package	Q5: TQFN40-5x5
2	Shipping	R: Tape & Reel

Example: GS9215 TQFN40-5x5 Tape & Reel ordering information is “GS9215Q5-R”

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VIN to GND	V_{IN}	-0.3 ~ 30	V
TON to GND	V_{TON}	-0.3 ~ 30	V
CS to GND	V_{CS}	-0.3 ~ 30	V
VDD5V to GND	V_{SUPPLY}	-0.3 ~ 6	V
VDDP to GND	V_{DDP}	-0.3 ~ 6	V
PGOOD, FB, EN, VOUT to GND		-0.3 ~ 6	V
BOOT Voltage	$V_{BOOT-GND}$	-0.3 ~ 39	V
BOOT to PHASE Voltage	$V_{BOOT-PHASE}$	-0.3 ~ 6	V
LGATE to GND	V_{GL}	-0.3 ~ 6	V
PHASE to GND GND - 8V (<400ns, 20μJ) to 33V (<200ns, VBOOT-GND<39V)	V_{PHASE}	-2 ~ 33	V
Package Power Dissipation at T_A≦25°C	$P_{\_TQFN40-5x5}$	4228	mW
Junction Temperature	T_J	- 45 ~ 150	°C
Storage Temperature	T_{STG}	- 55 ~ 150	°C
Lead Temperature (Soldering) 10S	T_{LEAD}	260	°C
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	$\theta_{JA\_TQFN40-5x5}$	23.65	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VIN to GND(Note 5)	VIN	3~28	V
VDDP to GND	VDDP	4.5~5.5	V
VDD5V to GND	VDD5V	4.5~5.5	V
EN to GND	V_{EN}	VEN=VDD	V
Junction Temperature	T_J	- 40 ~ 125	°C
Ambient Temperature	T_A	-40 ~ 85	°C

Electrical Characteristics

(RTON=250KOhm, VDD5V=5V, VIN= 8V, EN=VDD, T_A =25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY VOLTAGE						
Power Input Voltage	VIN		3	8	28	V
Chip Supply Voltage	VDDP		4.5	5	5.5	V
Reference Voltage						
FB Reference Voltage	VFB	VDD= 4.5V ~ 5.5V	0.693	0.7	0.707	V
Enable Logic						
EN Logic Low Voltage	EN_L	EN Falling(2V~0V), LGATE Falling			0.8	V
EN Floating Voltage	EN_F	VDD Power On, Stable State		2		V
EN Logic High Voltage	EN_H	EN Rising(2V~5V), LGATE Falling	3.3			V
Current Parameters						
Quiescent	IQ	FB=0.73V, VDD	400	560	755	uA
Shutdown Current	I_{SHTDN}	EN=0, I(VDD)	0.5	1.43	3.55	uA
		EN=0, I(TON)		0.001	1	uA
		EN=0,I(EN)	-0.88	-0.35	-0.11	uA
Ton Operating Current	I_{TON}	RTON=300K,VIN=8V, VFB=0.73V	22.4	24	25.8	uA
Logic Input Current		EN=5V	0.32	1.04	2.6	uA
		EN=0V	-0.88	-0.35	-0.11	uA
FB Input Bias Current	I_{FB}	FB=0.7V		0.003		uA
System Time & Driver On-Resistance						
On-Time	TON	V_{IN}=8V,V_{FB}=0.6V, R_{TON}=300K,V_{OUT}=1.1V	245	350	455	ns
Minimum Off-Time	TOFFMIN	V_{IN}=8V, V_{FB}=0.6V, R_{TON}=300K	177	280	412	ns
Dead Time	T_{DL}	UGATE Falling to LGATE Rising	40	50	60	ns
	T_{DH}	LGATE Falling to UGATE Rising	30	40	50	ns
UGATE Driver Pull Up	R_{U_UP}	BOOT-PHASE=5V, UGATE=High		1.9	3.0	ohms
LGATE Driver Pull Down	R_{L_DN}	BOOT-PHASE=5V, LGATE=Low		0.5	1.0	ohms
UGATE Driver Sink	R_{U_SINK}	BOOT-PHASE=5V, UGATE=Low		0.7	1.4	ohms
LGATE Driver Pull Up	R_{L_UP}	BOOT-PHASE=5V, LGATE=High		1.0	2	ohms
High side Driver(Note 6)						
HDRV Rise time		V_{PVCC}=5V, 10%to 90%		30.0		ns
HDRV Fall time		V_{PVCC}=5V, 90%to 10%		25.0		ns

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low side Driver (Note6)						
LDRV Rise time		V_{PVCC}=5V, 10%to 90%		25.0		ns
LDRV Fall time		V_{PVCC}=5V, 90%to 10%		20.0		ns
Current Sensing						
CS Source Current	ICS	VCS=1V	18	20	22	uA
ICS current temperature coefficient	TCCS	On the bias of 25C		4700		ppm/°C
Current Limit 1 (Rising)	V_{ILIM1}	GND-PHASE, RCS(R3)=18K	324	360	396	mV
Current Limit 2 (Rising)	V_{ILIM2}	GND-PHASE, RCS(R3)=10K	180	200	220	mV
Current Limit 3 (Rising)	V_{ILIM3}	GND-PHASE, RCS(R3)=2.5K	35	50	65	mV
Zero Crossing Threshold	V_{T_0}	GND-PHASE	-10		10	mV
Current Comparator Offset	V_{OS_VCL}	GND-CS	-10		10	mV
Voltage Fault Protection						
VIN5V UVLO Threshold 1	UVLO_W	Wake Up	4.2	4.38	4.5	V
VIN5V UVLO Threshold 2	UVLO_S	Shutdown	3.7	3.93	4.1	V
UV Threshold	UV_TH	PGOOD Falling Edge, PWM Disable	60	70	80	%
UV Blank Time	T_UV	From EN Rising to PGOOD Rising		512CLKs		ms
UV Fault Delay	UV_DELAY			256CLKS		ms
OVP Threshold	OV_TH	PGOOD Rising, LGATE Rising	120	125	130	%
OVP Delay	T_OV	PGOOD Falling to LGATE Rising	17	20	23	us
PGOOD Flag						
PGOOD Trip Threshold	PG_TH	PGOOD Falling, Measured at FB	87	90	93	%
PGOOD Fault Propagation Delay	T_PG_F	From FB Falling to PGOOD Falling	1.87	2.5	4.11	us
Leakage Current	I_{LEAK}	PGOOD=5V(To be Measured)			0.01	uA
Output Low Voltage	V_{PG_LOW}	I_{SINK}=1mA			0.4	V
Over Temperature Shutdown						
Thermal Shutdown start threshold	T_{TSDN}			155		°C
Thermal Shutdown Hysteresis	T_{HYS_TSDN}			10		°C
Out Voltage Discharge Resistance						
VOUT Shutdown Discharge Resistance	R_{DISC}	IOUT=10mA	8	12	20	ohms
Power MOS's RDS(ON)						
High side Switch On-Resistance	$R_{DS\_ON\_H}$	IDS=1A (5)		15	30	mΩ
Low side Switch On-Resistance	$R_{DS\_ON\_L}$	IDS=1A		7	15	mΩ

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Bootstrap Diode						
Internal Boost Charging Switch On_Resistance	R_{BT_D}	VDD to BOOT, 10mA			100	ohms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Recommend the Pulse time<100ns when VIN over than 30V.

Note 6. Guaranteed by design.

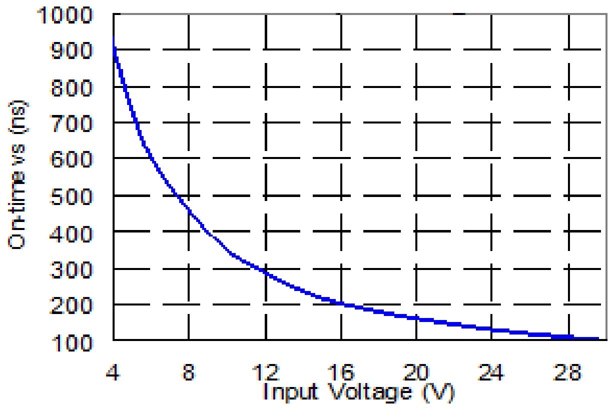
Note 7. Recommend total power less than 30W.

Note 8. If V(BOOT)-V(PHASE)<4V, a diode is recommended.

Typical Characteristics

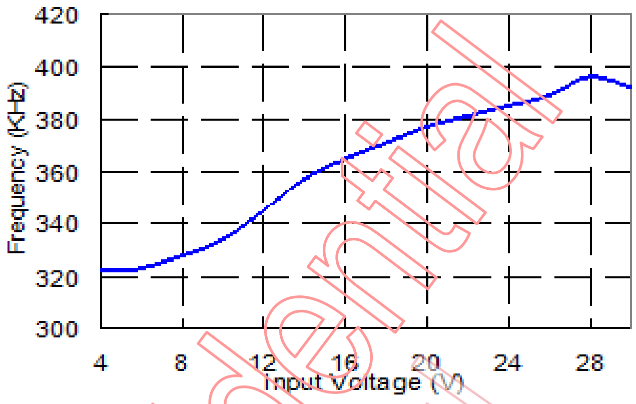
On-time vs. Input Voltage

(RTON=300K,ILOAD=10A,VOUT=1.04V)



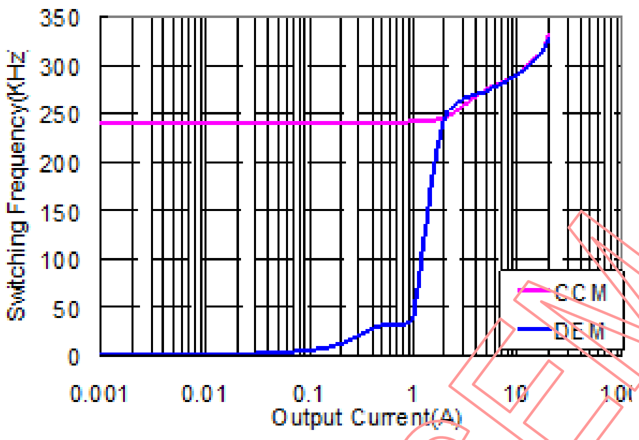
Frequency vs. Input Voltage

(RTON=300K,ILOAD=15A,VOUT=1.04V)



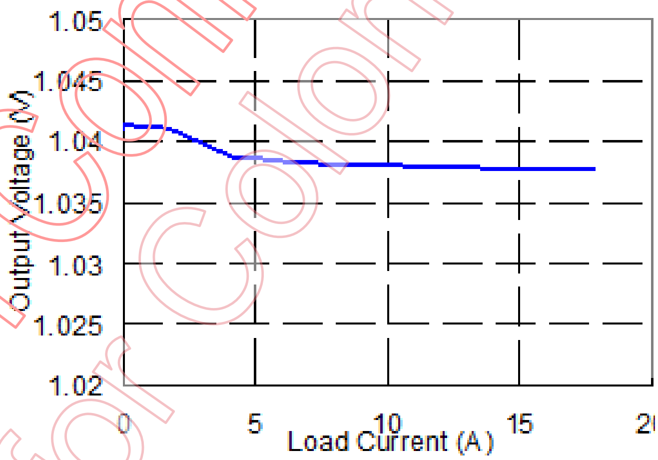
Frequency vs. Load Current

(RTON=300K,VIN=8V,VOUT=1.04V)



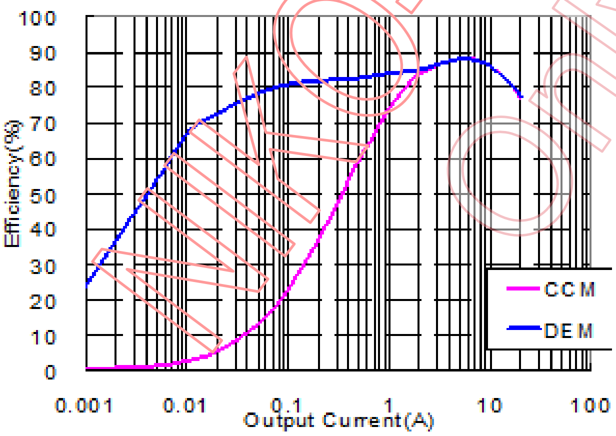
Output Voltage vs. Load Current

(RTON=300K,VIN=8V,VOUT=1.04V)



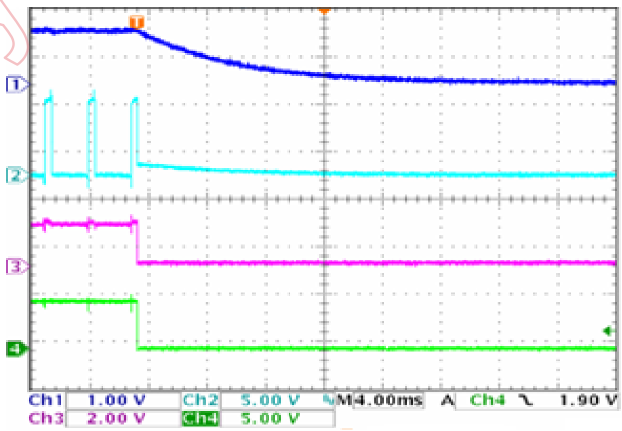
VOUT Efficiency vs. Load Current

(RTON=300K,VIN=8V,VOUT=1.04V)



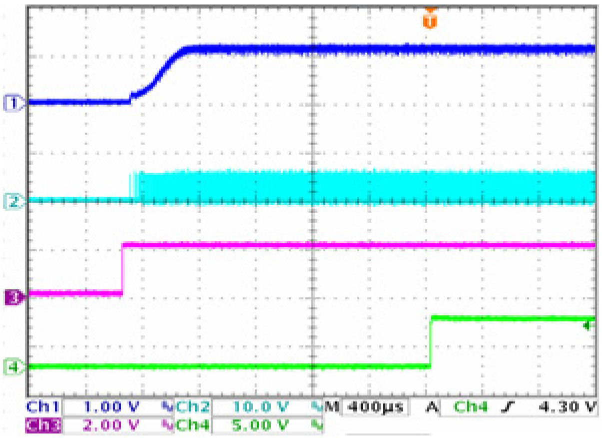
Power Off From EN

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



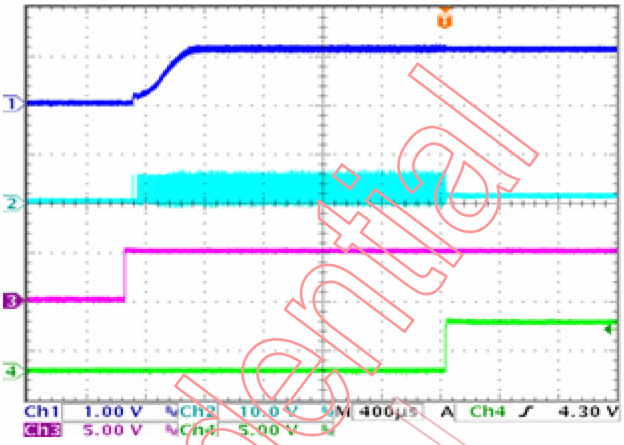
Power on from EN (CCM Mode, No Load)

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



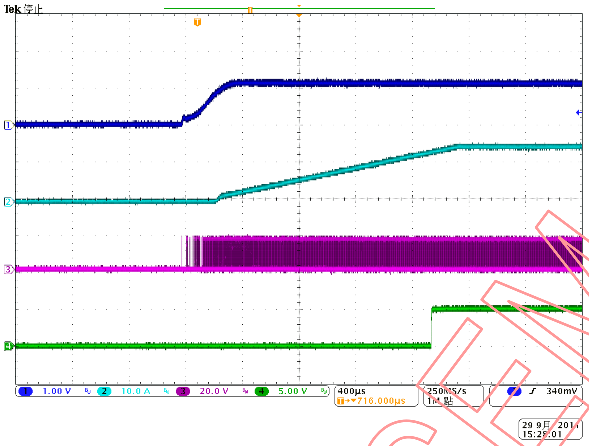
Power on from EN (DEM Mode, No Load)

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



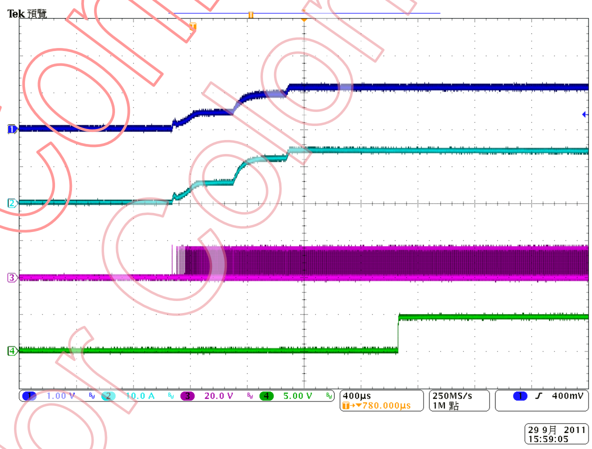
Power on from EN (15A Load)

CH1:VOUT CH2:IOUT CH3:UGATE CH4:PGOOD



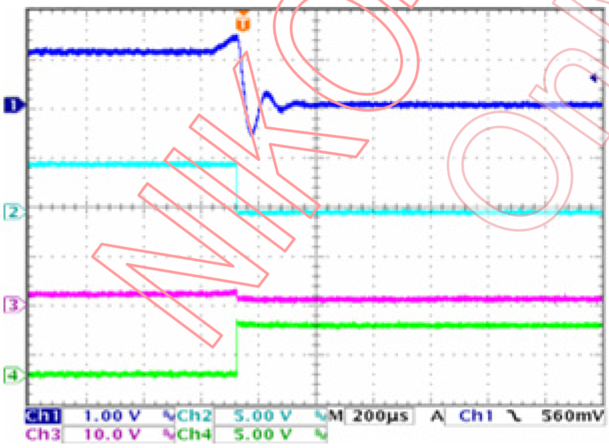
Power on from EN (73 mΩ Load)

CH1:VOUT CH2:IOUT CH3:UGATE CH4:PGOOD



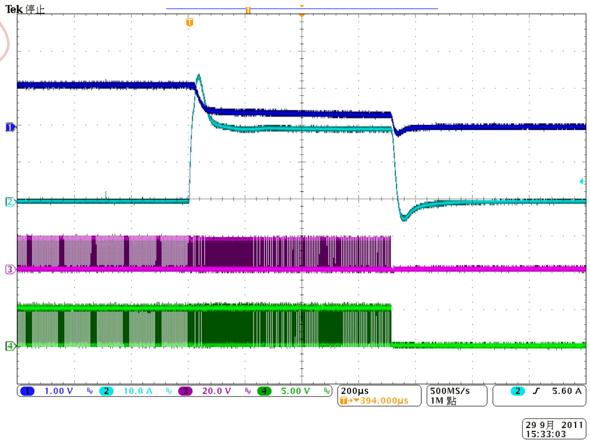
OVP

CH1:VOUT CH2:UGATE CH3:LGATE CH4:PGO



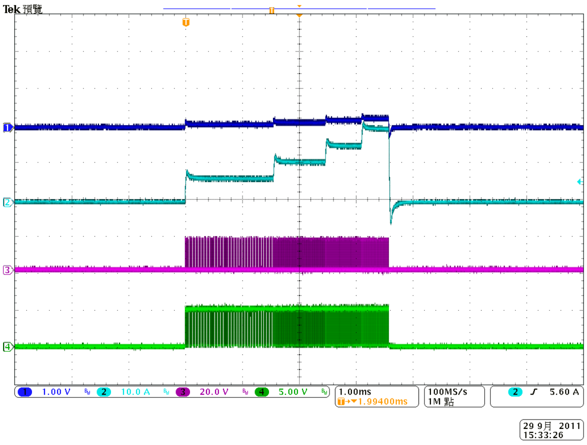
UVP

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



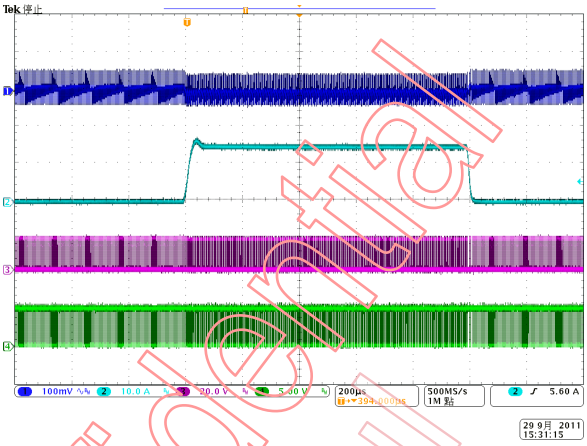
Power ON in Short Condition

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



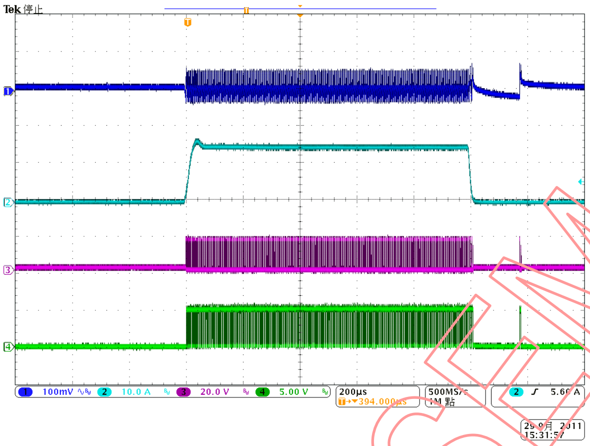
Load Transient CCM Mode

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



Load Transient DEM Mode

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



Application Information

The GS9215 is small size chip with a relative constant on-time synchronous buck Converter suitable for applications in notebook computers and other battery operated portable devices. Features include very wide input voltage range, high efficiency and a fast dynamic response with internal fast response scheme.

System Clock Generator and PWM Control

The on-time of GS9215 can be set by an external setting resistor from external Battery input voltage to TON pin and a sampled output voltage. The controller maintains the duty-circle as loop feedback path exists between the GS9215 controller, the integrated power MOSFET, low pass filter and voltage divider. For a given VIN to given VOUT buck application, the feedback maintains the constant duty-cycle. Due to the constant resistor, battery voltage and relative constant sampled output voltage, the GS9215 based buck converter has the relative constant frequency. Moreover, the GS9215 can increase the duty-cycle automatically as battery voltage falls down. Because of the constant on-time in each switching period, the controller maintains the relative frequency when the battery input voltage changes.

At the beginning of each switching cycle, upper power MOSFET is turned on, after typical fixed on-time, the upper MOSFET is turned off, and then lower power MOSFET is turned on after internal dead time. The upper MOSFET will not be turned on at the beginning of next cycle until output voltage falls down below the preset voltage and the dead time passes. The same events repeat the following switching cycles. To avoid the surge inductor current during large load transient, a minimum Off-time is added. Typical minimum off-time is around 420ns.

High Side Switch On-Time Count

The on-time is decided by the external setting resistor, battery input voltage and output voltage. Looking at the TON pin, the battery input voltage is converted to current which is inversely proportional to itself by dividing the external setting resistor. Simultaneously, the sample and hold module inside the chip samples the output voltage at each switching cycle. The input voltage-proportional current is used to charge an internal capacitor from zero volts. When the voltage between two terminals of the capacitor reaches to the sampled output voltage, on-time one-shot pulse is generated, and then upper power MOSFET is turned off and lower power MOSFET is turned on.

We can count the on-time and switching frequency according to the equations below:

$T_{ON}=8.22p\times R_{TON}\times V_{OUT}/(V_{IN}-0.8)$

Here, the VOUT is the sampled output voltage of VOUT PIN.For output voltalge VOUT<2.5V, the VOUT Voltage connects to VOUT PIN directly(refers to Figure 1a), the $V_{OUT}=V_{OUT}(0.7\sim2.5)$. For output voltalge VOUT >2.5V, the VOUT Voltage connects to VOUT PIN through the dividing resistors R_{VO1} and R_{VO2}(refers to Figure 1b), the typical VOUT is set to 2.5V, choose the R_{VO1} and R_{VO2} as follows: $V_{OUT}=Vout*R_{VO2}/(R_{VO1}+R_{VO2})$.

Then, the switching frequency is:

$F_{sw}=V_{OUT}/(V_{IN}\times T_{ON})$

RTON is a resistor connected from the input supply (VIN) to the TON pin.

For heavy load (more than 10A) application, due to ground bounced and the high impedance of R_{TON}, the TON pin should always be bypassed to GND using a several nF-order ceramic capacitor for reliable system operation.

EN/DEM, DEM Mode and Shutdown Soft-Discharge

The EN/DEM pin enables the power supply. When

EN/DEM is tied to VDD the GS9215 controller is enabled and diode-emulated mode (DEM, which is power save mode) will be also enabled. When the EN/DEM is floating or tri-stated, an internal tri-stated judged logic module will activate the controller and the DEM Mode will be disabled.

At light loads, GS9215 starts power save mode in order to maintain the on-time and decrease the system clock frequency to skip PWM pulses for better efficiency. If DEM Mode is enabled, the GS9215 zero crossing comparator will sense the inductor current and judge its value by comparing the phase node (PHASE) to PGND. Once the phase node voltage is equal to the PGND node voltage, the controller will enter the DEM Mode and turn off the low side power MOSFET. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than required the next switching cycle. The on-time is kept the same as that in the heavy-load condition.

If the EN/DEM pin is pulled low, the GS9215 internal logic will shutdown the switching clock and stop the buck controller, the related output will be discharged using a built-in switch resistor with a nominal resistance of 12ohms. This will ensure that the output is in a defined state next time when it is enabled. Since this is a soft discharge, that there are no dangerous negative voltage excursions to be concerned about. In order to maintain the correct function of the soft-discharge module, the chip power supply must be online.

Output Voltage Selection

The output voltage is set by the feedback resistors R7 and R8 of Figure 2 or Figure 3 above. The internal reference is 0.7V, so the voltage at the feedback pin is also 0.7V. Therefore the output can be set by the equation below:

$VOUT= (1+R6/R5) \times 0.7V$

Current Limit

The GS9215 uses the on-state resistance of the low-side power MOSFET as a current-sense resistor. In this case, the R_{CS} resistor between the PHASE pin and CS pin sets the over current threshold. This resistor R_{CS} is connected to a 20uA current source within the GS9215 which is turned on when the low side power MOSFET turns on. When the voltage drop across the low side power MOSFET equals the voltage crossing the current limit resistor R_{CS}, positive current limit will activate. The high side Power MOSFET will not be turned on until both the voltage drop across the sense element (low side power MOSFET) falls below the voltage across the R_{CS} resistor and the output voltage falls to preset value. The current sensing circuit actually regulates the inductor valley current. This means that if the magnitude of the current-sense signal at CS pin is above the current-limit threshold, the PWM is not allowed to initiate a new switching cycle. The equation for the current limit threshold is as follows:

$IL\_LIMIT=20uA\times R_{CS}/R_{DS\_ON\_L}$

Where RCS is R3 and $R_{DS\_ON\_L}$ is the resistance of low side power MOSFET ML. Ensure that noise and DC errors do not corrupt the current-sense signal seen by CS and PGND. Mount the IC close t the low side power MOSFET and sense resistor with short, direct traces, making a Kelvin sense connection to the sense resistor.

Power Good Indicator

When the output voltage is 25% above or 10% below its preset value, PGOOD gets pulled low. There is a 2.9us delay built into the PGOOD module to prevent false operations. It is held low until the output voltage returns to above 93% below OVP trigger point. PGOOD flag is also held low during soft-start .It will be pulled high immediately when soft-start is over and the output reaches 93% of its preset value. The Power Good indicator is open-drain architecture and requires an external pull-up resistor connected to PGOOD pin for system applications.

Output Over Voltage Protection

When the output voltage rises up to 125% of the preset voltage, the internal fault-logic module delays about 20us and turns on the low side Power MOSFET. It stays latched on and the GS9215 is latched off until Power Reset or EN Reset.

Output Under Voltage Protection

When the output voltage falls down to 70% of the preset voltage, the internal fault-logic module counts 256-CLKS and turns off both the high side and low side Power MOSFETs. Both switches stay latched off and the GS9215 is latched off until Power Reset or EN Reset. During soft-start, the UVP will be blanked around 512CLKS. But if the output voltage rises up above the UVP threshold tolerance during the counter period, the UVP counter is released immediately.

UVLO and Soft-Start

An internal under voltage lockout (UVLO) module is used to sense the VDD power supply. The PWM controller is forbidden by the under voltage lockout module when VDD rises above 4.3V, the GS9215 will initial the control logic circuitries and soft-start ramping generator, and then allows switching to occur if both the device and VIN power Supply is enabled. When VDD falls down to 3.9V, the PWM controller is forbidden again. At this time, both sides drive signal UGATE and LGATE are low.

After soft-start module starting, the GS9215 controller will limit the output current by 3-step current limiting logic cycle by cycle over a predetermined time period of 512CLKS. After UV blanking time (512CLKS), the output under voltage protection and power good indicator is enabled.

Power MOSFET Gate Drivers

The GS9215 has UGATE and LGATE drivers built-in, which can drive two large external N-type MOSFET used as high side and low side. External Boost diode and capacitor are need to power the internal floating drive module, A dead-time circuit is added to monitor the UGATE output and to prevent the high-side MOSFET from turning on until LGATE is fully off. The internal pull-down transistor that drives LGATE low is robust with a 0.5ohm typical on-resistance. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND. The dead-time circuit also monitors the LGATE output and prevents the low-side MOSFET from turning on until UGATE is fully off. The typical dead time from UGATE-falling to LGATE-rising is about 50ns.The typical dead time from LGATE-falling to UGATE-rising is about 40ns.

External Devices Selection

For loop stability, the 0 dB frequency (f0), defined in the follow equation:

$$f_0 = \frac{1}{2\pi \times RESR \times C_{OUT}} \le \frac{f_{SW}}{4}$$

The loop stability is determined by the output capacitor. Specialty polymer capacitors have C_{OUT} in the order of several 100uF and RESR in range of 10mohm is recommended. However, ceramic capacitors have f0 at more than 700 KHz, which is not recommended.

In order for the right regulate manner, the ripple voltage at the feedback pin (FB), should be approximately 15mV. This generates Vripple= (VOUT/0.7) ×15mV at the output node. The output capacitor RESR should meet this equation.

The external device selection is list below:

Choose Feedback Voltage Divider Resistor

Set R5=1K~10K ohm

$$R6 = \frac{(V_{OUT} - 0.7)}{0.7} \times R5$$

For output voltage Vout > 2.5V, Set VOUT PIN's voltage V_{OUT}=2.5V.

Choose R_{VO2}=1K~10K ohm

$$R_{VO1} = \frac{(V_{OUT} - 2.5)}{2.5} \times R_{VO2}$$

Choose RTON

$$T_{ON(Max)} = \frac{1}{f_{SW}} \times \frac{V_{OUT}}{V_{IN(Min)}}$$

$R_{ON\ (Max)} = T_{ON} \times (V_{IN\ (Min)} - 0.8) / (8.22P \times V_{OUT})$

Choose Inductor

Set the ripple current approximately 1/4 to 1/2 of the maximum output current. 1/3 is recommended.

$$L_{IND} = \frac{1}{I_{IND(ripple)} \times f} \times \frac{(V_{IN(\max)} - V_{OUT}) \times V_{OUT}}{V_{IN(\max)}}$$

$$L_{IND} = \frac{3}{I_{IOUT(\max)} \times f} \times \frac{(V_{IN(\max)} - V_{OUT}) \times V_{OUT}}{V_{IN(\max)}}$$

For applications that require fast transient response with minimum VOUT overshoot, consider a smaller inductance than above. The cost of a small inductance value is higher steady state ripple, larger line regulation, and higher switching loss.

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimate as follows.

$$L_{IND(peak)} = \frac{1}{L \times f} \times \frac{(V_{IN(\max)} - V_{OUT}) \times V_{OUT}}{V_{IN(\max)}} + \frac{V_{OC}}{R_{DS(on)}}$$

Choose Output Capacitors

$$RESR = \frac{1}{I_{ripple}} \times \frac{V_{OUT}}{0.7} \times 0.015$$

$$\approx \frac{3}{I_{OUT(\max)}} \times \frac{V_{OUT}}{0.7} \times 0.015$$

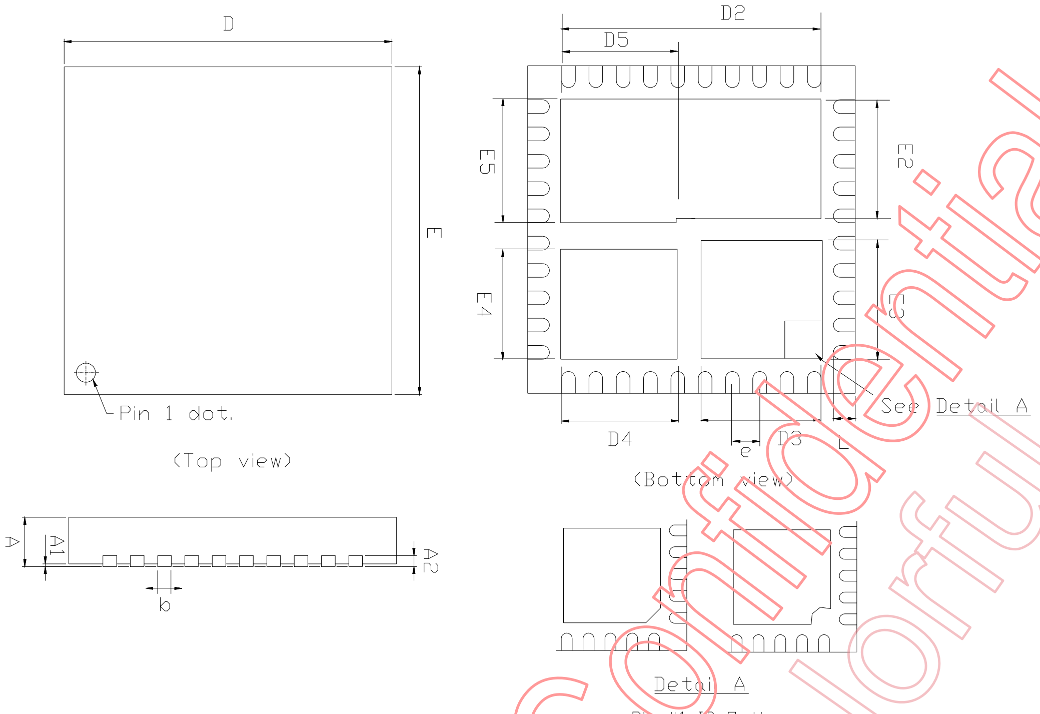
$$RESR \approx \frac{V_{OUT}}{I_{OUT(\max)}} \times 64(mohm)$$

Organic semiconductor capacitors or specialty polymer capacitors are recommended.

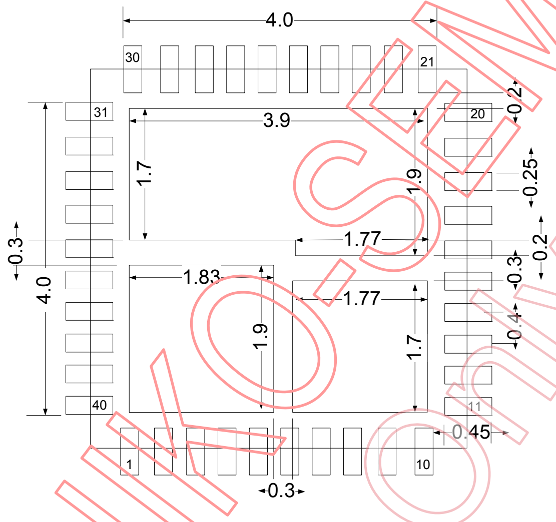
Choose RCS

Use the same equation above at item "Current Limit" section.

Package Dimensions, TQFN40-5x5



Pin #1 ID Options
Note:The configuration of the Pin#1 identifier is optional,but must be located within the zone indicated.



Unit: mm

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
A2	0.21 REF.	
b	0.15	0.25
D	4.90	5.10
D2	3.70	4.00
D3	1.45	1.93
D4	1.67	1.88
D5	1.67	1.88
E	4.90	5.10
E2	1.60	1.80
E3	1.80	2.00
E4	1.55	1.80
E5	1.80	2.00
e	0.40 REF.	
L	0.30	0.40

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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