100-Pin TQFP
Commercial Temp
Industrial Temp

36Mb Pipelined and Flow Through Synchronous NBT SRAMs

6.5 ns – 7.5 ns
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- Flow Through mode operation
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization; Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Pin compatible with 2Mb, 4Mb, 8Mb, and 16Mb devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ Pin for automatic power-down
- RoHS-compliant 100-lead TQFP package available

Functional Description

The GS8320FZ18/36AGT is a 36Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/ single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

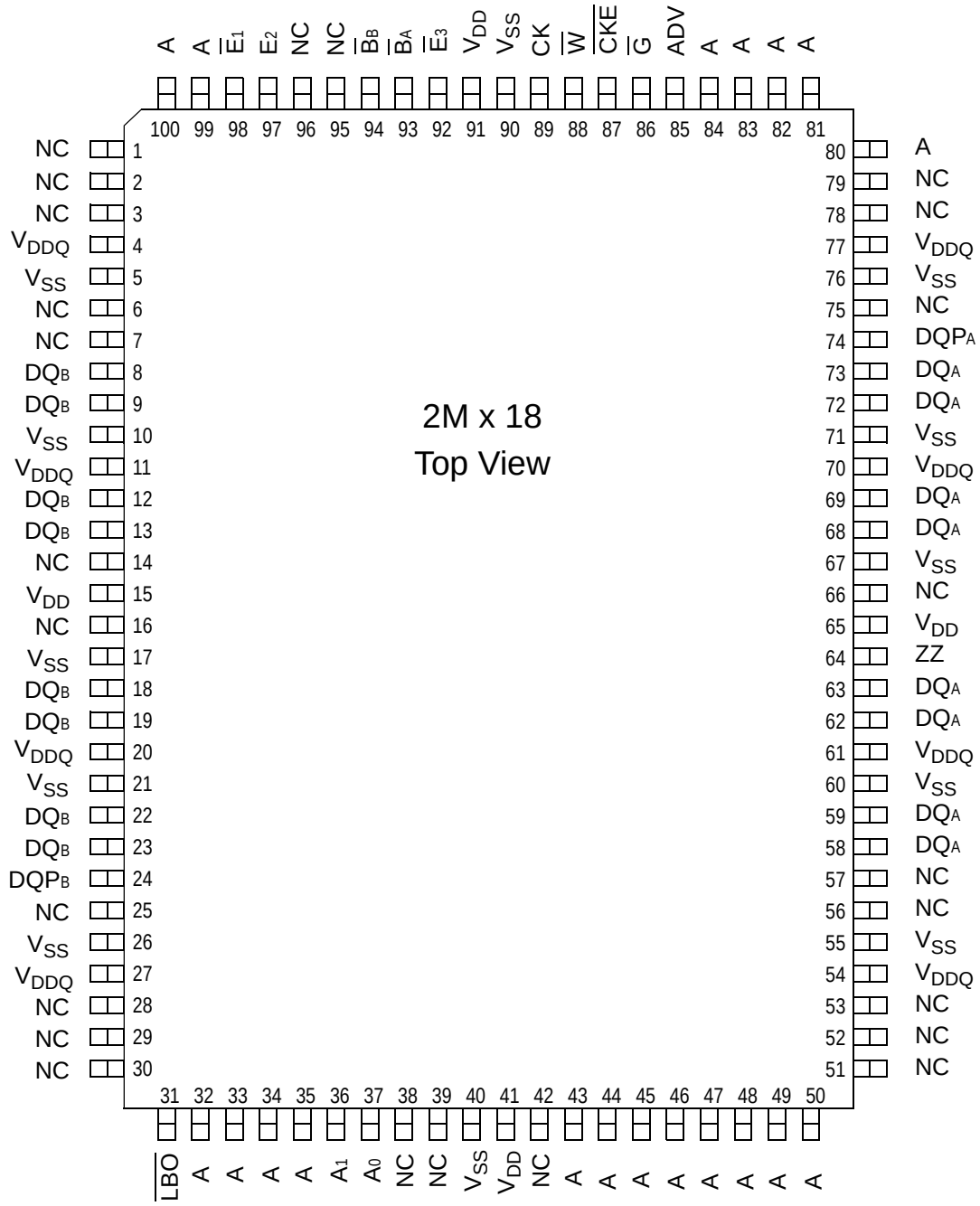
Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

The GS8320FZ18/36AGT is implemented with GSI's high performance CMOS technology and is available in a JEDEC-standard 100-pin TQFP package.

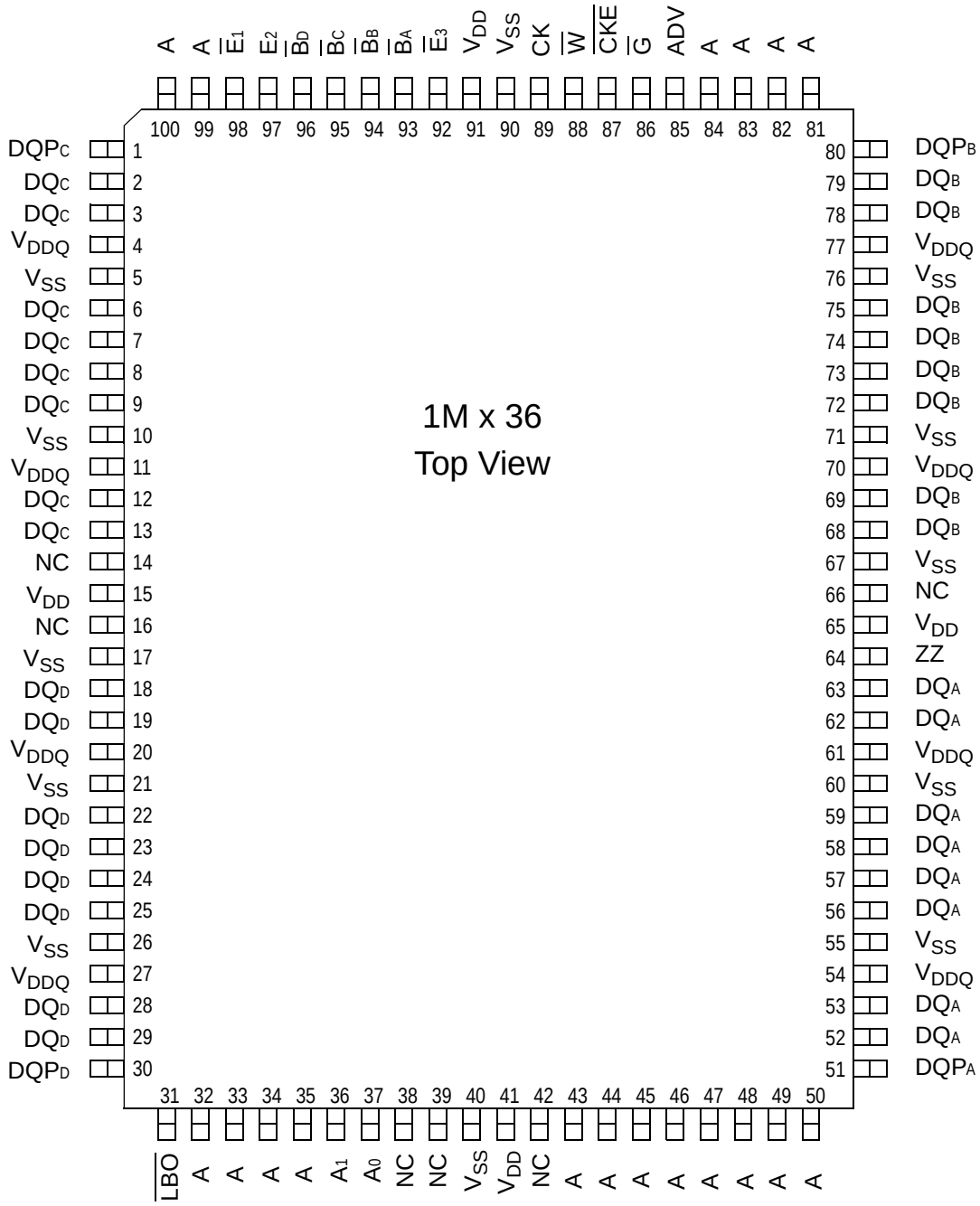
Parameter Synopsis

		-6.5	-7.5	Unit
Flow Through 2-1-1-1	t_{KQ}	6.5	7.5	ns
	tCycle	6.5	7.5	ns
	Curr (x18)	200	190	mA
	Curr (x36)	240	220	mA

GS8320FZ18AGT Pinout



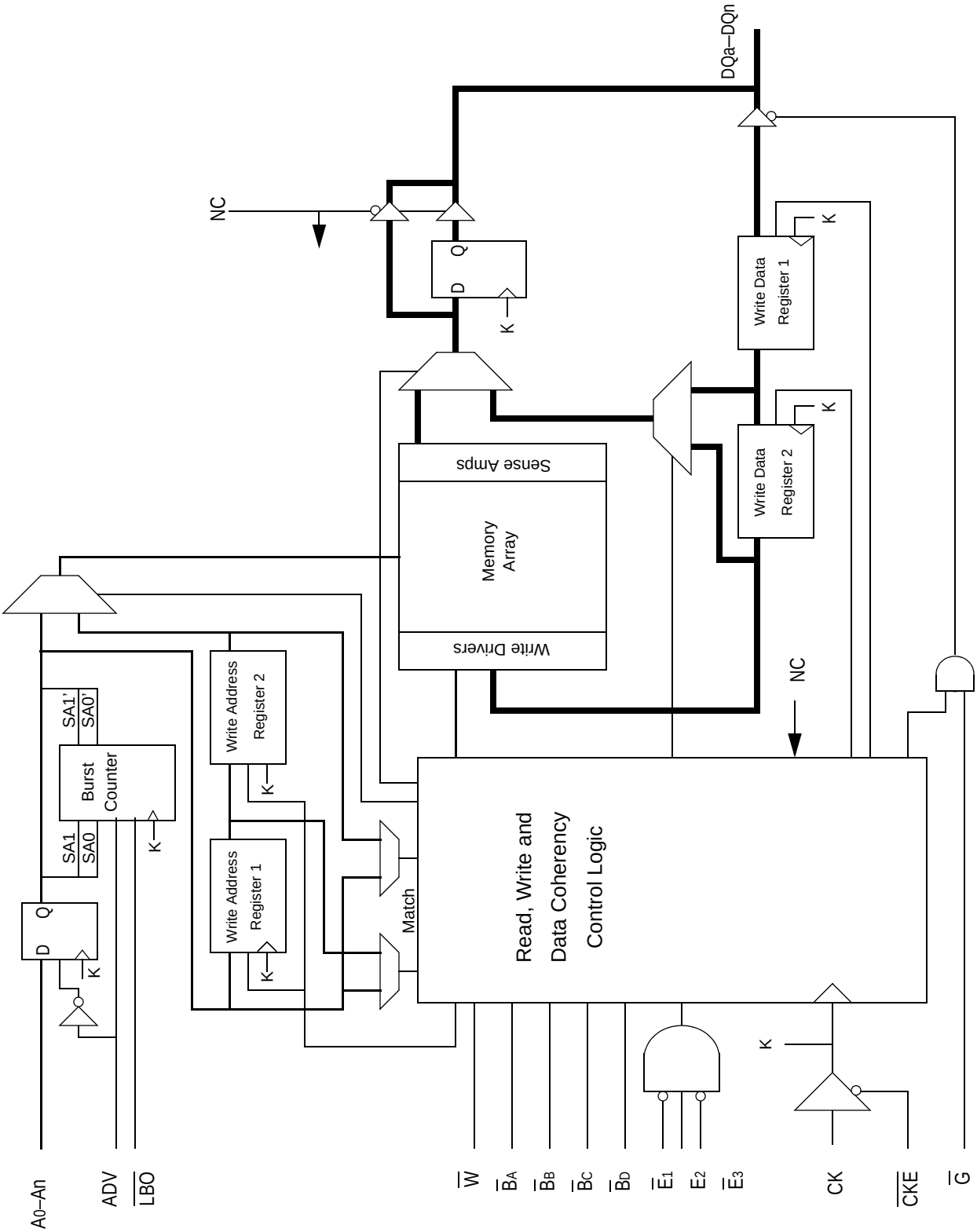
GS8320FZ36AGT Pinout



100-Pin TQFP Pin Descriptions

Symbol	Type	Description
A_0, A_1	In	Burst Address Inputs; Preload the burst counter
A	In	Address Inputs
CK	In	Clock Input Signal
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_{A1}-DQ_{A9}; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_{B1}-DQ_{B9}; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_{C1}-DQ_{C9}; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_{D1}-DQ_{D9}; active low
$\overline{W}$	In	Write Enable; active low
$\overline{E}_1$	In	Chip Enable; active low
E_2	In	Chip Enable; Active High. For self decoded depth expansion
$\overline{E}_3$	In	Chip Enable; Active Low. For self decoded depth expansion
$\overline{G}$	In	Output Enable; active low
ADV	In	Advance/$\overline{\text{Load}}$; Burst address counter control pin
$\overline{CKE}$	In	Clock Input Buffer Enable; active low
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ_C	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
ZZ	In	Power down control; active high
$\overline{LBO}$	In	Linear Burst Order; active low
V_{DD}	In	Core power supply
V_{SS}	In	Ground
V_{DDQ}	In	Output driver power supply
NC	—	No Connect

GS8320FZ18/36AGT NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{CKE}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

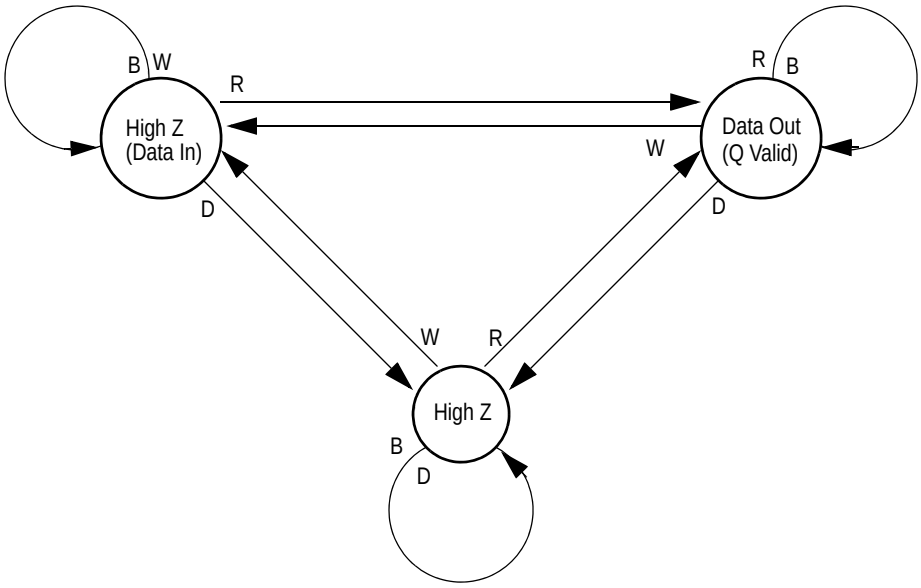
Synchronous Truth Table

Operation	Type	Address	CK	$\overline{CKE}$	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{E}1$	E2	$\overline{E}3$	$\overline{G}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,10
NOP/Read, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	2
Dummy Read, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Abort, Begin Burst	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Write Cycle, Continue Burst	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,3,10
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3,10
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

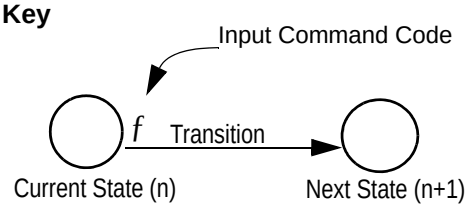
Notes:

1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

Flow Through Mode Data I/O State Diagram



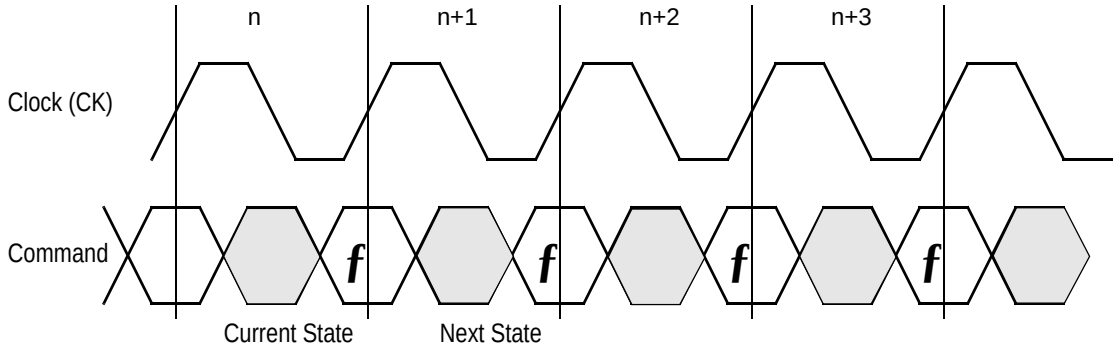
Key



Notes

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.

2. W, R, B and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{LBO}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{FT}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

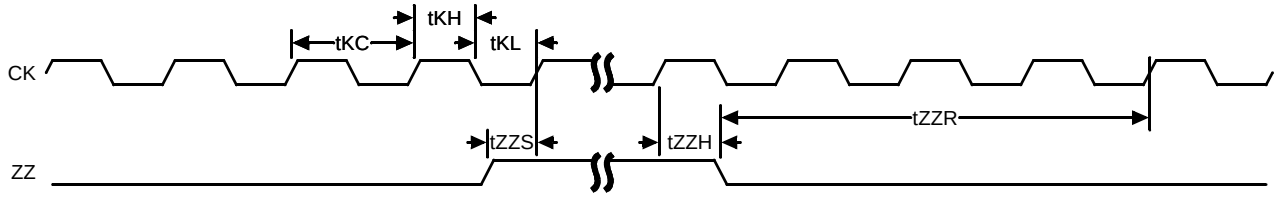
BPR 1999.05.18

Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a deselect or read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Notes:
1. V_{IH} (max) must be met for any instantaneous value of V_{DD}.
2. V_{DD} needs to power-up before or at the same time as V_{DDQ} to make sure V_{IH} (max) is not exceeded.

V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V

Notes:
1. V_{IH} (max) must be met for any instantaneous value of V_{DD}.
2. V_{DD} needs to power-up before or at the same time as V_{DDQ} to make sure V_{IH} (max) is not exceeded.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

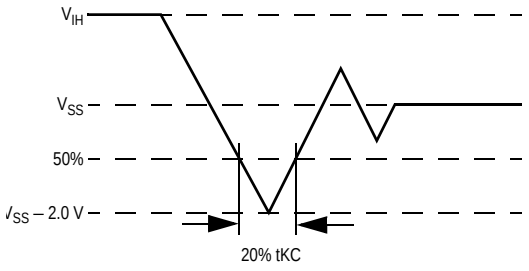
Note:
* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

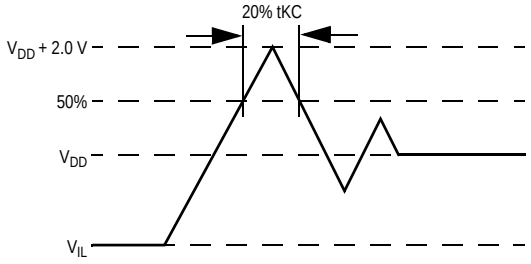
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100 TQFP	4-layer	28.7	23.8	22.3	15.1	6.5

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

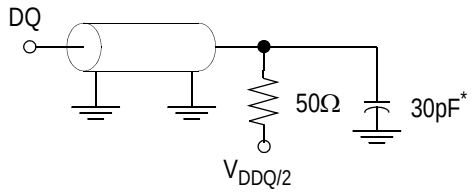
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode		Symbol	-6.5		-7.5		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	(x36)	Flow Through	I_{DD} I_{DDQ}	205 35	225 35	190 30	210 30	mA
		(x18)	Flow Through	I_{DD} I_{DDQ}	185 15	205 15	175 15	195 15	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	—	Flow Through	I_{SB}	55	75	55	75	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	Flow Through	I_{DD}	100	120	100	120	mA

Notes:

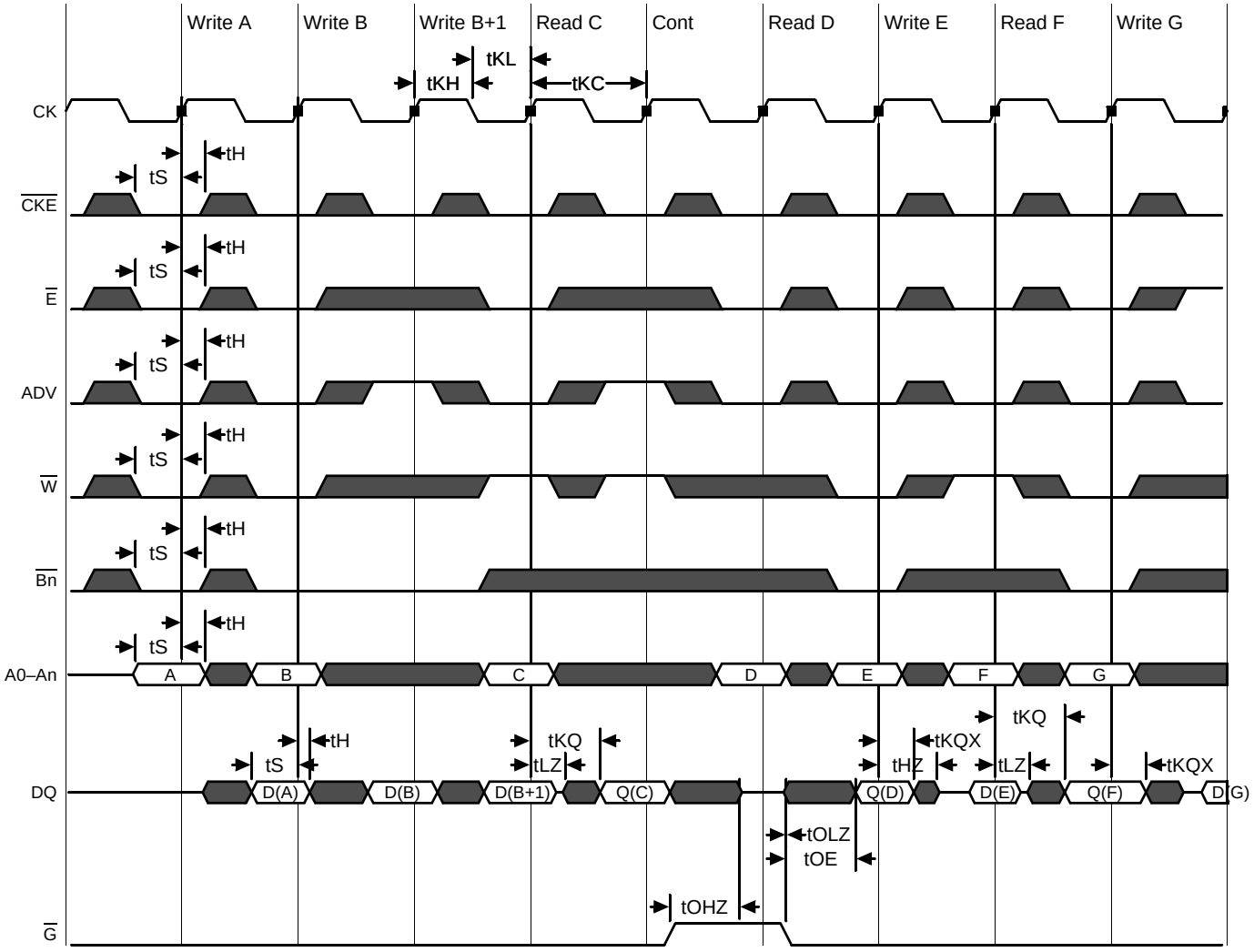
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

AC Electrical Characteristics

	Parameter	Symbol	-6.5		-7.5		Unit
			Min	Max	Min	Max	
Flow Through	Clock Cycle Time	tKC	6.5	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	6.5	—	7.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	ns
	Setup time	tS	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.3	—	1.5	—	ns
	Clock LOW Time	tKL	1.5	—	1.7	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	3.0	1.5	3.8	ns
	$\overline{G}$ to Output Valid	tOE	—	3.0	—	3.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	3.0	—	3.8	ns
	ZZ setup time	tZZS[2]	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

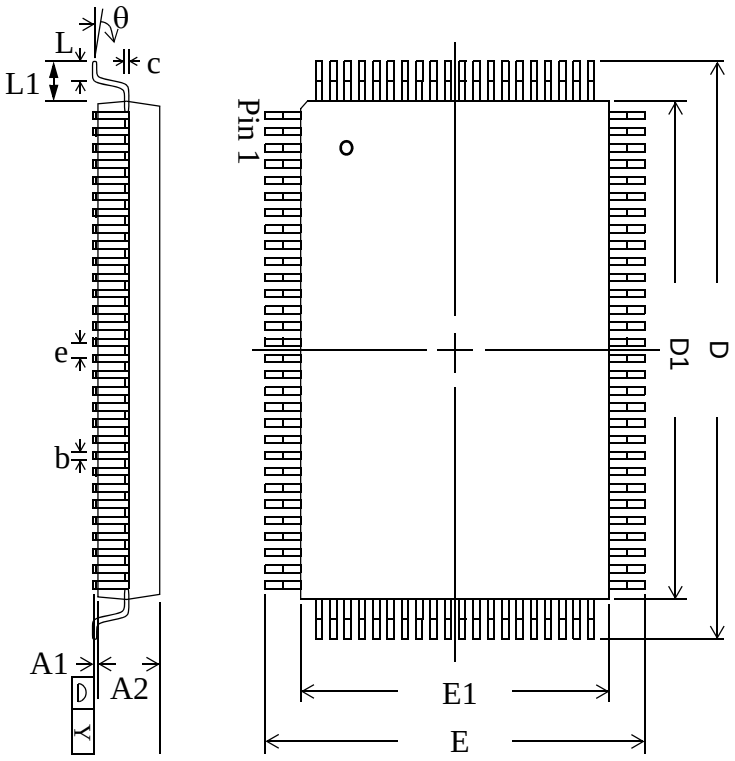
Flow Through Mode Timing (NBT)



*Note: $\overline{E}$ = High(False) if $\overline{E1}$ = 1 or E2 = 0 or $\overline{E3}$ = 1

TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Package	Speed (ns)	T_J[2]
2M x 18	GS8320FZ18AGT-6.5	NBT Flow Through	RoHS-compliant TQFP	6.5	C
2M x 18	GS8320FZ18AGT-7.5	NBT Flow Through	RoHS-compliant TQFP	7.5	C
1M x 36	GS8320FZ36AGT-6.5	NBT Flow Through	RoHS-compliant TQFP	6.5	C
1M x 36	GS8320FZ36AGT-7.5	NBT Flow Through	RoHS-compliant TQFP	7.5	C
2M x 18	GS8320FZ18AGT-6.5I	NBT Flow Through	RoHS-compliant TQFP	6.5	I
2M x 18	GS8320FZ18AGT-7.5I	NBT Flow Through	RoHS-compliant TQFP	7.5	I
1M x 36	GS8320FZ36AGT-6.5I	NBT Flow Through	RoHS-compliant TQFP	6.5	I
1M x 36	GS8320FZ36AGT-7.5I	NBT Flow Through	RoHS-compliant TQFP	7.5	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS8320FZ36AGT-6.50IT.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.
3. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

36Mb Sync SRAM Datasheet Revision History

File Name	Types of Changes Format or Content	Page;Revisions;Reason
8320FZxxA_r1		• Creation of new datasheet

