Preliminary

GS81320Z18/36CQ-333M/250M(S/Q/V)
GS8680Z18/36CQ-333M/250M(S/Q/V)
GS8360Z18/36CQ-333M/250M(S/Q/V)

100-Pin Ceramic QFP
Military Temp

Rad-Hard SRAM

144Mb/72Mb/36Mb PL/FT Synchronous NBT SRAMs

333 MHz–250 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- Aerospace-Level Product
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization; Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- User-configurable Pipeline and Flow Through mode
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ Pin for automatic power-down
- 100-pin Ceramic QFP package available

Radiation Performance

- Total Ionizing Dose (TID) > 300krads(Si)
- Soft Error Rate (SER) = TBR
- Neutrons = TBR
- Single Event Latchup Immunity > 80 MeV.cm^2/mg (125°C)

Functional Description

The GS81320Z18/36CQ (144Mb), GS8680Z18/36CQ (72Mb), and GS8360Z18/36CQ (36Mb) are Synchronous Static SRAMs. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because they are synchronous devices, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

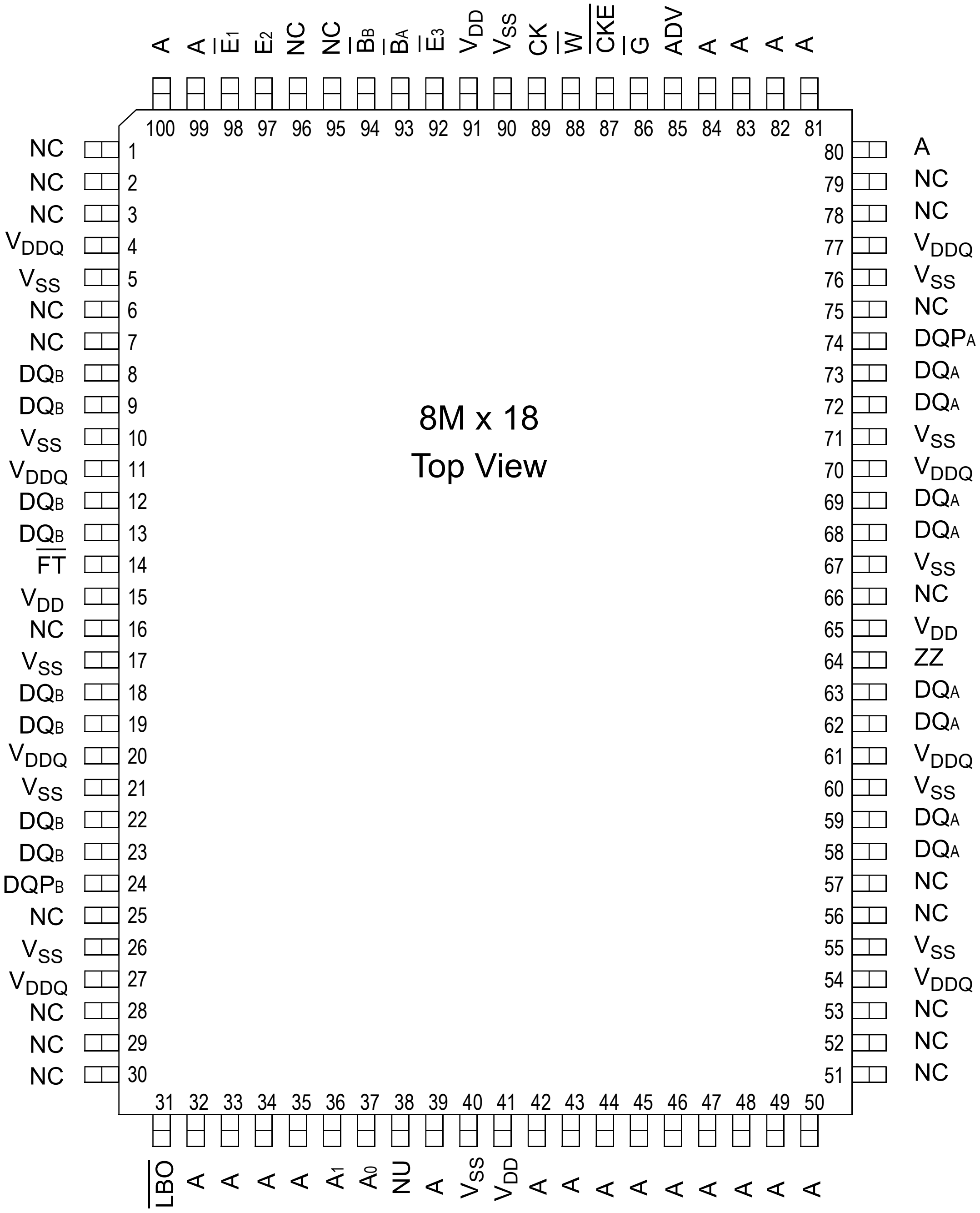
The GS81320Z18/36CQ (144Mb), GS8680Z18/36CQ (72Mb), and GS8360Z18/36CQ (36Mb) may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, meaning that in addition to the rising edge triggered registers that capture input signals, the devices incorporate a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

TheGS81320Z18/36CQ (144Mb), GS8680Z18/36CQ (72Mb), and GS8360Z18/36CQ (36Mb) are implemented with GSI's high performance CMOS technology and are available in a JEDEC-standard 100-pin Ceramic QFP package.

Parameter Synopsis

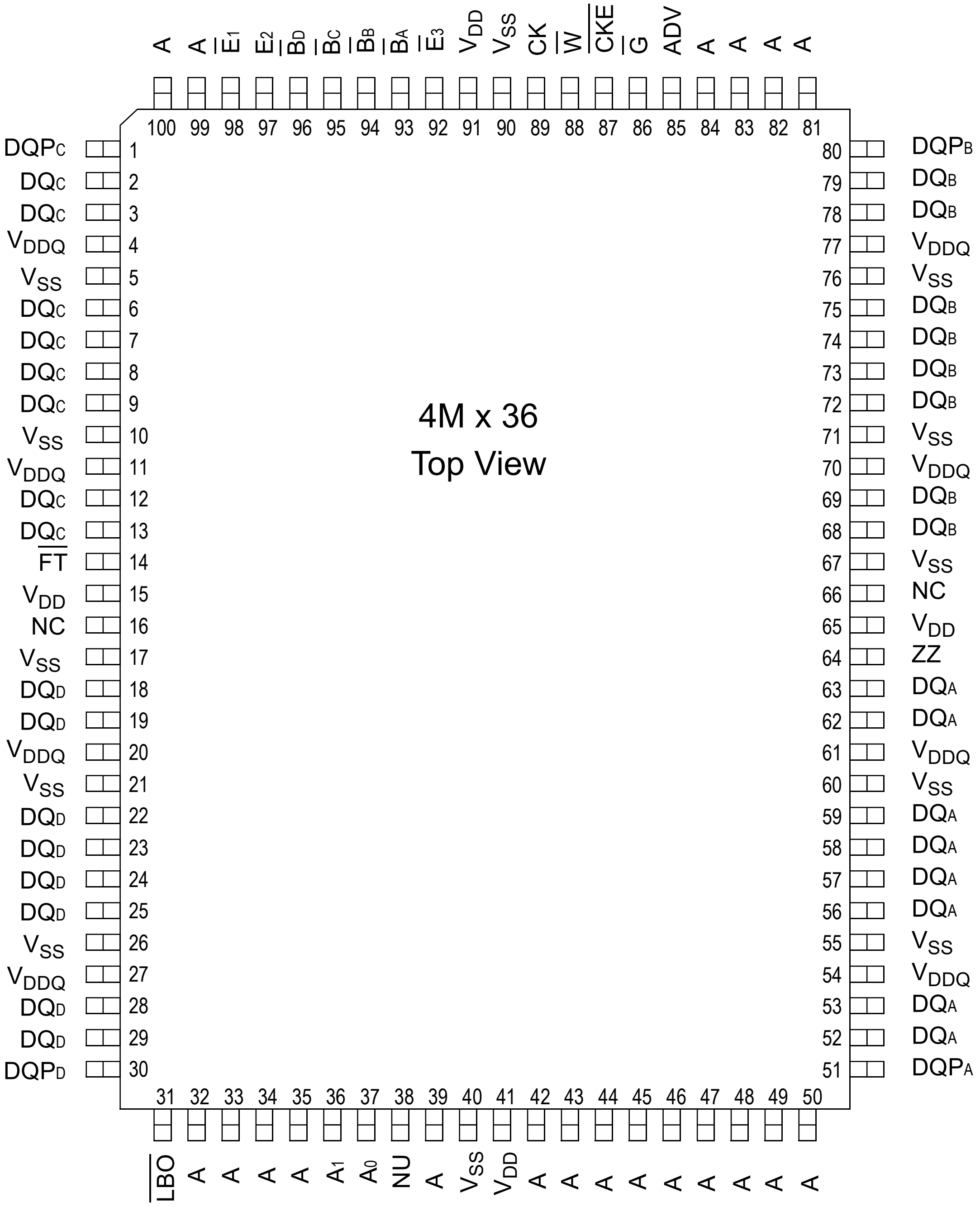
		-333M	-250M	Unit
Pipeline 3-1-1-1	tKQ	2.5	2.5	ns
	tCycle	3.0	4.0	ns
	Curr (x18)	650	550	mA
	Curr (x36)	720	590	mA
Flow Through 2-1-1-1	tKQ	4.5	5.5	ns
	tCycle	4.5	5.5	ns
	Curr (x18)	520	480	mA
	Curr (x36)	555	500	mA

GS81320Z18CQ Pinout (144Mb)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS81320Z36CQ Pinout (144Mb)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

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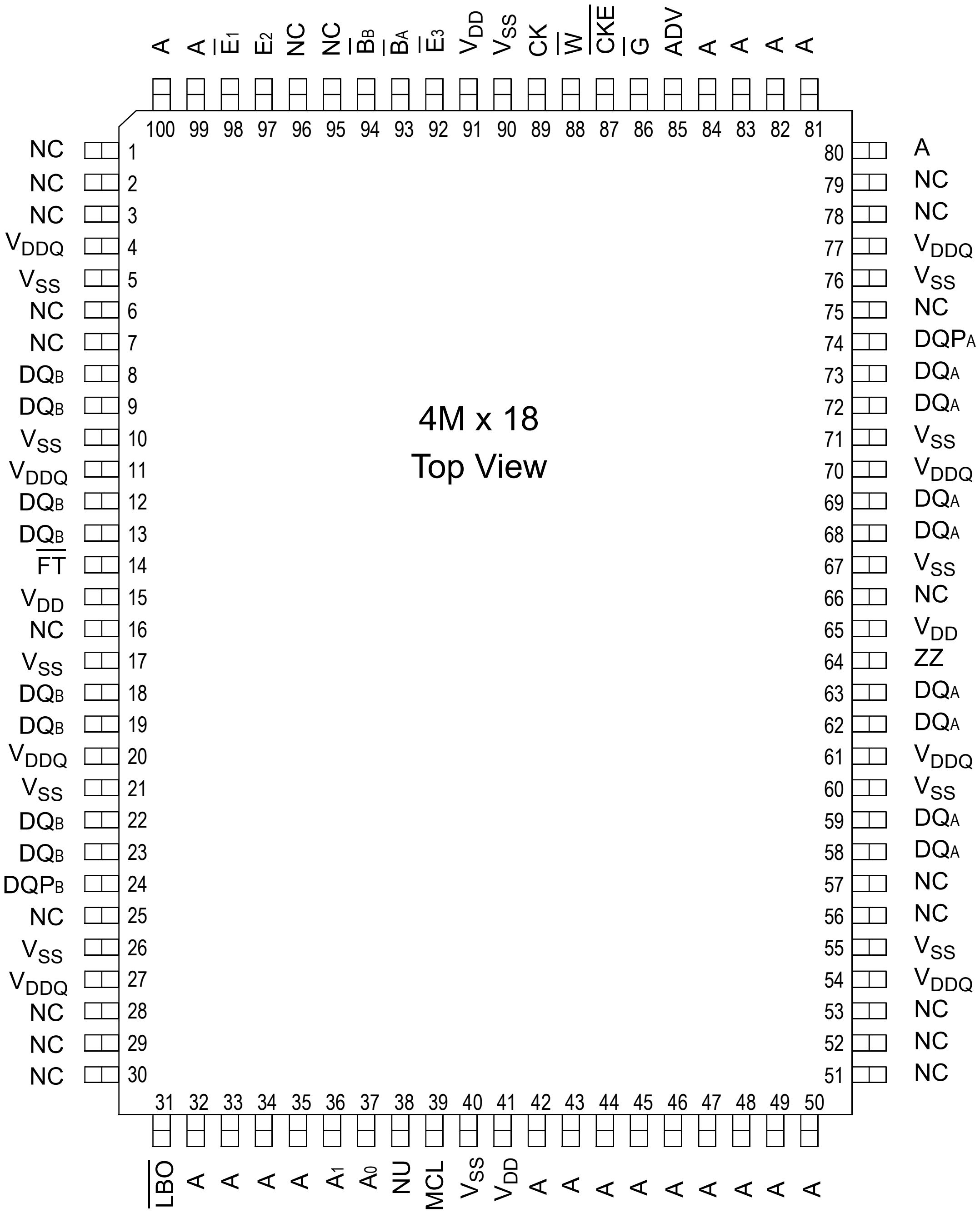
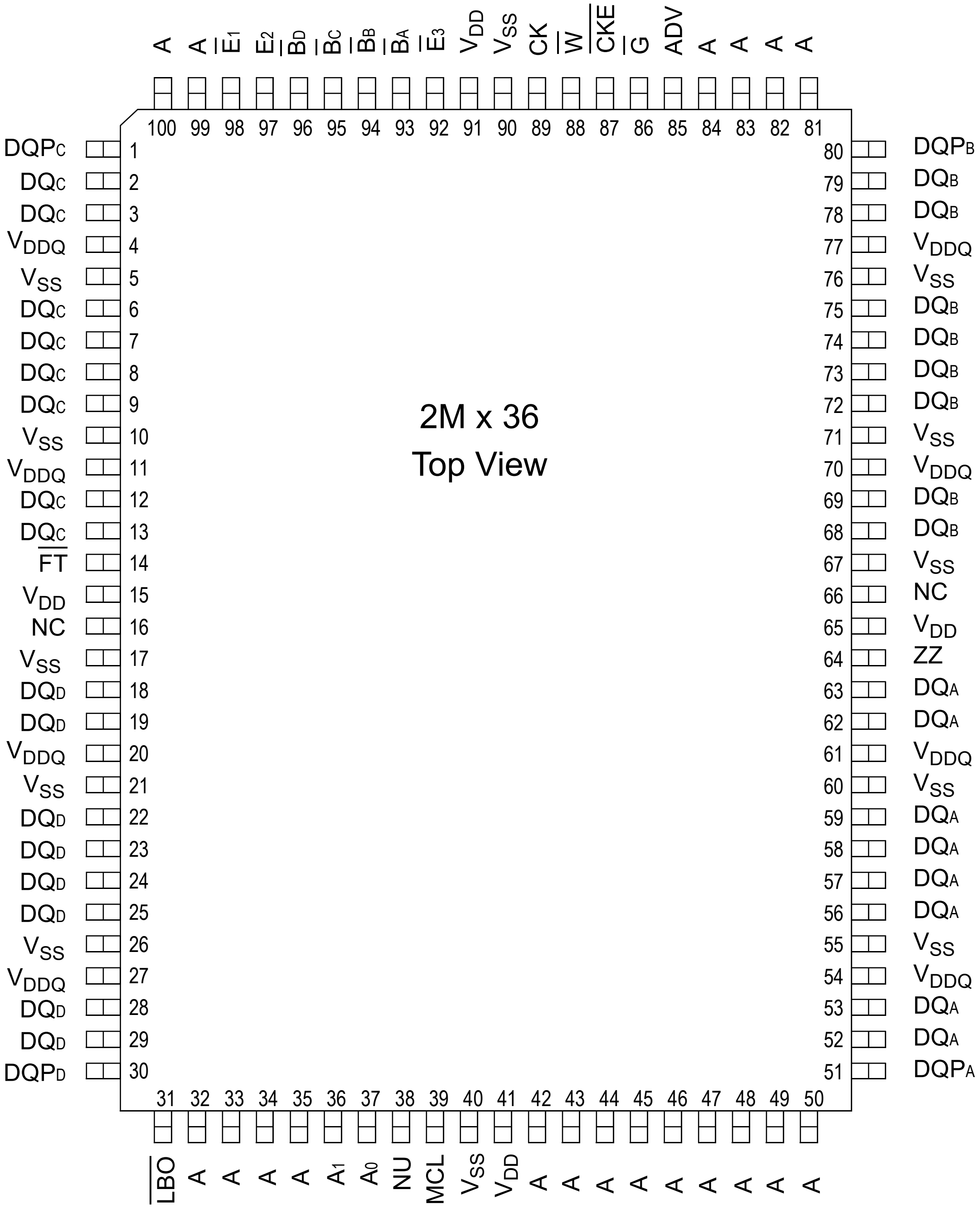
GS8680Z18CQ Pinout (72Mb)



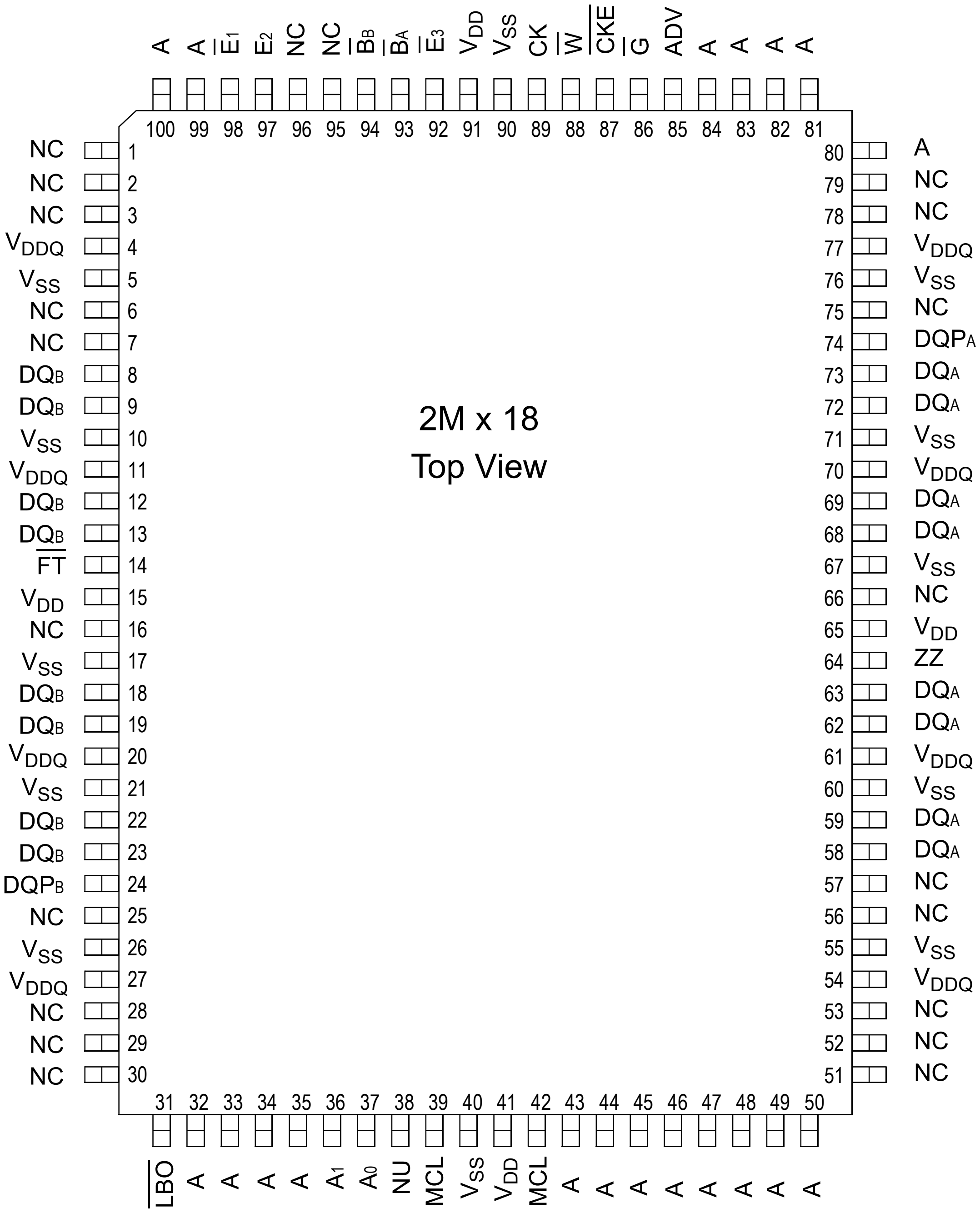
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS8680Z36CQ Pinout(72Mb)



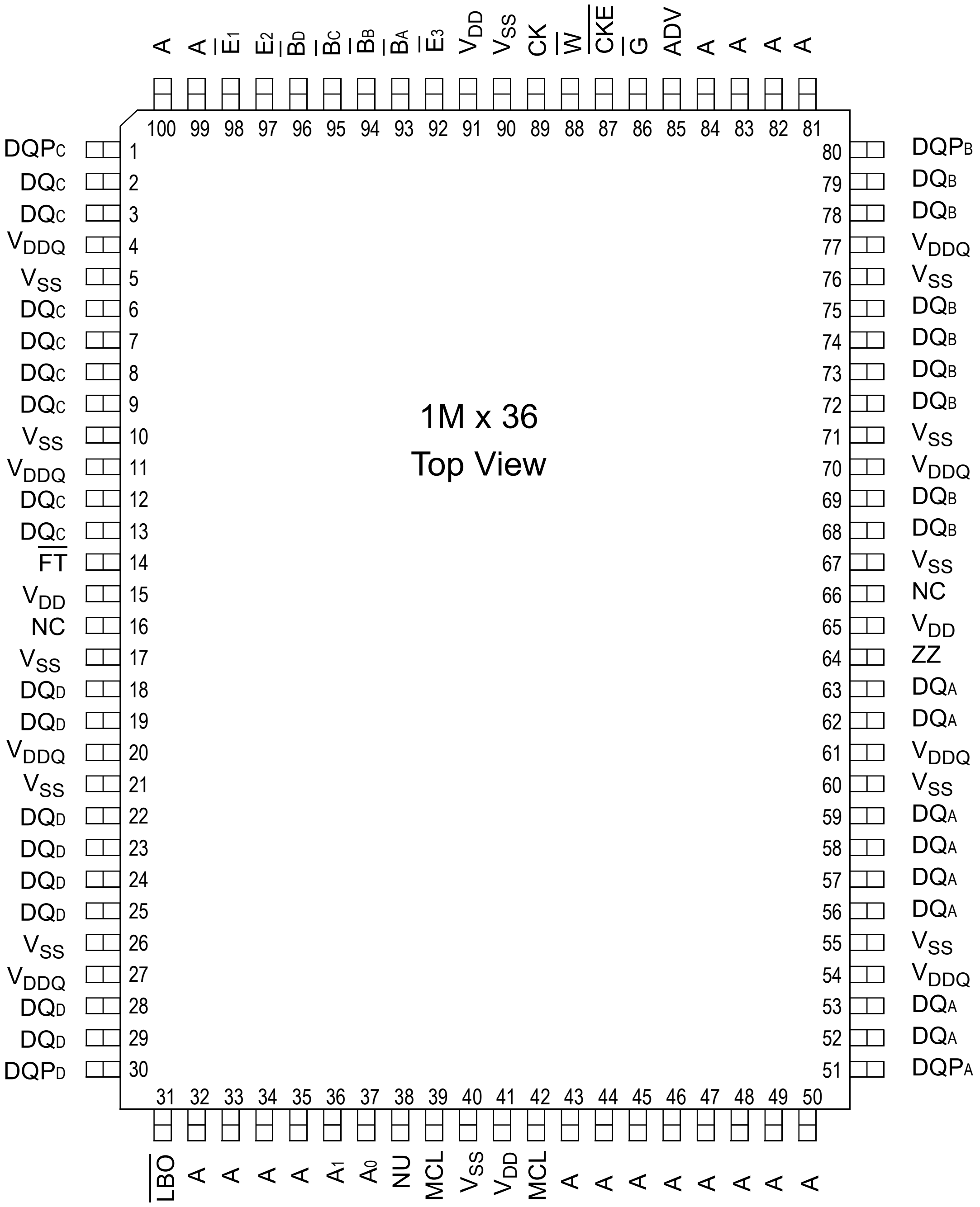
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS8360Z18CQ Pinout (36Mb)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS8360Z36CQ Pinout (36Mb)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

Ceramic QFP Pin Descriptions

Symbol	Type	Description
A_0, A_1	In	Burst Address Inputs; Preload the burst counter
A	In	Address Inputs
CK	In	Clock Input Signal
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_{A1}-DQ_{A9}; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_{B1}-DQ_{B9}; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_{C1}-DQ_{C9}; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_{D1}-DQ_{D9}; active low
$\overline{W}$	In	Write Enable; active low
$\overline{E}_1$	In	Chip Enable; active low
E_2	In	Chip Enable; Active High. For self decoded depth expansion
$\overline{E}_3$	In	Chip Enable; Active Low. For self decoded depth expansion
$\overline{G}$	In	Output Enable; active low
ADV	In	Advance/$\overline{\text{Load}}$; Burst address counter control pin
$\overline{\text{CKE}}$	In	Clock Input Buffer Enable; active low
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ_C	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
ZZ	In	Power down control; active high
$\overline{\text{FT}}$	In	Pipeline/Flow Through Mode Control; active low
$\overline{\text{LBO}}$	In	Linear Burst Order; active low
V_{DD}	In	Core power supply
V_{SS}	In	Ground
V_{DDQ}	In	Output driver power supply
NC	—	No Connect
NU	—	Not Used—There is an internal chip connection to these pins, but they are unused by the device. They may be left unconnected, tied Low (to V_{SS}), or tied High (to V_{DDQ} or V_{DD}).
MCL	In	Must Connect Low—May be tied to V_{SS} directly or via a 1kΩ resistor.

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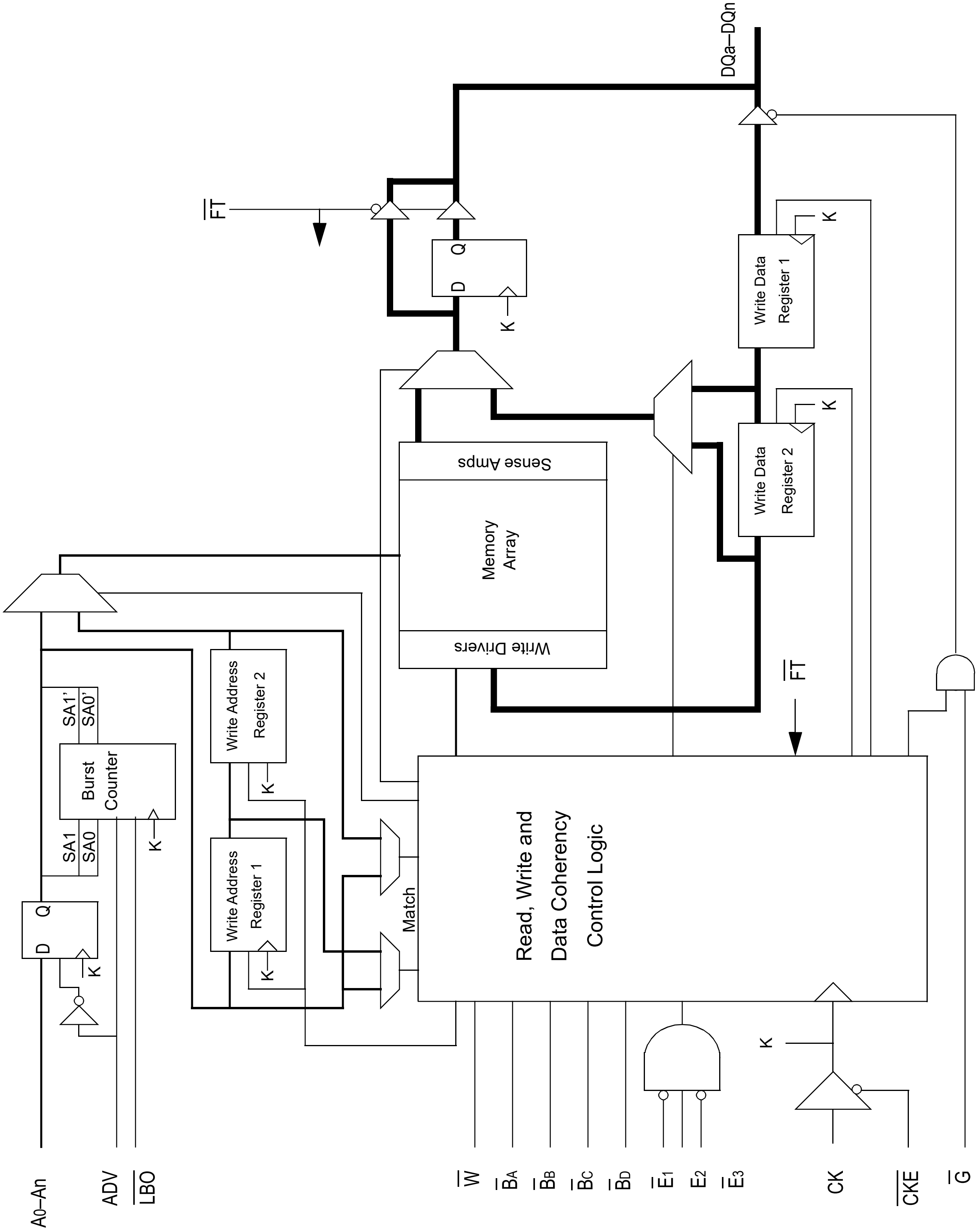
x36 NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{\text{CKE}}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/Load pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2 and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte “a”	L	L	H	H	H
Write Byte “b”	L	H	L	H	H
Write Byte “c”	L	H	H	L	H
Write Byte “d”	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{\text{CKE}}$ is asserted Low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active, and the Write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, & $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

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Synchronous Truth Table

Operation	Type	Address	CK	$\overline{\mathrm{CKE}}$	ADV	$\overline{\mathrm{W}}$	$\overline{\mathrm{Bx}}$	$\overline{\mathrm{E}}1$	E2	$\overline{\mathrm{E}}3$	$\overline{\mathrm{G}}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,10
NOP/Read, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	2
Dummy Read, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Abort, Begin Burst	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Write Cycle, Continue Burst	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,3,10
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3,10
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

Notes:

1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{\mathrm{W}}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
3. $\overline{\mathrm{G}}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{\mathrm{CKE}}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{\mathrm{CKE}}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don’t Care; H = Logic High; L = Logic Low; $\overline{\mathrm{Bx}}$ = High = All Byte Write signals are high; $\overline{\mathrm{Bx}}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{\mathrm{G}}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{\mathrm{CKE}}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

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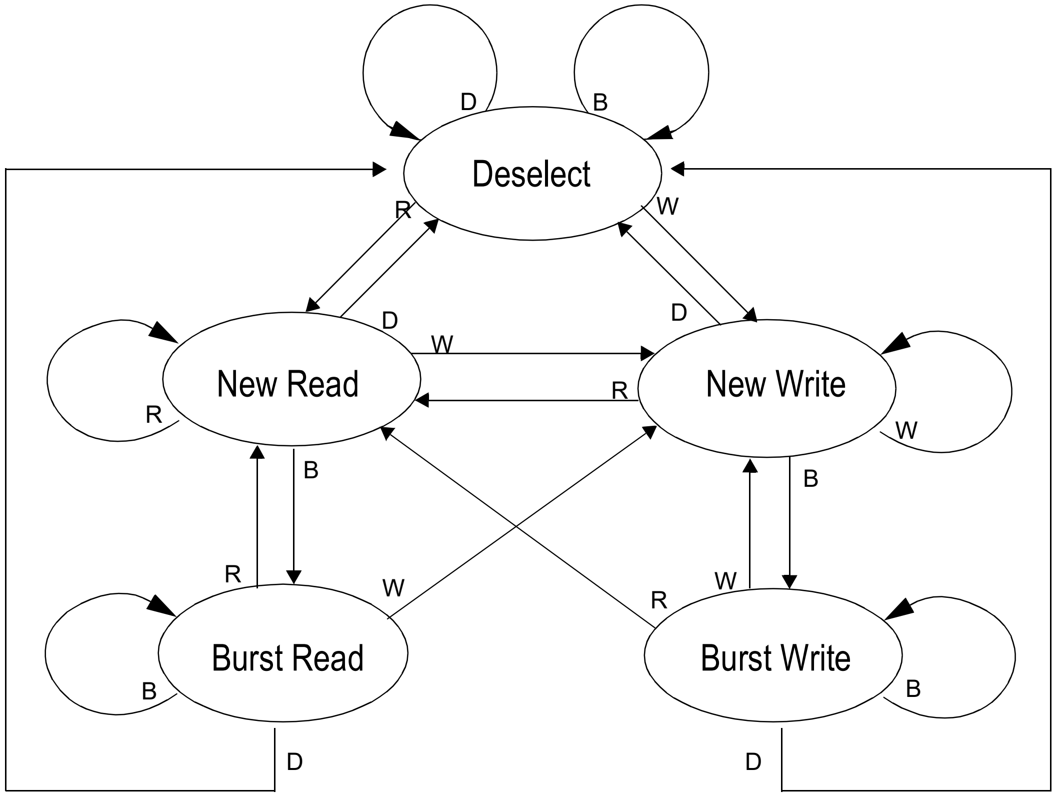
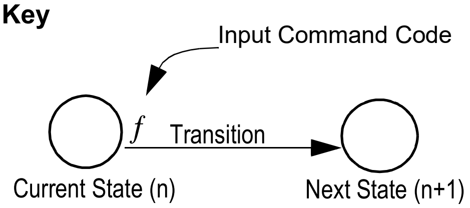
Pipeline and Flow Through Read Write Control State Diagram

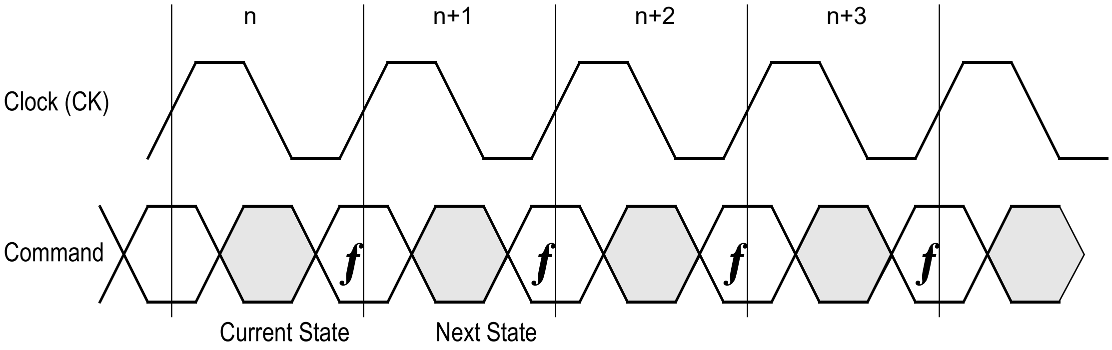


Key



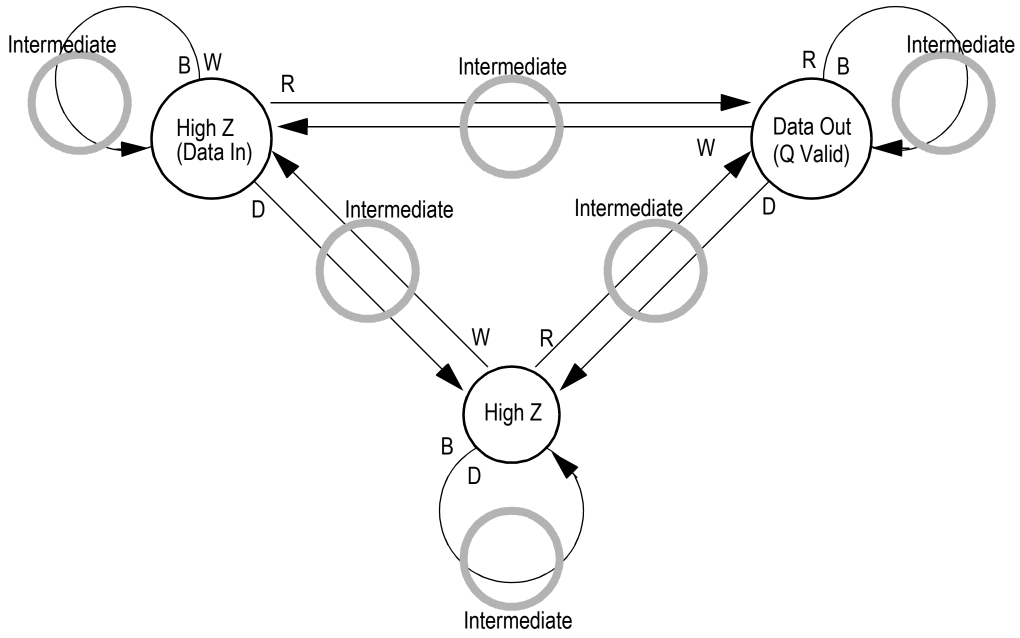
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B and D represent input command codes ,as indicated in the Synchronous Truth Table.



Current State and Next State Definition for Pipeline and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram



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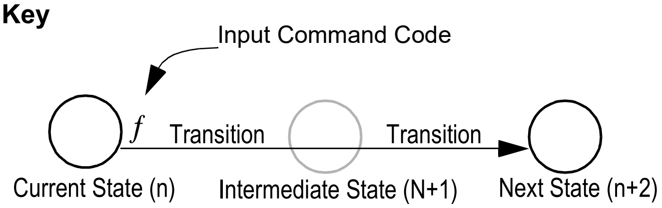
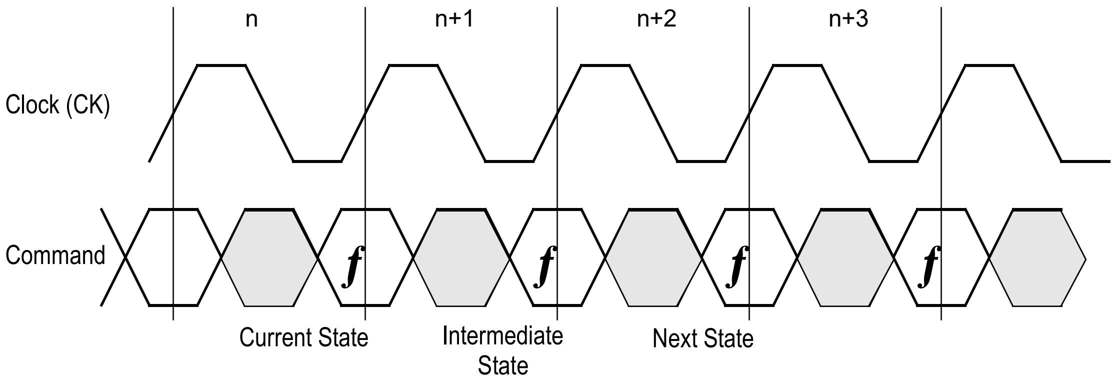


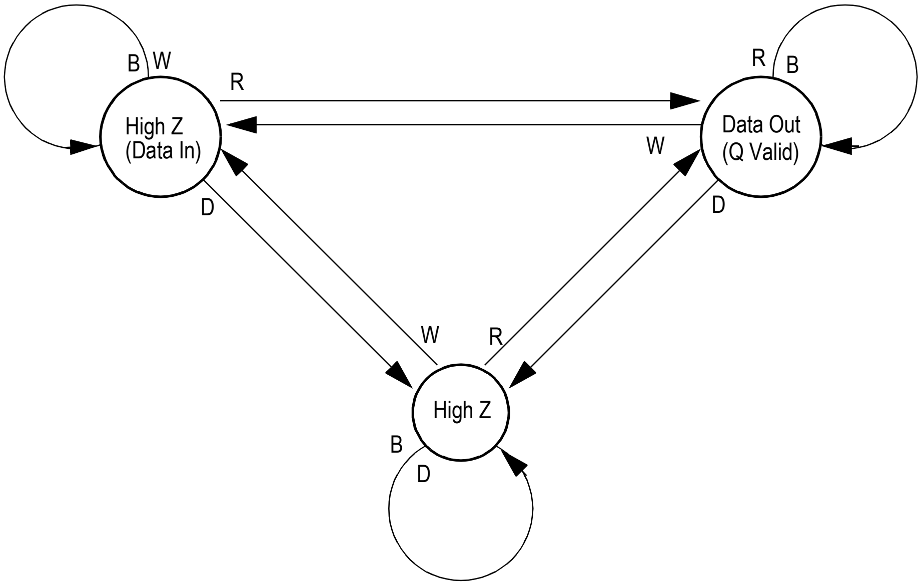
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram



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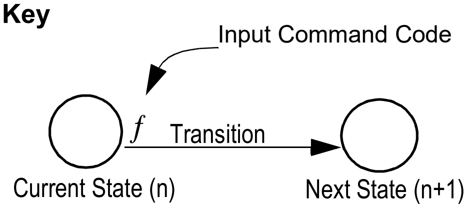
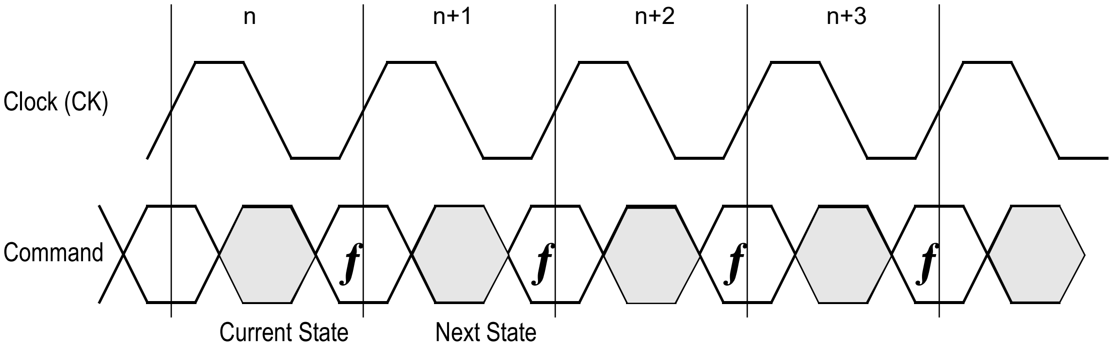


Notes

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{\text{LBO}}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

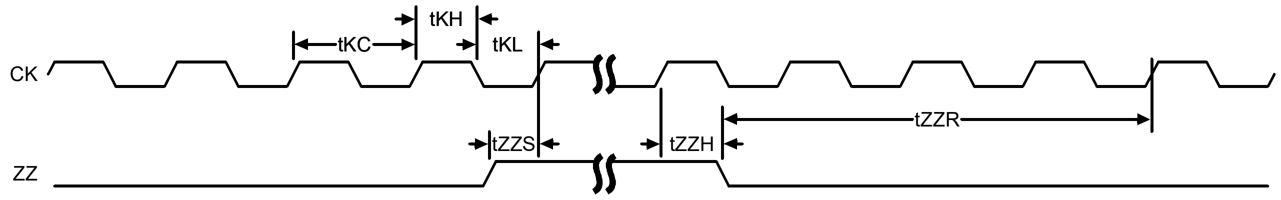
Note:
The burst counter wraps to initial state on the 5th clock.

Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a deselect or read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipeline mode via the $\overline{\text{FT}}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–65 to 150 (TBR)	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Note:

V_{IH} (max) must be met for any instantaneous value of V_{DD}.

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V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	$0.6*V_{DD}$	—	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	–0.3	—	$0.3*V_{DD}$	V

Note:
V_{IH} (max) must be met for any instantaneous value of V_{DD}.

Operating Temperature

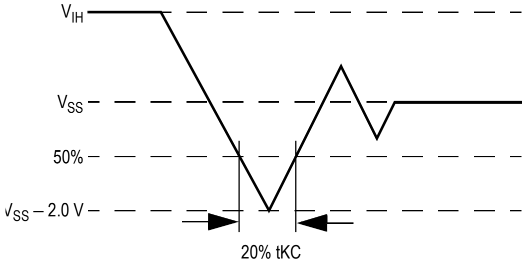
Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature	T_J	–55	25	125	°C

Thermal Impedance

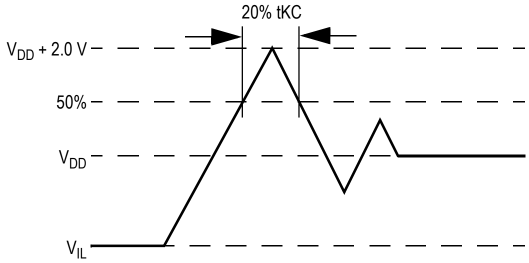
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100-pin Ceramic QFP	4-layer (TBR)	n/a	n/a	n/a	TBD	TBD

Notes:
1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Capacitance

($T_A = 25^oC$, f = 1 MHz, $V_{DD} = 2.5$ V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0$ V	6	7	pF

Note:
These parameters are sample tested.

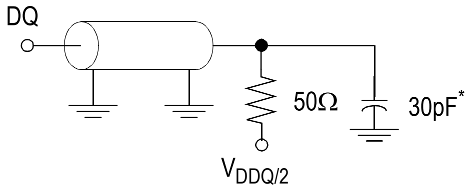
AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} – 0.2$ V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	**Fig. 1**

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{\text{FT}}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

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Operating Currents

Parameter	Test Conditions	Mode		Symbol	-333M	-250M	Unit
					–55 to 125°C	–55 to 125°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x32/x36)**	Pipeline	I_{DD}	720	590	mA
			Flow Through	I_{DD}	555	500	mA
		(x18)	Pipeline	I_{DD}	650	550	mA
			Flow Through	I_{DD}	520	480	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	220	220	mA
			Flow Through	I_{SB}	220	220	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	240	240	mA
			Flow Through	I_{DD}	240	240	mA

Notes:

1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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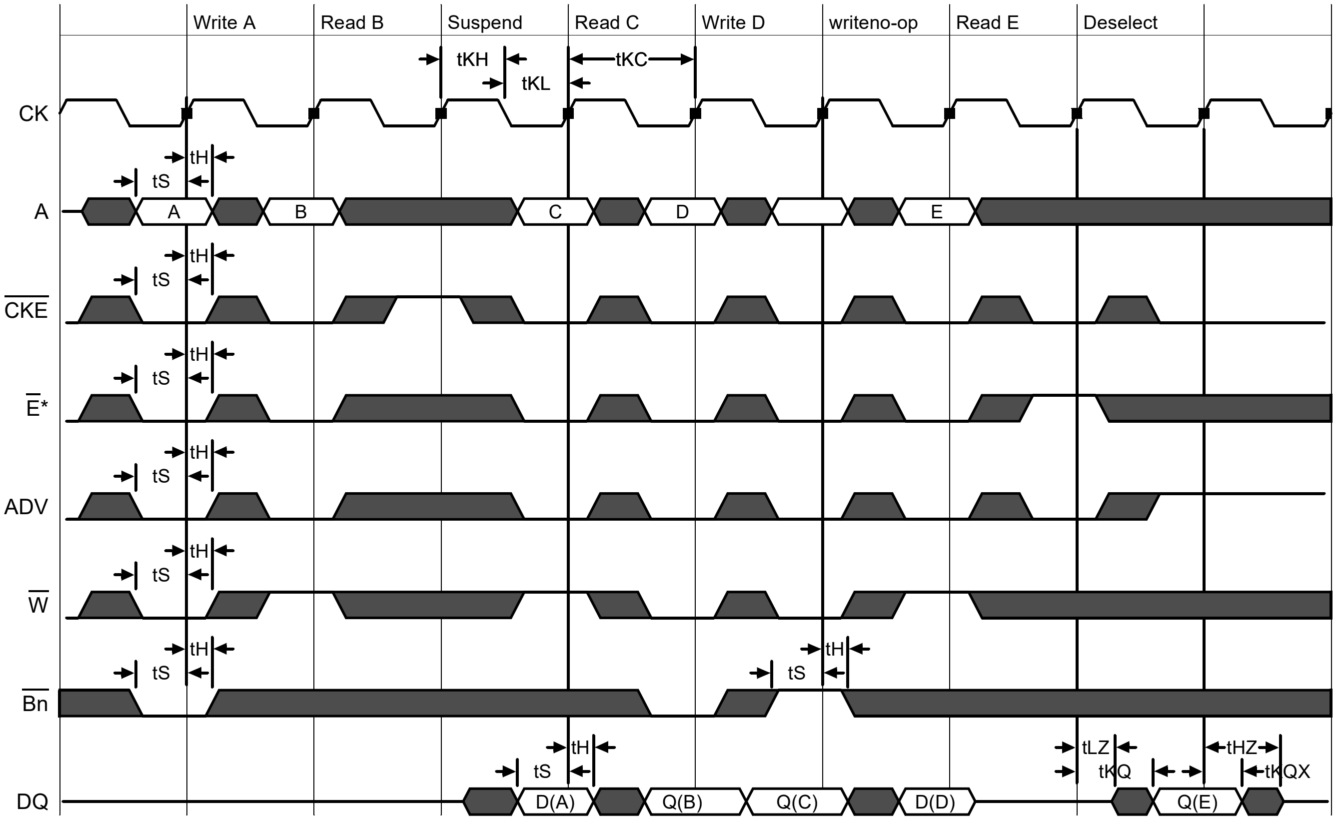
AC Electrical Characteristics

	Parameter	Symbol	-333M		-250M		Unit
			Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	3.0	—	4.0	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.5	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	ns
	Setup time	tS	1.0	—	1.2	—	ns
	Hold time	tH	0.1	—	0.2	—	ns
Flow Through	Clock Cycle Time	tKC	4.5	—	5.5	—	ns
	Clock to Output Valid	tKQ	—	4.5	—	5.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	ns
	Setup time	tS	1.3	—	1.5	—	ns
	Hold time	tH	0.3	—	0.5	—	ns
	Clock HIGH Time	tKH	1.0	—	1.3	—	ns
	Clock LOW Time	tKL	1.2	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	2.5	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	2.5	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	2.5	ns
	ZZ setup time	tZZS[2]	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	ns

Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing (NBT)



*Note: $\overline{E}$ = High(False) if $\overline{E1}$ = 1 or E2 = 0 or $\overline{E3}$ = 1

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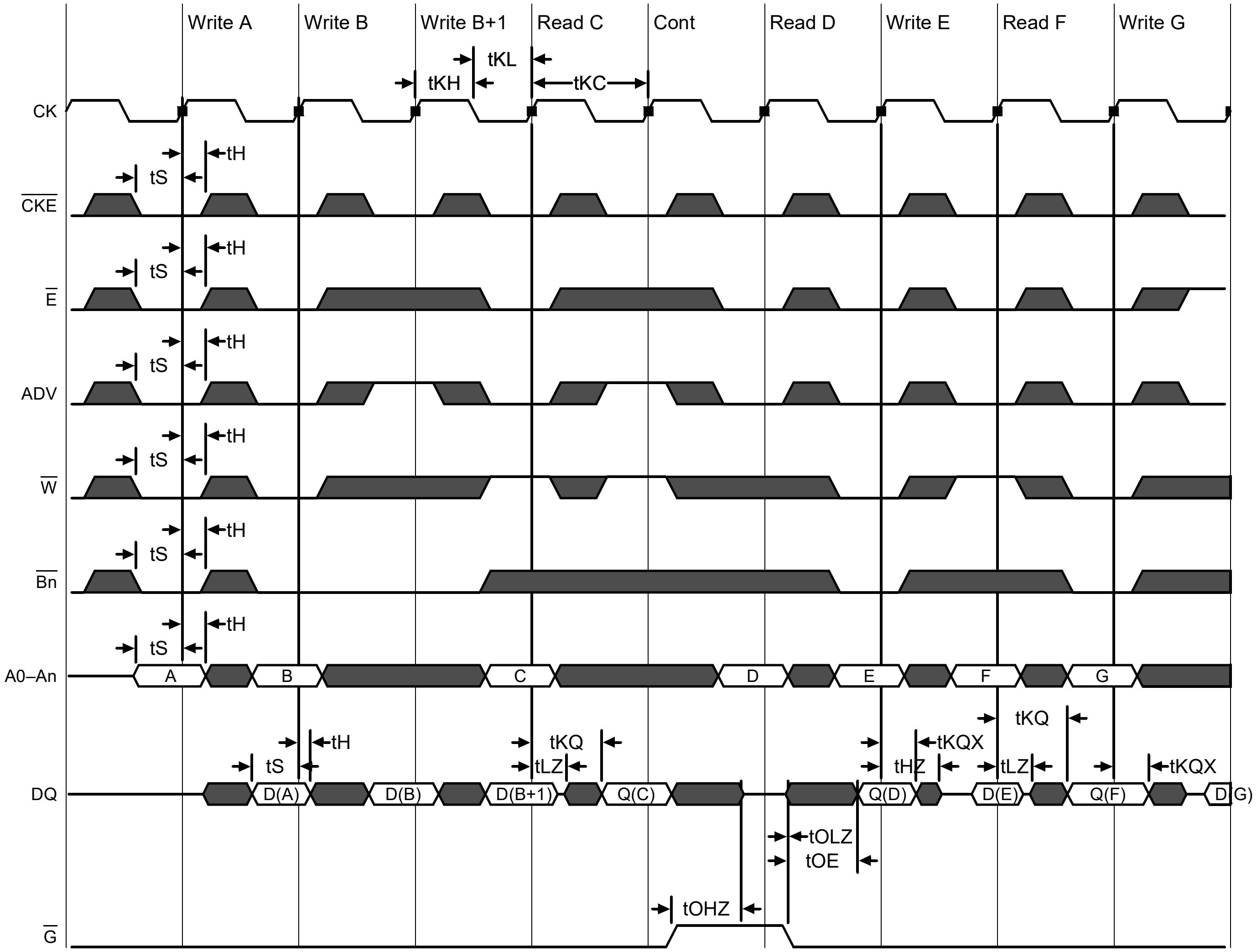
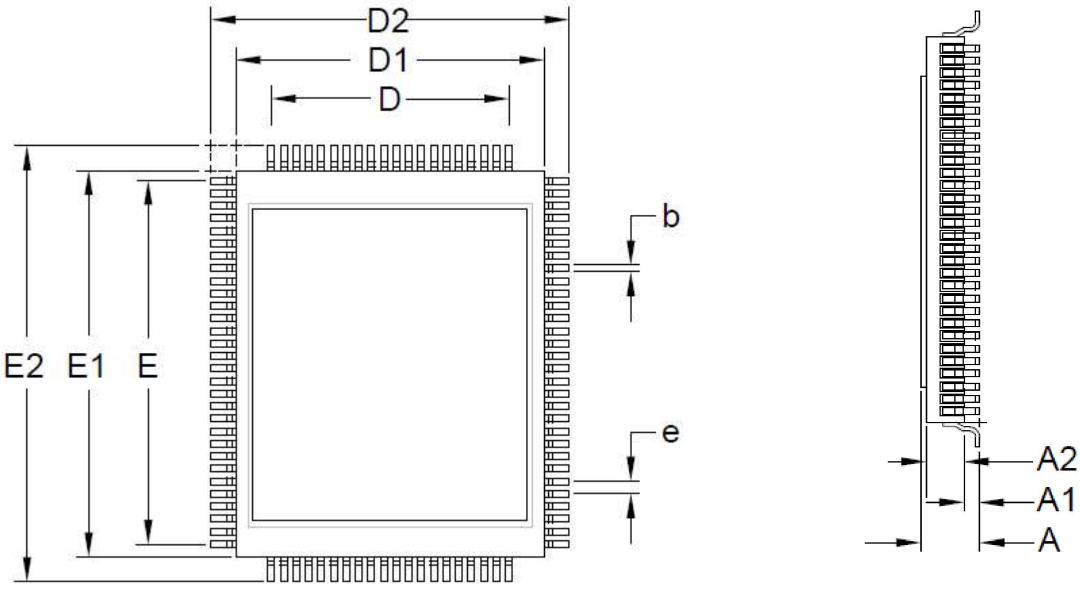
Flow Through Mode Timing (NBT)



*Note: $\overline{E}$ = High(False) if $\overline{E1}$ = 1 or E2 = 0 or $\overline{E3}$ = 1

Ceramic QFP Package Drawing (Package CQ)



Symbol	Min.	Max
A	2.84	3.03
A1	0.70	0.80
A2	1.88	1.98
b	0.30	0.35
c	0.19	0.20
D	12.35 BSC	
D1	15.84	16.16
D2	18.14	19.06
E	18.85 BSC	
E1	19.80	20.20
E2	22.10	23.10
e	0.65 BSC	
L	1.15	1.45
L1	0.40	0.70
R	0.19	0.20

Note:
All dimensions are in millimeters (mm).

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number	Type	Package	Speed (MHz)	T_J*
144Mb					
4M x 36	GS81320Z36CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
4M x 36	GS81320Z36CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
8M x 18	GS81320Z18CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
8M x 18	GS81320Z18CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
4M x 36	GS81320Z36CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
4M x 36	GS81320Z36CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
8M x 18	GS81320Z18CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
8M x 18	GS81320Z18CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
4M x 36	GS81320Z36CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
4M x 36	GS81320Z36CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
8M x 18	GS81320Z18CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
8M x 18	GS81320Z18CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
72Mb					
2M x 36	GS8680Z36CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
2M x 36	GS8680Z36CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
4M x 18	GS8680Z18CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
4M x 18	GS8680Z18CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
2M x 36	GS8680Z36CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
2M x 36	GS8680Z36CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M

* M = Military Temperature Range

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Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number	Type	Package	Speed (MHz)	T_J*
4M x 18	GS8680Z18CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
4M x 18	GS8680Z18CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
2M x 36	GS8680Z36CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
2M x 36	GS8680Z36CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
4M x 18	GS8680Z18CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
4M x 18	GS8680Z18CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
36Mb					
1M x 36	GS8360Z36CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
1M x 36	GS8360Z36CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
2M x 18	GS8360Z18CQ-333MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
2M x 18	GS8360Z18CQ-250MS	NBT Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
1M x 36	GS8360Z36CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
1M x 36	GS8360Z36CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
2M x 18	GS8360Z18CQ-333MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
2M x 18	GS8360Z18CQ-250MQ	NBT Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
1M x 36	GS8360Z36CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
1M x 36	GS8360Z36CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
2M x 18	GS8360Z18CQ-333MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
2M x 18	GS8360Z18CQ-250MV	NBT Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M

* M = Military Temperature Range

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144Mb Sync SRAM Datasheet Revision History

File Name	Types of Changes Format or Content	Revisions
0Z1836CQ_r1-RAD		• Creation of new datasheet • (Rev1.00a: Corrected erroneous Truth Table)
0Z1836CQ_r1_01-RAD	Content	• Added new part numbers to designate qualification nomenclature (S/Q/V) • (Rev1.01a: Changed unused address pins from NC to MCL; Changed pin 38 from NC to NU for 72Mb and 36Mb)

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