Features

- Low Supply Current ~ 55uA (per circuit)
- Low Shutdown Current ~0.1uA (Typ.)
- Output Current ~300mA
- High Power Supply Rejection Ratio ~75db@1KHz
- 1.7~5.5V Operation
- ±1.5% Initial Voltage Accuracy
- Low Temperature Drift Coefficient ~50ppm
- Line Regulation ~0.02%/V(Typ.)
- Low ESR Capacitor ~1uF ceramic capacitor
- SOT-23-6
 TSOT-23-6
 WDFN6-1.6x1.6
 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Portable communication equipment
- Notebook Computer
- Battery Powered Systems

Typical Application

General Description

The GS7129 is a CMOS linear regulator. It is featuring ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current, and supports preset 1.1V, 1.2V, 1.3V, 1.5V, 1.8V, 1.85V, 1.9V, 2.0V, 2.3V, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.3V output voltage versions.

Based on its low quiescent current consumption and its less than 1uA shutdown mode, the GS7129 is ideal for battery- powered applications. The high power supply rejection ratio of the GS7129 holds well for low input voltages typically encountered in battery- operated systems. The regulator is stable with small ceramic capacitive loads (1µF typical).

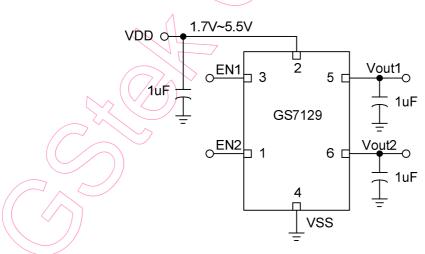
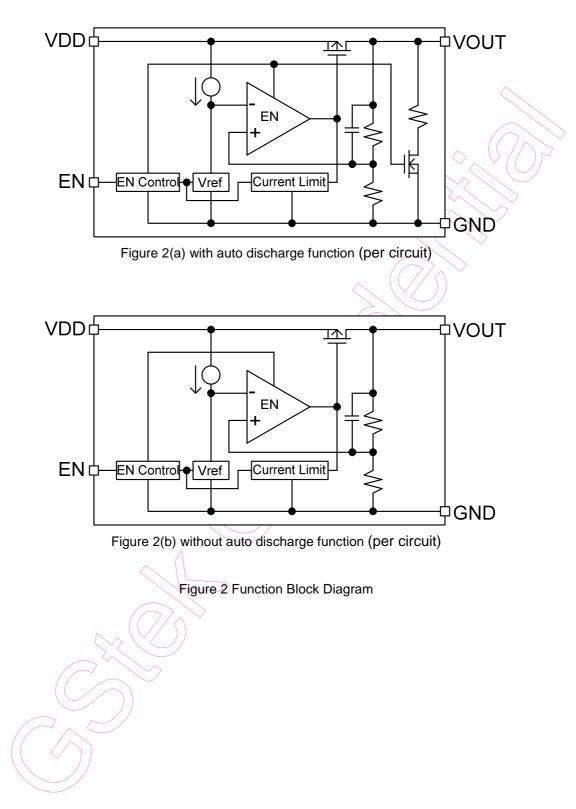


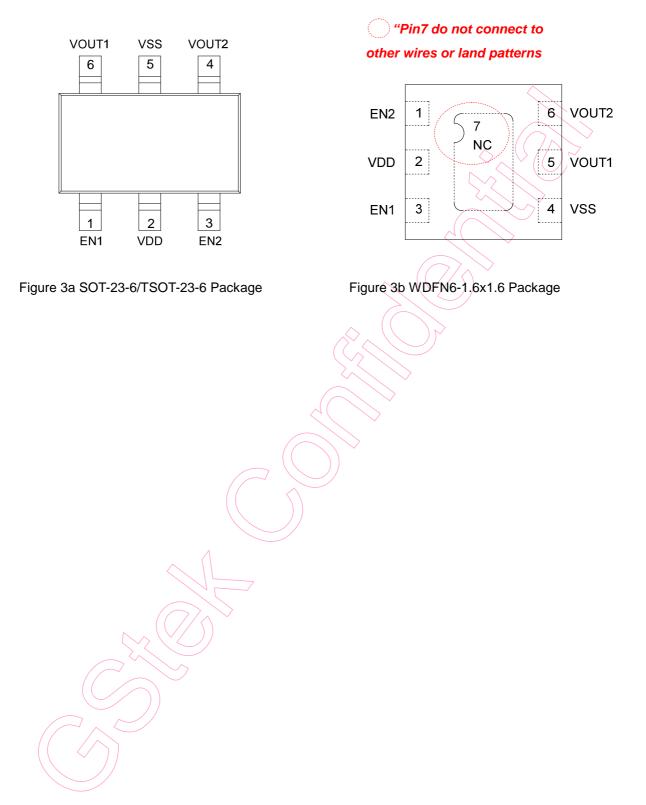
Figure.1 Typical Application of GS7129

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Function Block Diagram



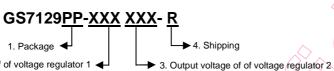
Pin Configuration



Pin Descriptions

	No			
SOT-23-6/ TSOT-23-6	WDFN6-1.6x1.6	Name	I/O type	Description
1	3	EN1	I	Enable Pin 1
2	2	VDD	I	Input Voltage Pin
3	1	EN2	I	Enable Pin 2
4	6	VOUT2	0	Output Voltage Pin2
5	4	VSS	I/O	Ground pin
6	5	VOUT1	0	Output Voltage Pin1
	7	NC		NC pin.

Ordering Information



2. Output voltage of of voltage regulator 1

No	Item	Contents
		ST: SOT-23-6
1	Package	TS:TSOT-23-6
		UD:WDFN6-1.6x1.6
		1P1:1.1V, 1P2: 1.2V, 1P3: 1.3V, 1P5: 1.5V, 1P8: 1.8V,
	Output voltage of voltage regulator 1	1P85: 1.85V, 1P9: 1.9V, 2P0: 2.0V, 2P3: 2.3V, 2P5: 2.5V,
2	Output voltage of voltage regulator 1	2P6: 2.6V, 2P7: 2.7V, 2P8: 2.8V, 285: 2.85V, 2P9: 2.9V,
		3P0: 3.0V, 3P1: 3.1V, 3P3: 3.3V
		1P1:1.1V, 1P2: 1.2V, 1P3: 1.3V, 1P5: 1.5V, 1P8: 1.8V,
3	Output voltage of voltage regulator 2	1P85: 1.85V, 1P9: 1.9V, 2P0: 2.0V, 2P3: 2.3V, 2P5: 2.5V,
3		2P6: 2.6V, 2P7: 2.7V, 2P8: 2.8V, 285: 2.85V, 2P9: 2.9V,
		3P0: 3.0V, 3P1: 3.1V, 3P3: 3.3V
4	Shipping	R: Tape & Reel

Example: G\$7129 SOT-23-6 1.8V and 2.8V Tape & Reel ordering information is "G\$7129ST-1P82P8-R"

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VIN to GND	V _{IN}	-0.3 < V _{IN} < 6	V
VEN to GND	V _{EN}	-0.3 < V _{EN} < 6	V
Output Voltage	V _{OUT}	-0.3 < V _{OUT} <v<sub>IN+0.3</v<sub>	V
Output Current	I _{OUT}	300	> mA
Package Power Dissipation at $T_A \leq 25$ °C	P _{D_SOT-23-6}	400	mW
Package Power Dissipation at $T_A \leq 25$ °C	P _{D_TSOT-23-6}	455	mW
Package Power Dissipation at $T_A \leq 25$ °C	P _{D_WDFN6-1.6x1.6}	560	mW
Junction Temperature	TJ	- 45 ~ 150	ĉ
Storage Temperature	T _{STG}	- 65 ~ 150	С С
Lead Temperature (Soldering) 10S	T _{LEAD}	260	С С
ESD (Human Body Mode) (Note 2)	$V_{ESD_{HBM}}$	2К	V
ESD (Machine Mode) (Note 2)	V _{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θJA_SOT-23-6	250	°C/W
Thermal Resistance Junction to Ambient	θ _{JA_TSOT-23-6}	220	°C/W
Thermal Resistance Junction to Ambient	θJA_WDFN6-1.6x1.6	179	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VIN to GND	V _{IN}	1.7 to 5.5	V
Junction Temperature	ΤJ	-40 ~ 125	ĉ
Ambient Temperature	T _A	-40 ~ 85	C

Electrical Characteristics

 $(V_{IN} = V_{OUT} + 1V, T_A = T_J = 25$ °C, C $_{IN} = C_L = 1$ uF, $I_{OUT} = 1$ mA, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Тур	Мах	Units		
SUPPLY VOLTAGE SECTION								
Supply Voltage	V _{IN}		1.7	\langle	5.5	V		
Supply Current (per circuit)	I _{VIN}	Unload		55	70	uA		
Standby Current	I _{STBY}	$V_{EN}=0$ or $V_{EN}=V_{IN}$	\land	0.1	1.0	uA		
EN Input Current	I _{EN}	V _{EN} = 6.5V		0.3	\sum	uA		
Output Current	I _{OUT}	$V_{DD} \ge V_{OUT}$ +1V	300			mA		
OUTPUT SECTION								
Output Voltage	V _{out}	I _{OUT} =1mA, V _{OUT} =1.1V,1.2V, 1.3V, 1.5V, 1.8V, 1.85V, 1.9V 2.0V, 2.3V, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V 3.3V	-1.5	>	+1.5	%		
Dropout Voltage (Note 5)	V _{DROP}	$V_{OUT}=1.1V$ $1.2V \le V_{OUT}<1.5^{\circ}$ $1.5V \le V_{OUT}<1.7^{\circ}$ $1.7V \le V_{OUT}<2.0^{\circ}$ $2.0V \le V_{OUT}<2.5^{\circ}$ $2.5V \le V_{OUT}<2.8^{\circ}$ $2.8V \le V_{OUT}<3.3^{\circ}$	V V V V	680 530 460 400 350 310 280	950 870 660 580 470 400 360	mV		
Line Regulation		V _{IN} = V _{OUT} +0.5V to 6.5V, I _{OUT} =1mA		0.05	0.10	%/V		
Load Regulation		V _{IN} = V _{OUT} +1V, I _{OUT} =1mA to 100mA		15	40	mV		
Ripple Rejection Rate	PSRR	V _{IN} =MAX{V _{OUT} +1.0V, 3V}, Ripple 0.2Vp-p, I _{OUT} =30mA, f=1KHz		75		dB		
Limit Current	llim	V _{IN} =3.5V	400	490	700	mA		
Short Current	Ishort	V _{OUT} =0V, V _{IN} =3.5V		50		mA		
EN Input Voltage High	V _{ENH}		1.2			V		
EN Input Voltage Low	V _{ENL}				0.3	V		
CL Auto-Discharge Resistance (Note 6)	Rdischg	V_{IN} =4.0V, (V_{EN} =0V or V_{EN} = V	(_N)	110		Ω		

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2-Circuit Low Noise 300mA LDO Regulator

GS7129

Temperature Drift		I _{OUT} =1mA, T _A = -40℃ to +85℃	50	ppm/° C
Thermal Shutdown Temperature	T_{SD}	$T_{J}Rising$	150	ĉ
Thermal Shutdown Returned Temperature			130	ĉ

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A=25$ °C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

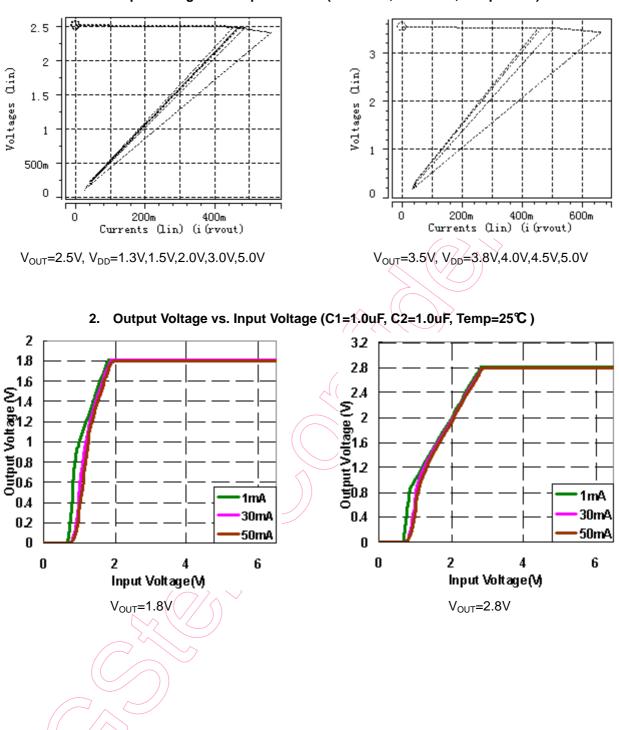
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The dropout voltage is defined as V_{IN} - V_{OUT} , which is measured when V_{OUT} is 98%* V_{OUT} .

Note 6. The output voltage Auto discharge function is optional.

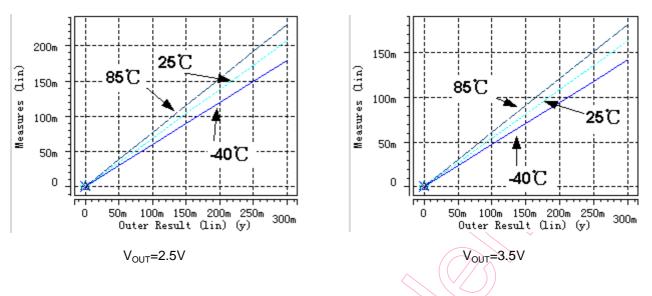
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Typical Characteristics



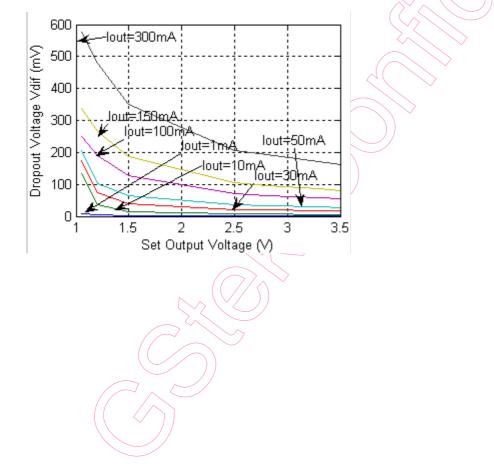
1. Output Voltage vs. Output Current (C1=1.0uF, C2=1.0uF, Temp=25℃)

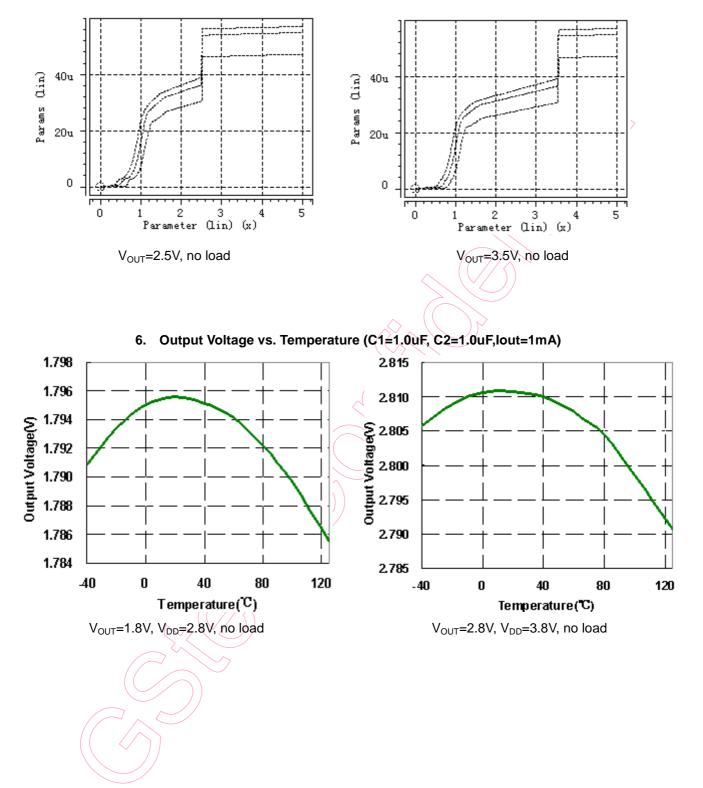
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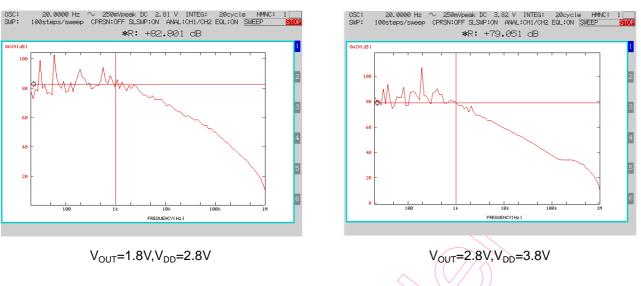
3. Dropout Voltage vs. Output Current (C1=1.0uF, C2=1.0uF)





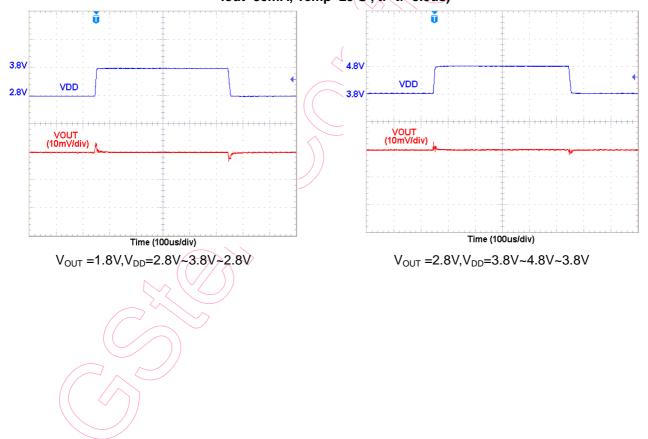


5. Current Consumption vs. Input Voltage (C1=1.0uF, C2=1.0uF, lout=1mA)

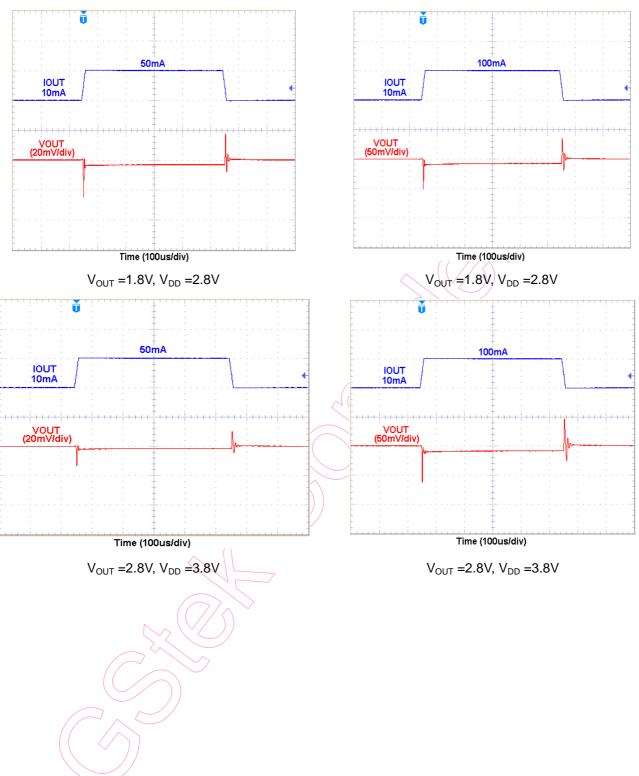


7. Ripple Rejection (C1=1.0uF, C2=1.0uF, lout=1mA, Temp=25℃)

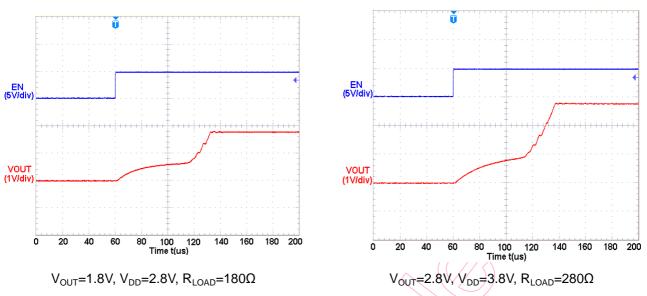
8. Transient Response Characteristics when Input Common to Vr1 and Vr2 (C1=1.0uF, C2=1.0uF, Iout=30mA, Temp=25°C, tr=tf=5.0us)



GS7129

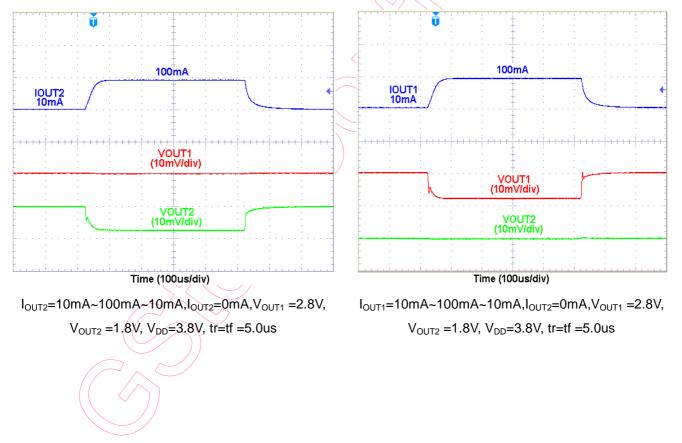


9. Transient Response Characteristics of load (C1=1.0uF, C2=1.0uF, Temp=25°C, tr=tf=5.0us)

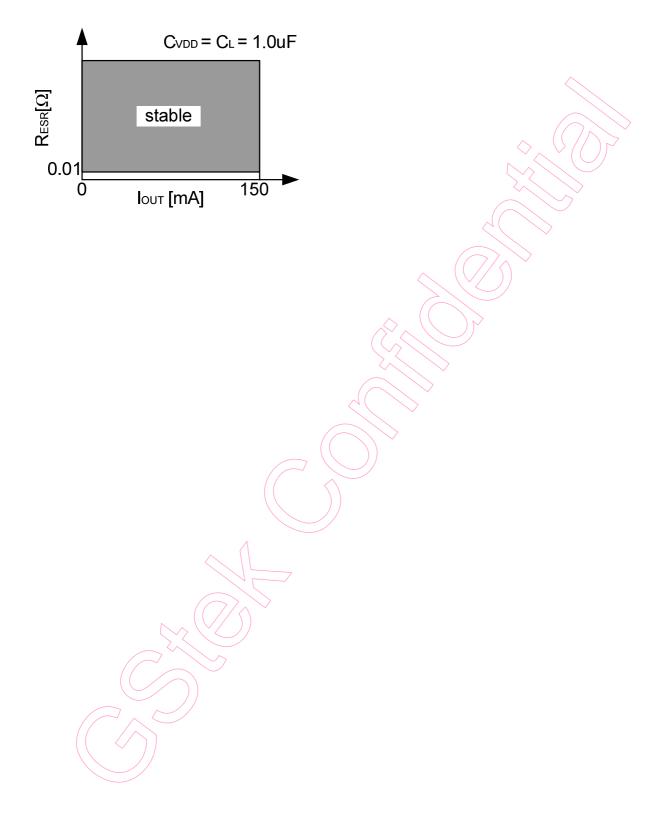


10. Transient Response Characteristics of ON/OFF Pin (C1=1.0uF, C2=1.0uF, Temp=25℃)

11. Transient Response Characteristics of Load's Mutual Interference (C1=1.0uF,C2= 1.0uF, Temp=25°C)



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Application Information Enable

The GS7129 has two enable pins. When the EN pin is set to the power-off level, the entire internal circuit stops operating, and the built-in P-channel MOS output transistor between the VDD and VOUT pin is turned off, in order to reduce the current consumption significantly. The VOUT pin is set to the VSS level. Note that the current consumption increases when a voltage of 0.3V to 1.2V is applied to the en pin.

Current Limit

The GS7129 contains an independent current limit and short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, limiting the output current to higher than 460mA typical. When the output voltage is less than 0.4V, the short circuit current protection starts the current fold back function and maintains the loading current 40mA. The output can be shorted to ground indefinitely without damaging the part.

Output Capacitor

The GS7129 is specifically designed to employ ceramic output capacitors as low as 1uF (X7R). The ceramic capacitors offer significant cost and space savings, along with high frequency noise filtering. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Ceramic capacitors have different temperature characteristics and bias characteristics which depend on their dimensions and manufacturers. If the setting voltage is 2.5V or more and the capacitor's dimensions for V_{OUT} equal to 1.0mm

by 0.5mm or smaller than that, the capacitance value might be extremely low. As a result, the capacitance might be much less than expected value. In such cases, the operation might be unstable at low temperature (-25°C or less). In that case, use a larger capacity, or a large dimensions' capacitor. (For example 1.6mm by 0.8mm)

Input Capacitor

Good bypassing is recommended from input to ground to help improve AC performance. A 1uF (X7R) input capacitor or greater located as close as possible to the IC is recommended. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Power Dissipation and Layout Considerations Excessive power dissipation may cause thermal overload, and hence the increase of the IC junction temperature beyond a safe operating level. For continuous operation, it is highly recommended to keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The relationship between θ_{JA} and $T_{J(MAX)}$ can be calculated as:

 $\mathsf{P}_{\mathsf{D}(\mathsf{MAX})} = (\mathsf{T}_{\mathsf{J}(\mathsf{MAX})} - \mathsf{T}_{\mathsf{A}}) / \theta_{\mathsf{JA}}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The power dissipation definition in device is:

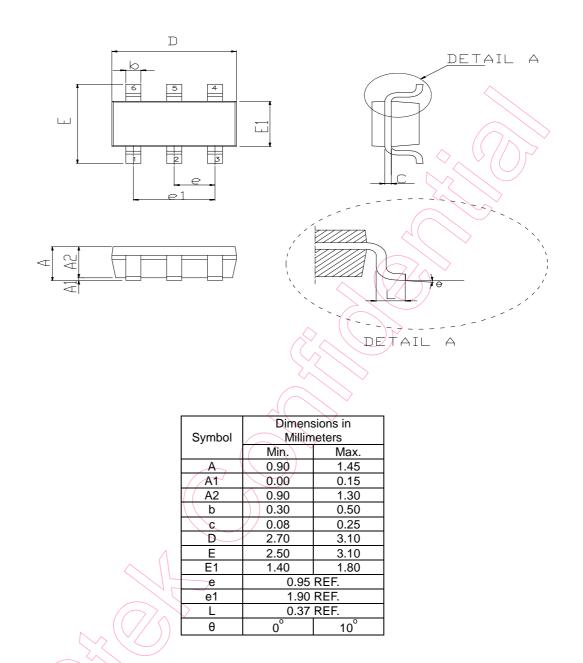
 $P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{DD} \times I_{Q}$

As the above equations indicate, it is desirable to work ICs whose θ_{JA} values are small such that $T_{J(MAX)}$ does not increase strongly with P_D. To

2-Circuit Low Noise 300mA LDO Regulator

avoid thermally overloading the GS7129, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating condition. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

Package Dimensions, SOT-23-6



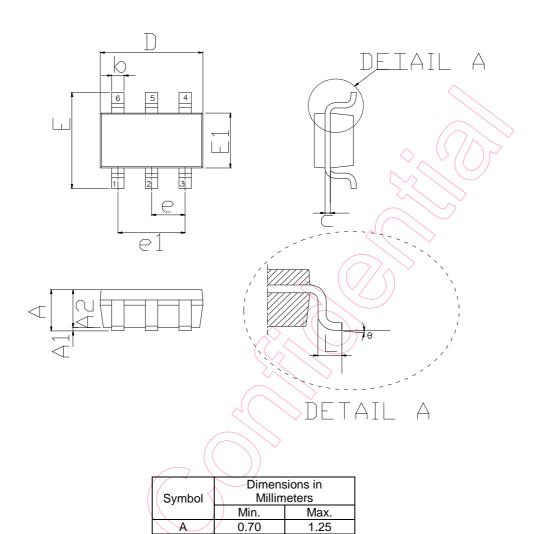
Note

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TSOT-23-6



Note

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

A1

A2

b

С

D

Е

E1

e e1

L

θ

0.00

0.70

0.30

2.70

2.50

1.40

0°

0.95 REF.

1.90 REF.

0.37 REF.

0.15

0.95

0.25

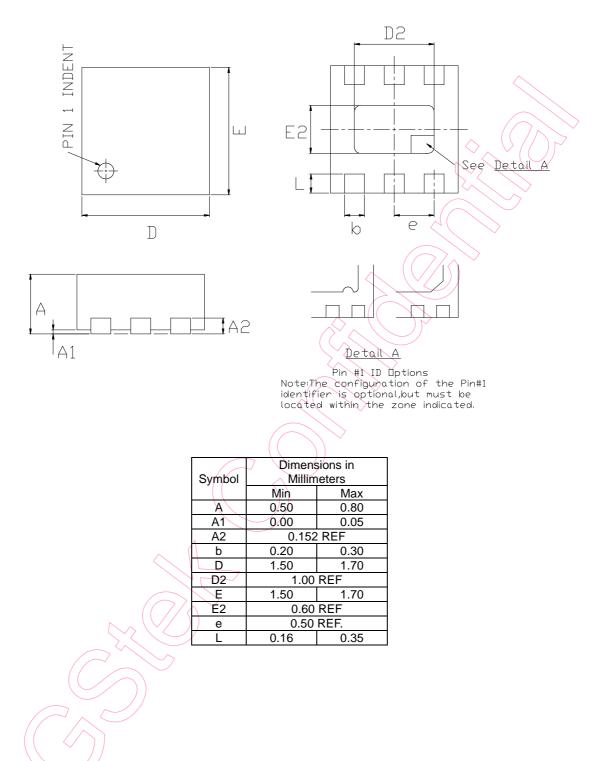
3.10

3.10

1.80

10[°]

Package Dimensions, WDFN6-1.6x1.6



Note

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

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