DATA SHEET

GPLD2080A

80 Channels SEGMENT STN LCD Driver

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Version 1.0

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80 Channels SEGMENT STN LCD Driver

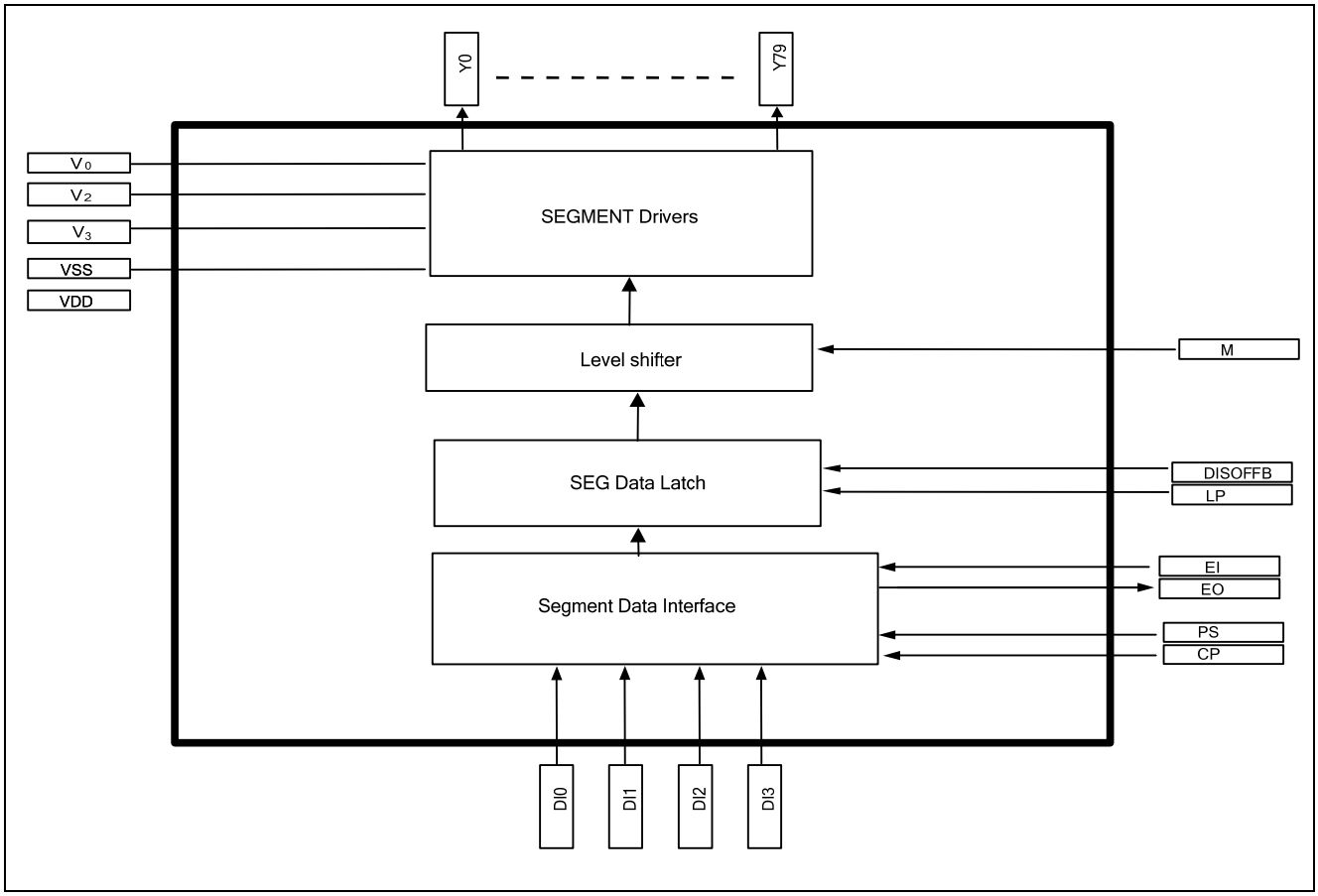
1. GENERAL DESCRIPTION

The GPLD2080A is an 80-channel segment driver IC and is suitable for driving small/medium scale dot matrix LCD panels. It is used in hand-hold game or electronic dictionary. The GPLD2080A is a segment driver and can display a STN-LCD panel with GPLD1080A.

2. FEATURES

- Number of LCD drive outputs: 80
- Supply voltage for LCD drive: 16V (max.)
- Supply voltage for logic system: 2.4V to 5.5V
- Adopts a data bus system
- 4-bits parallel /1-bit serial modes are selectable by PS pin.
- Automatic transfer function of enable signal (EI, EO)
- Chain function for different LCD resolution (EI, EO)
- Display off function
- Low power consumption
- Shift clock frequency
- 6 MHz (max.)

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Mnemonic	Type	Description
Y0 – Y79	O	LCD driver output pins.
V0, V2, V3	P	The bias voltages for LCD driving. Where V0>V2>V3>VSS.
VDD	P	Power supply for logic system. (+2.4V to +5.5V)
EI	I	When EI='H' the bus Data be accessed.
EO	O	When EO='H' the Next GPLD2080A can access bus data.
DI0 ~ DI3	I	Display data input at segment mode. 1). In 1-bit serial input mode (PS="L"), input data into the pin DI0. Connect DI1 – DI3 to VDD or VSS, avoid floating. 2). In 4-bit parallel input mode (PS="H"), input data into the four pins, DI3 - DI0.
DISOFFB	I	Display Off control input pin, Control input pin for output non-select level. When set to VSS, the LCD drive output pins (Y0 – Y79) are set to level VSS.
CP	I	Clock input for taking display data. 1). Data is read at the falling edge of the clock pulse.
LP	I	Latch pulse input for display data. 1). Data is latched at the falling edge of the clock pulse.
M	I	AC converting signal input for LCD drive waveform.
PS	I	Data input mode select pin. 1). When set to VSS, 1-bit serial input mode is set. 2). When set to VDD, 4-bit parallel input mode is set.
VSS	I	Ground (0V).
VSSH	I	Ground (0V).

5. FUNCTIONAL DESCRIPTIONS

5.1. Function Operations

5.1.1. Truth table

Segment outputs

M	Latch data	DISOFFB	Driver output voltage level
L	L	H	V2
L	H	H	V0
H	L	H	V3
H	H	H	VSS
X	X	L	VSS

Note1: V0 > V2 > V3 > VSS, L: VSS (0V), H: VDD (+2.4V to +5.5V), X: Don't care.

Note2: "Don't care" should be fixed to "H" or "L", avoiding floating. There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage is assigned by specification for each power pin.

5.2. Relationship between the Display Data and Driver Output Pins

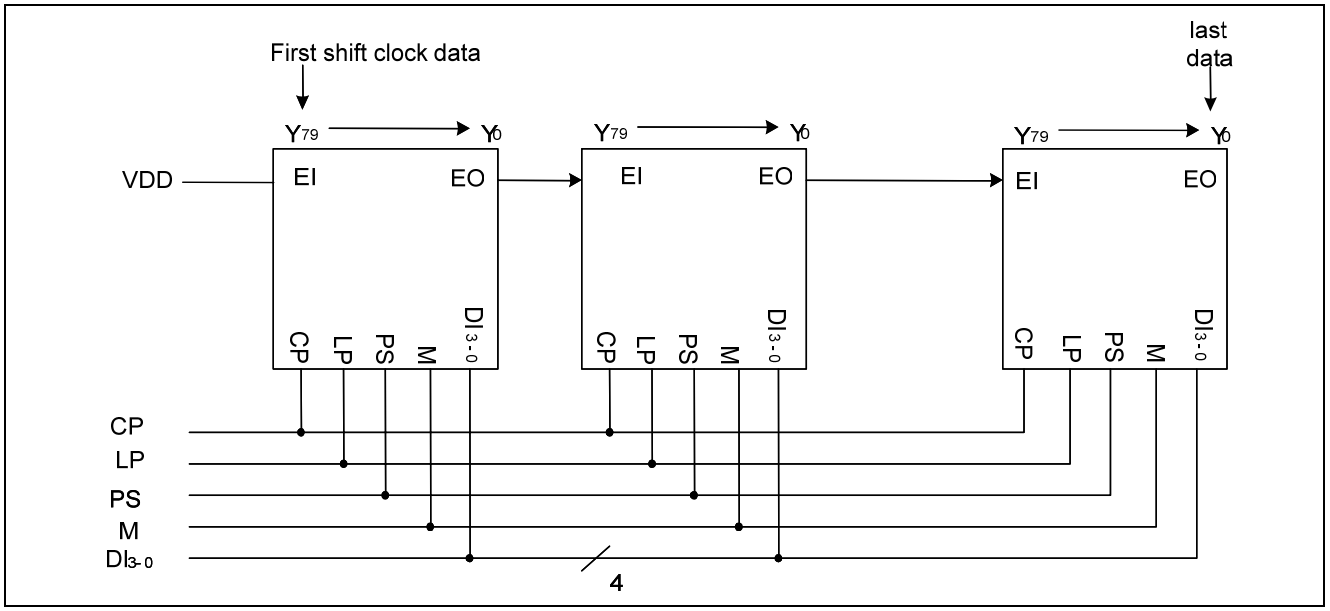
5.2.1. 4-bit parallel mode

EI	Input Data	Figure of Clock								
		1 Clock	2 Clock	3 Clock	• • •	• • •	• • •	18 Clock	19 Clock	20 Clock
H	DI0	Y76	Y72	Y68	• • •	• • •	• • •	Y8	Y4	Y0
	DI1	Y77	Y73	Y69	• • •	• • •	• • •	Y9	Y5	Y1
	DI2	Y78	Y74	Y70	• • •	• • •	• • •	Y10	Y6	Y2
	DI3	Y79	Y75	Y71	• • •	• • •	• • •	Y11	Y7	Y3

5.2.2. 1-bit serial mode

EI	Input Data	Figure of Clock								
		1 Clock	2 Clock	3 Clock	• • •	• • •	• • •	78 Clock	79 Clock	80 Clock
H	DI0	Y79	Y78	Y77	• • •	• • •	• • •	Y2	Y1	Y0

5.2.3. Connection examples of plural segment drivers



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply Voltage (1)	VDD	T_A = +25℃ Referenced to VSS (0V)	VDD	-0.3 to +6.5	V
Supply Voltage (2)	V0		V0	-0.3 to +18	V
	V2		V2	-0.3 to V0 + 0.3	V
	V3		V3	-0.3 to V0 + 0.3	V
Input Voltage	VI		DI3 - DI0, CP, LP, M, PS, EI, DISOFFB	-0.3 to VDD + 0.3	V
Storage Temperature	T_{STG}	-	-	-45 to +125	℃

Note1: T_A = +25℃

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD	Referenced to VSS (0V)	VDD	+2.4	-	+5.5	V
Supply Voltage (2)	V0		V0	+3	-	+16	V
Operating Temperature	T_{OPR}	-	-	-20	-	+75	℃

Note1: The applicable voltage on any pin with respect to VSS (0V).

Note2: Ensure that voltage are set such that V0 > V2 > V3 > VSS.

6.3. DC Characteristics

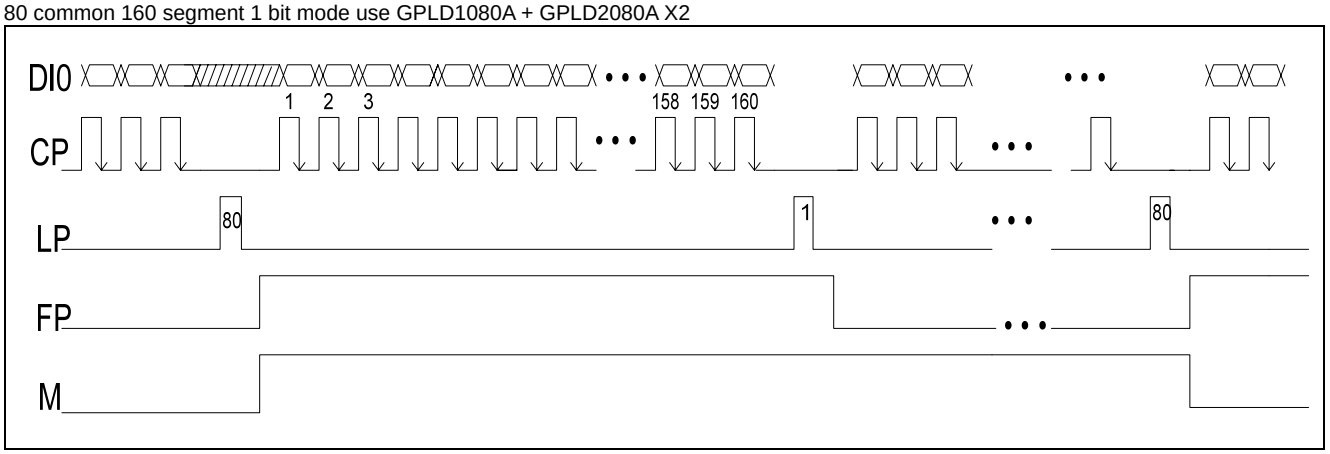
6.3.1. Segment mode (VSS = 0V, VDD = +2.4V to +5.5V, V0 = +3V to +16V, T_A = +25℃)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	DI3 - DI0, CP, LP, M, PS, DISOFFB	0.8VDD	-	--	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	I_{OH} = -0.4mA	EO	VDD - 0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input Leakage Current	I_{LIH}	V_I = VDD	DI3 - DI0, CP, LP, M, PS, DISOFFB, EI	-	-	+5	μA
	I_{LIL}	V_I = VSS		-	-	-5	μA
Output Resistance	R_{ON}	V0 = +16V	Y0 - Y79	-	1.5	2.0	KΩ
Stand-by Current	I_{STB}	DISOFFB = VSS	-	-	-	1	μA
Supply Current (1)	I_{DD}	*Note1	VDD	-	-	50	μA
Supply Current (2)	I_0	*Note1	V0	-	-	10	μA

Note1: VDD = +3.0V, V_0 = +10.5V, f_M = 35Hz, f_{LP} = 13.2KHz, f_{CP} = 396KHz, EI=VDD, PS=VDD (4-bit Parallel input mode), DI[3:0]=1010, DISOFFB=VDD, No LCD Panel loading.

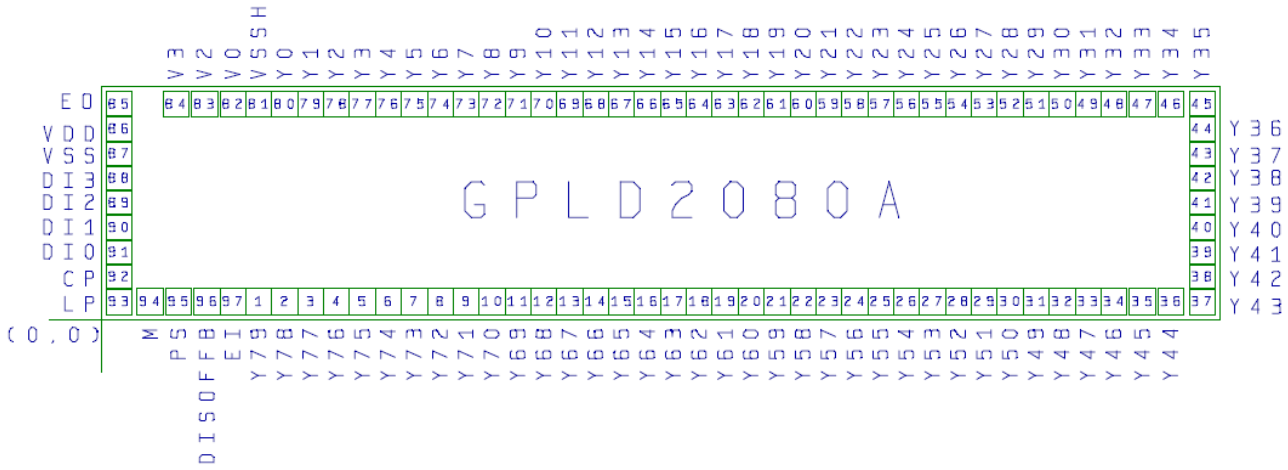
6.4. AC Characteristics

80 common 160 segment 1 bit mode use GPLD1080A + GPLD2080A X2



7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, bond all VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

7.2. Ordering Information

Product Number	Package Type
GPLD2080A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

8. DISCLAIMER

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9. REVISION HISTORY

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